LTC2153-14, LTC2153-12, LTC2152-14, LTC2152-12, LTC2151-14, LTC2151-12, LTC2150-14, LTC2150-12
12-Bit/14-Bit, 170Msps to 310Msps ADCs

DESCRIPTION

Demonstration circuit 1565A supports a family of 12-Bit/14-Bit 170Msps to 310Msps ADCs. Each assembly features one of the following devices: LTC2153-14/LTC2153-12, LTC2152-14/LTC2152-12, LTC2151-14/LTC2151-12, LTC2150-14/LTC2150-12, high speed ADCs.

The versions of the 1565A demo board are listed in Table 1. Depending on the required resolution and sample rate, the DC1565A is supplied with the appropriate ADC. The circuitry on the analog inputs is optimized for analog input frequencies from 5MHz to 140MHz. Refer to the data sheet for proper input networks for different input frequencies.

Design files for this circuit board are available at http://www.linear.com/demo

Table 1. DC1565A Variants

DC1565A VARIANTS	ADC PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
1565A-A	LTC2152-14	14-Bit	250Msps	5MHz to 140MHz
1565A-B	LTC2151-14	14-Bit	210Msps	5MHz to 140MHz
1565A-C	LTC2150-14	14-Bit	170Msps	5MHz to 140MHz
1565A-D	LTC2152-12	12-Bit	250Msps	5MHz to 140MHz
1565A-E	LTC2151-12	12-Bit	210Msps	5MHz to 140MHz
1565A-F	LTC2150-12	12-Bit	170Msps	5MHz to 140MHz
1565A-G	LTC2153-14	14-Bit	310Msps	5MHz to 140MHz
1565A-H	LTC2153-12	12-Bit	310Msps	5MHz to 140MHz

PERFORMANCE SUMMARY (T_A = 25°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage – DC1565A	Depending on Sampling Rate and the A/D Converter Provided, This Supply Must Provide Up to 500mA.	3	3.6	6	V
Analog Input Range	Depending on SENSE Pin Voltage		1.5 or 1.32		V_{P-P}
Logic Input Voltages	Minimum Logic High Maximum Logic Low		1.3 0.6		V V
Logic Output Voltages (Differential)	Nominal Logic Levels (100Ω Load, 3.5mA Mode) Common Mode Minimum Logic Levels (100Ω Load, 3.5mA Mode) Common Mode		350 1.25 247 1.25		mV V mV V
Sampling Frequency (Convert Clock Frequency)	See Table 1				
Encode Clock Level	Differential Encode Mode (ENC⁻ Not Tied to GND)	0.2		1.9	V
Resolution	See Table 1				

PERFORMANCE SUMMARY (T_A = 25°C)

Input Frequency Range	See Table 1		
SFDR	See Applicable Data Sheet		
SNR	See Applicable Data Sheet		

QUICK START PROCEDURE

Demonstration circuit 1565A is easy to set up to evaluate the performance of the LTC2152 A/D converter family. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

Setup

If a DC1371 Data Acquisition and Collection System was supplied with the DC1565A demonstration circuit, follow the DC1371 Quick Start Guide to install the required software and for connecting the DC1371 to the DC1565A and to a PC.

DC1565A Demonstration Circuit Board Jumpers

The DC1565A demonstration circuit board should have the following jumper settings as default positions: (as per Figure 1)

JP2 PAR/SER: Selects parallel or serial programming mode. (default - serial)

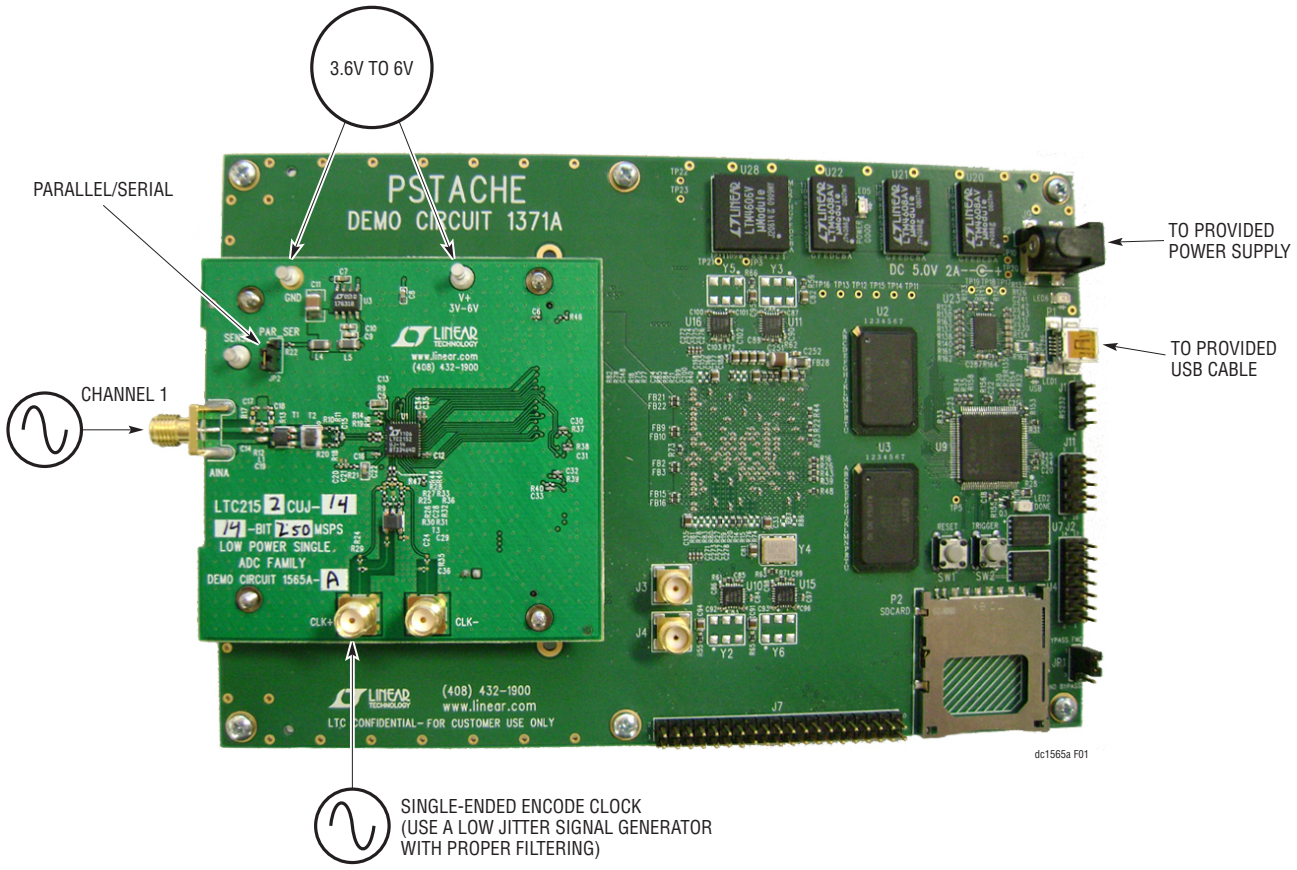


Figure 1. DC1565 Setup

QUICK START PROCEDURE

Applying Power and Signals to the DC1565A Demonstration Circuit

The DC1371 is used to acquire data from the DC1565A, the DC1371 must first be connected to a powered USB port and have 5V applied power before applying 3.6V to 6V across the pins marked V^+ and GND on the DC1565A. DC1565A requires 3.6V for proper operation.

Regulators on the board produce the voltages required for the ADC. The DC1565A demonstration circuit requires up to 500mA depending on the sampling rate and the A/D converter supplied.

The DC1565A should not be removed, or connected to the DC1371 while power is applied.

Analog Input Network

For optimal distortion and noise performance the RC network on the analog inputs may need to be optimized for different analog input frequencies. For input frequencies above 140MHz, refer to the LTC2152 data sheet for a proper input network. Other input networks may be more appropriate for input frequencies less that 5MHz.

In almost all cases, filters will be required on both analog input and encode clock to provide data sheet SNR.

The filters should be located close to the inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to obtain low distortion.

If your generator cannot deliver full-scale signals without distortion, you may benefit from a medium power amplifier based on a Gallium Arsenide Gain block prior to the final filter. This is particularly true at higher frequencies where IC based operational amplifiers may be unable to deliver the combination of low noise figure and High IP3 point required. A high order filter can be used prior to this final amplifier, and a relatively lower Q filter used between the amplifier and the demo circuit.

Apply the analog input signal of interest to the SMA connector on the DC1565A demonstration circuit board marked J4 AINA. This input is capacitively coupled to a balun transformer ETC1-1-13 (lead free part number: MABA007159-000000).

Encode Clock

NOTE: Apply an encode clock to the SMA connector on the DC1565A demonstration circuit board marked CLK^+. As a default the DC1565A is populated to have a single-ended input.

For the best noise performance, the encode input must be driven with a very low jitter, sine wave source. The amplitude should be large, up to $3V_{P-P}$ or 13dBm.

Using bandpass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. Data sheet FFT plots are taken with 10-pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broadband noise. Low phase noise Agilent 8644B generators are used for both the clock input and the analog input.

Digital Outputs

The data outputs, data clock, and frame clock signals are available on J1 of the DC1565A. This connector follows the VITA-57/FMC standard, but all signals should be verified when using an FMC carrier card other than the DC1371.

Software

The DC1371 is controlled by the PScope™ System Software provided or downloaded from the Linear Technology website at http://www.linear.com/software/.

To start the data collection software if PScope.exe, is installed (by default) in \Program Files\LTC\PScope\, double click the PScope icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC1565A demonstration circuit is properly connected to the DC1371, PScope should automatically detect the DC1565A, and configure itself accordingly.

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the Collect button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC1371 Quick Start Guide and in the online help available within the PScope program itself.

QUICK START PROCEDURE

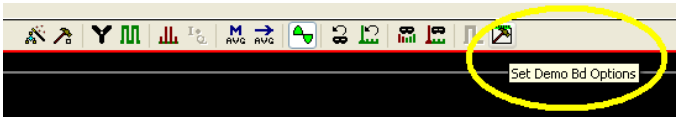


Figure 2. PScope Toolbar

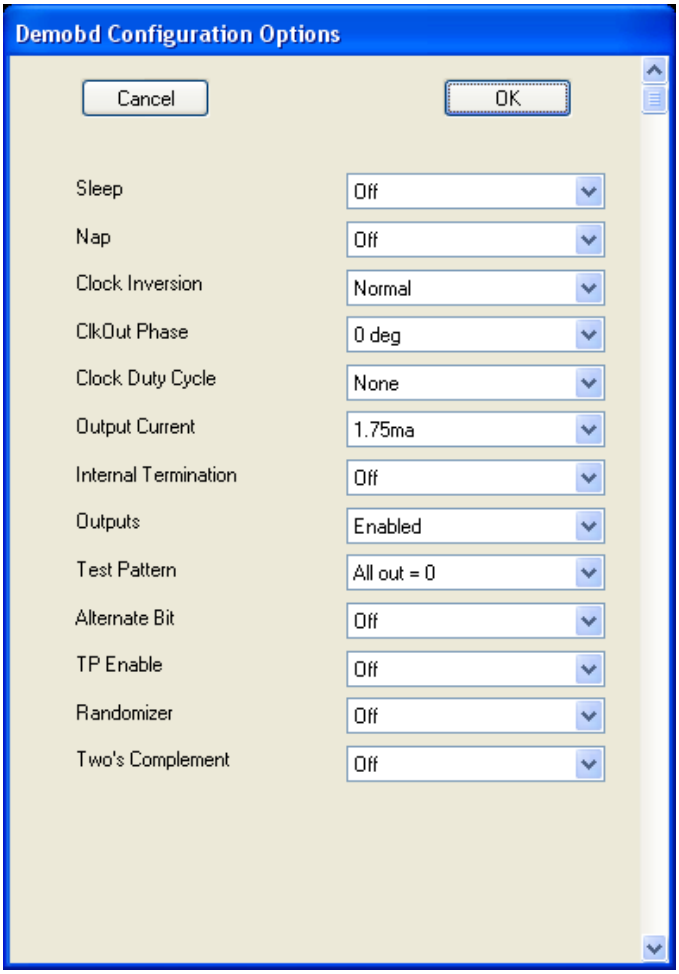


Figure 3. Demobd Configuration Options

Serial Programming

PScope has the ability to program the DC1565A board serially through the DC1371. There are several options available in the LTC2152 family that are only available through serially programming. PScope allows all of these features to be tested.

These options are available by first clicking on the Set Demo Bd Options icon on the PScope toolbar (Figure 2).

This will bring up the menu shown in Figure 3.

This menu allows any of the options available for the LTC2152 family to be programmed serially. The LTC2152 family has the following options:

Sleep Mode: Selects between normal operation, sleep mode.

- Off (Default): Entire ADC is powered, and active
- On: The entire ADC is powered down

NAP: Selects between normal operation and nap mode.

- Off (Default): Channel one is active
- On: Channel one is in nap mode

Clock Inversion: Selects the polarity of the CLKOUT signal:

- Normal (Default): Normal CLKOUT polarity
- Inverted: CLKOUT polarity is inverted

ClkOut Phase: Selects the phase delay of the CLKOUT signal:

- None (Default): No CLKOUT delay
- 45 deg: CLKOUT delayed by 45 degrees
- 90 deg: CLKOUT delayed by 90 degrees
- 135 deg: CLKOUT delayed by 135 degrees

Clock Duty Cycle: Enable or disables duty cycle stabilizer

- Stabilizer off (Default): Duty cycle stabilizer disabled
- Stabilizer on: Duty cycle stabilizer enabled

QUICK START PROCEDURE

Output Current: Selects the LVDS output drive current

- 1.75mA (Default): LVDS output driver current
- 2.1mA: LVDS output driver current
- 2.5mA: LVDS output driver current
- 3.0mA: LVDS output driver current
- 3.5mA: LVDS output driver current
- 4.0mA: LVDS output driver current
- 4.5mA: LVDS output driver current

Internal Termination: Enables LVDS internal termination

- Off (Default): Disables internal termination
- On: Enables internal termination

Outputs: Enables digital outputs

- Enabled (Default): Enables digital outputs
- Disabled: Disables digital outputs

Test Pattern: Selects digital output test patterns

- All out = 0 (default): All digital outputs are 0
- All out = 1: All digital outputs are 1
- Checkerboard: OF, and D13-D0 Alternate between 101 0101 1010 0101 and 010 1010 0101 1010 on alternating samples.
- Alternating: Digital outputs alternate between all 1's and all 0's on alternating samples

Alternate Bit: Alternate bit polarity mode

- Off (Default): Disables alternate bit polarity
- On: Enables alternate bit polarity (Before enabling ABP, be sure the part is in offset binary mode)

TP Enable: Selects digital output test patterns. The desired test pattern can be entered into the text boxes provided.

- Off(default): ADC input data is displayed
- On: Test pattern is displayed.

Randomizer: Enables data output randomizer

- Off (Default): Disables data output randomizer
- On: Enables data output randomizer

Two's Complement: Enables two's complement mode

- Off (Default): Selects offset binary mode
- On: Selects two's complement mode

Once the desired settings are selected hit OK and PScope will automatically update the register of the device on the DC1565A demo board.

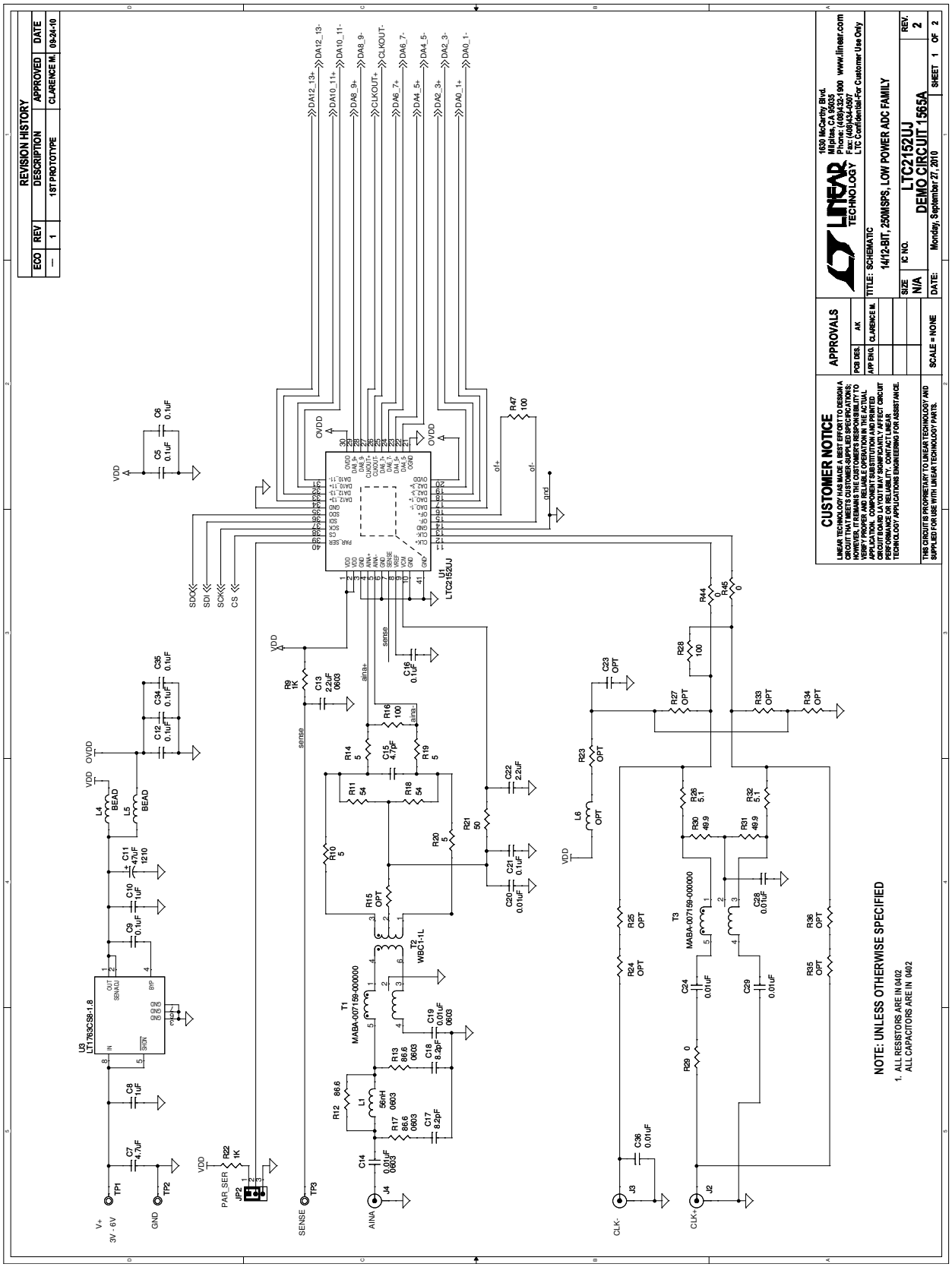
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	4	C1, C3, C8, C10	Capacitor, X7R, 1µF, 10V, 10%, 0603	AVX, 0603ZC105KAT2A
2	2	C2, C9	Capacitor, X5R, 0.1µF, 10V, 10%, 0603	AVX, 0603ZD104KAQ2A
3	2	C4, C11	Capacitor, X7R, 47µF, 10V, 10%, 1210	Murata, GRM32ER71A476KE15L
4	8	C5, C6, C12, C16, C21, C23,	Capacitor, X5R, 0.1µF, 10V, 10%, 0402	AVX, 0402ZD104KAQ2A
		C34, C35		
5	1	C7	Capacitor, X5R, 4.7µF, 6.3V, 20%, 0603	AVX, 06036D475MAT2A
6	1	C13	Capacitor, X5R, 2.2µF, 10V, 20%, 0603	AVX, 0603ZD225MAT2A
7	2	C14, C19	Capacitor, X7R, 0.01µF, 50V, 10%, 0603	AVX, 06035C103KAQ2A
8	3	C15, C26, C27	Capacitor, C0G, 4.7pF, 50V, 5%, 0402	AVX, 04025A4R7JAT2A
9	2	C17, C18	Capacitor, C0G, 8.2pF, 50V, 5%, 0402	AVX, 04025A8R2JAT2A
10	5	C20, C24, C28, C29, C36	Capacitor, X7R, 0.01µF, 16V, 10%, 0402	Murata, GRM155R71C103KA01D
11	1	C22	Capacitor, X5R, 2.2µF, 10V, 20%, 0603	AVX, 0603ZD225MAT2A
12	0	R15, C25	OPT 0402	
13	4	C30, C31, C32, C33	Capacitor, C0G, 47pF, 16V, 10%, 0402	AVX, 0402YA470KA
14	1	D1	Diode Schottky, RF SER, 15V, SOT-23	Avago, HSMS-2822-TR1G
15	1	JP1	Header, 2-Pin 0.079 Single Row	Samtec, TMM-102-02-L-S
16	1	J1	BGA Connector, 40 × 10	Samtec, SEAM-40-02.0-S-10-2-A-K-TR
17	2	J2, J3	Connector, SMA, 50Ω, Straight Mount	Connex., 132134
18	1	J4	Connector, SMA, 50Ω, EDGE-LANCH	E. F. Johnson, 142-0701-851
19	1	L1	Inductor, 56nH, 0603	Murata, LQP18MN56NG02D
20	0	L2	OPT 0603	
21	3	L3, L4, L5	Ferrite Bead, 1206	Murata, BLM31PG330SN1L
22	0	L6	Bead, OPT 1206	
23	22	R1, R2, R3, R4, R5, R6, R7, R8, R10, R16, R20, R21, R23, R24, R25, R27, R28, R33, R34, R35, R36, R47	Resistor, Chip, 100, 1/16W, 5%, 0402	NIC, NRC04J101TRF
24	5	R9, R37, R38, R39, R40	Resistor, Chip, 1k, 1/16W, 5%, 0402	Yageo, RC0402FR-071KL
25	2	R11, R18	Resistor, Chip, 33.2Ω, 1/16W, 1%, 0402	NIC, NRC04F33R2TRF
26	1	R12	Resistor, Chip, 86.6Ω, 1/16W, 1%, 0402	NIC, NRC04F86R6TRF
27	2	R13, R17	Resistor, Chip, 86.6Ω, 1/16W, 1%, 0603	Vishay, CRCW060386R6FNEA
28	2	R14, R19	Resistor, Chip, 10Ω, 1/16W, 5%, 0402	Vishay, CRCW040210R0JNED

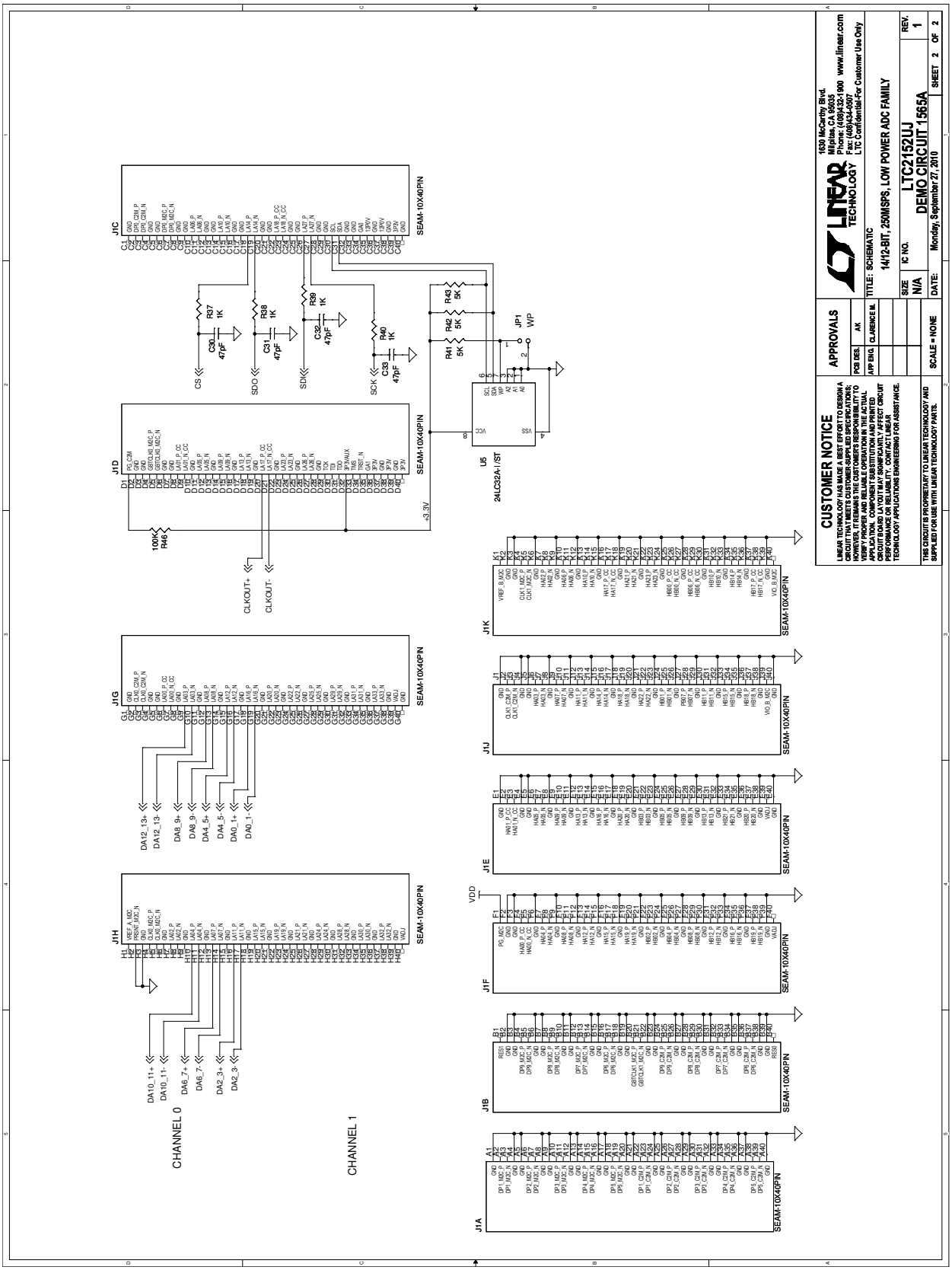
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
29	2	R26, R32	Resistor, Chip, 5.1Ω, 1/16W, 1%, 0402	Vishay, CRCW04025R10FKED
30	1	R29	PES., Chip, 0Ω, 0402	Vishay, CRCW04020000Z0ED
31	2	R30, R31	Resistor, Chip, 49.9Ω, 1/16W, 1%, 0402	Yageo, RC0402FR-0749R9L
32	3	R41, R42, R43	Resistor, Chip, 5.1k, 1/16W, 1%, 0402	NIC, NRC04F5101TRF
33	3	TP1, TP2, TP3	Testpoint, Turret, 0.094" pbf	Mill-Max, 2501-2-00-80-00-00-07-0
34	2	T1, T3	Transformer, MABA-007159-000000	M/A-COM, MABA-007159-000000
35	1	T2	Transformer, WBC1-1L	Coilcraft, WBC1-1L
36	1	U1	IC, LTC2152CUJ, 40-Pin QFN 6mm × 6mm	Linear Technology, LTC2152CUJ#PBF
37	1	U3	IC, LT1763CS8-1.8, SO8	Linear Technology, LT1763CS8-1.8#TRPBF
38	1	U4	IC, LT1763CS8-3-3, SO8	Linear Technology, LT1763CS8-3.3#TRPBF
39	1	U5	IC, EEPROM, 32k, 400khz, 8TSSOP	MICROChip, 24LC32A-I/ST
40	1		Fab, Printed Circuit Board	Demo Circuit 1565A
41	2		Top & Botton Stencil for Proto	Stencil 1565A

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



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Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035