74ALVCH16841

20-bit bus interface D-type latch; 3-state

Rev. 3 — 12 September 2018

Product data sheet

1. General description

The 74ALVCH16841 has two 10-bit D-type latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. The two sections of each register are controlled independently by the latch enable (nLE) and output enable ($\overline{\text{NOE}}$) control gates.

When $n\overline{OE}$ is LOW, the data in the registers appears at the outputs. When $n\overline{OE}$ is HIGH the outputs are in High-impedance OFF state. Operation of the $n\overline{OE}$ input does not affect the state of the flip-flops.

The 74ALVCH16841 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

2. Features and benefits

- Wide supply voltage range of 1.2 V to 3.6 V
- CMOS low power consumption
- · Direct interface with TTL levels
- Current drive ±24 mA at V_{CC} = 3.0 V
- · MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimize noise and ground bounce
- All data inputs have bushold
- Output drive capability 50 Ω transmission lines at 85 °C
- · 3-state non-inverting outputs for bus oriented applications
- Complies with JEDEC standards:
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001 exceeds 2000 V
 - CDM JESD22-C101E exceeds 1000 V

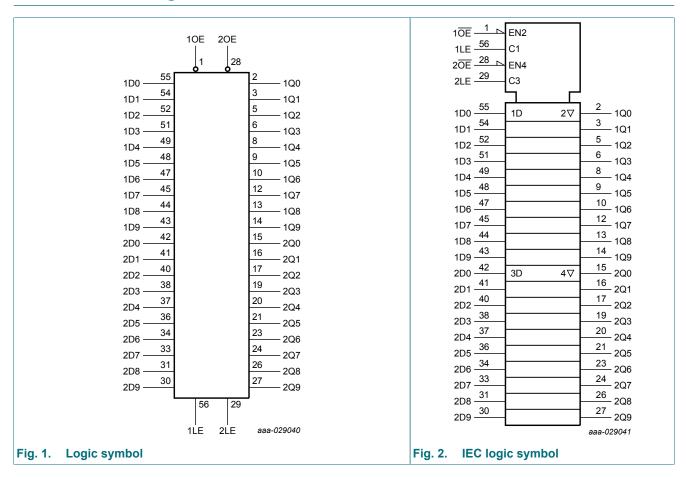
3. Ordering information

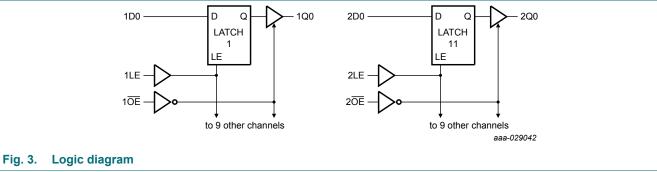
Table 1. Ordering information

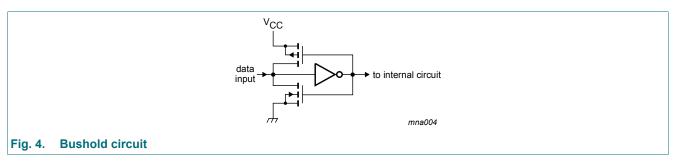
Type number	Package	ackage							
	Temperature range	Name	Description	Version					
74ALVCH16841DGG	-40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1					



4. Functional diagram

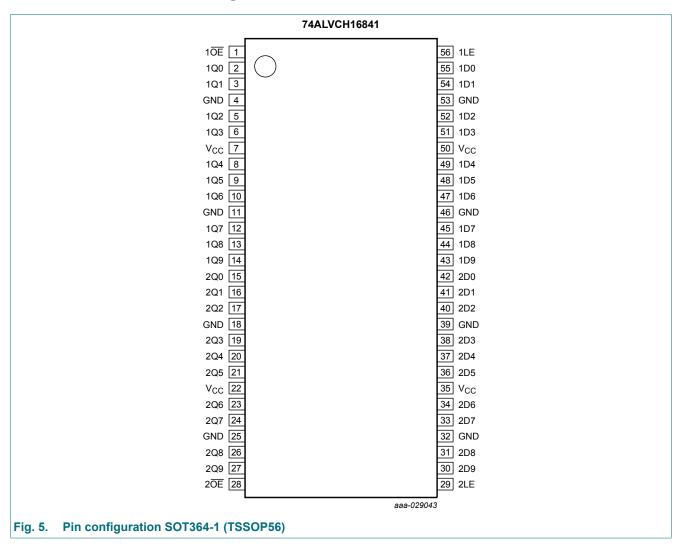






5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7, 1D8, 1D9	55, 54, 52, 51, 49, 48, 47, 45, 44, 43	data input
2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7, 2D8, 2D9	42, 41, 40, 38, 37, 36, 34, 33, 31, 30	data input
1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7, 1Q8, 1Q9	2, 3, 5, 6, 8, 9, 10, 12, 13, 14	data output
2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7, 2Q8, 2Q9	15, 16, 17, 19, 20, 21, 23, 24, 26, 27	data output
10E, 20E	1, 28	output enable inputs (active-LOW)
1LE, 2LE	56, 29	latch enable inputs
GND	4, 11, 18, 25, 32, 39, 46, 53	ground (0 V)
V _{CC}	7, 22, 35, 50	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Inputs nOE	Outputs		
nŌĒ	nLE	nDn	nQn
L	Н	L	L
L	Н	Н	Н
L	L	X	Q_0
Н	X	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
VI	input voltage	For control pins [1]	-0.5	+4.6	V
		For data inputs [1]	-0.5	V _{CC} + 0.5	V
Vo	output voltage	[1]	-0.5	V _{CC} + 0.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
Io	output current	$V_O = 0 \text{ V to } V_{CC}$	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C [2]	-	600	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage	for maximum speed performance; 30 pF output load	2.3	2.7	V
		for maximum speed performance; 50 pF output load	3.0	3.6	V
VI	input voltage		0	V _{CC}	V
V _O	output voltage		0	V _{CC}	V
T _{amb}	ambient temperature	in free air	-40	+85	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.3 V to 3.0 V	-	20	ns/V
		V _{CC} = 3.0 V to 3.6 V	-	10	ns/V

^[2] Above 55 °C the value of Ptot derates linearly with 8 mW/K.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V). T_{amb} = -40 °C to +85 °C

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V _{IH}	HIGH-level	V _{CC} = 2.3 V to 2.7 V	1.7	1.2	-	V
	input voltage	V _{CC} = 2.7 V to 3.6 V	2.0	1.5	-	V
V _{IL}	LOW-level	V _{CC} = 2.3 V to 2.7 V	-	1.2	0.7	V
	input voltage	V _{CC} = 2.7 V to 3.6 V	-	1.5	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}				
	output voltage	I _O = -100 μA; V _{CC} = 2.3 V to 3.6 V	V _{CC} - 0.2	V _{CC}	-	V
		I _O = -6 mA; V _{CC} = 2.3 V	V _{CC} - 0.3	V _{CC} - 0.08	-	V
		I _O = -12 mA; V _{CC} = 2.3 V	V _{CC} - 0.6	V _{CC} - 0.26	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	V _{CC} - 0.5	V _{CC} - 0.14	-	V
		I_{O} = -12 mA; V_{CC} = 3.0 V	V _{CC} - 0.6	V _{CC} - 0.09	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	V _{CC} - 1.0	V _{CC} - 0.28	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}				
	output voltage	I _O = 100 μA; V _{CC} = 2.3 V to 3.6 V	-	GND	0.20	V
		I _O = 6 mA; V _{CC} = 2.3 V	-	0.07	0.40	V
		I _O = 12 mA; V _{CC} = 2.3 V	-	0.15	0.70	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	0.14	0.40	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	0.27	0.55	V
l _l	input leakage current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{CC} or GND	-	0.1	5	μΑ
I _{OZ}	OFF-state output current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{IH} or V_{IL} ; V_O = V_{CC} or GND	-	0.1	10	μΑ
I _{CC}	supply current	V_{CC} = 2.3 V to 3.6 V; V_{I} = V_{CC} or GND; I_{O} = 0 A	-	0.2	40	μΑ
ΔI _{CC}	additional supply current	V_{CC} = 2.3 V to 3.6 V; V_{I} = V_{CC} - 0.6 V; I_{O} = 0 A	-	150	750	μΑ
I _{BHL}	bus hold LOW	V _{CC} = 2.3 V; V _I = 0.7 V	45	-	-	μA
	current	V _{CC} = 3.0 V; V _I = 0.8 V	75	150	-	μA
I _{BHH}	bus hold HIGH	V _{CC} = 2.3 V; V _I = 1.7 V	-45	-	-	μA
	current	V _{CC} = 3.0 V; V _I = 2.0 V	-75	-175	-	μA
I _{BHLO}	bus hold LOW overdrive current	V _{CC} = 3.6 V	500	-	-	μΑ
Івнно	bus hold HIGH overdrive current	V _{CC} = 3.6 V	-500	-	-	μА
Cı	input capacitance		-	5.0	-	pF

^[1] All typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 10; T_{amb} = -40 °C to +85 °C

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t _{pd}	propagation delay	nDn to nQn; see Fig. 6 [2]				
		V _{CC} = 2.3 V to 2.7 V	1.0	2.5	5.0	ns
		V _{CC} = 2.7 V	1.0	2.6	4.7	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.4	3.9	ns
		nLE to nQn; see Fig. 7				
		V _{CC} = 2.3 V to 2.7 V	1.0	2.5	5.6	ns
		V _{CC} = 2.7 V	1.0	2.6	5.1	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.4	4.3	ns
t _{en}	enable time	nOE to nQn; see Fig. 9 [3]				
		V _{CC} = 2.3 V to 2.7 V	1.0	2.7	6.2	ns
		V _{CC} = 2.7 V	1.0	3.1	6.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.3	4.9	ns
t _{dis}	disable time	nOE to nQn; see Fig. 9 [4]				
		V _{CC} = 2.3 V to 2.7 V	1.1	2.2	5.3	ns
		V _{CC} = 2.7 V	1.3	3.1	4.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.3	2.9	4.1	ns
t _{su}	set-up time	nDn to nLE; see Fig. 8				
		V _{CC} = 2.3 V to 2.7 V	1.3	0.1	-	ns
		V _{CC} = 2.7 V	1.1	0.1	-	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	0.6	-	ns
t _h	hold time	nDn to nLE; see Fig. 8				
		V _{CC} = 2.3 V to 2.7 V	1.4	0.3	-	ns
		V _{CC} = 2.7 V	1.7	0.2	-	ns
		V _{CC} = 3.0 V to 3.6 V	1.4	0.2	-	ns
t _W	pulse width	nLE HIGH; V _{CC} = 2.3 V to 3.6 V; see Fig. 7	3.3	1.5	-	ns
C _{PD}	power dissipation	per latch; $V_I = GND$ to V_{CC} [5]				1
	capacitance	outputs enabled	-	19	-	pF
		outputs disabled	-	3	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C
 - Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V.
 - Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [3] t_{en} is the same as t_{PZL} and t_{PZH} .
- [4] t_{dis} is the same as t_{PLZ} and t_{PHZ} .
- [5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

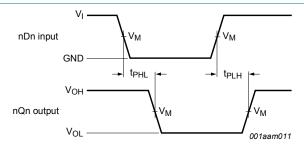
C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

 $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs.}$

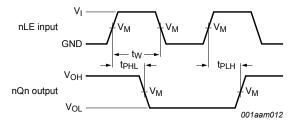
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

 $\ensuremath{V_{OL}}$ and $\ensuremath{V_{OH}}$ are typical voltage output levels that occur with the output load.

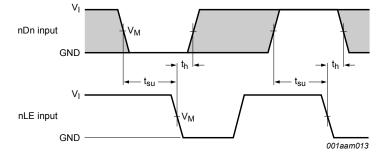
Fig. 6. Input (nDn) to output (nQn) propagation delays



Measurement points are given in Table 8.

 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

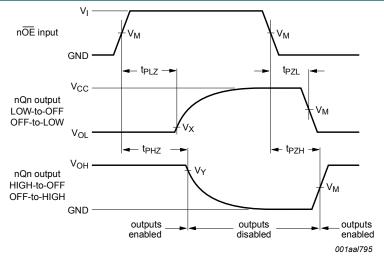
Fig. 7. Latch enable input (nLE) to data output (nQn) propagation delays and pulse width (nLE)



Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 8. Data setup and hold times for input (nDn) to input (nLE)



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output levels that occur with the output load.

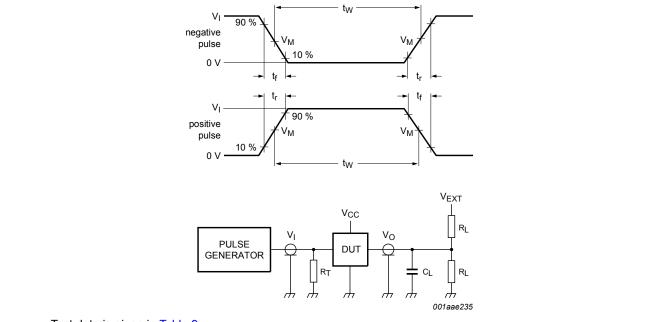
Fig. 9. 3-State enable and disable times

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20-bit bus interface D-type latch; 3-state

Table 8. Measurement points

Input			Output				
V _{CC}	V _I	V _M	V _M	V _x	V _y		
< 2.3 V	V _{CC}	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V		
2.3 V to 2.7 V	V _{CC}	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V		
2.7 V	2.7 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V		
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V		



Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistance;

 C_L = Load capacitance including jig and probe capacitance;

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator;

 V_{EXT} = External voltage for measuring switching times.

Fig. 10. Test circuit for measuring switching times

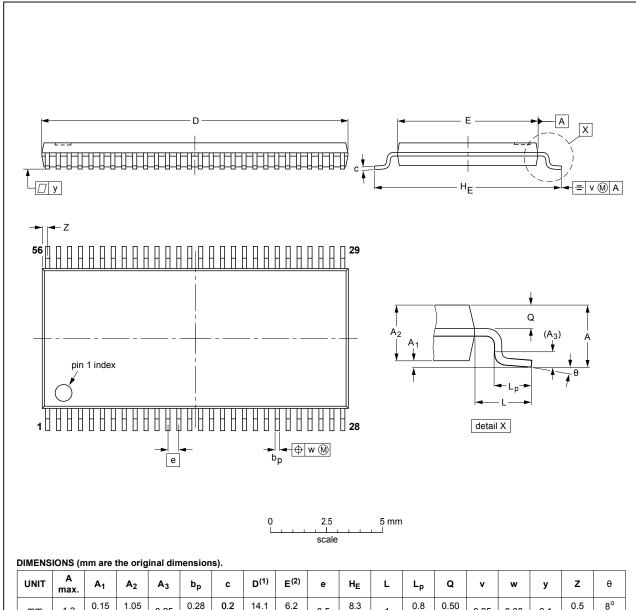
Table 9. Test data

Input	Load	oad V _{EXT}					
V _{CC}	V _I	t _r , t _f	R_L	CL	t_{PHZ} , t_{PZH}	t_{PLZ}, t_{PZL}	t _{PLH} , t _{PHL}
< 2.3 V	V _{CC}	≤ 2.0 ns	500 Ω	30 pF	GND	2 × V _{CC}	open
2.3 V to 2.7 V	V _{CC}	≤ 2.0 ns	500 Ω	30 pF	GND	2 × V _{CC}	open
2.7 V	2.7 V	≤ 2.5 ns	500 Ω	50 pF	GND	2 × V _{CC}	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	500 Ω	50 pF	GND	2 × V _{CC}	open

11. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	C	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	٧	w	у	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT364-1		MO-153			99-12-27 03-02-19

Fig. 11. Package outline SOT364-1 (TSSOP56)

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12. Abbreviations

Table 10. Abbreviations

Acronym	Description			
CDM	Charged Device Model			
CMOS	Complementary Metal-Oxide Semiconductor			
DUT	Device Under Test			
ESD	ElectroStatic Discharge			
НВМ	Human Body Model			
TTL	Transistor-Transistor Logic			

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74ALVCH16841 v.3	20180912	Product data sheet	-	74ALVCH16841 v.2	
Modifications:	of Nexperia.	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74ALVCH16841 v.2	19980727	Product specification	-	74ALVCH16841 v.1	
74ALVCH16841 v.1	19980727	Product specification	-		

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
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