

**FEATURES**

**0.8  $\Omega$  typical on resistance**  
**Less than 1  $\Omega$  maximum on resistance at 85°C**  
**1.8 V to 5.5 V single supply**  
**High current carrying capability: 300 mA continuous**  
**Rail-to-rail switching operation**  
**Fast-switching times: <17 ns**  
**Typical power consumption: <0.1  $\mu$ W**  
**1.30 mm  $\times$  1.60 mm mini LFCSP**

**APPLICATIONS**

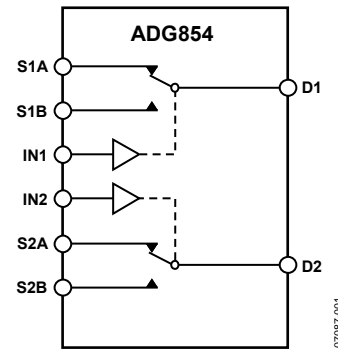
**Cellular phones**  
**PDA's**  
**MP3 players**  
**Power routing**  
**Battery-powered systems**  
**PCMCIA cards**  
**Modems**  
**Audio and video signal routing**  
**Communication systems**

**GENERAL DESCRIPTION**

The ADG854 is a low voltage CMOS device containing two independently selectable single-pole, double-throw (SPDT) switches. This device offers ultralow on resistance of <1  $\Omega$  over the full temperature range. The ADG854 is fully specified for 5.5 V and 3.3 V supply operation.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. The ADG854 exhibits break-before-make switching action.

The ADG854 is available in a 1.3 mm  $\times$  1.6 mm 10-lead mini LFCSP.

**FUNCTIONAL BLOCK DIAGRAM**


SWITCHES SHOWN FOR  
A LOGIC 1 INPUT

Figure 1.

**PRODUCT HIGHLIGHTS**

1. <1  $\Omega$  over full temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .
2. Single 1.8 V to 5.5 V operation.
3. Compatible with 1.8 V CMOS logic.
4. High current handling capability: 300 mA continuous current per channel.
5. Low THD + N: 0.08% typical.
6. 1.30 mm  $\times$  1.60 mm mini LFCSP.

**Rev. 0**

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## REVISION HISTORY

6/08—Revision 0: Initial Version

## SPECIFICATIONS

$V_{DD} = 4.2\text{ V to }5.5\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 1.**

Parameter	+25°C	−40°C to +85°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>				
Analog Signal Range		0 to $V_{DD}$	V	
On Resistance, $R_{ON}$	0.8		$\Omega$ typ	$V_{DD} = 4.2\text{ V}$ , $V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = 100\text{ mA}$ ; see Figure 16
	0.85	1	$\Omega$ max	
On Resistance Match Between Channels, $\Delta R_{ON}$	0.02		$\Omega$ typ	$V_{DD} = 4.2\text{ V}$ , $V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = 100\text{ mA}$
		0.04	$\Omega$ max	
On Resistance Flatness, $R_{FLAT(ON)}$	0.17		$\Omega$ typ	$V_{DD} = 4.2\text{ V}$ , $V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = 100\text{ mA}$
		0.23	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>				
Source Off Leakage, $I_S$ (Off)	$\pm 10$		$\mu\text{A typ}$	$V_{DD} = 5.5\text{ V}$ $V_S = 0.6\text{ V}/4.2\text{ V}$ , $V_D = 4.2\text{ V}/0.6\text{ V}$ ; see Figure 17
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 30$		$\mu\text{A typ}$	$V_S = V_D = 0.6\text{ V or }4.2\text{ V}$ ; see Figure 18
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.0	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current				
$I_{INL}$ or $I_{INH}$	0.002		$\mu\text{A typ}$	$V_{IN} = V_{GND}$ or $V_{DD}$
		0.05	$\mu\text{A max}$	
Digital Input Capacitance, $C_{IN}$	2.5		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>				
$t_{ON}$	17		ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
	23	28	ns max	$V_S = 3\text{ V}/0\text{ V}$ ; see Figure 19
$t_{OFF}$	6		ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
	8.5	9.2	ns max	$V_S = 3\text{ V}$ ; see Figure 19
Break-Before-Make Time Delay, $t_{BBM}$	14		ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
		8	ns min	$V_{S1} = V_{S2} = 1.5\text{ V}$ ; see Figure 20
Charge Injection	30		pC typ	$V_S = 1.5\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 21
Off Isolation	−75		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 22
Channel-to-Channel Crosstalk	−85		dB typ	S1A to S2A/S1B to S2B, $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 25
	−73		dB typ	S1A to S1B/S2A to S2B, $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 24
Total Harmonic Distortion + Noise, THD + N	0.08		% typ	$R_L = 32\ \Omega$ , $f = 20\text{ Hz to }20\text{ kHz}$ , $V_S = 3.5\text{ V p-p}$
Insertion Loss	−0.06		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 23
−3 dB Bandwidth	100		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 23
$C_S$ (Off)	19.5		pF typ	
$C_D$ , $C_S$ (On)	50		pF typ	
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.002		$\mu\text{A typ}$	$V_{DD} = 5.5\text{ V}$ Digital inputs = 0 V or 5.5 V
		1.0	$\mu\text{A max}$	

<sup>1</sup> Guaranteed by design, not subject to production test.

# ADG854

$V_{DD} = 2.7\text{ V}$  to  $3.6\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 2.**

Parameter	+25°C	−40°C to +85°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>				
Analog Signal Range		0 to $V_{DD}$	V	
On Resistance, $R_{ON}$	1.3		$\Omega$ typ	$V_{DD} = 2.7\text{ V}$ , $V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = 100\text{ mA}$ ; see Figure 16
	1.5	1.7	$\Omega$ max	
On Resistance Match Between Channels, $\Delta R_{ON}$	0.03		$\Omega$ typ	$V_{DD} = 2.7\text{ V}$ , $V_S = 0.6\text{ V}$ , $I_{DS} = 100\text{ mA}$
		0.05	$\Omega$ max	
On Resistance Flatness, $R_{FLAT(ON)}$	0.48		$\Omega$ typ	$V_{DD} = 2.7\text{ V}$ , $V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = 100\text{ mA}$
		0.66	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>				
Source Off Leakage, $I_S$ (Off)	$\pm 10$		pA typ	$V_{DD} = 3.6\text{ V}$ $V_S = 0.6\text{ V}/3.3\text{ V}$ , $V_D = 3.3\text{ V}/0.6\text{ V}$ ; see Figure 17
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 30$		pA typ	$V_S = V_D = 0.6\text{ V}$ or $3.3\text{ V}$ ; see Figure 18
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		1.35	V min	
Input Low Voltage, $V_{INL}$		0.7	V max	
Input Current				
$I_{INL}$ or $I_{INH}$	0.002		$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
		0.05	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	4		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>				
$t_{ON}$	25		ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
	37	43	ns max	$V_S = 1.5\text{ V}/0\text{ V}$ ; see Figure 19
$t_{OFF}$	7		ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
	7.4	8	ns max	$V_S = 1.5\text{ V}$ ; see Figure 19
Break-Before-Make Time Delay, $t_{BBM}$	22		ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
		13	ns min	$V_{S1} = V_{S2} = 1\text{ V}$ ; see Figure 20
Charge Injection	23		pC typ	$V_S = 1.5\text{ V}$ , $R_S = 0\text{ V}$ , $C_L = 1\text{ nF}$ ; see Figure 21
Off Isolation	−75		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 22
Channel-to-Channel Crosstalk	−85		dB typ	S1A to S2A/S1B to S2B; $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 25
	−73		dB typ	S1A to S1B/S2A to S2B; $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; see Figure 24
Total Harmonic Distortion, THD	0.15		% typ	$R_L = 32\ \Omega$ , $f = 20\text{ Hz}$ to $20\text{ kHz}$ , $V_S = 1.5\text{ V p-p}$
Insertion Loss	−0.07		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 23
−3 dB Bandwidth	100		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 23
$C_S$ (Off)	20		pF typ	
$C_D$ , $C_S$ (On)	52		pF typ	
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.002		$\mu\text{A}$ typ	$V_{DD} = 3.6\text{ V}$ Digital inputs = $0\text{ V}$ or $3.6\text{ V}$
		1.0	$\mu\text{A}$ max	

<sup>1</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

Parameter	Rating
$V_{DD}$ to GND	-0.3 V to +6 V
Analog Inputs <sup>1</sup>	-0.3 V to $V_{DD} + 0.3$ V
Digital Inputs <sup>1</sup>	-0.3 V to $V_{DD} + 0.3$ V or 10 mA, whichever occurs first
Peak Current per Channel, S or D	500 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current per Channel, S or D	300 mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
10-Lead Mini LFCSP	
$\theta_{JA}$ Thermal Impedance, 3-Layer Board	131.6°C/W
Reflow Soldering, Pb-Free	
Peak Temperature	260(+0/-5)°C
Time at Peak Temperature	10 sec to 40 sec

<sup>1</sup> Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# ADG854

## PIN CONFIGURATION AND FUNCTION DESCRIPTION



Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 7, 9	S1A, S1B, S2B, S2A	Source Terminal. This pin can be an input or output.
2, 8	D1, D2	Drain Terminal. This pin can be an input or output.
4	IN1	Logic Control Input.
5	IN2	Logic Control Input.
6	V <sub>DD</sub>	Most Positive Power Supply Potential.
10	GND	Ground (0 V) Reference.

Table 5. ADG854 Truth Table

Logic (IN1/IN2)	Switch A (S1A or S2A)	Switch B (S1B or S2B)
0	Off	On
1	On	Off

# TYPICAL PERFORMANCE CHARACTERISTICS



Figure 3. On Resistance vs.  $V_D$  ( $V_S$ ),  $V_{DD} = 4.2$  V to 5.5 V

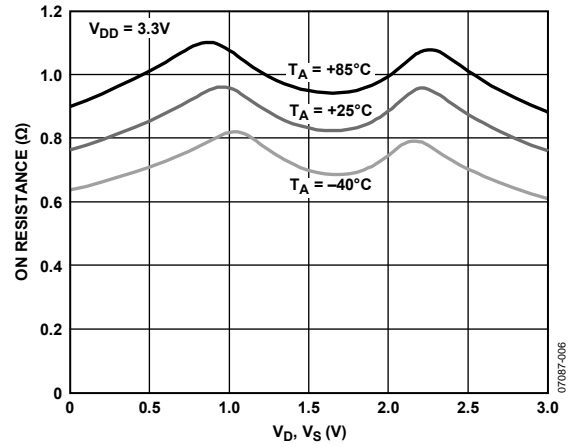


Figure 6. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures,  $V_{DD} = 3.3$  V



Figure 4. On Resistance vs.  $V_D$  ( $V_S$ ),  $V_{DD} = 2.7$  V to 3.6 V

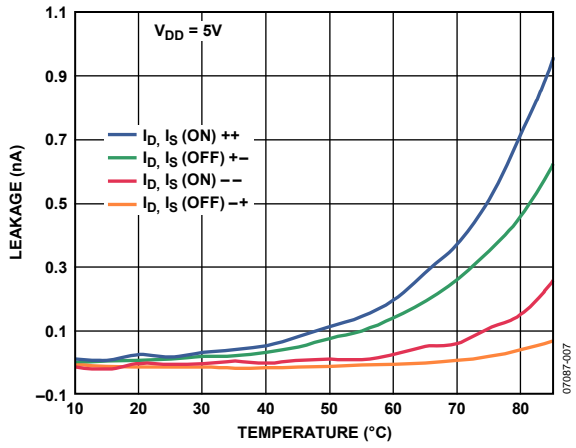


Figure 7. Leakage Current vs. Temperature,  $V_{DD} = 5$  V



Figure 5. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures,  $V_{DD} = 5$  V

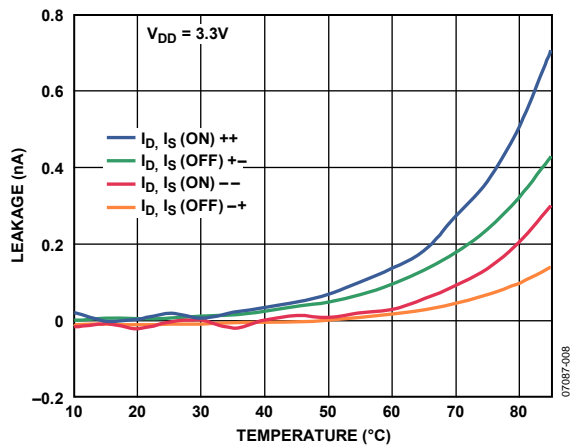


Figure 8. Leakage Current vs. Temperature,  $V_{DD} = 3.3$  V



Figure 9. Charge Injection vs. Source Voltage



Figure 12. Off Isolation vs. Frequency



Figure 10.  $t_{ON}/t_{OFF}$  Times vs. Temperature

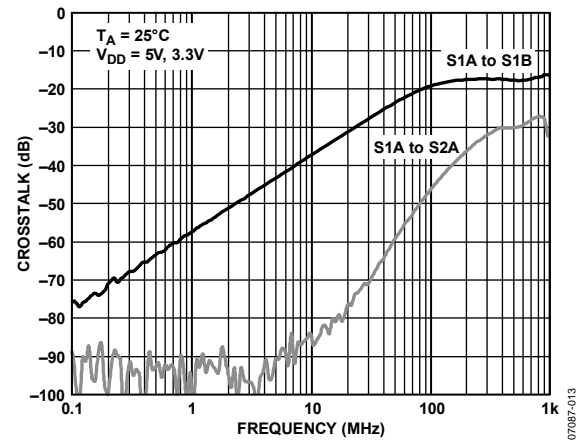


Figure 13. Crosstalk vs. Frequency

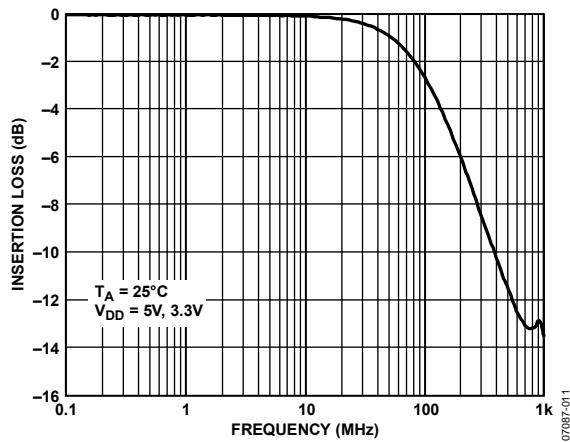


Figure 11. Bandwidth

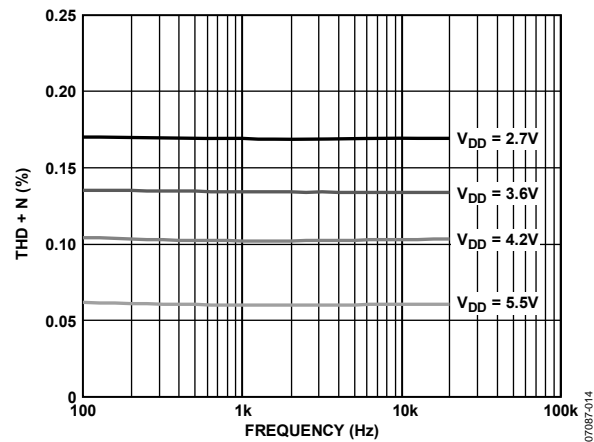


Figure 14. Total Harmonic Distortion + Noise (THD+N) vs. Frequency



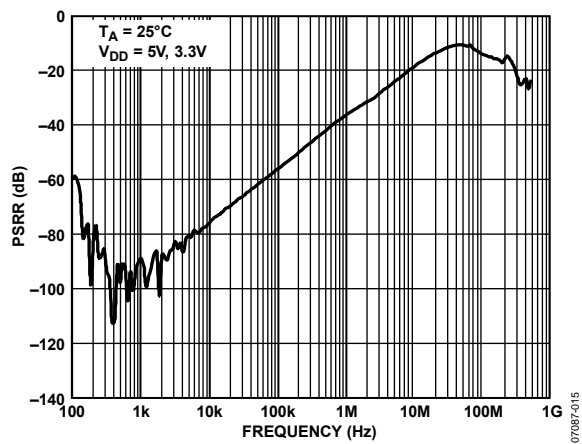


Figure 15. PSRR vs. Frequency

## TEST CIRCUITS



Figure 16. On Resistance

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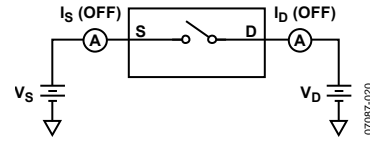


Figure 17. Off Leakage

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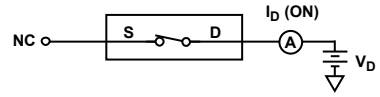


Figure 18. On Leakage

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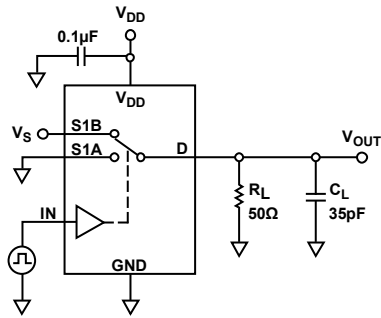
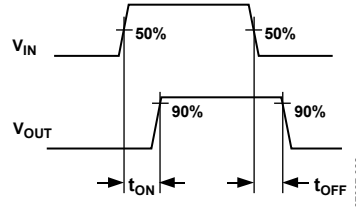


Figure 19. Switching Times,  $t_{ON}$ ,  $t_{OFF}$



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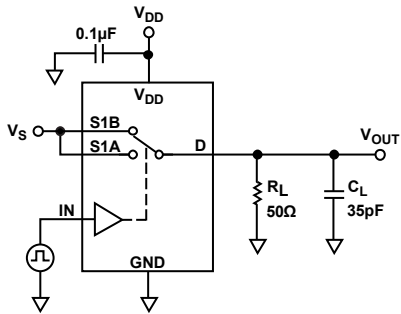


Figure 20. Break-Before-Make Time Delay,  $t_{BBM}$

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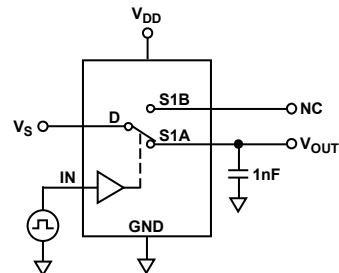
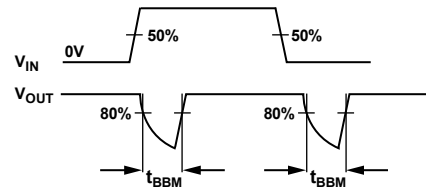
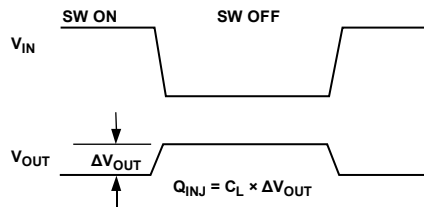


Figure 21. Charge Injection

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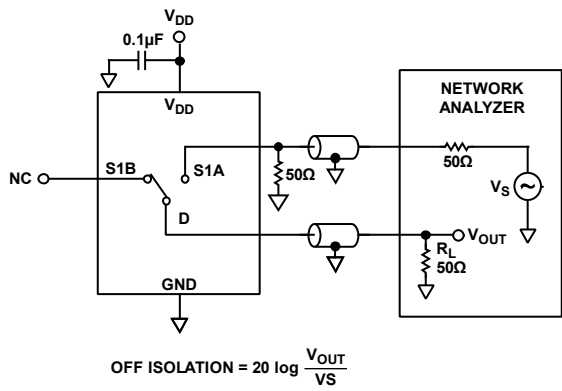


Figure 22. Off Isolation

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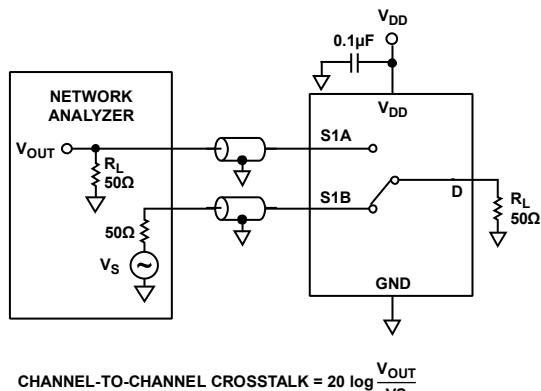


Figure 24. Channel-to-Channel Crosstalk (S1A to S1B/S2A to S2B)

07087-027

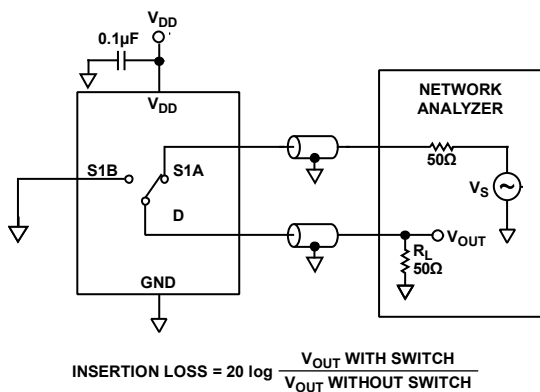


Figure 23. Bandwidth

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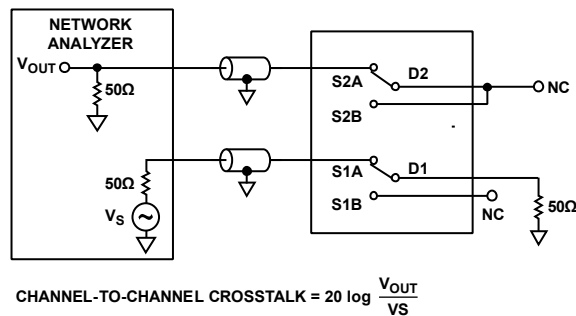


Figure 25. Channel-to-Channel Crosstalk (S1A to S2A, S1B to S2B)

07087-028

## TERMINOLOGY

### **I<sub>DD</sub>**

Positive supply current.

### **V<sub>D</sub> (V<sub>S</sub>)**

Analog voltage on Terminal D and Terminal S.

### **R<sub>ON</sub>**

Ohmic resistance between Terminal D and Terminal S.

### **R<sub>FLAT (ON)</sub>**

The difference between the maximum and minimum values of on resistance as measured on the switch.

### **ΔR<sub>ON</sub>**

On resistance match between any two channels.

### **I<sub>S</sub> (Off)**

Source leakage current with the switch off.

### **I<sub>D</sub> (Off)**

Drain leakage current with the switch off.

### **I<sub>D</sub>, I<sub>S</sub> (On)**

Channel leakage current with the switch on.

### **V<sub>INL</sub>**

Maximum input voltage for Logic 0.

### **V<sub>INH</sub>**

Minimum input voltage for Logic 1.

### **I<sub>INL</sub> (I<sub>INH</sub>)**

Input current of the digital input.

### **C<sub>S</sub> (Off)**

Off switch source capacitance. Measured with reference to ground.

### **C<sub>D</sub> (Off)**

Off switch drain capacitance. Measured with reference to ground.

### **C<sub>D</sub>, C<sub>S</sub> (On)**

On switch capacitance. Measured with reference to ground.

### **C<sub>IN</sub>**

Digital input capacitance.

### **t<sub>ON</sub>**

Delay time between the 50% and 90% points of the digital input and switch on condition.

### **t<sub>OFF</sub>**

Delay time between the 50% and 90% points of the digital input and switch off condition.

### **t<sub>BEM</sub>**

On or off time measured between the 80% points of both switches when switching from one to another.

### **Charge Injection**

Measure of the glitch impulse transferred from the digital input to the analog output during on/off switching.

### **Off Isolation**

Measure of unwanted signal coupling through an off switch.

### **Crosstalk**

Measure of unwanted signal that is coupled from one channel to another because of parasitic capacitance.

### **-3 dB Bandwidth**

Frequency at which the output is attenuated by 3 dB.

### **On Response**

Frequency response of the on switch.

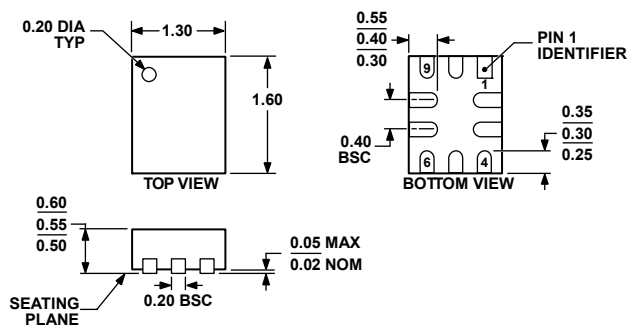
### **Insertion Loss**

The loss due to the on resistance of the switch.

### **THD + N**

Ratio of the harmonics amplitude plus noise of a signal to the fundamental.

## OUTLINE DIMENSIONS



033007-A

Figure 26. 10-Lead Lead Frame Chip Scale Package [LFCSP\_UQ]  
 1.30 × 1.60 mm Body, Ultrathin Quad  
 (CP-10-10)  
 Dimensions shown in millimeters

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADG854BCPZ-REEL <sup>1</sup>	-40°C to +85°C	10-Lead Lead Frame Chip Scale Package [LFCSP_UQ]	CP-10-10	C
ADG854BCPZ-REEL7 <sup>1</sup>	-40°C to +85°C	10-Lead Lead Frame Chip Scale Package [LFCSP_UQ]	CP-10-10	C

<sup>1</sup> Z = RoHS Compliant Part.

**ADG854**

**NOTES**

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