UM11062

TEA1999DB1504 synchronous rectifier controller demo board

Rev. 1.1 — 20 February 2018 User manual

Document information

Information	Content
Keywords	TEA1999DB1504, TEA1999TK, flyback converter, Synchronous Rectifier (SR) driver, HVSON8, high efficiency, power supply, demo board
Abstract	This user manual describes the TEA1999DB1504 demo board. The TEA1999DB1504 demo board can be connected to a flyback converter. The TEA1999DB1504 demo board contains a TEA1999TK SR controller in a HVSON-8 package. Additionally, the TEA1999DB1504 demo board contains two possible options to place power MOSFETs. It replaces the secondary rectification part of the flyback converter.

Revision history

Rev	Date	Description
v.1.1	20180220	updated issue
Modifications:		• Section 5 "Board photographs" has been updated.
v.1	20171201	first issue

1 Introduction

Warning	
 	The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire. This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits. This product shall never be operated unattended.

This document describes the TEA1999DB1504 demo board. A functional description is provided, including instructions about how to connect the board, for the best results and performance. The TEA1999DB1504 demo board contains the secondary part of a single output flyback converter, excluding the output capacitors and the feedback control hardware. To use the TEA1999DB1504 demo board correctly, a flyback converter board in which the demo board can replace the secondary rectifier part is required.

2 Safety warning

The board application is AC mains voltage powered. Avoid touching the board while it is connected to the mains voltage and when it is in operation. An isolated housing is obligatory when used in uncontrolled, non-laboratory environments. Galvanic isolation from the mains phase using a fixed or variable transformer is always recommended.

Figure 1 shows the symbols on how to recognize these devices.

a. Isolated b. Not isolated

Figure 1. Isolation symbols

3 Specifications

Table 1. TEA1999DB1504 specifications

Symbol	Parameter	Value	Conditions
V_{XV}	voltage on pin XV	−0.4 V to +12 V	MOSFET = 60 V
		−0.4 V to +26 V	MOSFET = 100 V
V_{DRAIN}	voltage on pin DRAIN	−0.8 V to +60 V	MOSFET = 60 V
		−0.8 V to +100 V	MOSFET = 100 V
V_{SOURCE}	voltage on pin SOURCE		−0.4 V to +0.4 V
$P_{i(noload)}$	no-load input power	1 mW to 1.5 mW	V_{XV} = 5 V

4 TEA1999TK SR controller

The TEA1999TK is a dedicated controller IC for synchronous rectification on the secondary side of flyback converters. It incorporates the sensing stage and driver stages for driving the SR MOSFET. The SR MOSFET rectifies the output of the secondary transformer winding.

The TEA1999TK can generate its own supply voltage for battery charging applications with low output voltage or for applications with high-side rectification.

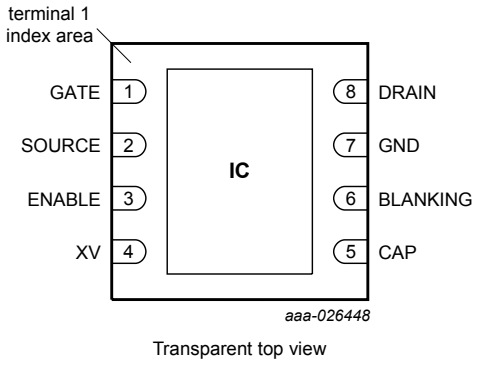
The TEA1999TK can be used in all power supplies that require a high efficiency, like:

- Chargers
- Adapters
- Flyback power supplies with very low and/or variable output voltages

4.1 Features

- Operates in an output voltage range between 26 V and 0 V
- Drain sense pin capable of handling input voltages up to 120 V
- Self-supply function
- Operates with standard and logic level SR MOSFETs
- Supports USB BC, QuickCharge, and smart charging applications
- Adaptive gate drive for fast turn-off at the end of conduction
- Under Voltage Lockout (UVLO) with active gate pull-down
- Blanking input for low and high switching frequency
- Enable input for CCM operation and for disabling at start-up or shorted output

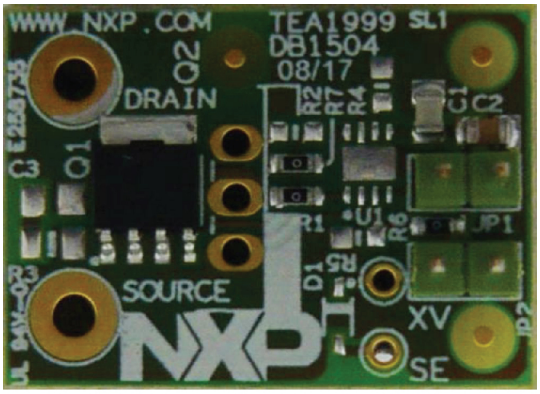
4.2 Pinning



Transparent top view

Figure 2. TEA1999TK pin configuration (SOT782-1)

5 Board photographs



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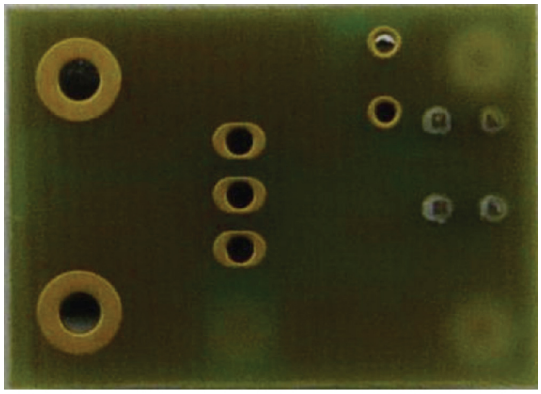
a. Front view



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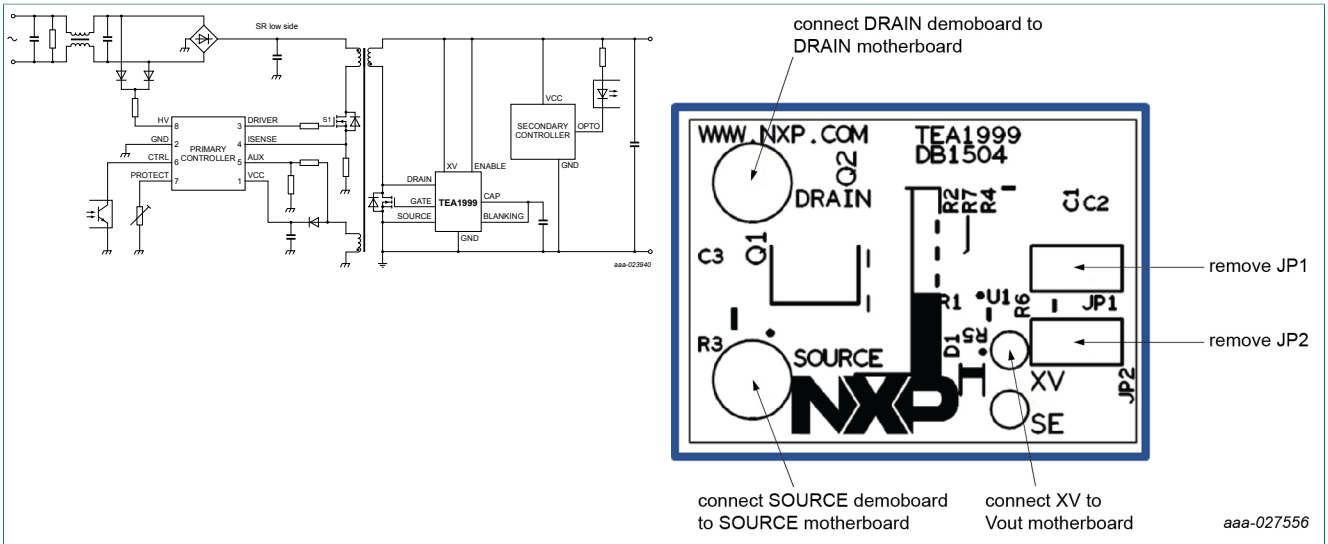
b. Back view

Figure 3. TEA1999DB1504 demo board photographs

Keep the board clean after soldering. For no_clean fluxes, keep the board under pollution degree 1 board conditions (IEC 60065).

6 Board connections

6.1 Connections for low-side SR



a. TEA1999TK default applications

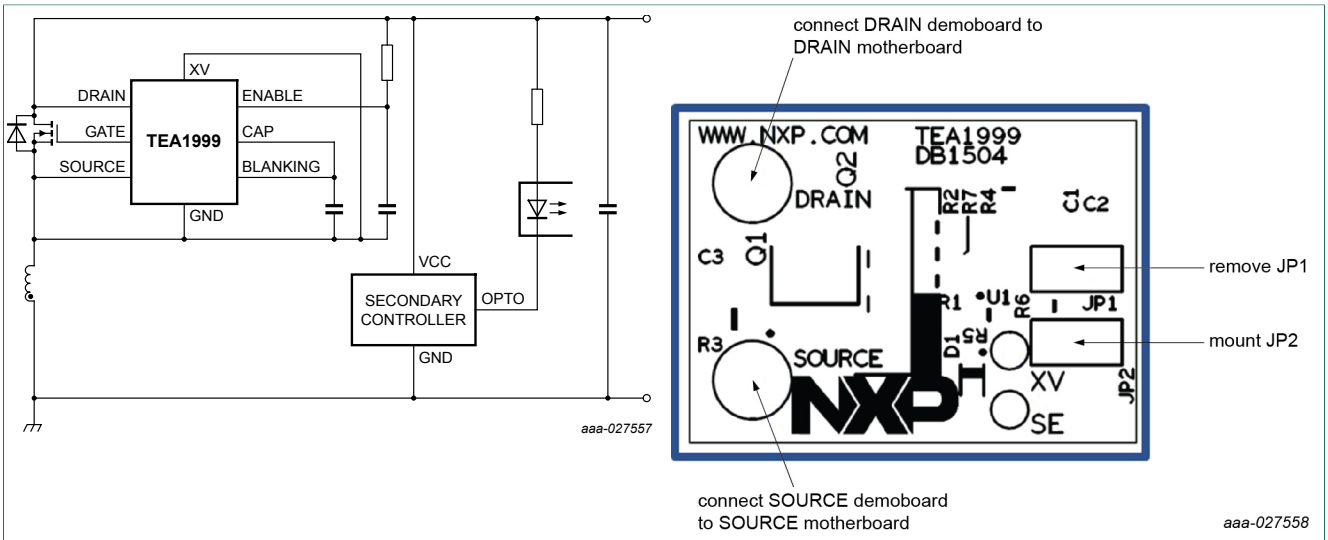
b. TEA1999DB1504 demo board application

Figure 4. Connections for low-side SR

Figure 4 (a) shows the default TEA1999TK application for low-side SR. The drain, gate, and source connection of the TEA1999TK can be coupled directly to the corresponding pins of the MOSFET. Put small, 0 Ω resistors in the drain and gate tracks. To reduce high gate current spikes, the resistor in the gate track can be modified (maximum: 10 Ω). The resistor in the drain track can protect this track from being damaged during pin short conditions. Normally, a snubber provision, like R3/C3 in Figure 4 (b), is also recommended. For low-frequency (up to 150 kHz) applications, the BLANKING pin can be directly connected to the CAP pin. For higher frequencies (> 150 kHz), the BLANKING pin can be connected directly to ground. Connect the ENABLE pin via a low pass R/C filter, which is connected to the output voltage. In this way, the SR gate driver is automatically disabled if output short conditions occur.

Figure 4 (b) shows how to connect the TEA1999DB1504 demo board to an existing application. First, remove the original rectifier circuit in the existing application. The original rectifier circuit consists of either a diode or the combination of an SR controller and a MOSFET. Then, connect the DRAIN, SOURCE, and XV pins of the demo board to the drain, source, and V_{out} connections of the main application with short wires. Also, remove the JP1 and JP2 jumpers. This way, the SR controller functions in a correct way for output voltages up to 12 V and the circuit can be evaluated. For output voltages higher than 12 V (up to 26 V), replace MOSFET Q1 (60 V version) on the demo board with a more robust MOSFET (100 V version).

6.2 Connections for high-side SR with self-supply



a. TEA1999TK default application

b. TEA1999DB1504 demo board application

Figure 5. Connections for high-side SR with self-supply

Figure 5 (a) shows the default TEA1999TK application for high-side SR. The drain, gate, and source connection of the TEA1999TK can be coupled directly to the corresponding pins of the MOSFET. Put small, 0 Ω resistors in the drain and gate tracks. To reduce high gate current spikes, the resistor in the gate track can be modified (maximum: 10 Ω). The resistor in the drain track can protect this track from being damaged during pin short conditions. Normally, a snubber provision, like R3/C3 in Figure 5 (b), is also recommended. For low-frequency (up to 150 kHz) applications, the BLANKING pin can be directly connected to the CAP pin. For higher frequencies (> 150 kHz), the BLANKING pin can be connected directly to ground. The ENABLE pin can best be connected via a low pass R/C filter, which is connected to the output voltage. This way, the SR gate driver is automatically disabled if output short conditions occur.

Figure 5 (b) shows how to connect the TEA1999DB1504 demo board to an existing application. First, remove the original rectifier circuit in the existing application. The original rectifier circuit consists of either a diode or the combination of an SR controller and a MOSFET. Then, connect The DRAIN and SOURCE pins of the demo board to the drain and source connections of the main application with short wires. Remove jumper JP1 and mount jumper JP2. This way, the XV pin is connected to the GND pin and the CAP voltage is charged to a level of approximately 9.8 V. The SR controller functions in a correct way for output voltages up to 12 V and the circuit can be evaluated. For output voltages higher than 12 V (up to 26 V), replace MOSFET Q1 (60 V version) on the demo board with a more robust MOSFET (100 V version).

7 Schematic

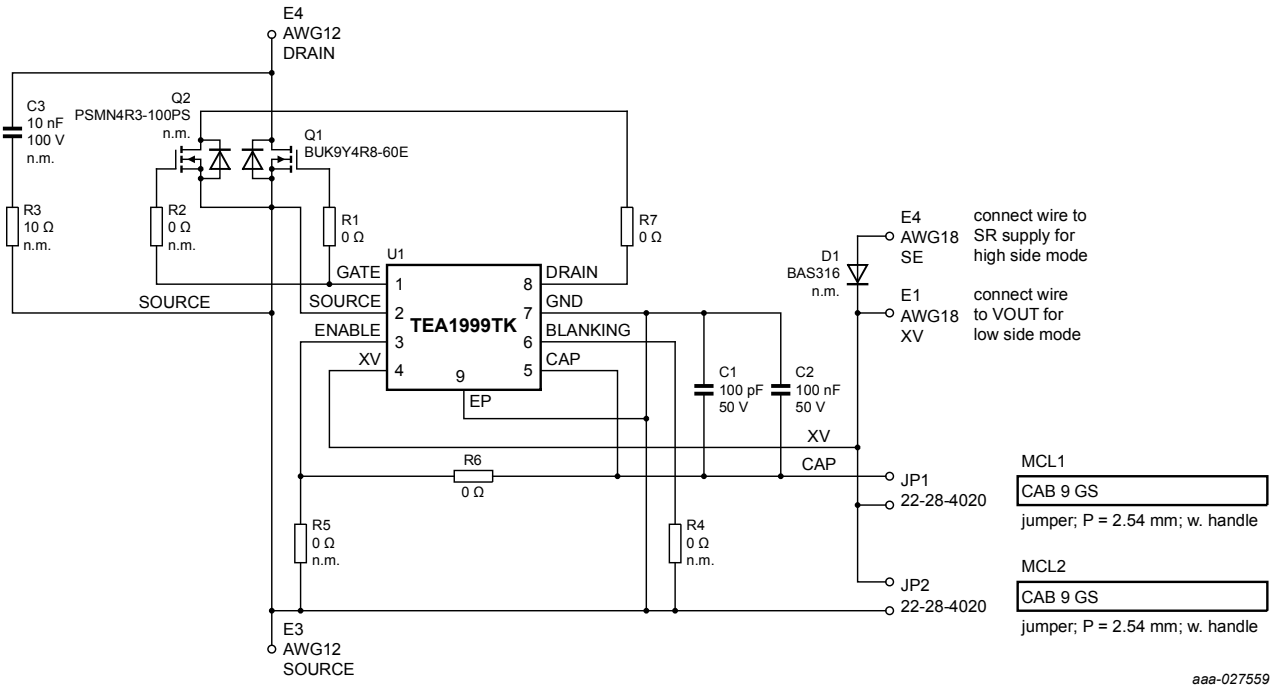


Figure 6. TEA1999DB1504 schematic diagram

Figure 6 shows the schematic diagram of the TEA1999DB1504 demo board. The board incorporates the TEA1999TK controller and a 60 V logic-level power MOSFET. To facilitate easy connection for low-side, high-side, or self-supply applications, some adjustments have been made to the board:

- The ENABLE pin is connected to the CAP pin by default
- The BLANKING pin is left open. However, it has an internal pull-up to the CAP pin
- By default, a 60 V logic level MOSFET is mounted. For applications with an output voltage > 12 V, use a MOSFET type with a higher V_{ds} capability (use a rating of approximately 5 * V_{out})
- By default, jumpers JP1 and JP2 are not mounted (only to be used for high-side applications)

By default, the LFPAK MOSFET Q1 is mounted with a 0 Ω gate resistor (R1). It is also possible to mount a TO220 MOSFET Q2 with gate resistor R2. Capacitors C1 and C2 are decoupling capacitors for the V_{CC} of the TEA1999TK. Connect these capacitors close to the IC.

To ensure sufficient charge power to drive the external MOSFET during the secondary stroke, a value of 100 nF is used for capacitor C2. When a MOSFET with a higher value, which requires much more gate charge, is used, it can be necessary to increase this value for stable operation. To prevent unwanted oscillation of the V_{CC} supply, capacitor C1 is added.

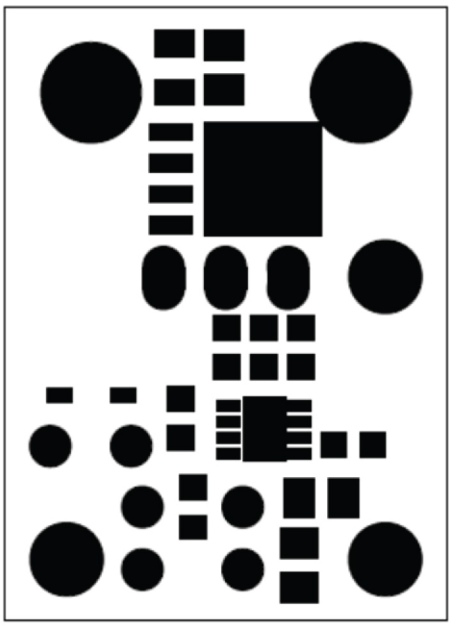
A provision is made for snubber R3/C3. The components are not mounted. However, if high-voltage spikes occur on the drain-source connections of the MOSFETs, they can be added.

8 Bill Of Materials (BOM)

Table 2. TEA1999DB1504 demo board bill of materials

Reference	Description and values	Part number	Manufacturer
C1	capacitor; 100 pF; 10 %; 50 V; C0G; 0805	-	-
C2	capacitor; 100 nF; 10 %; 50 V; X7R; 0805	-	-
C3	capacitor; not mounted; 10 nF; 10 %; 100 V; X7R; 0805	-	-
D1	diode; not mounted; 100 V; 250 mA	BAS316	NXP Semiconductors
E1; E4	wire hole; AWG18; 1 mm	-	-
E2; E3	wire hole; AWG12; 2 mm	-	-
JP1; JP2	header; straight; 1 x 2-way; 2.54 mm	22-28-4020	Molex
MCL1; MCL2	jumper; P = 2.54 mm; without handle	CAB 9 GS	FISCHER
Q1	MOSFET-N; 60 V; 100 A	BUK9Y4R8-60E	NXP Semiconductors
Q2	MOSFET-N; not mounted; 100 V; 120 A	PSMN4R3-100PS	NXP Semiconductors
R1; R6; R7	resistor; 0 Ω; jumper; 63 mW; 0603	-	-
R2; R4; R5	resistor; not mounted; 0 Ω; jumper; 63 mW; 0603	-	-
R3	resistor; not mounted; 10 Ω; 1 %; 100 mW; 0805	-	-
U1	synchronous rectifier controller; TEA1999TK	TEA1999TK	NXP Semiconductors

9 Layout



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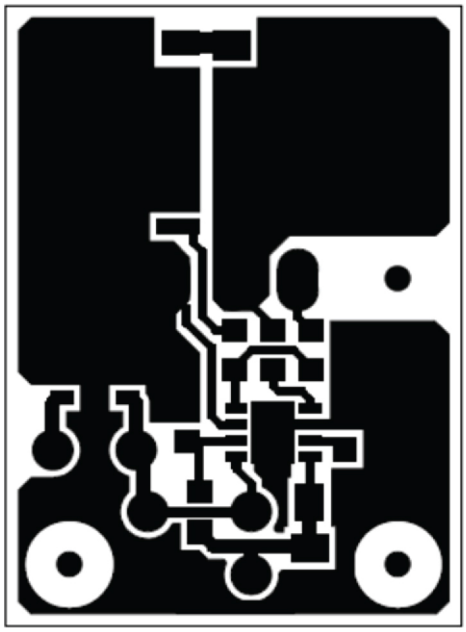
a. Front view



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b. Back view

Figure 7. TEA1999DB1504 demo board layout

Some important guidelines for a good layout:

- Keep the trace from the DRAIN pin to the MOSFET drain as short as possible.
- Keep the trace from the SOURCE pin to the MOSFET source as short as possible.
- Keep the area of the loop from the DRAIN pin to the MOSFET drain, to the MOSFET source, and to the SOURCE pin as small as possible. Ensure that the overlap of this loop over the power drain track or the power source track is as small as possible. Take care that the two loops do not cross each other.
- Keep the track from the GATE pin to the gate of the MOSFET as short as possible.
- Use separate clean tracks for the XV and the GND pins. If possible, use a small ground plane underneath the IC, which improves the heat dispersion.

10 Abbreviations

Table 3. Abbreviations

Acronym	Description
CCM	Continuous Conduction Mode
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
SR	Synchronous Rectifier
UVLO	UnderVoltage LockOut
IC	Integrated Circuit
USB BC	Universal Serial Bus Battery Charging

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