



# Low-Voltage, High-Speed, Quad, SPST CMOS Analog Switches

MAX4614/MAX4615/MAX4616

## General Description

## Features

The MAX4614/MAX4615/MAX4616 quad, low-voltage, high-speed, single-pole/single-throw (SPST) analog switches are pin compatible with the industry-standard 74HC4066/MAX4610 analog switches. On-resistance ( $10\Omega$  max) is matched between switches to  $1\Omega$  max and is flat ( $1\Omega$  max) over the specified signal range. Each switch handles  $V+$  to GND analog signal levels. Maximum off-leakage current is only  $1\text{nA}$  at  $T_A = +25^\circ\text{C}$  and  $6\text{nA}$  at  $T_A = +85^\circ\text{C}$ .

The MAX4614 has four normally open (NO) switches, and the MAX4615 has four normally closed (NC) switches. The MAX4616 has two NO switches and two NC switches. These CMOS switches operate from a single  $+2\text{V}$  to  $+5.5\text{V}$  supply. All digital inputs have  $+0.8\text{V}$  and  $+2.4\text{V}$  logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single  $+5\text{V}$  supply.

- ♦ **Fast Switching Times**  
12ns  $t_{\text{ON}}$ , 10ns  $t_{\text{OFF}}$
- ♦ **Pin Compatible with Industry-Standard 74HC4066/MAX4610**
- ♦ **Guaranteed On-Resistance**  
10 $\Omega$  max (+5V supply)  
20 $\Omega$  max (+3V supply)
- ♦ **Guaranteed Match Between Channels (1 $\Omega$  max)**
- ♦ **Guaranteed Flatness Over Signal Range (1 $\Omega$  max)**
- ♦ **<6nA Off-Leakage Current Over Temperature ( $T_A = +85^\circ\text{C}$ )**
- ♦ **Rail-to-Rail<sup>®</sup> Signal Handling**
- ♦ **TTL/CMOS-Logic Compatible**

## Applications

## Ordering Information

- Battery-Operated Equipment
- Audio/Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Sample-and-Hold Circuits
- Communication Circuits

PART	TEMP. RANGE	PIN-PACKAGE
MAX4614CUD	0°C to +70°C	14 TSSOP
MAX4614CSD	0°C to +70°C	14 Narrow SO
MAX4614CPD	0°C to +70°C	14 Plastic DIP
MAX4614EUD	-40°C to +85°C	14 TSSOP
MAX4614ESD	-40°C to +85°C	14 Narrow SO
MAX4614EPD	-40°C to +85°C	14 Plastic DIP

Ordering Information continued at end of data sheet.

## Pin Configurations/Truth Tables

TOP VIEW

**MAX4614**

TSSOP/SO/DIP

INPUT	SWITCH STATE
LOW	OFF
HIGH	ON

**MAX4615**

TSSOP/SO/DIP

INPUT	SWITCH STATE
LOW	ON
HIGH	OFF

**MAX4616**

TSSOP/SO/DIP

INPUT	NO1, NO3	NC2, NC4
LOW	OFF	ON
HIGH	ON	OFF

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.



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# Low-Voltage, High-Speed, Quad, SPST CMOS Analog Switches

## ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND)

V+, IN_	.....-0.3V to +6V
COM_, NO_, NC_ (Note 1)	.....-0.3V to (V+ + 0.03V)
Continuous Current (any terminal)	.....±75mA
Peak Current (NO_, NC_, COM_) (pulsed at 1ms, 10% duty cycle)	.....±200mA

Continuous Power Dissipation (TA = +70°C)

14-Pin TSSOP (derate 6.3mW/°C above +70°C)	.....500mW
14-Pin Narrow SO (derate 8.00mW/°C above +70°C)	...640mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C)	...800mW

Operating Temperature Ranges

MAX461_C_	.....0°C to +70°C
MAX461_E_	.....-40°C to +85°C
Storage Temperature Range	.....-65°C to +150°C
Lead Temperature (soldering, 10sec)	.....+300°C

**Note 1:** Signals on NO\_, NC\_, or COM\_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, VIN\_H = 2.4V, VIN\_L = 0.8V, TA = TMIN to TMAX, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
<b>ANALOG SWITCH</b>							
Analog Signal Range (Note 3)	VCOM_, VNO_, VNC_			0		V+	V
On-Resistance	RON	V+ = 4.5V, ICOM_ = 10mA, VNO_ = VNC_ = 3V	TA = +25°C	8	10		Ω
			TA = TMIN to TMAX			13	
On-Resistance Match Between Channels (Note 4)	ΔRON	V+ = 4.5V, ICOM_ = 10mA, VNO_ = VNC_ = 3V	TA = +25°C	0.2	1		Ω
			TA = TMIN to TMAX			1.2	
On-Resistance Flatness (Note 5)	RFLAT(ON)	V+ = 4.5V; ICOM_ = 10mA; VNO_ = VNC_ = 3V, 2V, 1V	TA = +25°C	0.3	1		Ω
			TA = TMIN to TMAX			1.2	
NO_ or NC_ Off-Leakage Current (Note 6)	INO(OFF)	V+ = 5.5V; VCOM_ = 1V, 4.5V; VNO_ = 4.5V, 1V	TA = +25°C	-1	0.01	1	nA
			TA = TMIN to TMAX	-6		6	
COM_ Off-Leakage Current (Note 6)	ICOM(OFF)	V+ = 5.5V; VCOM_ = 1V, 4.5V; VNO_ = VNC_ = 4.5V, 1V	TA = +25°C	-1	0.01	1	nA
			TA = TMIN to TMAX	-6		6	
COM_ On-Leakage Current (Note 6)	ICOM(ON)	V+ = 5.5V; VCOM_ = 1V, 4.5V; VNO_ = VNC_ = 1V, 4.5V, or floating	TA = +25°C	-2	0.02	2	nA
			TA = TMIN to TMAX	-12		12	

# Low-Voltage, High-Speed, Quad, SPST CMOS Analog Switches

MAX4614/MAX4615/MAX4616

## ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +5V ±10%, V<sub>IN\_H</sub> = 2.4V, V<sub>IN\_L</sub> = 0.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>LOGIC INPUT</b>							
Input Current with Input Voltage High	I <sub>IN_H</sub>	V <sub>IN_</sub> = 2.4V	-10	0.3	10	nA	
Input Current with Input Voltage Low	I <sub>IN_L</sub>	V <sub>IN_</sub> = 0.8V	-10	0.3	10	nA	
Input Voltage High	V <sub>IN_H</sub>		2.4			V	
Input Voltage Low	V <sub>IN_L</sub>				0.8	V	
<b>SWITCH DYNAMIC</b>							
Turn-On Time (Note 3)	t <sub>ON</sub>	V <sub>COM_</sub> = 3V, Figure 2	T <sub>A</sub> = +25°C		5	12	ns
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			14	
Turn-Off Time (Note 3)	t <sub>OFF</sub>	V <sub>COM_</sub> = 3V, Figure 2	T <sub>A</sub> = +25°C		2.5	10	ns
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			12	
On-Channel Bandwidth	BW	Signal = 0dBm, Figure 4, 50Ω in and out, T <sub>A</sub> = +25°C		70		MHz	
Charge Injection	Q	Signal = 0dBm, Figure 4, 50Ω in and out, T <sub>A</sub> = +25°C		6.5		pC	
Off-Isolation (Note 7)	V <sub>ISO</sub>	R <sub>L</sub> = 50Ω, f = 100kHz, Figure 4, T <sub>A</sub> = +25°C		-85		dB	
Crosstalk (Note 8)	V <sub>CT</sub>	R <sub>L</sub> = 50Ω, f = 100kHz, Figure 5, T <sub>A</sub> = +25°C		-96		dB	
NO_ or NC_ Capacitance	C <sub>(OFF)</sub>	f = 1MHz, Figure 6, T <sub>A</sub> = +25°C		5		pF	
COM_ Off-Capacitance	C <sub>COM(OFF)</sub>	f = 1MHz, Figure 6, T <sub>A</sub> = +25°C		5		pF	
COM_ On-Capacitance	C <sub>COM(ON)</sub>	f = 1MHz, Figure 6, T <sub>A</sub> = +25°C		11		pF	
Total Harmonic Distortion	THD	600Ω IN and OUT, f = 20Hz to 20kHz, 2Vp-p, T <sub>A</sub> = +25°C		0.034		%	
<b>POWER SUPPLY</b>							
Power-Supply Range			2		5.5	V	
Power-Supply Current	I+	V <sub>IN</sub> = 0 or V+, all switches on or off	-1	0.001	1	μA	

# Low-Voltage, High-Speed, Quad, SPST CMOS Analog Switches

## ELECTRICAL CHARACTERISTICS—Single +3.3V Supply

(V+ = +3.3V ±10%, VIN\_H = 2.4V, VIN\_L = 0.5V, TA = TMIN to TMAX, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>ANALOG SWITCH</b>							
Analog Signal Range (Note 3)	VCOM_, VNO_, VNC_		0		V+	V	
On-Resistance	RON	V+ = 3V, INO = 10mA, VCOM_ = 1.5V	TA = +25°C	8	20	Ω	
			TA = TMIN to TMAX		25		
On-Resistance Match Between Channels (Note 4)	ΔRON	V+ = 3V, ICOM_ = 1mA, VNO_ = VNC_ = 1.5V	TA = +25°C	0.5	1.5	Ω	
			TA = TMIN to TMAX		2		
NO_ or NC_ Off-Leakage Current (Notes 3, 6)	INO(OFF)	V+ = 3.6V; VCOM_ = 1V, 3V; VNO_ = VNC_ = 3V, 1V	TA = +25°C	-1	0.002	1	nA
			TA = TMIN to TMAX	-10		10	
COM_ Off-Leakage Current (Notes 3, 6)	ICOM(OFF)	V+ = 3.6V; VCOM_ = 1V, 3V; VNO_ = VNC_ = 3V, 1V	TA = +25°C	-1	0.002	1	nA
			TA = TMIN to TMAX	-10		10	
COM_ On-Leakage Current (Notes 3, 6)	ICOM(ON)	V+ = 3.6V; VCOM_ = 1V, 3V; VNO_ = VNC_ = 1V, 3V, or floating	TA = +25°C	-1	0.002	1	nA
			TA = TMIN to TMAX	-10		10	
<b>LOGIC INPUT</b>							
Input Current with Input Voltage High	IIN_H	VIN_ = 2V	-10	0.003	10	nA	
Input Current with Input Voltage Low	IIN_L	VIN_ = 0.8V	-10	0.003	10	nA	
Input Voltage High	VIN_H		2.0			V	
Input Voltage Low	VIN_L				0.8	V	
<b>SWITCH DYNAMIC</b> (Note 3)							
Turn-On Time	tON	VCOM_ = 1.5V, Figure 2	TA = +25°C	6	15	ns	
			TA = TMIN to TMAX		20		
Turn-Off Time	tOFF	VCOM_ = 1.5V, Figure 2	TA = +25°C	4	12	ns	
			TA = TMIN to TMAX		15		
Charge Injection	Q	CL = 1nF, VGEN = 0, RGEN = 0, TA = +25°C		6.5		pC	
<b>POWER SUPPLY</b>							
Power-Supply Current	I+	V+ = 3.6V, VIN = 0 or V+, all channels on or off	-1	0.001	1	μA	

# Low-Voltage, High-Speed, Quad, SPST CMOS Analog Switches

MAX4614/MAX4615/MAX4616

## ELECTRICAL CHARACTERISTICS—Single +2.5V Supply

(V+ = +2.5V, VINH = 0.7VCC, VINL = 0.5V, TA = TMIN to TMAX, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
<b>ANALOG SWITCH</b>							
Analog Signal Range (Note 3)	VCOM_, VNO_, VNC_			0		V+	V
COM_ to NO_ or NC_ On-Resistance	RON	V+ = 2.5V, ICOM_ = 10mA, VNO = 1.2V	TA = +25°C		30	60	Ω
			TA = TMIN to TMAX			100	
<b>SWITCH DYNAMIC</b> (Note 3)							
Turn-On Time	tON	VNO_ or VNC_ = 1V, TA = +25°C			6.5		ns
Turn-Off Time	tOFF	VNO_ or VNC_ = 1V, TA = +25°C			2.8		ns

**Note 2:** The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

**Note 3:** Guaranteed by design.

**Note 4:**  $\Delta R_{ON} = R_{ON}(\text{max}) - R_{ON}(\text{min})$ .

**Note 5:** Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

**Note 6:** Leakage parameters are 100% tested at maximum-rated hot temperature and guaranteed by correlation at +25°C.

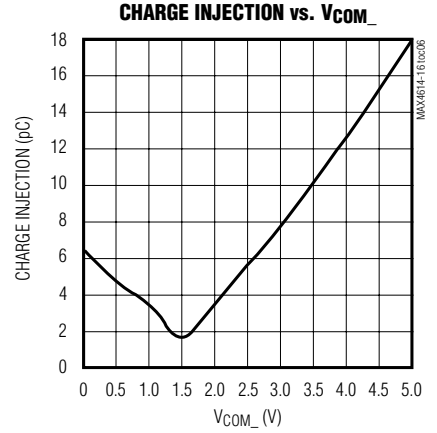
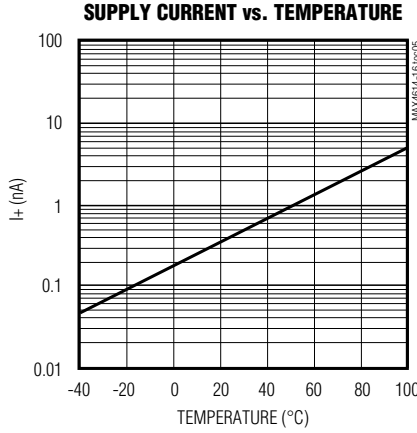
**Note 7:** Off-Isolation =  $20\log_{10}(V_{COM\_} / V_{NO\_})$ , VCOM\_ = output, VNO\_ = input to off switch.

**Note 8:** Between any two switches.

# Low-Voltage, High-Speed, Quad, SPST CMOS Analog Switches

## Typical Operating Characteristics

(V+ = +5V, GND = 0, TA = +25°C, unless otherwise noted.)



# Low-Voltage, High-Speed, Quad, SPST CMOS Analog Switches

## Typical Operating Characteristics (continued)

( $V_+ = +5V$ ,  $GND = 0$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



## Pin Description

PIN			NAME	FUNCTION
MAX4614	MAX4615	MAX4616		
1, 3, 8	—	1, 8	NO1–NO3	Analog Switch Normally Open Terminal (bidirectional)
—	1, 3, 8	—	NC1–NC3	Analog Switch Normally Closed Terminal (bidirectional)
—	—	3	NC2	Analog Switch Normally Closed Terminal (bidirectional)
2, 4, 9, 10	2, 4, 9, 10	2, 4, 9, 10	COM1–COM4	Analog Switch Common Terminal (bidirectional)
5, 6, 12, 13	5, 6, 12, 13	5, 6, 12, 13	IN1–IN4	Logic Control Inputs
7	7	7	GND	Ground
—	11	11	NC4	Analog Switch Normally Closed Terminal (bidirectional)
11	—	—	NO4	Analog Switch Normally Open Terminal (bidirectional)
14	14	14	$V_+$	Positive Supply Voltage

MAX4614/MAX4615/MAX4616

# Low-Voltage, High-Speed, Quad, SPST CMOS Analog Switches

## Applications Information

### Power-Supply Sequencing and Overvoltage Protection

Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals or logic inputs, especially if the analog or logic signals are not current limited. If this sequencing is not possible, and if the analog or logic inputs are not current limited to 20mA, add a small-signal diode (D1) as shown in Figure 1. If the analog signal can dip below GND, add D2. Adding protection diodes reduces the analog signal range to a diode drop (about 0.7V) below V+ (for D1), and to a diode drop above ground (for D2). Leakage is unaffected by adding the diodes. On-resistance increases by a small amount at low supply voltages. Maximum supply voltage (V+) must not exceed 6V.

Adding protection diodes causes the logic thresholds to be shifted relative to the power-supply rails. This can be significant when low supply voltages (+5V or less) are used. With a +5V supply, TTL compatibility is not guaranteed when protection diodes are added. Driving IN1 and IN2 all the way to the supply rails (i.e., to a



Figure 1. Overvoltage Protection Using Two External Blocking Diodes

diode drop higher than the V+ pin, or to a diode drop lower than the GND pin) is always acceptable.

Protection diodes D1 and D2 also protect against some overvoltage situations. With Figure 1's circuit, if the supply voltage is below the absolute maximum rating, and if a fault voltage up to the absolute maximum rating is applied to an analog signal pin, no damage will result.

## Test Circuits/Timing Diagrams



Figure 2. Switching Time



# Low-Voltage, High-Speed, Quad, SPST CMOS Analog Switches

## Test Circuits/Timing Diagrams (continued)

MAX4614/MAX4615/MAX4616



Figure 3. Charge Injection



Figure 4. Off-Isolation/On-Channel Bandwidth



Figure 5. Crosstalk

# Low-Voltage, High-Speed, Quad, SPST CMOS Analog Switches

## Test Circuits/Timing Diagrams (continued)

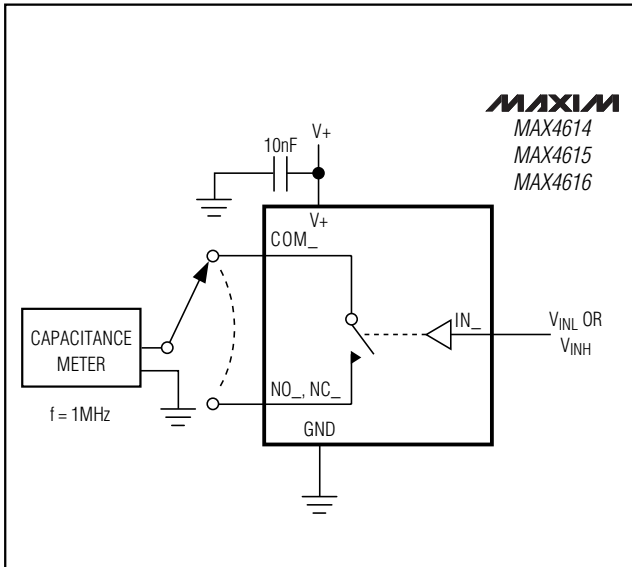


Figure 6. Channel Off/On-Capacitance

## Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
<b>MAX4615CUD</b>	0°C to +70°C	14 TSSOP
MAX4615CSD	0°C to +70°C	14 Narrow SO
MAX4615CPD	0°C to +70°C	14 Plastic DIP
MAX4615EUD	-40°C to +85°C	14 TSSOP
MAX4615ESD	-40°C to +85°C	14 Narrow SO
MAX4615EPD	-40°C to +85°C	14 Plastic DIP
<b>MAX4616CUD</b>	0°C to +70°C	14 TSSOP
MAX4616CSD	0°C to +70°C	14 Narrow SO
MAX4616CPD	0°C to +70°C	14 Plastic DIP
MAX4616EUD	-40°C to +85°C	14 TSSOP
MAX4616ESD	-40°C to +85°C	14 Narrow SO
MAX4616EPD	-40°C to +85°C	14 Plastic DIP

## Chip Information

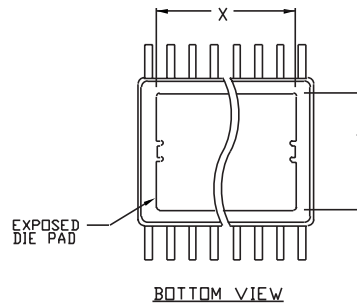
TRANSISTOR COUNT: 89

# Low-Voltage, High-Speed, Quad, SPST CMOS Analog Switches

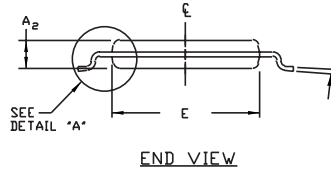
## Package Information

MAX4614/MAX4615/MAX4616

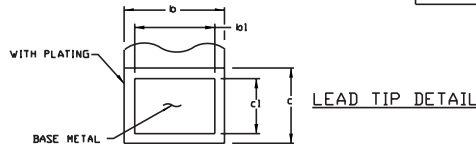
TSSOP EP5



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10	—	.043
A <sub>1</sub>	0.05	0.15	.002	.006
A <sub>2</sub>	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b <sub>1</sub>	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c <sub>1</sub>	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	.112	.124
α	0°	8°	0°	8°



JEDEC	N	VARIATIONS				
		MILLIMETERS		INCHES		
		MIN.	MAX.	MIN.	MAX.	
AB	14	D	4.90	5.10	.193	.201
AC	16	D	4.90	5.10	.193	.201
AC-EP	16	D	4.90	5.10	.193	.201
		X	2.85	3.15	.112	.124
AD	20	D	6.40	6.60	.252	.260
AD-EP	20	D	6.40	6.60	.252	.260
		X	4.00	4.34	.157	.171
AE	24	D	7.70	7.90	.303	.311
AF	28	D	9.60	9.80	.378	.386
AF-EP		D	9.60	9.80	.378	.386
		X	5.35	5.65	.211	.222



- NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
  2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 mm PER SIDE.
  3. CONTROLLING DIMENSION: MILLIMETER.
  4. MEETS JEDEC OUTLINE MD-153 VARIATIONS AB, AC, AD, AE, AF.
  5. DIMENSIONS X AND Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY.
  6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".

<b>MAXIM</b>			
PROPRIETARY INFORMATION			
TITLE: PACKAGE OUTLINE, TSSOP, 4.40mm BODY, 0.65mm PITCH			
APPROVAL	DOCUMENT CONTROL NO. 21-0066	REV C	1/1

# Low-Voltage, High-Speed, Quad, SPST CMOS Analog Switches

## Package Information (continued)

	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS		N	MS012
	MIN	MAX	MIN	MAX		
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:  
 1. D&E DO NOT INCLUDE MOLD FLASH  
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")  
 3. LEADS TO BE COPLANAR WITHIN .102mm (.004")  
 4. CONTROLLING DIMENSION: MILLIMETER  
 5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE  
 6. N = NUMBER OF PINS

**MAXIM** 120 SAN GABRIEL DR. SUNNYVALE CA 94086 FAX (408) 737-7704 PROPRIETARY INFORMATION  
 PACKAGE FAMILY OUTLINE: SOIC .150" 1/1  
 21-0041 A DOCUMENT CONTROL NUMBER REV

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