

## FEATURES

**Voltage noise density: 2.8 nV/ $\sqrt{\text{Hz}}$  typical**

**Peak-to-peak noise: 77 nV p-p typical**

**Gain bandwidth product: 10 MHz**

**Low input bias current: 14 nA maximum**

**Low offset voltage: 75  $\mu\text{V}$  maximum**

**High open-loop gain: 1000 V/mV (120 dB)**

**Low supply current per amplifier: 3 mA typical**

**Dual-supply operation:  $\pm 5\text{ V}$  to  $\pm 15\text{ V}$**

**Unity-gain stable**

**No phase reversal**

## ENHANCED PRODUCT FEATURES

**Supports defense and aerospace applications (AQEC standard)**

**Extended temperature range:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$**

**Controlled manufacturing baseline**

**One assembly/test site**

**One fabrication site**

**Enhanced product change notification**

**Qualification data available on request**

## APPLICATIONS

**Phase-locked loop (PLL) filters**

**Filters for GPS**

**Instrumentation**

**Sensors and controls**

**Professional quality audio**

## PIN CONFIGURATION

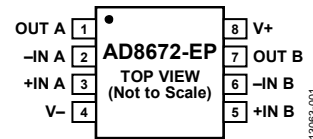


Figure 1.

## GENERAL DESCRIPTION

The **AD8672-EP** is a very high precision amplifier featuring very low noise, very low offset voltage and drift, low input bias current, 10 MHz bandwidth, and low power consumption. Outputs are stable with capacitive loads of over 1000 pF. Supply current is less than 3 mA per amplifier at 30 V.

The combination of ultralow noise, high precision, speed, and stability within the **AD8672-EP** is unmatched. Applications for this amplifier include high quality PLL filters, precision filters, medical and analytical instrumentation, precision power supply controls, ATE, data acquisition, and precision controls, as well as professional quality audio.

The **AD8672-EP** is available in an 8-lead SOIC narrow package. It is specified over a  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  temperature range.

Additional application and technical information can be found in the **AD8672** data sheet.

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**REVISION HISTORY**

9/15—Revision 0: Initial Version

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS, $\pm 5$ V

$V_{SY} = \pm 5.0$  V,  $V_{CM} = 0$  V,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-55^\circ\text{C} < T_A < +125^\circ\text{C}$		20	75	$\mu\text{V}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-55^\circ\text{C} < T_A < +125^\circ\text{C}$		30	125	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	$25^\circ\text{C} < T_A < 125^\circ\text{C}$	-14	+3	+14	nA
		$-55^\circ\text{C} < T_A < +125^\circ\text{C}$	-20	+5	+20	nA
Input Offset Current	$I_{OS}$	$25^\circ\text{C} < T_A < 125^\circ\text{C}$	-60	+8	+60	nA
		$-55^\circ\text{C} < T_A < +125^\circ\text{C}$	-14	+6	+14	nA
		$25^\circ\text{C} < T_A < 125^\circ\text{C}$	-20	+6	+20	nA
		$-55^\circ\text{C} < T_A < +125^\circ\text{C}$	-60	+8	+60	nA
Input Voltage Range			-2.5		+2.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -2.5$ V to $+2.5$ V	100	120		dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2$ k $\Omega$ , $V_O = -3$ V to $+3$ V	1000	6000		V/mV
Input Capacitance						
Common Mode	$C_{INCM}$			6.25		pF
Differential Mode	$C_{INDM}$			7.5		pF
Input Resistance						
Common Mode	$R_{IN}$			3.5		G $\Omega$
Differential Mode	$R_{INDM}$			15		M $\Omega$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage						
High	$V_{OH}$	$R_L = 2$ k $\Omega$ , $-55^\circ\text{C}$ to $+125^\circ\text{C}$	+3.8	+4.0		V
		$R_L = 600$ $\Omega$	+3.7	+3.9		V
Low	$V_{OL}$	$R_L = 2$ k $\Omega$ , $-55^\circ\text{C}$ to $+125^\circ\text{C}$		-3.9	-3.8	V
		$R_L = 600$ $\Omega$		-3.8	-3.7	V
Output Current	$I_{OUT}$			$\pm 10$		mA
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4$ V to $\pm 18$ V	110	130		dB
Supply Current per Amplifier	$I_{SY}$	$V_O = 0$ V $-55^\circ\text{C} < T_A < +125^\circ\text{C}$		3	3.5	mA
					4.2	mA
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2$ k $\Omega$		4		V/ $\mu\text{s}$
Settling Time	$t_S$	To 0.1% (4 V step, $G = 1$ )		1.4		$\mu\text{s}$
		To 0.01% (4 V step, $G = 1$ )		5.1		$\mu\text{s}$
Gain Bandwidth Product	GBP			10		MHz
<b>NOISE PERFORMANCE</b>						
Peak-to-Peak Noise	$e_{n\text{ p-p}}$	0.1 Hz to 10 Hz		77	100	nV p-p
Voltage Noise Density	$e_n$	$f = 1$ kHz		2.8	3.8	nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1$ kHz		0.3		pA/ $\sqrt{\text{Hz}}$
Channel Separation	$C_S$	$f = 1$ kHz		-130		dB
		$f = 10$ kHz		-105		dB

**ELECTRICAL CHARACTERISTICS,  $\pm 15$  V**

$V_S = \pm 15.0$  V,  $V_{CM} = 0$  V,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$			20	75	$\mu\text{V}$
		$-55^\circ\text{C} < T_A < +125^\circ\text{C}$		30	125	$\mu\text{V}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-55^\circ\text{C} < T_A < +125^\circ\text{C}$		0.3	0.8	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$		-14	+3	+14	nA
		$25^\circ\text{C} < T_A < 125^\circ\text{C}$	-20	+5	+20	nA
		$-55^\circ\text{C} < T_A < +125^\circ\text{C}$	-60	+8	+60	nA
Input Offset Current	$I_{OS}$		-14	+6	+14	nA
		$25^\circ\text{C} < T_A < 125^\circ\text{C}$	-20	+6	+20	nA
		$-55^\circ\text{C} < T_A < +125^\circ\text{C}$	-60	+8	+60	nA
Input Voltage Range			-12		+12	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -12$ V to +12 V	100	120		dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2$ k $\Omega$ , $V_O = -10$ V to +10 V	1000	6000		V/mV
Input Capacitance						
Common Mode	$C_{INCM}$			6.25		pF
Differential Mode	$C_{INDM}$			7.5		pF
Input Resistance						
Common Mode	$R_{IN}$			3.5		G $\Omega$
Differential Mode	$R_{INDM}$			15		M $\Omega$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage						
High	$V_{OH}$	$R_L = 2$ k $\Omega$ , $-55^\circ\text{C}$ to $+125^\circ\text{C}$	13.2	13.8		V
		$R_L = 600$ $\Omega$	11	12.3		V
Low	$V_{OL}$	$R_L = 2$ k $\Omega$ , $-55^\circ\text{C}$ to $+125^\circ\text{C}$		-13.8	-13.2	V
		$R_L = 600$ $\Omega$		-12.4	-11	V
Output Current	$I_{OUT}$			$\pm 20$		mA
Short Circuit Current	$I_{SC}$			$\pm 30$		mA
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4$ V to $\pm 18$ V	110	130		dB
Supply Current per Amplifier	$I_{SY}$	$V_O = 0$ V $-55^\circ\text{C} < T_A < +125^\circ\text{C}$		3	3.5	mA
					4.2	mA
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2$ k $\Omega$		4		V/ $\mu\text{s}$
Settling Time	$t_s$	To 0.1% (10 V step, $G = 1$ )		2.2		$\mu\text{s}$
		To 0.01% (10 V step, $G = 1$ )		6.3		$\mu\text{s}$
Gain Bandwidth Product	GBP			10		MHz
<b>NOISE PERFORMANCE</b>						
Peak-to-Peak Noise	$e_{n\text{ p-p}}$	0.1 Hz to 10 Hz		77	100	nV p-p
Voltage Noise Density	$e_n$	$f = 1$ kHz		2.8	3.8	nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1$ kHz		0.3		pA/ $\sqrt{\text{Hz}}$
Channel Separation	$C_S$	$f = 1$ kHz		-130		dB
		$f = 10$ kHz		-105		dB

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	$V_{S-}$ to $V_{S+}$
Differential Input Voltage	$\pm 0.7$ V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Operating Temperature Range	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
Junction Temperature Range	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Lead Temperature Range (Soldering, 60 sec)	$300^{\circ}\text{C}$

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is,  $\theta_{JA}$  is specified for the device soldered on a 4-layer circuit board for surface-mount packages.

Table 4.

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead SOIC_N (R-8)	120	43	$^{\circ}\text{C}/\text{W}$

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

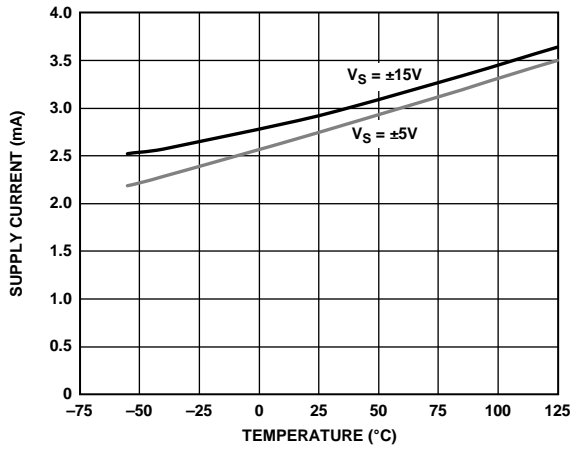


Figure 2. Supply Current vs. Temperature

13063-101

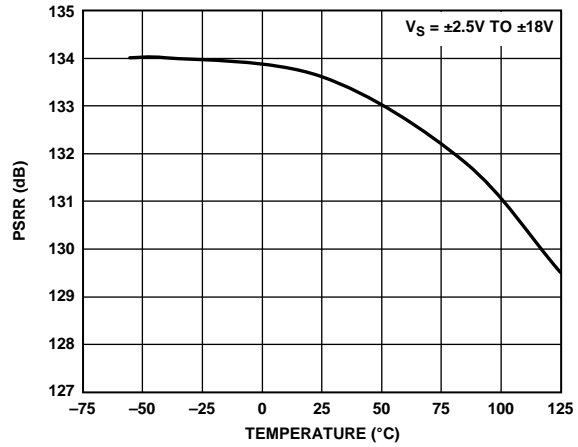


Figure 5. PSRR vs. Temperature

13063-104

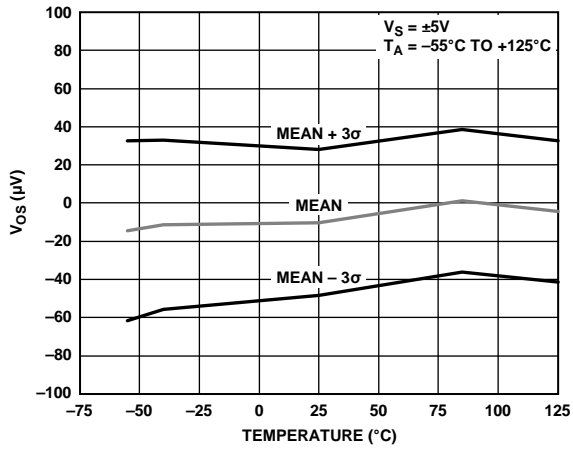


Figure 3. Input Offset Voltage ( $V_{OS}$ ) vs. Temperature,  $V_S = \pm 5V$

13063-102

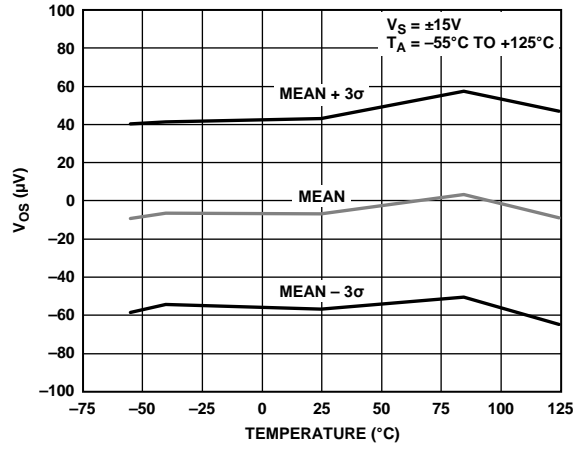


Figure 6. Input Offset Voltage ( $V_{OS}$ ) vs. Temperature,  $V_S = \pm 15V$

13063-105

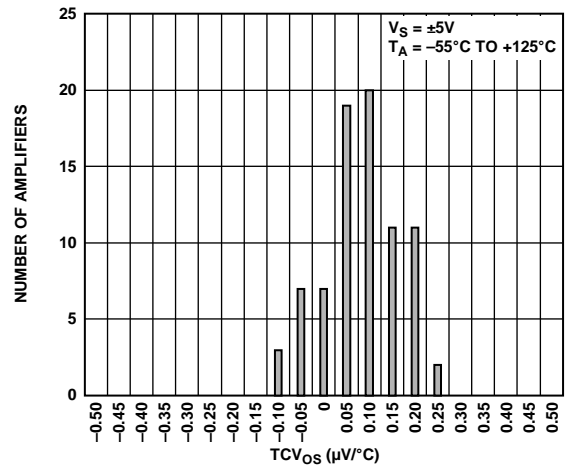


Figure 4. Input Offset Voltage Drift ( $TCV_{OS}$ ) Distribution,  $V_S = \pm 5V$

13063-103

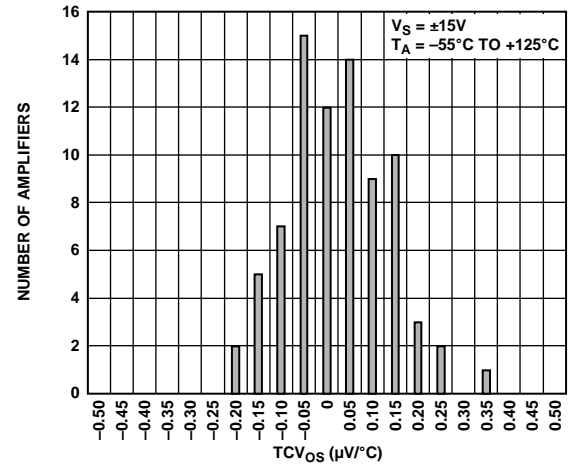


Figure 7. Input Offset Voltage Drift ( $TCV_{OS}$ ) Distribution,  $V_S = \pm 15V$

13063-106

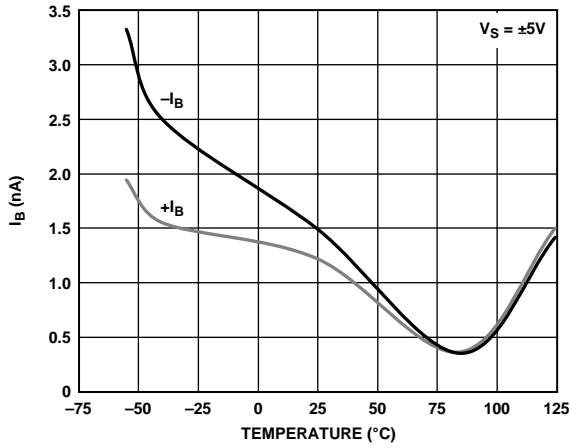


Figure 8. Input Bias Current ( $I_B$ ) vs. Temperature,  $V_S = \pm 5V$

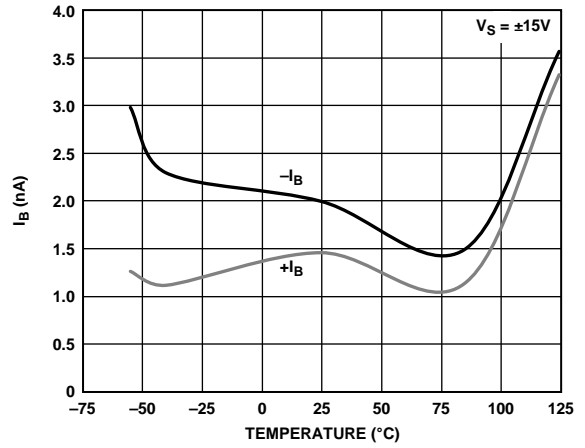


Figure 11. Input Bias Current ( $I_B$ ) vs. Temperature,  $V_S = \pm 15V$

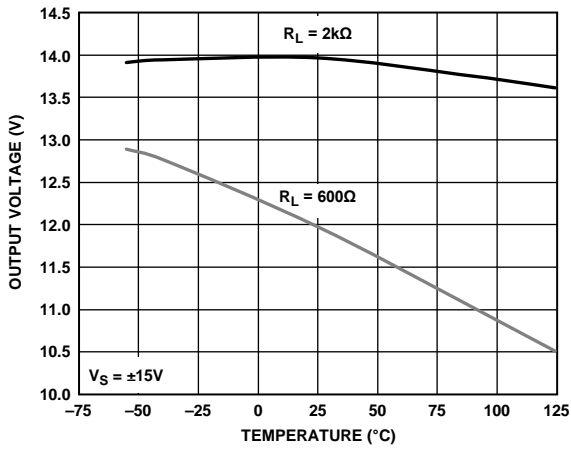


Figure 9. Output Voltage High vs. Temperature

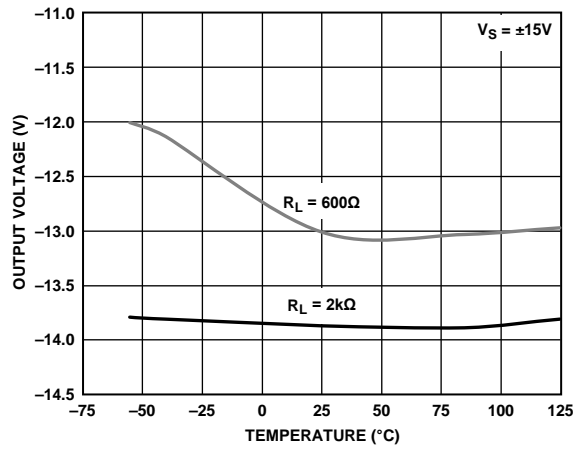


Figure 12. Output Voltage Low vs. Temperature

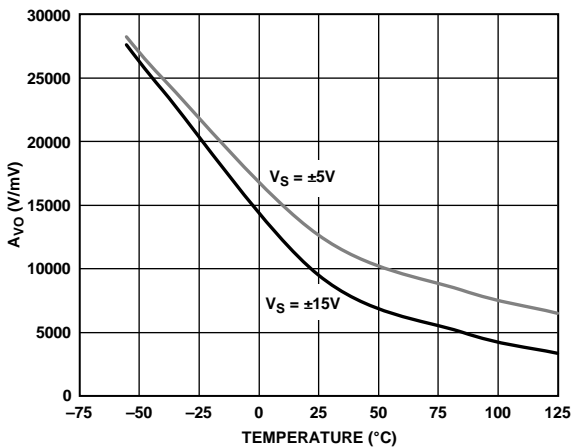
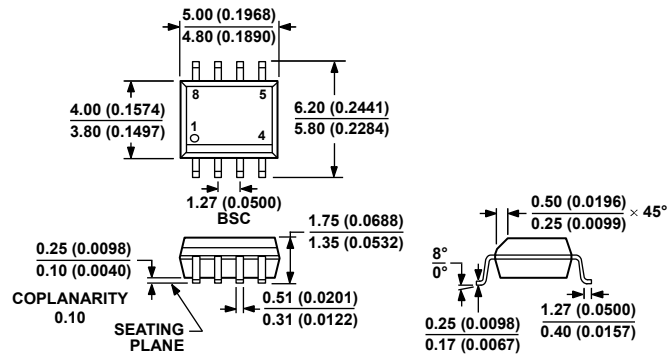


Figure 10. Open-Loop Gain ( $A_{vo}$ ) vs. Temperature

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 13. 8-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body (R-8)  
 Dimensions shown in millimeters and (inches)

012407-A

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
AD8672TRZ-EP	-55°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD8672TRZ-EP-R7	-55°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8

<sup>1</sup> Z = RoHS Compliant Part.