



100V, 4A, High Frequency Half-Bridge Gate Driver

DESCRIPTION

The MPQ1924 is a high-frequency, 100V, half-bridge, N-channel, power MOSFET driver. Its low-side and high-side driver channels are independently controlled and matched with less than 5ns in time delay. Under-voltage lockout on both high-side and low-side supplies force their outputs low in case of insufficient supply. The integrated bootstrap diode reduces external component count.

FEATURES

- Drives an N-Channel MOSFET Half Bridge
- 118V V_{BST} Voltage Range
- On-Chip Bootstrap Diode
- Typical Propagation Delay of 20ns
- Gate Drive Matching of Less than 5ns
- Drives a 2.2nF Load with 15ns Rise Time and 12ns Fall Time at 12V VDD
- TTL-Compatible Input
- Quiescent Current of Less than 150 μ A
- UVLO for Both High Side and Low Side
- SOIC-8 Package

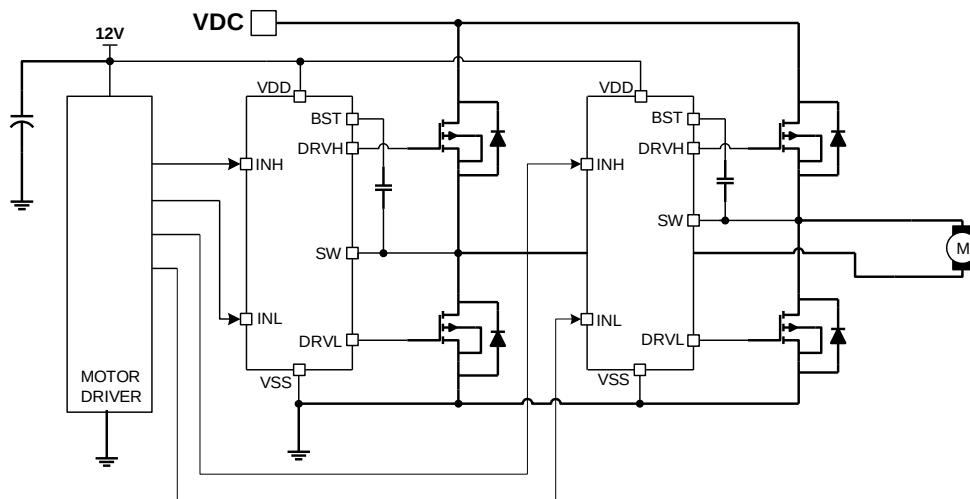
APPLICATIONS

- Motor Drivers
- Telecom Half-Bridge Power Supplies
- Avionics DC-DC Converters
- Two-Switch Forward Converters
- Active-Clamp Forward Converters

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TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking
MPQ1924HS*	SOIC-8	See Below

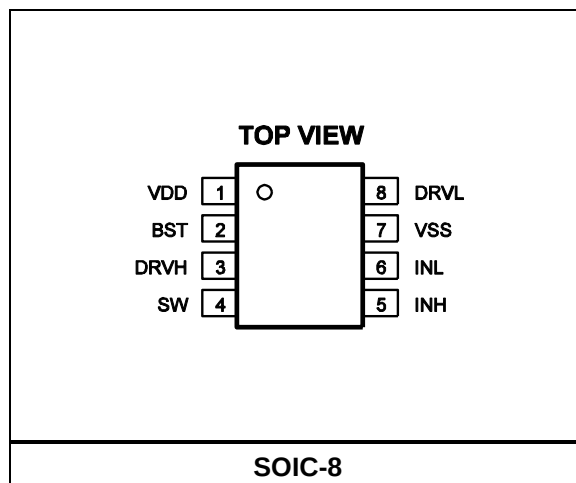
* For Tape & Reel, add suffix -Z (e.g. MPQ1924HS-Z)
For RoHS compliant packaging, add suffix -LF (e.g. MPQ1924HS-LF-Z)

TOP MARKING

MP1924
LLLLLLLL
MPSYWW

MP1924: product code of MPQ1924HS;
LLLLLLLL: lot number;
MPS: MPS prefix;
Y: year code;
WW: week code;

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply Voltage (V_{DD})	-0.3V to 18V
SW Voltage (V_{SW})	-5.0V to 105V
BST Voltage (V_{BST})	-0.3V to 118V
BST to SW	-0.3V to 18V
DRVH to SW	-0.3V to (BST-SW) + 0.3V
DRVL to VSS	-0.3V to (V_{DD} + 0.3V)
All Other Pins	-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation ($T_A = 25^\circ\text{C}$) ⁽²⁾	
SOIC-8	1.3W
Junction Temperature	150°C
Lead Temperature	260°C
Storage Temperature	-65°C to 150°C

Recommended Operating Conditions ⁽³⁾

Supply Voltage V_{DD}	9.0V to 16.0V
SW Voltage (V_{SW})	-1.0V to 100V
SW Slew Rate	<50V/ns
Operating Junction Temp. (T_J)	-40°C to 125°C

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}
SOIC-8	96	45

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature $T_J(\text{MAX})$, the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(\text{MAX}) = (T_J(\text{MAX}) - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{BST} - V_{SW} = 12V$, $V_{SS} = V_{SW} = 0V$, No load at DRVH and DRVL, $T_A = +25^\circ C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Currents						
VDD quiescent current	I _{DDQ}	INL = INH = 0		100	150	μA
VDD operating current	I _{DDO}	fsw = 500kHz		9		mA
Floating driver quiescent current	I _{BSTQ}	INL = INH = 0		60	90	μA
Floating driver operating current	I _{BSTO}	fsw = 500kHz		7.5		mA
Leakage current	I _{LK}	BST = SW = 100V		0.05	1	μA
Inputs						
INL/INH High				2	2.4	V
INL/INH Low			1	1.4		V
INL/INH internal pull-down resistance	R _{IN}			185		kΩ
Under Voltage Protection						
VDD rising threshold	V _{DDR}		8.1	8.4	8.8	V
VDD hysteresis	V _{DDH}			0.5		V
(BST-SW) rising threshold	V _{BSTR}		6.9	7.3	7.7	V
(BST-SW) hysteresis	V _{BSTH}			0.55		V
Bootstrap Diode						
Bootstrap diode VF @ 100μA	V _{F1}			0.5		V
Bootstrap diode VF @ 100mA	V _{F2}			0.95		V
Bootstrap diode dynamic R	R _D	@ 100mA		2		Ω
Low Side Gate Driver						
Low level output voltage	V _{OLL}	I _O = 100mA		0.08		V
High level output voltage to rail	V _{OHL}	I _O = -100mA		0.23		V
Source Current ⁽⁵⁾	I _{OHL}	V _{DRVL} = 0V, V _{DD} = 12V		3		A
		V _{DRVL} = 0V, V _{DD} = 16V		4.7		A
Sink Current ⁽⁵⁾	I _{OLL}	V _{DRVL} = V _{DD} = 12V		4.5		A
		V _{DRVL} = V _{DD} = 16V		6		A
Floating Gate Driver						
Low level output voltage	V _{OLH}	I _O = 100mA		0.08		V
High level output voltage to rail	V _{OHH}	I _O = -100mA		0.23		V
Source Current ⁽⁵⁾	I _{OHH}	V _{DRVH} = 0V, V _{DD} = 12V		2.6		A
		V _{DRVH} = 0V, V _{DD} = 16V		4		A
Sink Current ⁽⁵⁾	I _{OLH}	V _{DRVH} = V _{DD} = 12V		4.5		A
		V _{DRVH} = V _{DD} = 16V		5.9		A

ELECTRICAL CHARACTERISTICS (continued)

$V_{DD} = V_{BST} - V_{SW} = 12V$, $V_{SS} = V_{SW} = 0V$, No load at DRVH and DRVL, $T_A = +25^\circ C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switching Spec. --- Low Side Gate Driver						
Turn-off propagation delay INL falling to DRVL falling	T_{DLFF}			20		ns
Turn-on propagation delay INL rising to DRVL rising	T_{DLRR}			20		
DRVL rise time		$C_L = 2.2nF$		15		ns
DRVL fall time		$C_L = 2.2nF$		9		ns
Switching Spec. --- Floating Gate Driver						
Turn-off propagation delay INH falling to DRVH falling	T_{DHFF}			20		ns
Turn-on propagation delay INH rising to DRVH rising	T_{DHRR}			20		ns
DRVH rise time		$C_L = 2.2nF$		15		ns
DRVH fall time		$C_L = 2.2nF$		12		ns
Switching Spec. --- Matching						
Floating driver turn-off to low side drive turn-on ⁽⁵⁾	T_{MON}			1	5	ns
Low side driver turn-off to floating driver turn-on ⁽⁵⁾	T_{MOFF}			1	5	ns
Minimum input pulse width that changes the output ⁽⁵⁾	T_{PW}				50	ns
Bootstrap diode turn-on or turn- off time ⁽⁵⁾	T_{BS}			10		ns
Thermal shutdown				150		$^\circ C$
Thermal shutdown hysteresis				25		$^\circ C$

Note:

5) Guaranteed by design.

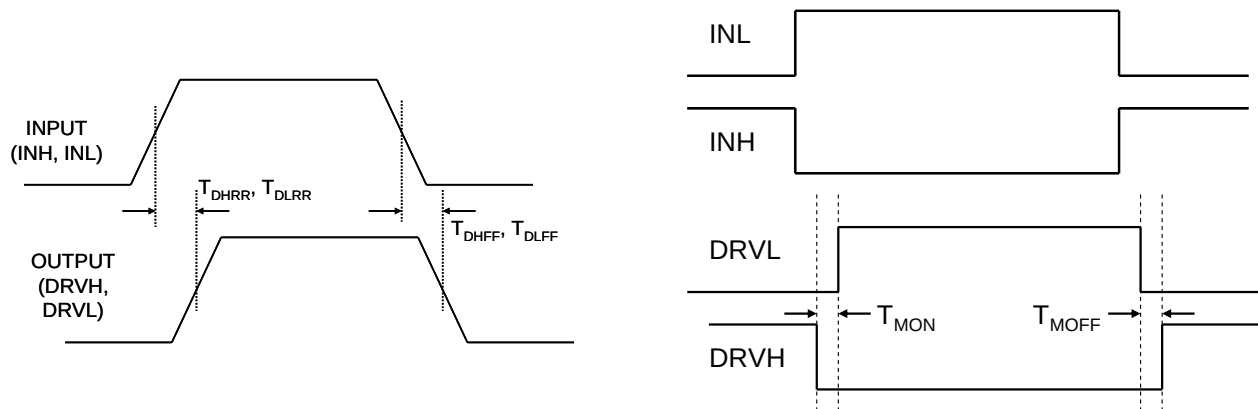


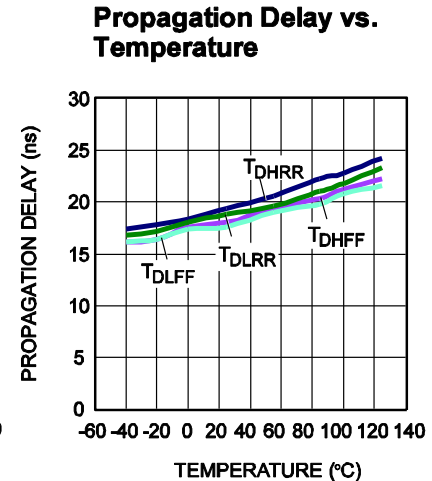
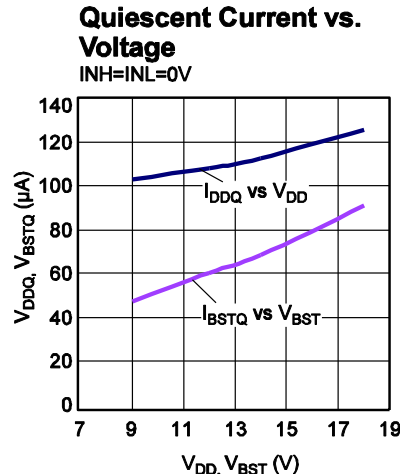
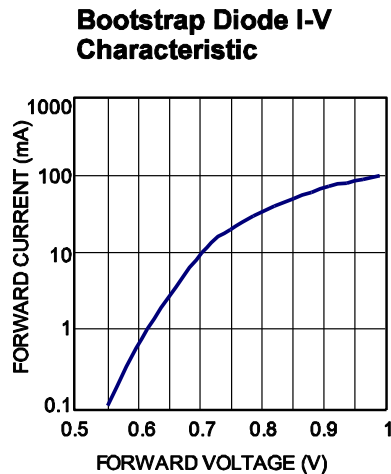
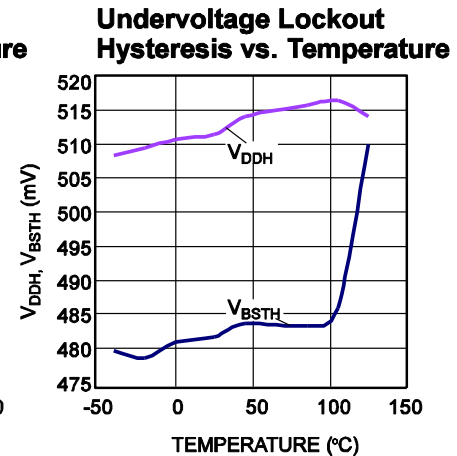
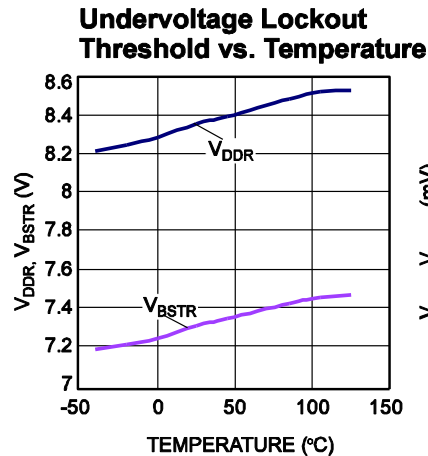
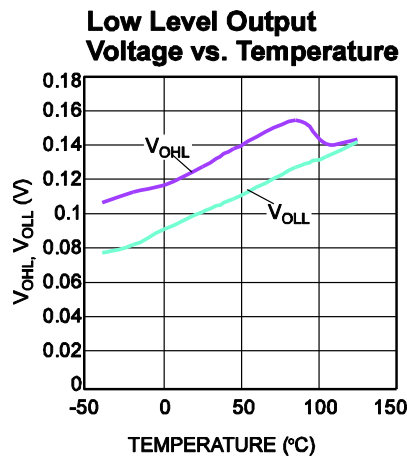
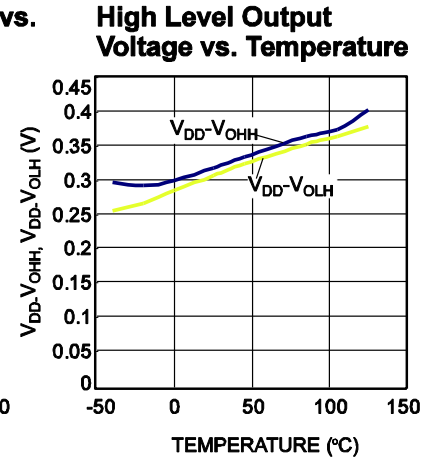
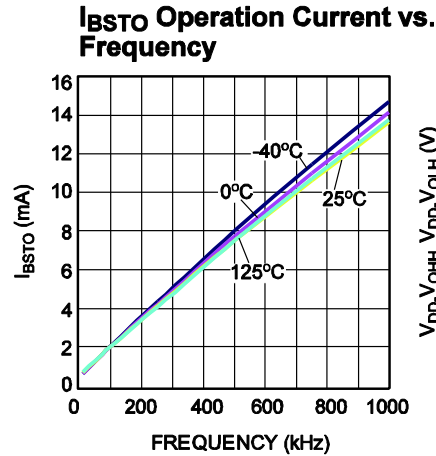
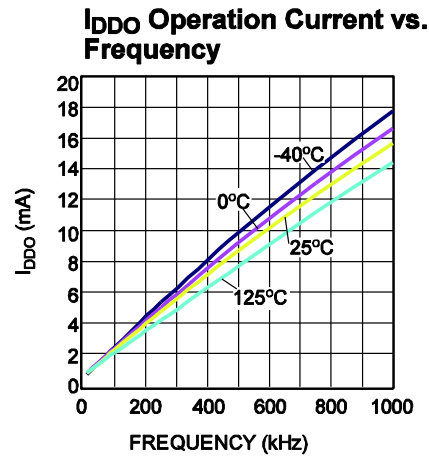
Figure 1: Timing Diagram

PIN FUNCTIONS

SOIC-8 Pin #	Name	Description
1	VDD	Supply input. This pin supplies power to all the internal circuitry. Place a decoupling capacitor to ground close to this pin to ensure stable and clean supply.
2	BST	Bootstrap. This is the positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between this pin and SW pin.
3	DRVH	Floating driver output.
4	SW	Switching node.
	NC	No connection.
5	INH	Control signal input for the floating driver.
6	INL	Control signal input for the low side driver.
7	VSS, exposed pad	Chip ground. Connect exposed pad to VSS for proper thermal operation.
8	DRVL	Low side driver output.

TYPICAL PERFORMANCE CHARACTERISTICS

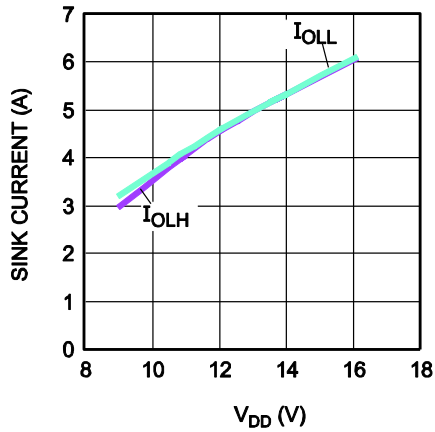
$V_{DD} = 12V$, $V_{SS} = V_{SW} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.



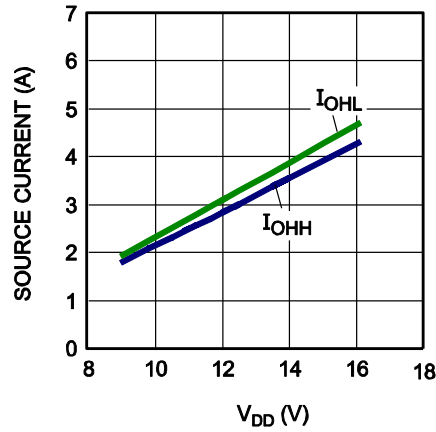
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{DD} = 12V$, $V_{SS} = V_{SW} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.

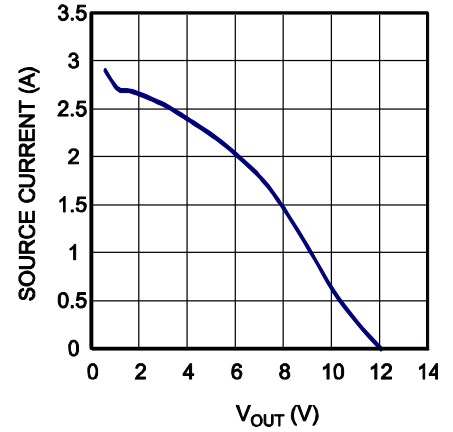
**Sink Current vs.
 V_{DD} Voltage**



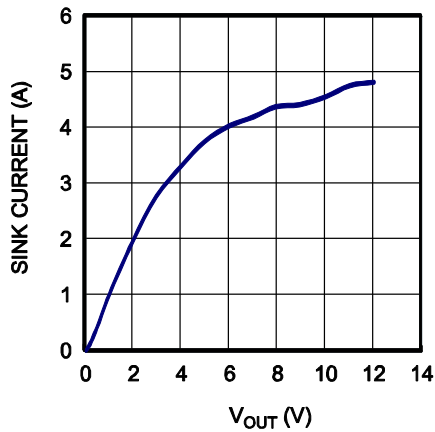
**Source Current vs.
 V_{DD} Voltage**



**Source Current vs.
Output Voltage**
 $V_{DD} = 12V$



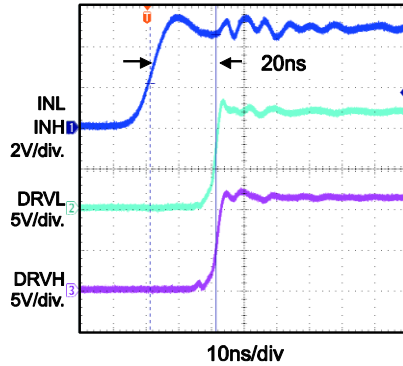
**Sink Current vs.
Output Voltage**
 $V_{DD} = 12V$



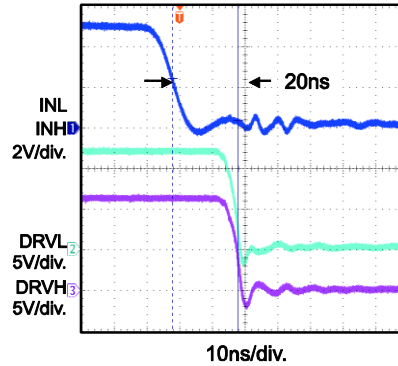
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{DD} = 12V$, $V_{SS} = V_{SW} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.

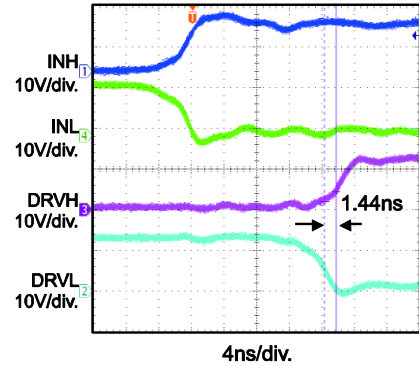
Turn-on Propagation Delay



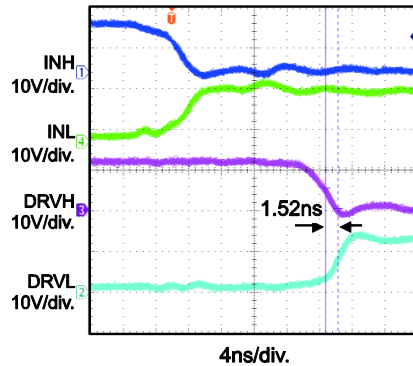
Turn-off Propagation Delay



Gate Drive Matching T_{MOFF}

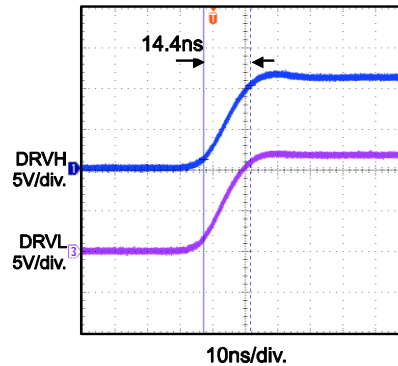


Gate Drive Matching T_{MON}



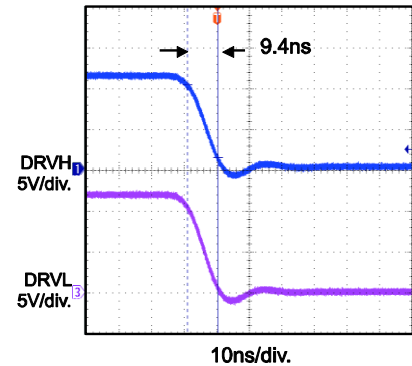
Drive Rise Time

2.2nF Load



Drive Fall Time

2.2nF Load



BLOCK DIAGRAM

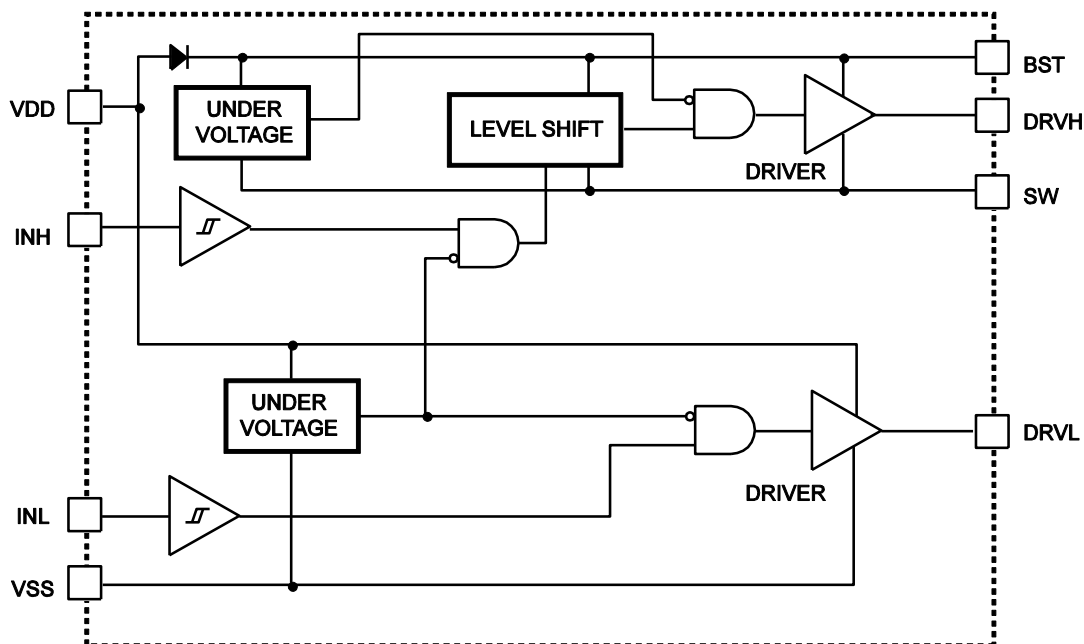


Figure 2: Function Block Diagram

APPLICATION

The input signals of INH and INL can be controlled independently. If both INH and INL control the high-side MOSFET and low-side MOSFET of the same bridge, then users must avoid shoot through by

setting sufficient dead time between INH and INL low, and vice versa. See Figure 3 below. Dead time is defined as the time interval between INH low and INL low.

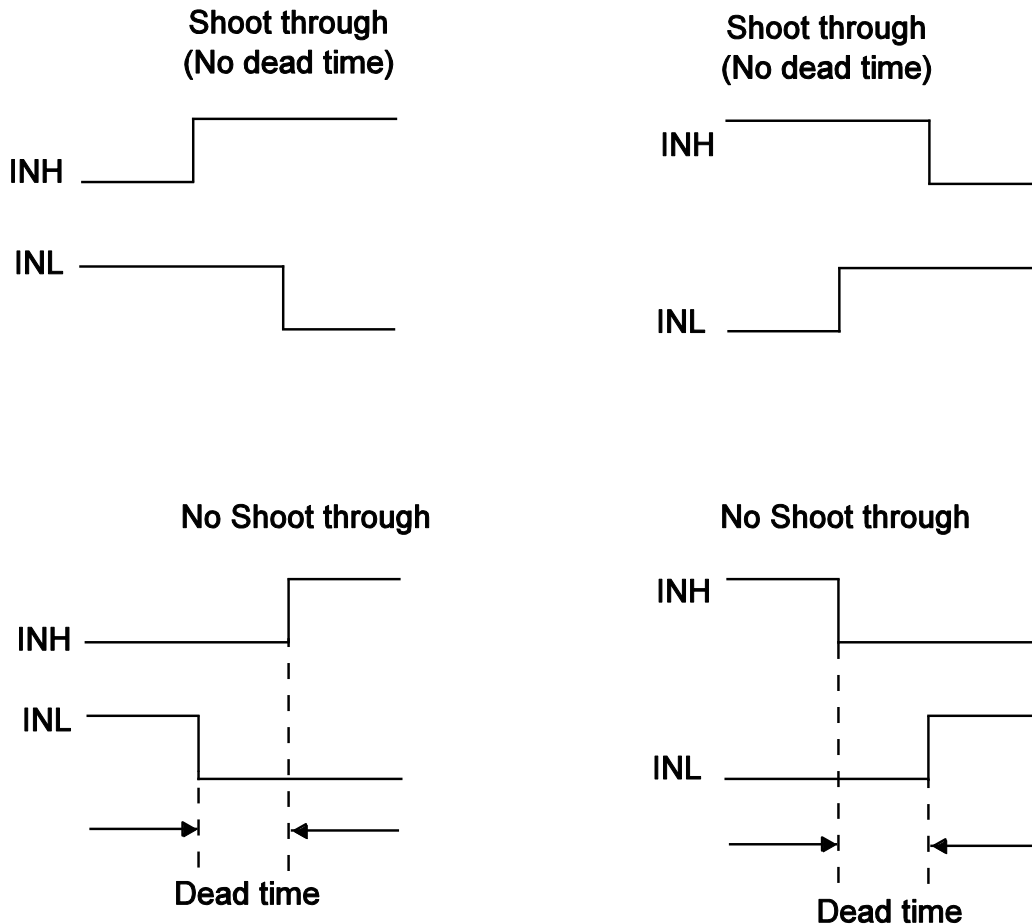


Figure 3: Shoot-Through Timing Diagram

REFERENCE DESIGN CIRCUITS

Half Bridge Converter

The MPQ1924 drives the MOSFETs with alternating signals (with dead time) in half-bridge converter topology. Therefore, from the PWM

controller drives INH and INL with alternating signals the input voltage can go up to 100V.

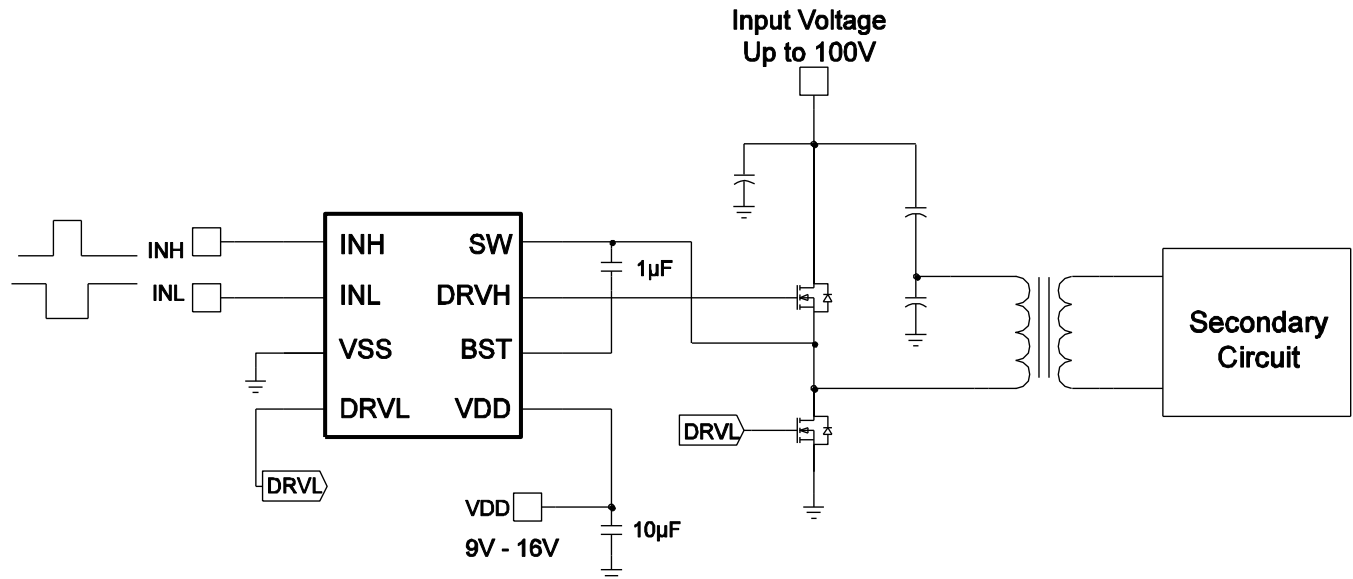


Figure 4: Half Bridge Converter

Two-Switch Forward Converter

In two-switch forward converter topology, both MOSFETs are turned on and off simultaneously. The input signal (INH and INL) comes from a PWM controller that senses the output voltage (and output current during current-mode control).

The Schottky diodes clamp the reverse swing of the power transformer and must be rated for the input voltage. The input voltage can go up to 100V.

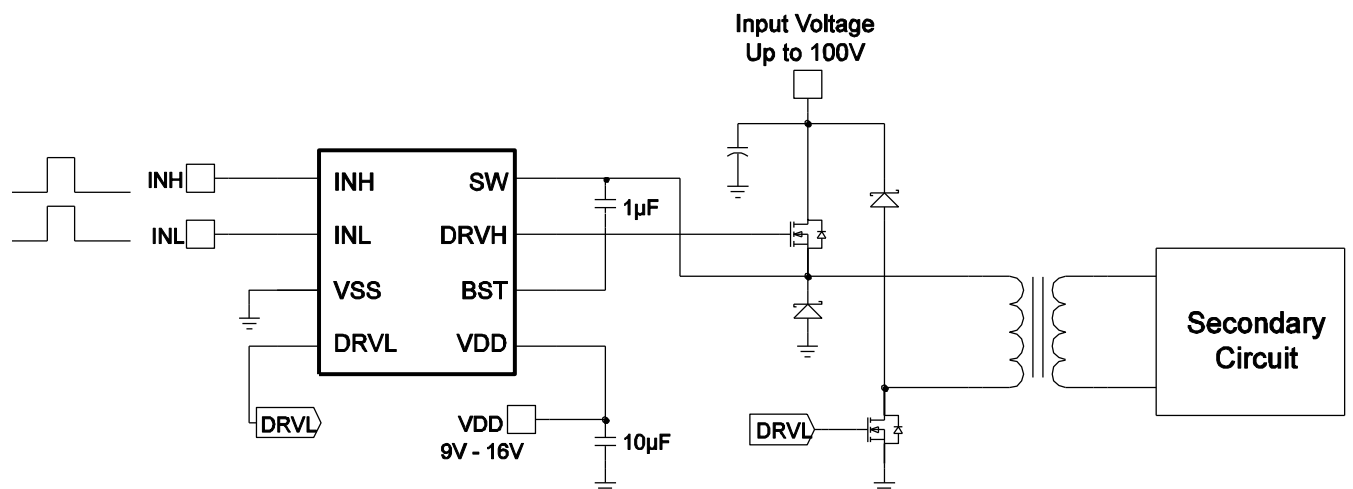


Figure 5: Two-Switch Forward Converter

Active-Clamp Forward Converter

In active-clamp forward converter topology, the MPQ1924 drives the MOSFETs with alternating signals. The high-side MOSFET, in conjunction with C_{reset} , is used to reset the power transformer in a lossless manner.

This topology lends itself well to run at duty cycles exceeding 50%. The device may not be able to run at 100V under this topology.

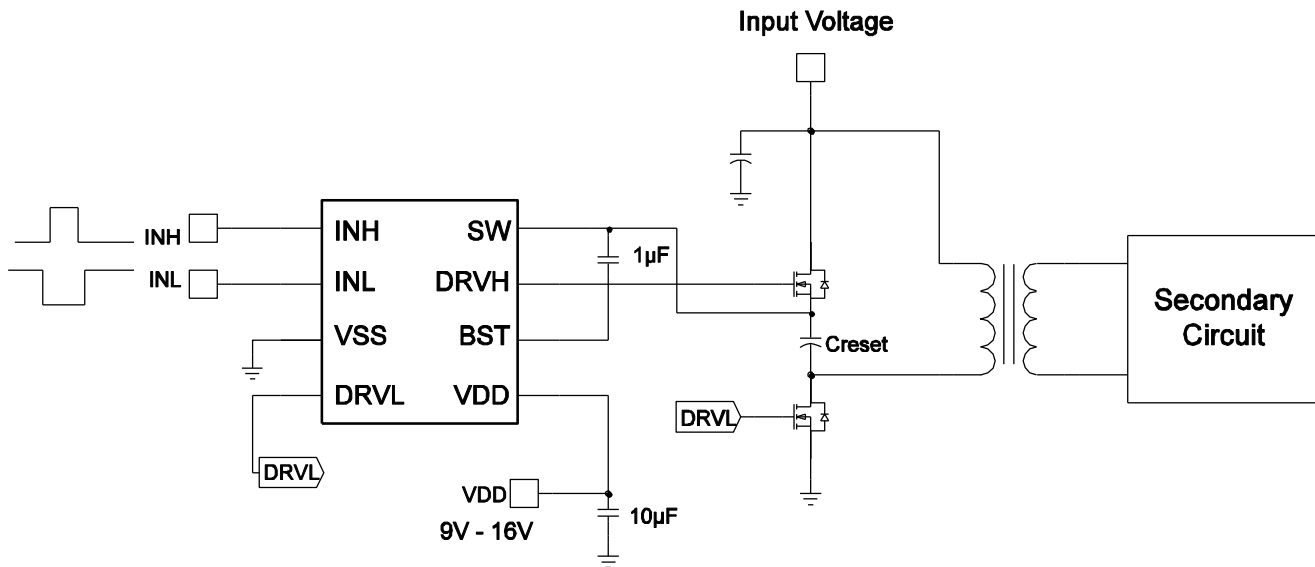
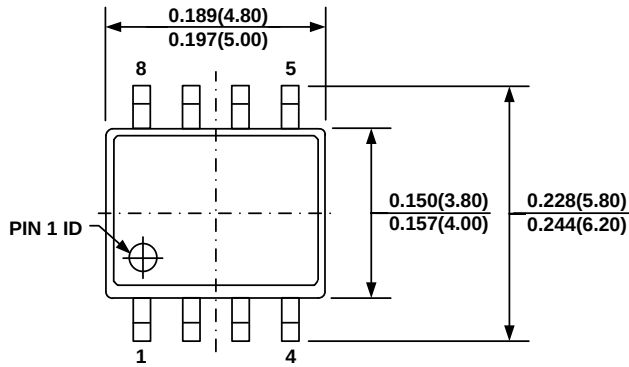


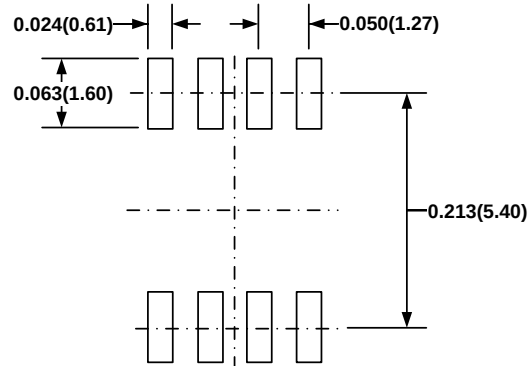
Figure 6 Active-Clamp Forward Converter

PACKAGE INFORMATION

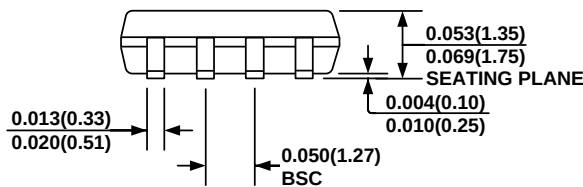
SOIC-8



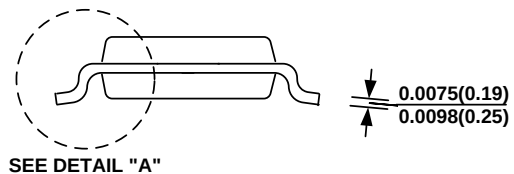
TOP VIEW



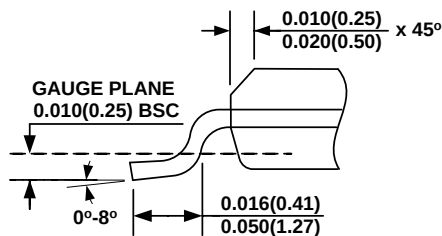
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

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