

## 0.7 A 6.8 V Dual H-Bridge Motor Driver

The 17533 is a monolithic dual H-Bridge power IC ideal for portable electronic applications containing bipolar stepper motors and/or brush DC-motors (e.g., cameras and disk drive head positioners).

The 17533 operates from 2.0 V to 6.8 V, with independent control of each H-Bridge via parallel MCU interface (3.0 V and 5.0 V compatible logic). The device features built-in shoot-through current protection and an undervoltage shutdown function.

The 17533 has four operating modes: forward, reverse, brake, and tri-stated (high-impedance). The 17533 has a low total  $R_{DS(ON)}$  of 1.2  $\Omega$  (max at 25  $^{\circ}\text{C}$ ).

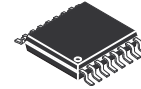
The 17533's low output resistance and high slew rate provides efficient drive for many types of micromotors.

### Features

- Low total  $R_{DS(ON)}$  0.8  $\Omega$  (typ), 1.2  $\Omega$  (max) at 25  $^{\circ}\text{C}$
- Output current 0.7 A (DC), 1.4 A (peak)
- Shoot-through current protection circuit
- 3.0 V/5.0 V CMOS-compatible inputs
- PWM control Input frequency up to 200 kHz
- Built-in 2-channel H-Bridge driver
- Low power consumption
- Undervoltage detection and shutdown circuit

17533

H-BRIDGE MOTOR DRIVER



EV SUFFIX (Pb-FREE)  
98ASA10614D  
16-PIN VMFP

### ORDERING INFORMATION

| Device<br>(For Tape and Reel, add<br>an R2 Suffix) | Temperature<br>Range ( $T_A$ )                  | Package |
|--|---|---------|
| MPC17533EV/EL                                      | -20 $^{\circ}\text{C}$ to 65 $^{\circ}\text{C}$ | 16 VMFP |

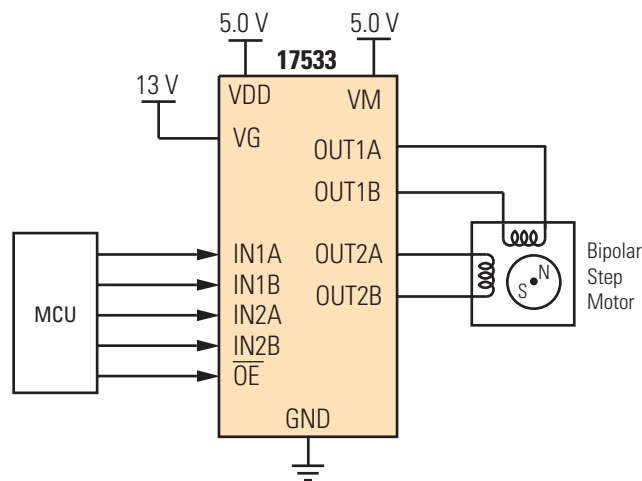


Figure 1. 17533 Simplified Application Diagram

## INTERNAL BLOCK DIAGRAM

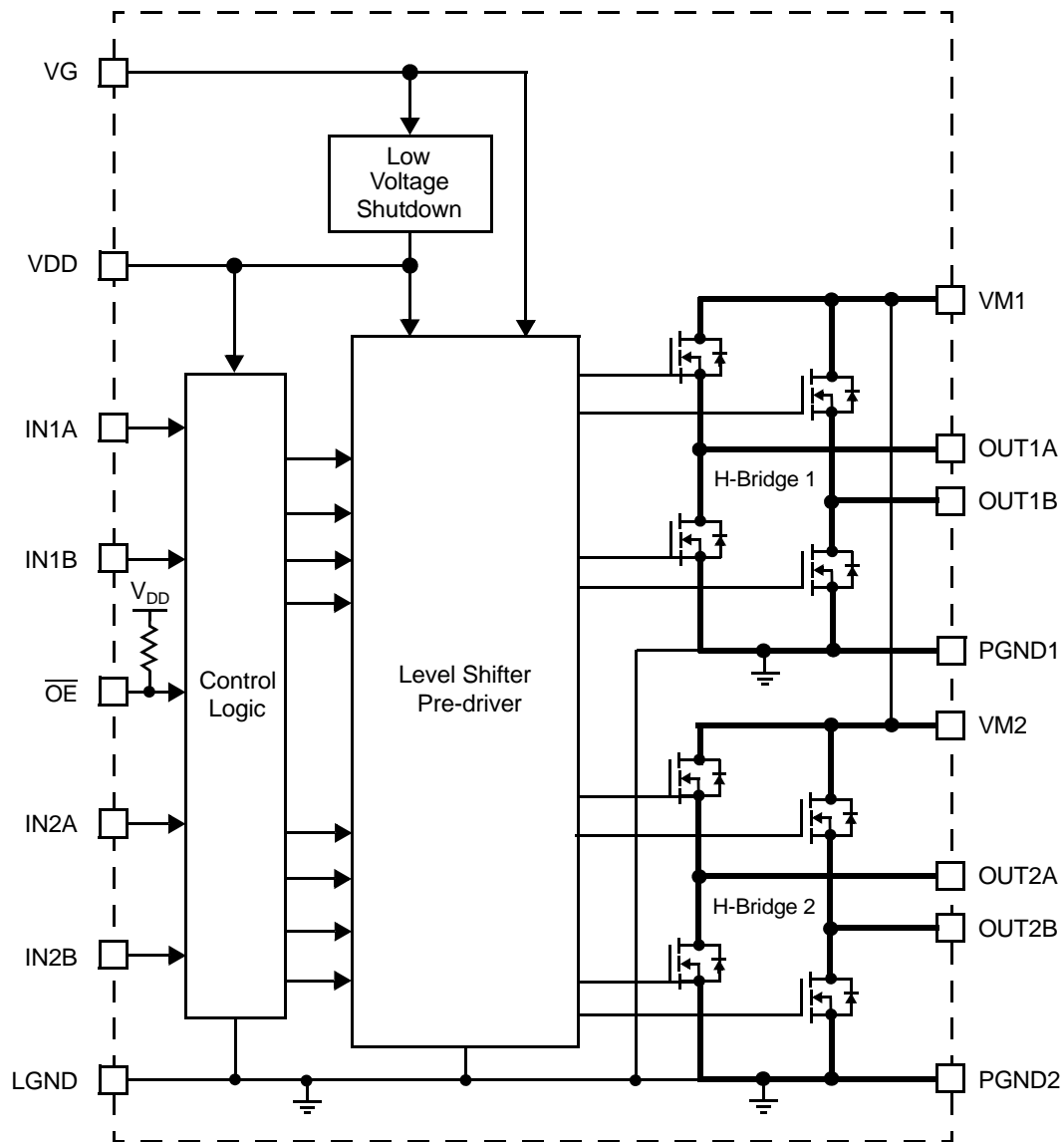


Figure 2. 17533 Simplified Internal Block Diagram

## PIN CONNECTIONS

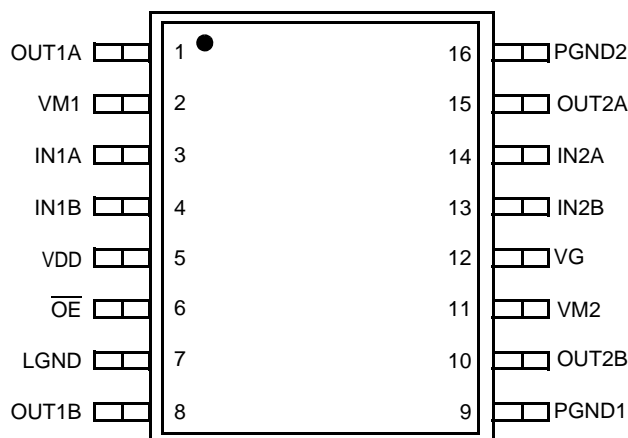


Figure 3. 17533 Pin Connections

Table 1. PIN Function Description

| Pin | Pin Name        | Formal Name                       | Definition   |
|-----|-----------------|-----------------------------------|--|
| 1   | OUT1A           | H-Bridge Output 1A                | Output A of H-Bridge channel 1.  |
| 2   | VM1             | Motor Drive Power Supply 1        | Positive power source connection for H-Bridge 1 (Motor Drive Power Supply).            |
| 3   | IN1A            | Logic Input Control 1A            | Logic input control of OUT1A (refer to <a href="#">Table 5. Truth Table</a> , page 7). |
| 4   | IN1B            | Logic Input Control 1B            | Logic input control of OUT1B (refer to <a href="#">Table 5. Truth Table</a> , page 7). |
| 5   | VDD             | Logic Supply                      | Control circuit power supply pin.  |
| 6   | $\overline{OE}$ | Output Enable                     | Logic output Enable control of H-Bridges (Low = True).                                 |
| 7   | LGND            | Logic Ground                      | Low-current logic signal ground.   |
| 8   | OUT1B           | H-Bridge Output 1B                | Output B of H-Bridge channel 1.  |
| 9   | PGND1           | Power Ground 1                    | High-current power ground 1.   |
| 10  | OUT2B           | H-Bridge Output 2B                | Output B of H-Bridge channel 2.  |
| 11  | VM2             | Motor Drive Power Supply 2        | Positive power source connection for H-Bridge 2 (Motor Drive Power Supply).            |
| 12  | VG              | Gate Driver Circuit Voltage Input | Input pin for the gate drive voltage.  |
| 13  | IN2B            | Logic Input Control 2B            | Logic input control of OUT2B (refer to <a href="#">Table 5. Truth Table</a> , page 7). |
| 14  | IN2A            | Logic Input Control 2A            | Logic input control of OUT2A (refer to <a href="#">Table 5. Truth Table</a> , page 7). |
| 15  | OUT2A           | H-Bridge Output 2A                | Output A of H-Bridge channel 2.  |
| 16  | PGND2           | Power Ground 2                    | High-current power ground 2.   |

## ELECTRICAL CHARACTERISTICS

### MAXIMUM RATINGS

**Table 2. Maximum Ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding the ratings may cause a malfunction or permanent damage to the device.

| Rating  | Symbol          | Value                | Unit |
|---|-----------------|----------------------|------|
| Motor Supply Voltage  | $V_M$           | -0.5 to 8.0          | V    |
| Gate Driver Circuit Power Supply Voltage                          | $V_G$           | -0.5 to 14           | V    |
| Logic Supply Voltage  | $V_{DD}$        | -0.5 to 7.0          | V    |
| Signal Input Voltage  | $V_{IN}$        | -0.5 to $V_{DD}+0.5$ | V    |
| Driver Output Current   |                 |                      | A    |
| Continuous  | $I_O$           | 0.7                  |      |
| Peak <sup>(1)</sup>   | $I_{OPK}$       | 1.4                  |      |
| ESD Voltage <sup>(2)</sup>  |                 |                      | V    |
| Human Body Model  | $V_{ESD1}$      | $\pm 1500$           |      |
| Machine Model   | $V_{ESD2}$      | $\pm 200$            |      |
| Operating Junction Temperature                                    | $T_J$           | -55 to 150           | °C   |
| Operating Ambient Temperature                                     | $T_A$           | -20 to 65            | °C   |
| Storage Temperature Range   | $T_{STG}$       | -55 to 150           | °C   |
| Thermal Resistance <sup>(3)</sup>                                 | $R_{\theta JA}$ | 150                  | °C/W |
| Power Dissipation <sup>(4)</sup>                                  | $P_D$           | 830                  | mW   |
| Peak Package Reflow Temperature During Reflow <sup>(5), (6)</sup> | $T_{PPRT}$      | Note 6               | °C   |

**Notes**

- $T_A = 25^\circ\text{C}$ . 10 ms pulse at 200 ms intervals.
- ESD1 testing is performed in accordance with the Human Body Model ( $C_{ZAP} = 100 \text{ pF}$ ,  $R_{ZAP} = 1500 \Omega$ ), ESD2 testing is performed in accordance with the Machine Model ( $C_{ZAP} = 200 \text{ pF}$ ,  $R_{ZAP} = 0 \Omega$ ).
- Mounted on 37 mm x 50 mm x 1.6 mm glass epoxy board mount.
- $T_A = 25^\circ\text{C}$ .
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
- Freescall's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to [www.freescale.com](http://www.freescale.com), search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxx enter 33xxx), and review parametrics.

## STATIC ELECTRICAL CHARACTERISTICS

**Table 3. Static Electrical Characteristics**

Characteristics noted under conditions  $T_A = 25\text{ }^{\circ}\text{C}$ ,  $V_{DD} = V_M = 5.0\text{ V}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25\text{ }^{\circ}\text{C}$  under nominal conditions unless otherwise noted.

| Characteristic   | Symbol                        | Min                 | Typ | Max                 | Unit          |
|--|-------------------------------|---------------------|-----|---------------------|---------------|
| <b>POWER</b>   |                               |                     |     |                     |               |
| Motor Supply Voltage   | $V_M$                         | 2.0                 | 5.0 | 6.8                 | V             |
| Logic Supply Voltage   | $V_{DD}$                      | 2.7                 | 5.0 | 5.7                 | V             |
| Quiescent Power Supply Current   |                               |                     |     |                     | $\mu\text{A}$ |
| Driver Circuit Power Supply Current  | $I_{QM}$                      | –                   | –   | 1.0                 |               |
| Logic Supply Current <sup>(7)</sup>  | $I_{QVDD}$                    | –                   | –   | 20                  |               |
| Gate Driver Circuit Power Supply Current   | $I_{QVG}$                     | –                   | –   | 150                 |               |
| Operating Power Supply Current   |                               |                     |     |                     | mA            |
| Logic Supply Current <sup>(8)</sup>  | $I_{VDD}$                     | –                   | –   | 3.0                 |               |
| Gate Driver Circuit Power Supply Current <sup>(9)</sup>  | $I_{VG}$                      | –                   | –   | 0.7                 |               |
| Low $V_{DD}$ Detection Voltage <sup>(10)</sup>   | $V_{DDET}$                    | 1.5                 | 2.0 | 2.5                 | V             |
| Driver Output ON Resistance  |                               |                     |     |                     | $\Omega$      |
| Source+Sink at $I_O = 0.7\text{ A}$ <sup>(11)</sup>  | $R_{DS(ON)}$                  | –                   | 0.8 | 1.2                 |               |
| $V_G = 9.5\text{ V}$ , $V_M = 5.0\text{ V}$ , $T_A = 25\text{ }^{\circ}\text{C}$ <sup>(12)</sup> | $R_{DS(ON)2}$                 | –                   | –   | 1.5                 |               |
| <b>GATE DRIVE</b>  |                               |                     |     |                     |               |
| Gate Drive Circuit Power Supply Voltage  | $V_G$                         | 12                  | 13  | 13.5                | V             |
| <b>CONTROL LOGIC</b>   |                               |                     |     |                     |               |
| Logic Input Voltage  | $V_{IN}$                      | 0                   | –   | $V_{DD}$            | V             |
| Logic Inputs ( $2.7\text{ V} < V_{DD} < 5.7\text{ V}$ )  |                               |                     |     |                     |               |
| High-Level Input Voltage   | $V_{IH}$                      | $V_{DD} \times 0.7$ | –   | –                   | V             |
| Low-Level Input Voltage  | $V_{IL}$                      | –                   | –   | $V_{DD} \times 0.3$ | V             |
| High-Level Input Current   | $I_{IH}$                      | –                   | –   | 1.0                 | $\mu\text{A}$ |
| Low-Level Input Current  | $I_{IL}$                      | –1.0                | –   | –                   | $\mu\text{A}$ |
| $\overline{\text{OE}}$ Pin Input Current Low   | $I_{IL-\overline{\text{OE}}}$ | –                   | 50  | 100                 | $\mu\text{A}$ |

**Notes**

- $I_{QVDD}$  includes the current to pre-driver circuit.
- $I_{VDD}$  includes the current to pre-driver circuit at  $f_{IN} = 100\text{ kHz}$ .
- At  $f_{IN} = 20\text{ kHz}$ .
- Detection voltage is defined as when the output becomes high-impedance after  $V_{DD}$  drops below the detection threshold. When gate voltage  $V_G$  is applied from an external source,  $V_G = 7.5\text{ V}$ .
- The total H-Bridge ON resistance when  $V_G$  is 13 V.
- Increased  $R_{DS(ON)}$  value as the result of a reduced  $V_G$  value of 9.5 V.

## DYNAMIC ELECTRICAL CHARACTERISTICS

**Table 4. Dynamic Electrical Characteristics**

Characteristics noted under conditions  $T_A = 25\text{ }^{\circ}\text{C}$ ,  $V_{DD} = V_M = 5.0\text{ V}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted.

| Characteristic                             | Symbol       | Min | Typ | Max         | Unit          |
|--|--------------|-----|-----|-------------|---------------|
| <b>INPUT</b>                               |              |     |     |             |               |
| Pulse Input Frequency                      | $f_{IN}$     | –   | –   | 200         | kHz           |
| Input Pulse Rise Time <sup>(13)</sup>      | $t_R$        | –   | –   | 1.0<br>(14) | $\mu\text{s}$ |
| Input Pulse Fall Time <sup>(15)</sup>      | $t_F$        | –   | –   | 1.0<br>(14) | $\mu\text{s}$ |
| <b>OUTPUT</b>                              |              |     |     |             |               |
| Propagation Delay Time <sup>(16)</sup>     |              |     |     |             | $\mu\text{s}$ |
| Turn-ON Time                               | $t_{PLH}$    | –   | 0.1 | 0.5         | $\mu\text{s}$ |
| Turn-OFF Time                              | $t_{PHL}$    | –   | 0.1 | 0.5         |               |
| Low Voltage Detection Time <sup>(17)</sup> | $t_{VDDDET}$ | –   | –   | 10          | ms            |

**Notes**

13. Time is defined between 10% and 90%.
14. That is, the input waveform slope must be steeper than this.
15. Time is defined between 90% and 10%.
16. Load of Output is  $8.0\text{ }\Omega$  resistance. see [Figure 4](#)
17. See [Figure 5](#)

## TIMING DIAGRAMS

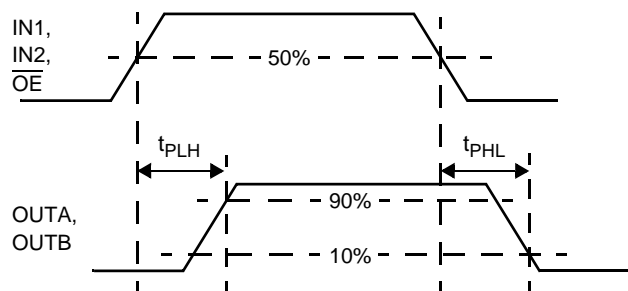


Figure 4.  $t_{PLH}$ ,  $t_{PHL}$ , and  $t_{PZH}$  Timing

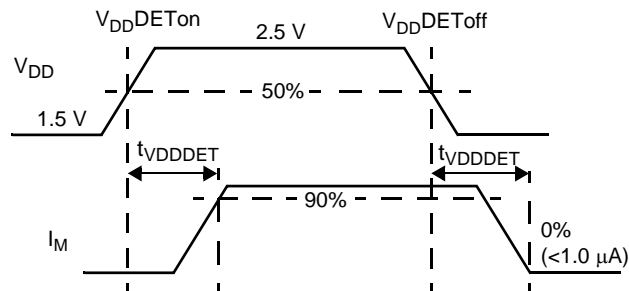


Figure 5. Low-Voltage Detection Timing Diagram

Table 5. Truth Table

| INPUT           |              |              | OUTPUT         |                |
|-----------------|--------------|--------------|----------------|----------------|
| $\overline{OE}$ | IN1A<br>IN2A | IN1B<br>IN2B | OUT1A<br>OUT2A | OUT1B<br>OUT2B |
| L               | L            | L            | L              | L              |
| L               | H            | L            | H              | L              |
| L               | L            | H            | L              | H              |
| L               | H            | H            | Z              | Z              |
| H               | X            | X            | Z              | Z              |

H = High.

L = Low.

Z = High-impedance.

X = Don't care.

$\overline{OE}$  pin is pulled up to  $V_{DD}$  with internal resistance.

## FUNCTIONAL DESCRIPTION

### INTRODUCTION

The 17533 is a monolithic dual H-Bridge ideal for portable electronic applications to control bipolar stepper motors and brush DC motors, such as those found in camera lens assemblies, camera shutters, optical disk drives, etc.

The 17533 operates from 2.0 V to 6.8 V, with independent control of each H-Bridge via parallel MCU interface (3.0 V and 5.0 V compatible I/O). The device features built-in shoot-through current protection and undervoltage shutdown.

The 17533 has four operating modes: forward, reverse, brake, and tri-Stated (high-impedance). The MOSFETs comprising the output bridge have a total source + sink  $R_{DS(ON)} \leq 1.2 \Omega$ .

The 17533 can simultaneously drive two brush DC motors or, as shown in [Figure 1, 17533 Simplified Application Diagram](#) on page 1, one bipolar stepper motor. The drivers are designed to be PWM'ed at frequencies up to 200 kHz.

### FUNCTIONAL PIN DESCRIPTION

#### LOGIC SUPPLY (VDD)

The VDD pin carries the logic supply voltage and current into the logic sections of the IC. VDD has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input control pins.

#### LOGIC INPUT CONTROL (IN1A, IN1B, IN2A, AND IN2B)

These logic input pins control each H-Bridge output (e.g., IN1A logic HIGH = OUT1A HIGH, etc.). However, if all inputs are taken HIGH, the outputs bridges are both tri-stated (refer to [Table 5, Truth Table](#), page 7).

#### OUTPUT ENABLE ( $\overline{OE}$ )

The  $\overline{OE}$  pin is a LOW = TRUE enable input. When  $\overline{OE}$  = HIGH, all H-Bridge outputs (OUT1A, OUT1B, OUT2A, and OUT2B) are tri-stated (high-impedance), regardless of logic inputs (IN1A, IN1B, IN2A, and IN2B) states.

#### OUTPUT A AND B OF H-BRIDGE CHANNEL 1 AND 2 (OUT1A, OUT1B, OUT2A, AND OUT2B)

These pins provide connection to the outputs of each of the internal H-Bridges (see [Figure 2, 17533 Simplified Internal Block Diagram](#), page 2).

#### MOTOR DRIVE POWER SUPPLY (VM1 AND VM2)

The VM pins carry the main supply voltage and current into the power sections of the IC. This supply then becomes controlled and/or modulated by the IC as it delivers the power to the loads attached between the output pins. All VM pins must be connected together on the printed circuit board.

#### GATE DRIVER CIRCUIT VOLTAGE INPUT (VG)

The VG pin is the input pin for the gate drive voltage.

#### POWER GROUND (PGND)

Power ground pins. They must be tied together on the PCB.

#### LOGIC GROUND (LGND)

Logic ground pin.



## TYPICAL APPLICATIONS

### INTRODUCTION

Figure 6 shows a typical application for the 17533. When applying the gate voltage to the VG pin from an external source, be sure to connect it via a resistor equal to, or greater than,  $R_G = V_G/0.02 \Omega$ .

Care must be taken to provide sufficient gate-source voltage for the high-side MOSFETs when  $V_M \gg V_{DD}$  (e.g.,  $V_M = 5.0 \text{ V}$ ,  $V_{DD} = 3.0 \text{ V}$ ), in order to ensure full enhancement of the high-side MOSFET channels.

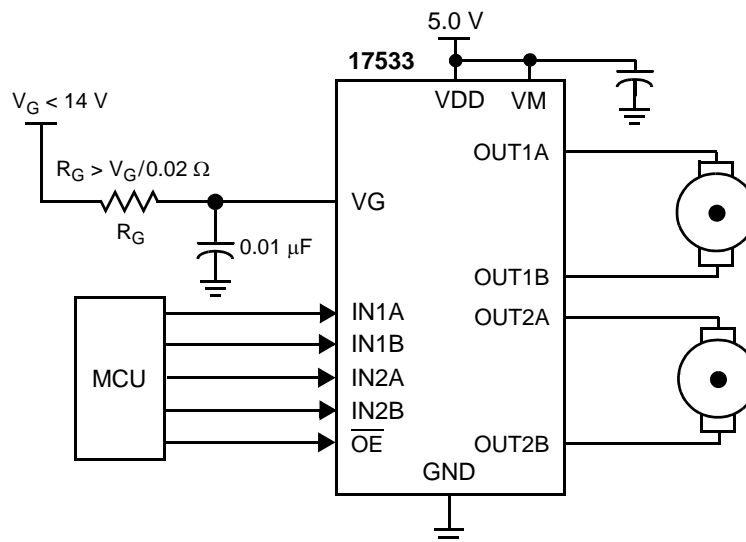


Figure 6. 17533 Typical Application Diagram

### CEMF SNUBBING TECHNIQUES

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commuting currents in inductive loads. Typical practice is to provide snubbing of voltage transients by placing a zener or a capacitor at the supply pin (VM) (see Figure 7).

### PCB LAYOUT

When designing the printed circuit board (PCB), connect sufficient capacitance between power supply and ground pins to ensure proper filtering from transients. For all high-current paths, use wide copper traces and shortest possible distances.

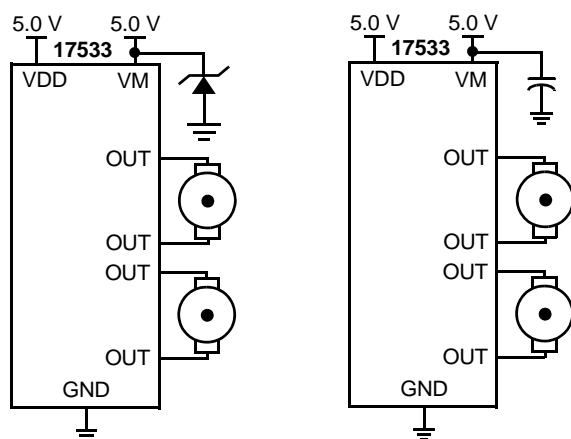


Figure 7. CEMF Snubbing Techniques



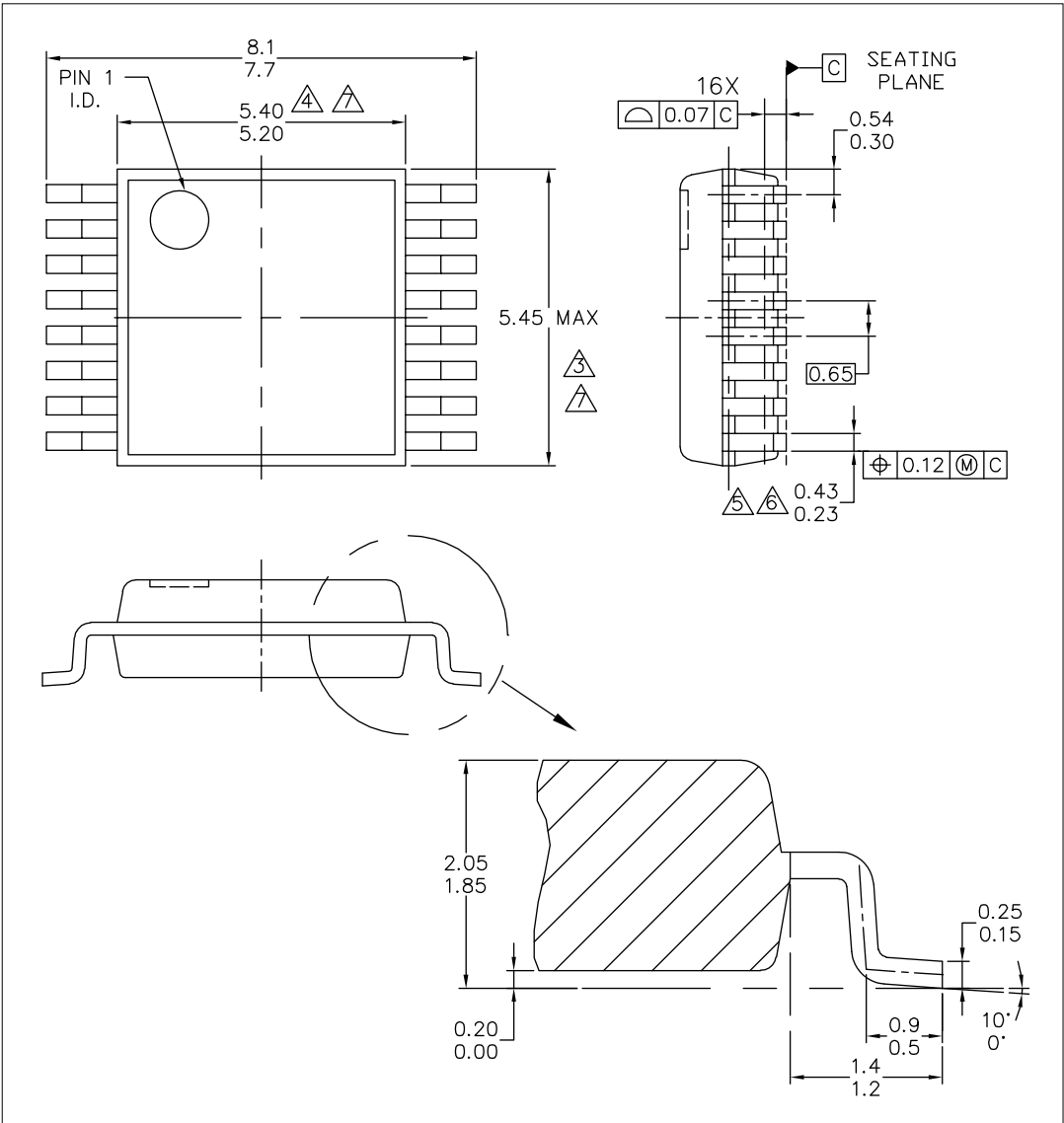
## PACKAGING

### PACKAGE DIMENSIONS

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to [www.freescale.com](http://www.freescale.com) and perform a keyword search for the drawing's document number.

**Table 6.**

| Package     | Suffix | Package Outline Drawing Number |
|-------------|--------|--------------------------------|
| 16-PIN VMFP | EV     | 98ASA10614D                    |



|   |                          |  |                            |  |
|---|--------------------------|--|----------------------------|--|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED.         | MECHANICAL OUTLINE       |  | PRINT VERSION NOT TO SCALE |  |
| TITLE: 16LD VMFP, 5.30 X 5.45 PKG<br>0.65 PITCH<br>CASE OUTLINE | DOCUMENT NO: 98ASA10614D |  | REV: B                     |  |
|   | CASE NUMBER: 1563-02     |  | 07 NOV 2007                |  |
|   | STANDARD: NON-JEDEC      |  |                            |  |

**EV (Pb-FREE) SUFFIX**  
16-LEAD VMFP  
98ASA10614D  
ISSUE B

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
7. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

|   |                           |                            |
|---|---------------------------|----------------------------|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED.         | <b>MECHANICAL OUTLINE</b> | PRINT VERSION NOT TO SCALE |
| TITLE: 16LD VMFP, 5.30 X 5.45 PKG<br>0.65 PITCH<br>CASE OUTLINE | DOCUMENT NO: 98ASA10614D  | REV: B                     |
|   | CASE NUMBER: 1563-02      | 07 NOV 2007                |
|   | STANDARD: NON-JEDEC       |                            |

**EV (Pb-FREE) SUFFIX**  
16-LEAD VMFP  
98ASA10614D  
ISSUE B

## REVISION HISTORY

| REVISION | DATE    | DESCRIPTION OF CHANGES  |
|----------|---------|---|
| 2.0      | 5/2006  | <ul style="list-style-type: none"> <li>• Converted to Freescale format</li> <li>• Added Revision History page</li> </ul>  |
| 3.0      | 7/2006  | <ul style="list-style-type: none"> <li>• Updated to the prevailing form and style</li> <li>• Corrected device isometric drawing on page 1</li> <li>• Added RoHS compliance</li> </ul> |
|          | 12/2013 | <ul style="list-style-type: none"> <li>• No technical changes</li> <li>• Revised back page</li> <li>• Updated document properties</li> </ul>  |

**How to Reach Us:**

**Home Page:**  
freescale.com

**Web Support:**  
freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: [freescale.com/SalesTermsandConditions](http://freescale.com/SalesTermsandConditions).

Freescale and the Freescale logo, are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. SMARTMOS is a trademark of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© 2013 Freescale Semiconductor, Inc.

Document Number: MPC17533  
Rev. 3.0  
12/2013

