74HC191

Presettable synchronous 4-bit binary up/down counter

Rev. 5 — 13 August 2019 Product data sheet

1. General description

The 74HC191 is an asynchronously presettable 4-bit binary up/down counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation. Asynchronous parallel load capability permits the counter to be preset to any desired value. Information present on the parallel data inputs (D0 to D3) is loaded into the counter and appears on the outputs when the parallel load ($\overline{PL}$) input is LOW. This operation overrides the counting function. Counting is inhibited by a HIGH level on the count enable ($\overline{CE}$) input. When $\overline{CE}$ is LOW internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The up/down ($\overline{U}$/D) input signal determines the direction of counting as indicated in the function table. The $\overline{CE}$ input may go LOW when the clock is in either state, however, the LOW-to-HIGH $\overline{CE}$ transition must occur only when the clock is HIGH. Also, the $\overline{U}$/D input should be changed only when either $\overline{CE}$ or CP is HIGH. Overflow/underflow indications are provided by two types of outputs, the terminal count (TC) and ripple clock ($\overline{RC}$). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches '15' in the count-up-mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output. When TC is HIGH and $\overline{CE}$ is LOW, the $\overline{RC}$ output follows the clock pulse (CP). This feature simplifies the design of multistage counters as shown in Fig. 5 and Fig. 6. In Fig. 5, each $\overline{RC}$ output is used as the clock input to the next higher stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This can be a disadvantage of this configuration in some applications. Fig. 6 shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all clock inputs are driven in parallel. In this configuration the duration of the clock LOW state must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH there is no such restriction on the HIGH-state duration of the clock. In Fig. 7, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input for a given stage. An enable must be included in each carry gate in order to inhibit counting. The TC output of a given stage it not affected by its own $\overline{CE}$ signal therefore the simple inhibit scheme of Fig. 5 and Fig. 6 does not apply. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Complies with JEDEC standard no. 7A
- CMOS input levels:
- Synchronous reversible counting
- Asynchronous parallel load
- Count enable control for synchronous expansion
- Single up/down control input
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC191D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC191DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC191PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

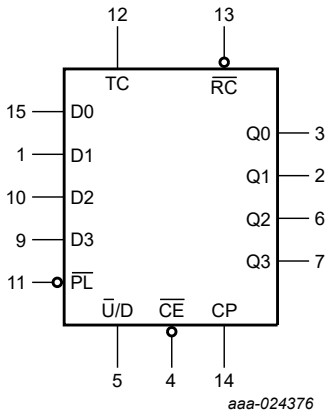


Fig. 1. Logic symbol

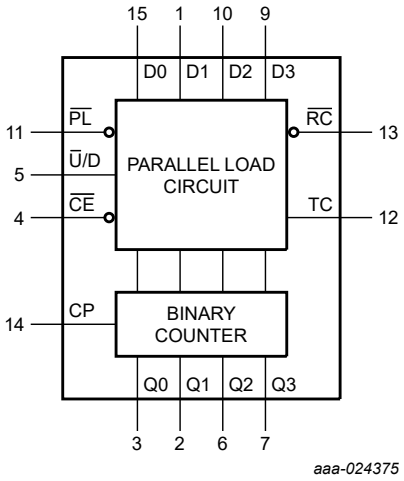


Fig. 2. Functional diagram

5. Pinning information

5.1. Pinning

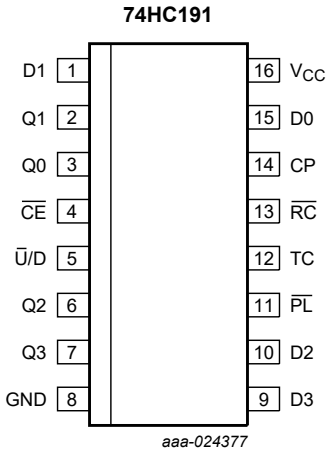


Fig. 3. Pin configuration SOT109-1 (SO16)

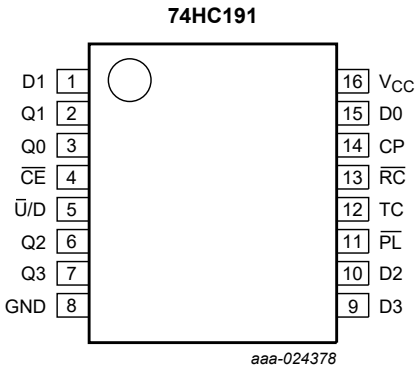


Fig. 4. Pin configuration SOT338-1 (SSOP16) and SOT403-1 (TSSOP16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
D0, D1, D2, D3	15, 1, 10, 9	data input
Q0, Q1, Q2, Q3	3, 2, 6, 7	flip-flop output
$\overline{CE}$	4	count enable input (active LOW)
$\overline{U}$/D	5	up/down input
GND	8	ground (0 V)
$\overline{PL}$	11	parallel load input (active LOW)
TC	12	terminal count output
$\overline{RC}$	13	ripple clock output (active LOW)
CP	14	clock input (LOW-to-HIGH, edge-triggered)
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition; X = don't care;
↑ = LOW-to-HIGH clock transition

Operating mode	Input					Output
	$\overline{PL}$	$\overline{U}$/D	$\overline{CE}$	CP	Dn	Qn
parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
count up	H	L	l	↑	X	count up
count down	H	H	l	↑	X	count down
Hold (do nothing)	H	X	H	X	X	no change

Table 4. TC and $\overline{RC}$ Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ⊔ *= one LOW level pulse;*
⌊ *= TC goes LOW on a LOW-to-HIGH clock transition.*

Input			Terminal count state				Output	
$\overline{U}$/D	$\overline{CE}$	CP	Q0	Q1	Q2	Q3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊔	H	H	H	H	⌊	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	⌊	⊔

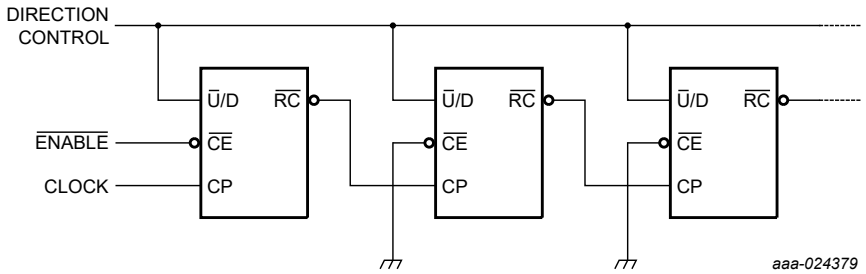


Fig. 5. N-stage ripple counter using ripple clock

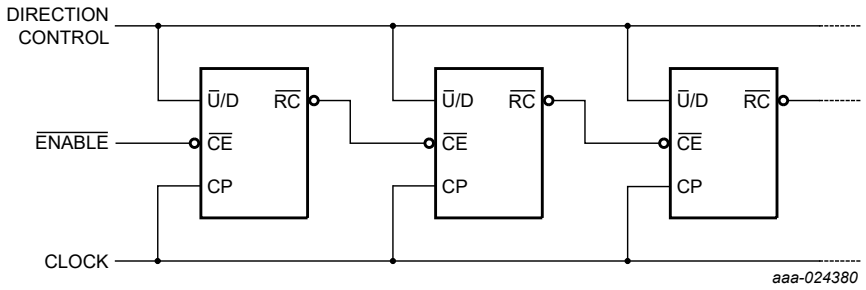


Fig. 6. Synchronous n-stage counter using ripple carry/borrow

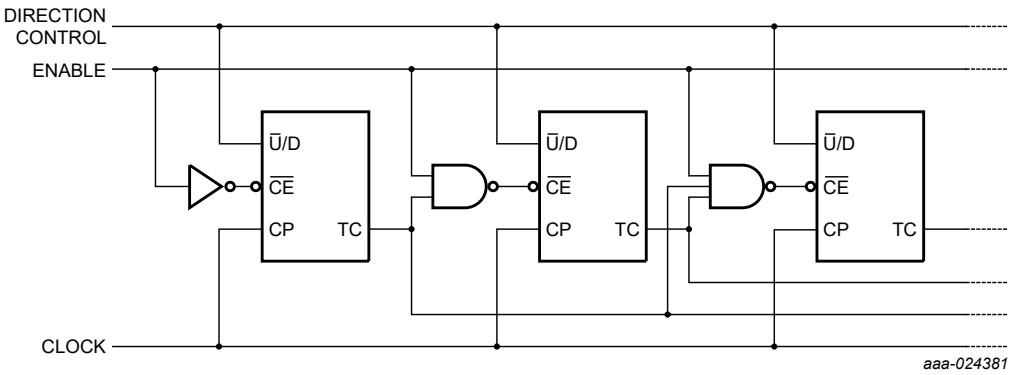


Fig. 7. Synchronous n-stage counter with parallel gated carry/borrow

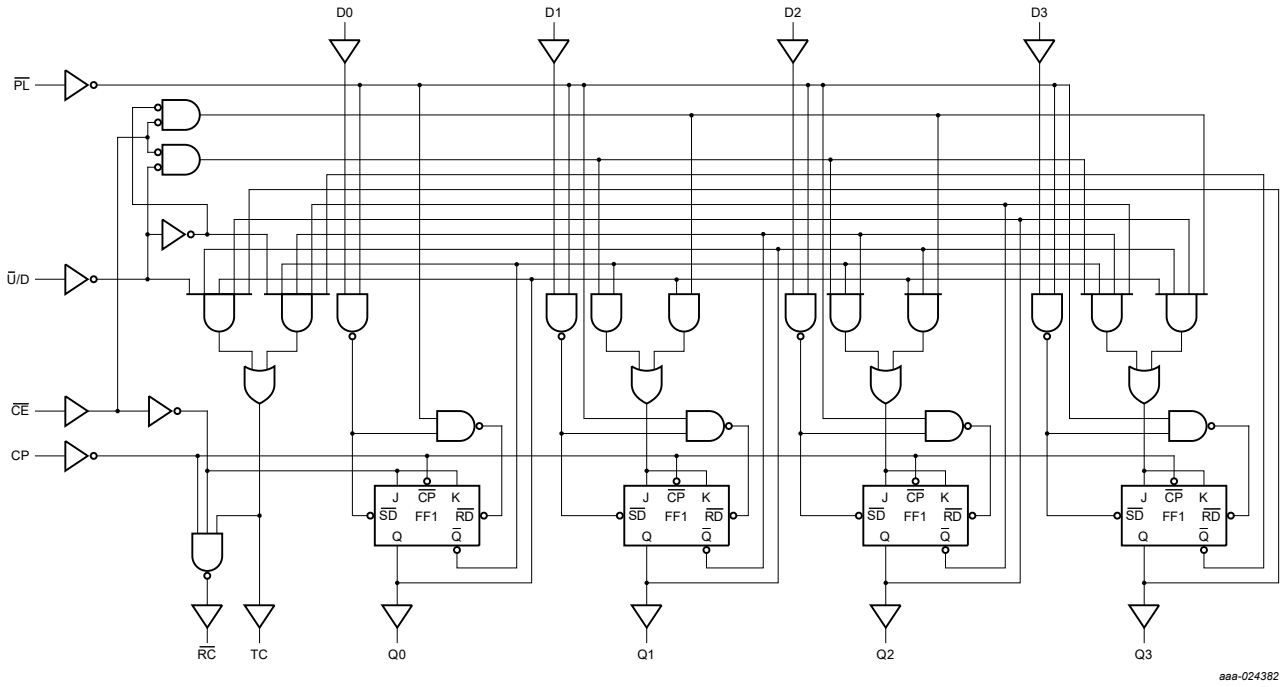
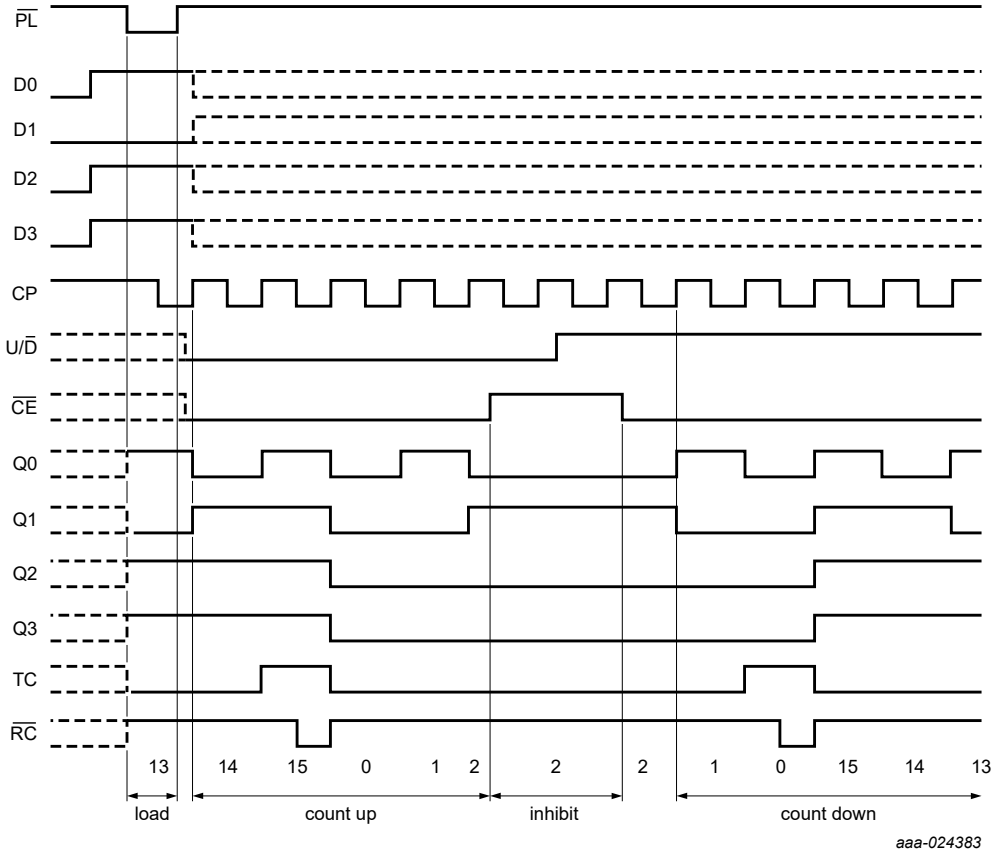


Fig. 8. Logic diagram



Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one and two; inhibit.

Fig. 9. Typical timing sequence

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	[1]	-	500	mW

[1] For SOT109-1 (SO16) packages: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT338-1 (SSOP16) packages: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT403-1 (TSSOP16) packages: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	ns/V
		V_{CC} = 4.5 V	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	ns/V

9. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -4.0; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -5.2; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80.0	-	160.0	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Fig. 18.

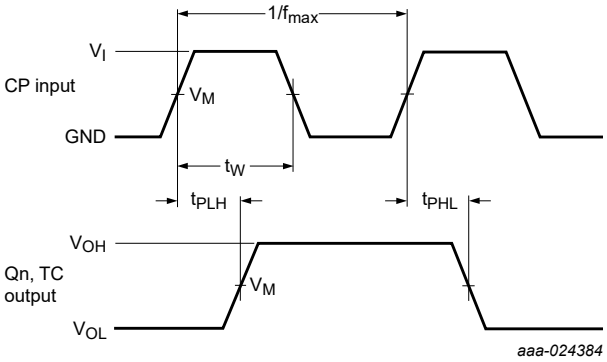
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	CP to Qn; see Fig. 10 [1]								
		V_{CC} = 2.0 V	-	72	220	-	275	-	330	ns
		V_{CC} = 4.5 V	-	26	44	-	55	-	66	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	22	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	21	37	-	47	-	56	ns
		CP to TC; see Fig. 10								
		V_{CC} = 2.0 V	-	83	255	-	320	-	395	ns
		V_{CC} = 4.5 V	-	30	51	-	64	-	77	ns
		V_{CC} = 6.0 V	-	24	43	-	54	-	65	ns
		CP to $\overline{RC}$; see Fig. 11								
		V_{CC} = 2.0 V	-	47	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	17	30	-	38	-	45	ns
		V_{CC} = 6.0 V	-	14	26	-	33	-	38	ns
		$\overline{CE}$ to $\overline{RC}$; see Fig. 11								
		V_{CC} = 2.0 V	-	33	130	-	165	-	195	ns
		V_{CC} = 4.5 V	-	12	26	-	33	-	39	ns
		V_{CC} = 6.0 V	-	10	22	-	28	-	33	ns
		Dn to Qn; see Fig. 12								
		V_{CC} = 2.0 V	-	61	220	-	275	-	330	ns
		V_{CC} = 4.5 V	-	22	44	-	55	-	66	ns
		V_{CC} = 6.0 V	-	18	37	-	47	-	56	ns
		$\overline{PL}$ to Qn; see Fig. 13								
		V_{CC} = 2.0 V	-	61	220	-	275	-	330	ns
		V_{CC} = 4.5 V	-	22	44	-	55	-	66	ns
		V_{CC} = 6.0 V	-	18	37	-	47	-	56	ns
		$\overline{U}$/D to TC; see Fig. 14								
		V_{CC} = 2.0 V	-	44	190	-	240	-	285	ns
		V_{CC} = 4.5 V	-	16	38	-	48	-	57	ns
		V_{CC} = 6.0 V	-	13	32	-	41	-	48	ns
		$\overline{U}$/D to $\overline{RC}$; see Fig. 14								
		V_{CC} = 2.0 V	-	50	210	-	265	-	315	ns
		V_{CC} = 4.5 V	-	18	42	-	53	-	63	ns
		V_{CC} = 6.0 V	-	14	36	-	45	-	54	ns
t_t	transition time	see Fig. 15 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_W	pulse width	CP; HIGH or LOW; see Fig. 10								
		V_{CC} = 2.0 V	125	28	-	155	-	195	-	ns
		V_{CC} = 4.5 V	25	10	-	31	-	39	-	ns
		V_{CC} = 6.0 V	21	8	-	26	-	33	-	ns
		$\overline{PL}$; LOW; see Fig. 15								
		V_{CC} = 2.0 V	100	22	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	8	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	6	-	21	-	26	-	ns
t_{rec}	recovery time	$\overline{PL}$ to CP; see Fig. 15								
		V_{CC} = 2.0 V	35	8	-	45	-	55	-	ns
		V_{CC} = 4.5 V	7	3	-	9	-	11	-	ns
		V_{CC} = 6.0 V	6	2	-	8	-	9	-	ns
t_{su}	set-up time	$\overline{U}$/D to CP; see Fig. 16								
		V_{CC} = 2.0 V	205	50	-	255	-	310	-	ns
		V_{CC} = 4.5 V	41	18	-	51	-	62	-	ns
		V_{CC} = 6.0 V	35	14	-	43	-	53	-	ns
		Dn to $\overline{PL}$; see Fig. 17								
		V_{CC} = 2.0 V	100	19	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	7	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	6	-	21	-	26	-	ns
		$\overline{CE}$ to CP; see Fig. 16								
		V_{CC} = 2.0 V	140	44	-	175	-	210	-	ns
		V_{CC} = 4.5 V	28	16	-	35	-	42	-	ns
		V_{CC} = 6.0 V	24	13	-	30	-	36	-	ns
t_h	hold time	$\overline{U}$/D to CP; see Fig. 16								
		V_{CC} = 2.0 V	0	-39	-	0	-	0	-	ns
		V_{CC} = 4.5 V	0	-14	-	0	-	0	-	ns
		V_{CC} = 6.0 V	0	-11	-	0	-	0	-	ns
		Dn to $\overline{PL}$; see Fig. 17								
		V_{CC} = 2.0 V	0	-11	-	0	-	0	-	ns
		V_{CC} = 4.5 V	0	-4	-	0	-	0	-	ns
		V_{CC} = 6.0 V	0	-3	-	0	-	0	-	ns
		$\overline{CE}$ to CP; see Fig. 16								
		V_{CC} = 2.0 V	0	-28	-	0	-	0	-	ns
		V_{CC} = 4.5 V	0	-10	-	0	-	0	-	ns
		V_{CC} = 6.0 V	0	-8	-	0	-	0	-	ns
f_{max}	maximum frequency	CP; see Fig. 10								
		V_{CC} = 2.0 V	4.0	11	-	3.2	-	2.6	-	MHz
		V_{CC} = 4.5 V	20	33	-	16	-	13	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	36	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	24	39	-	19	-	15	-	MHz

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 5 V; f_i = 1 MHz [3]	-	31	-	-	-	-	-	pF

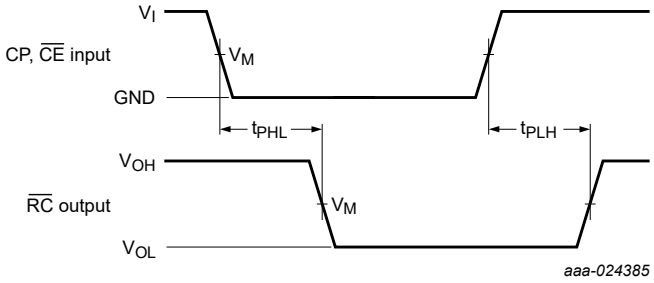
[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] t_t is the same as t_{THL} and t_{TLH}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



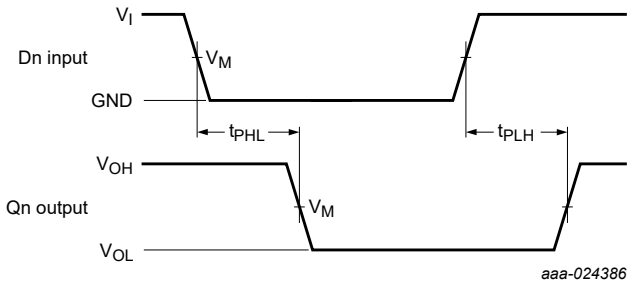
Measurement points are given in Table 9.
Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 10. The clock input (CP) to outputs (Qn, TC) propagation delays, clock pulse width and maximum clock frequency



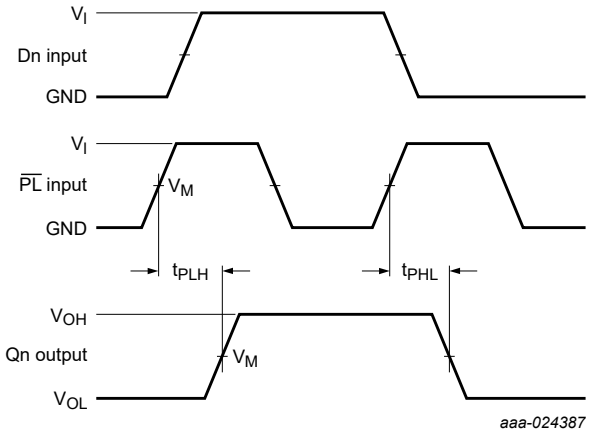
Measurement points are given in Table 9.
Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 11. The clock and count enable inputs (CP, $\overline{CE}$) to ripple clock output ($\overline{RC}$) propagation delays



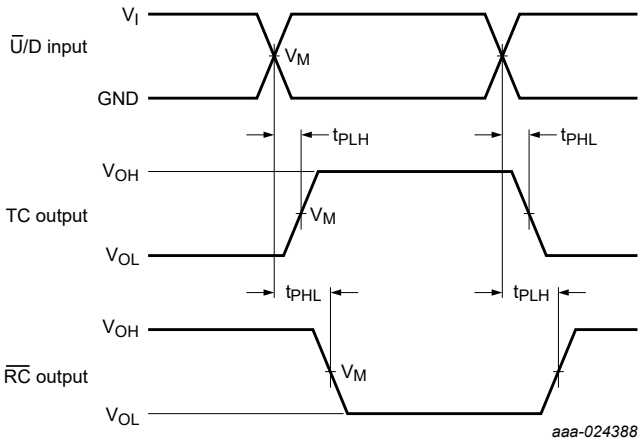
Measurement points are given in Table 9.
Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 12. The input (Dn) to output (Qn) propagation delays



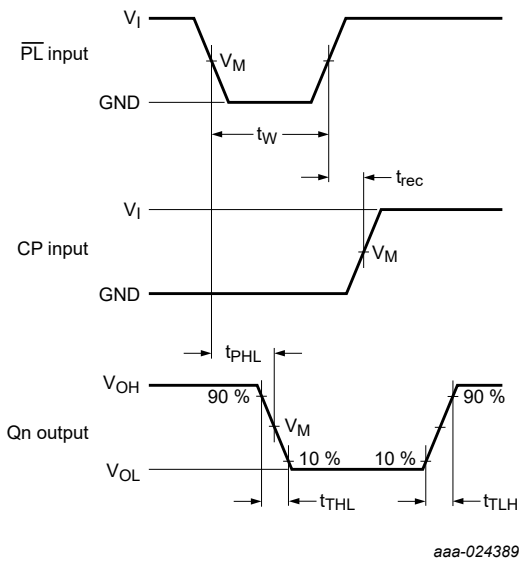
Measurement points are given in Table 9.
Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 13. The parallel load input ($\overline{PL}$) to output (Qn) propagation delays



Measurement points are given in Table 9.
Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

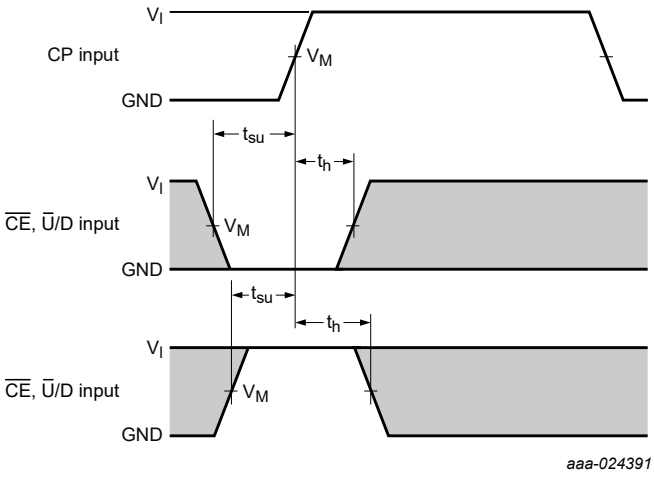
Fig. 14. The up/down count input ($\overline{U}$/D) to terminal count and ripple clock output (TC, $\overline{RC}$) propagation delays



Measurement points are given in Table 9.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

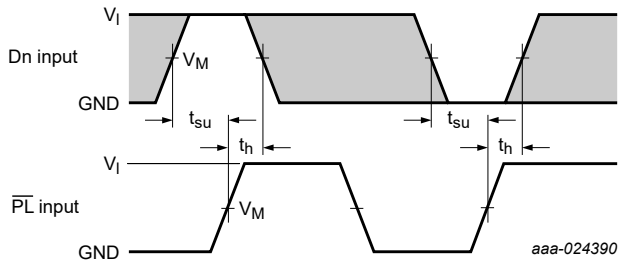
Fig. 15. The parallel load input ($\overline{PL}$) to clock (CP) recovery times, parallel load pulse width and output (Qn) transition times



Measurement points are given in Table 9.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 16. The count enable and up/down count inputs ($\overline{CE}$, $\overline{U}$/D) to clock input (CP) set-up and hold times



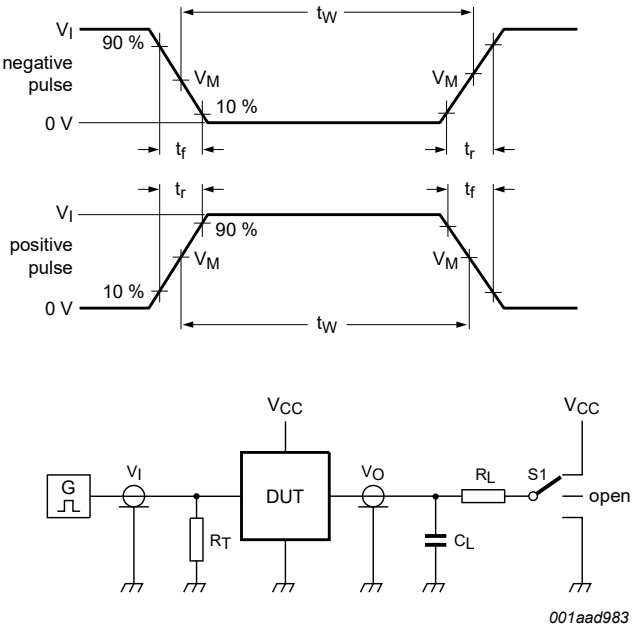
Measurement points are given in Table 9.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 17. The parallel load input ($\overline{PL}$) to data input (Dn) set-up and hold times

Table 9. Measurement points

Input		Output
V_M	V_I	V_M
0.5 x V_{CC}	GND to V_{CC}	0.5 x V_{CC}



Test data is given in Table 10.

Test circuit definitions:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

R_L = Load resistance.

S1 = Test selection switch

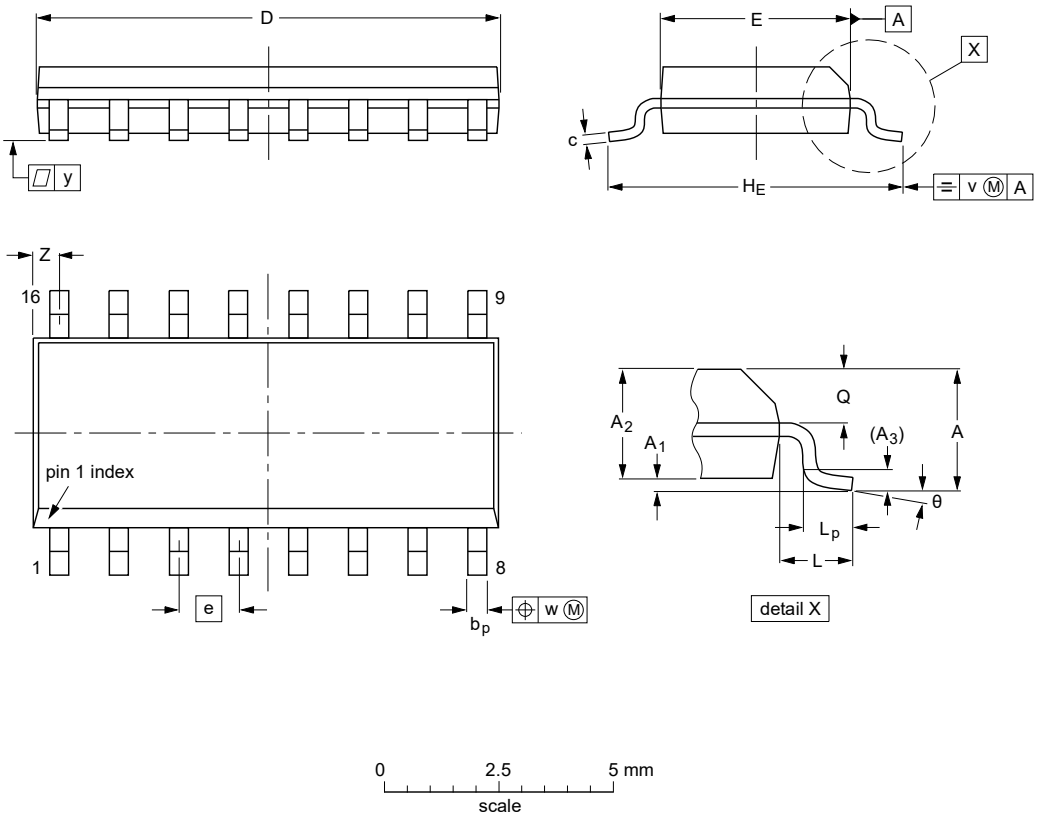
Fig. 18. Test circuit for measuring switching times

Table 10. Test data

Input		Load		S1 position
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

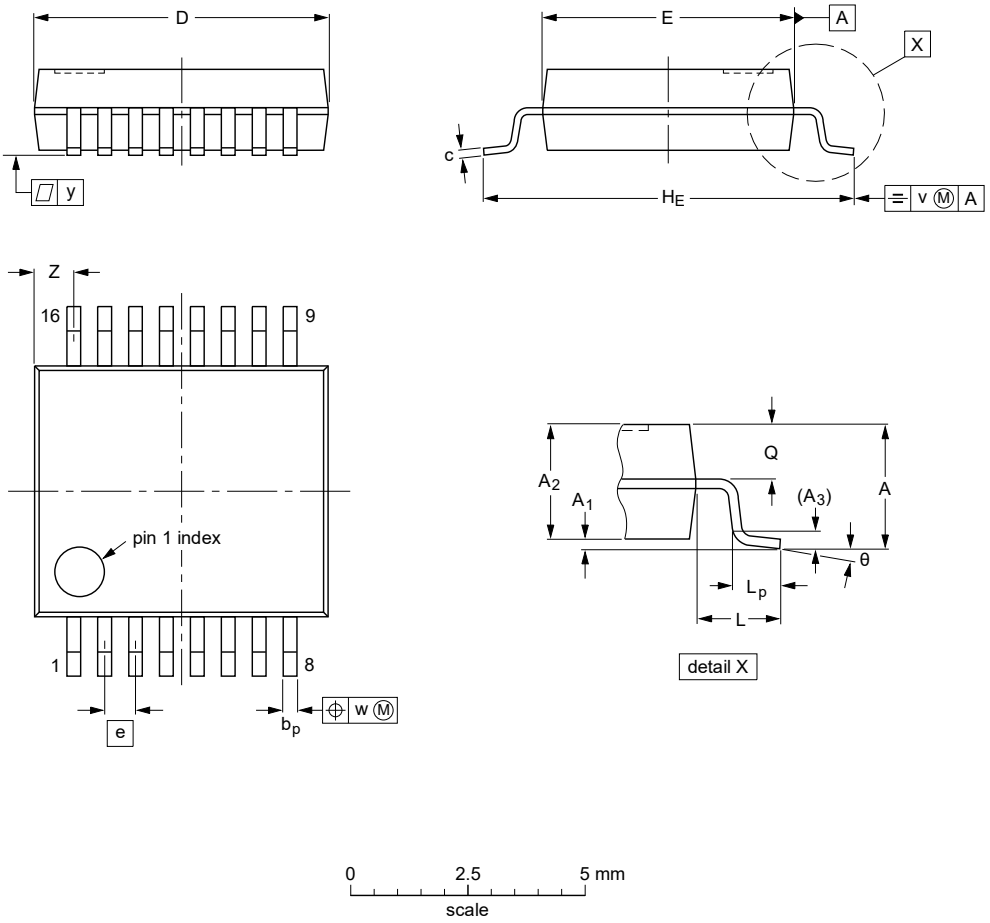
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig. 19. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

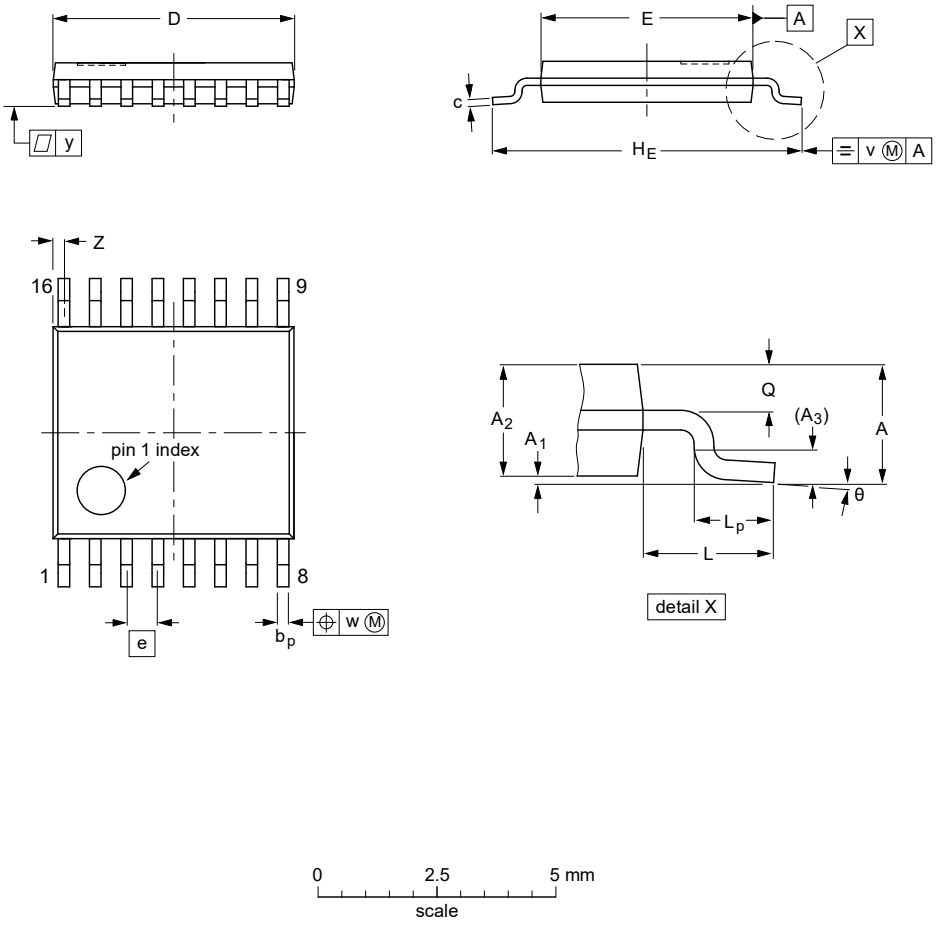
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig. 20. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 21. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC191 v.5	20190813	Product data sheet	-	74HC191 v.4
Modifications:	• Type number 74HC191DB (SOT338-1 / SSOP16) added. • Table 5: Derating values for P_{tot} total power dissipation updated			
74HC191 v.4	20181005	Product data sheet	-	74HC191 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74HC191DB (SOT338-1 / SSOP16) removed.			
74HC191 v.3	20170103	Product data sheet	-	74HC_HCT191 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HCT191D, 74HCT191DB, 74HCT191PW removed.			
74HC_HCT191_CNV v.2	19901201	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 13 August 2019