Backlight Driver for 7 LEDs with Charge Pump and PWM Control

Features

- Input supply voltage range — 2.9V to 5.5V
- Charge pump modes — 1x, 1.5x and 2x
- PWM dimming control with low pass filter provides DC backlight current (not pulsed)
- Two independently configurable backlight banks
- PWM frequency range — 200Hz to 50kHz
- Seven adjustable current sinks — 500µA to 25mA
- Backlight current accuracy ±1.5% typical
- Backlight current matching ±0.5% typical
- LED float detection
- Charge pump frequency — 250kHz
- Low shutdown current — 0.1µA typical
- Ultra-thin package — 3 x 3 x 0.6(mm)
- Fully WEEE and RoHS compliant, and halogen free.

Applications

- Cellular phones, smart phones, and PDAs
- LCD display modules
- Portable media players
- Digital cameras
- Personal navigation devices
- Display/keypad backlighting and LED indicators

Description

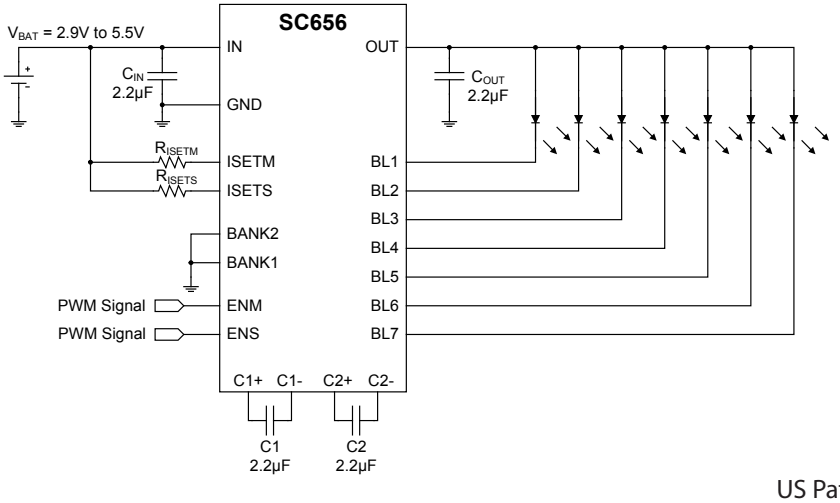
The SC656 is a high efficiency charge pump LED driver using Semtech's proprietary charge pump technology. Performance is optimized for use in single-cell Li-ion battery applications.

The device provides backlight current using up to seven matched current sinks. The load and supply conditions determine whether the charge pump operates in 1x, 1.5x, or 2x mode. The seven backlights can be configured as a single group or split into two independent banks by setting the state of the BANK2 and BANK1 pins. If only one bank is needed, the BANK2, BANK1, ENS and ISETS pins must be grounded.

The maximum current per LED in each bank is set by a resistor connected to ISETM or ISETS. LED current can be set between 500µA and 25mA. Backlight current is varied by applying a pulse-width modulated (PWM) signal to the ENM pin for the main LED bank and the ENS pin for the sub LED bank. The resulting DC current in each LED (I_{BL}) is equal to the maximum current setting multiplied by the duty cycle of the PWM signal. During PWM operation, a low-pass filter is used to develop a DC current through the LED. The resulting power conversion is more efficient than comparable pulsed current solutions. Backlight fading is initiated when the duty cycle is changed.

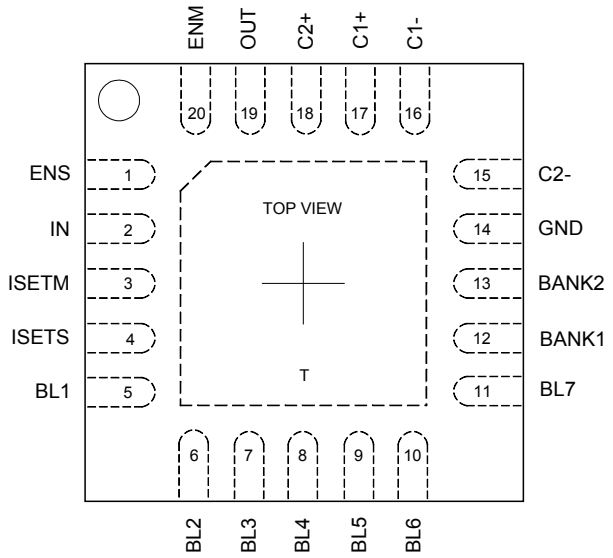
The 3 x 3 (mm) package and minimal number of small external components make the SC656 an ideal backlight driver solution for space-limited designs.

Typical Application Circuit



US Patents: 6,504,422; 6,794,926

Pin Configuration



MLPQ-UT-20; 3x3, 20 LEAD

θ_{JA} = 35°C/W

Ordering Information

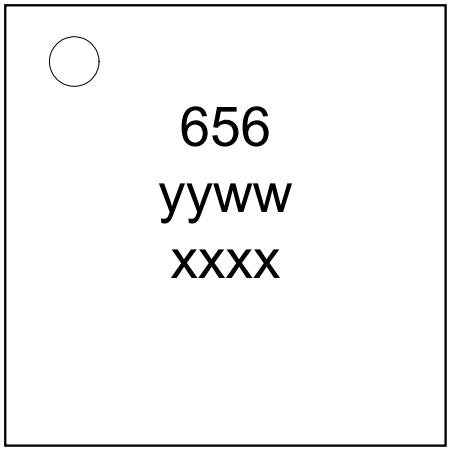
Device	Package
SC656ULTRT[1][2]	MLPQ-UT-20 3×3
SC656EVB	Evaluation Board

Notes:

(1) Available in tape and reel only. A reel contains 3,000 devices.

(2) Lead-free package only. Device is WEEE and RoHS compliant, and halogen free.

Marking Information



yyww = Date Code

xxxx = Semtech Lot Number

SEMTECH

Absolute Maximum Ratings

IN, OUT (V) ..... -0.3 to +6.0
C1+, C2+ (V) ..... -0.3 to (V_{OUT} + 0.3)
Pin Voltage — All Other Pins (V) ..... -0.3 to (V_{IN} + 0.3)
OUT Short Circuit Duration ..... Continuous
ESD Protection Level[1] (kV) 3

Recommended Operating Conditions

Ambient Temperature Range (°C) ..... $-40 \le T_A \le +85$
Input Voltage (V) ..... 2.9 to 5.5
Output Voltage (V) ..... 2.5 to 5.25
Voltage Difference between any two LEDs (V) ... $\Delta V_F \le 1.0$[2]

Thermal Information

Thermal Resistance, Junction to Ambient[3] (°C/W) ... 40
Maximum Junction Temperature (°C) ..... +150
Storage Temperature Range (°C) ..... -65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C) ..... +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114-B.
(2) $\Delta V_{F(max)}$ = 1.0V when V_{IN} = 2.9V, higher V_{IN} supports higher $\Delta V_{F(max)}$
(3) Calculated from package in still air, mounted to 3 x 4.5(in), 4 layer FR4 PCB per JESD51 standards.

Electrical Characteristics

Unless otherwise noted, T_A = +25°C for Typ, -40°C to +85°C for Min and Max, $T_{J(MAX)}$ = 125°C, V_{IN} = 3.7V, C_{IN}= C_{OUT} = C_1= C_2= 2.2µF, (ESR = 0.03Ω), 500µA < I_{FS_BL} < 25mA, Duty Cycle of PWM = 100%, All 7 LEDs connected and enabled as a single bank.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Shutdown Current	$I_{Q(OFF)}$	T_A = 25°C		0.1	2	µA
Quiescent Current	I_Q	1x mode, V_{IN} = 3.7V, 7 LEDs at 1mA on main bank, PWM duty cycle = 5%, R_{ISETM} = 4.99kΩ		2.5		mA
		1.5x mode, V_{IN} = 3.2V, 7 LEDs at 1mA on main bank, PWM duty cycle = 5%, R_{ISETM} = 4.99kΩ		2.8		
		2x mode, V_{IN} = 2.9V, 7 LEDs at 1mA on main bank, PWM duty cycle = 5%, R_{ISETM} = 4.99kΩ		3.0		
Maximum Total Output Current	$I_{OUT(MAX)}$	V_{IN} > 3.0V, sum of all active LED currents, $V_{OUT(MAX)}$ = 4.2V	175			mA
Backlight Current Setting	I_{FS_BL}	PWM duty cycle = 100%, 200kΩ ≥ R_{ISETX} ≥ 4kΩ	0.5		25	mA
Current Gain[1]	I_{GAIN}	Gain from I_{ISETX} to I_{FS_BL}		100		A/A
Current Set Voltage	$V_{IN - ISET}$	Voltage across R_{ISETX}		1		V
Backlight Current Matching[2]	I_{BL-BL}	I_{FS_BL} = 12mA, Duty = 100%	-3.5	±0.5	+3.5	%
Backlight Current Accuracy	I_{BL_ACC}	I_{FS_BL} = 12mA, Duty = 100%		±1.5		%
EN/PWM Input Frequency	$f_{EN/PWM}$	Duty-cycle percentage changes linearly with I_{FS_BL}	0.2		50	kHz
ENM, ENS Minimum High	t_{HIGH_MIN}			1		µs

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Current Transition Settling Time	t_s	Duty cycle change from 100% to 50%(1)(4)		0.5		s
ENM/ENS Low Time	t_{LT}	Time that voltage on ENM or ENS can be low without disabling the device			5	ms
1x Mode to 1.5x Mode Falling Transition Voltage	$V_{TRANS1x}$	I_{OUT} = 70mA, I_{BLn} = 10mA, V_{OUT} = 3.2V		3.26		V
1.5x Mode to 2x Mode Falling Transition Voltage	$V_{TRANS1.5x}$	I_{OUT} = 70mA, I_{BLn} = 10mA, V_{OUT} = 4.0V(3)		2.90		V
Current Sink Off-State Leakage Current	$I_{BLn(off)}$	$V_{IN} = V_{BLn}$ = 4.2V		0.1	1	µA
Charge Pump Frequency	f_{PUMP}	V_{IN} = 3.2V		250		kHz
Output Short Circuit Current Limit	$I_{OUT(SC)}$	OUT pin shorted to GND		50		mA
		V_{OUT} > 2.5V		400		
Under Voltage Lockout Threshold	V_{UVLO}	Increasing V_{IN} — lockout released		2.4		V
UVLO Hysteresis	$V_{UVLO-HYS}$			500		mV
Over-Voltage Protection	V_{OVP}	OUT pin open circuit, $V_{OUT} = V_{OVP}$, V_{IN} rising threshold		5.7	6.0	V
Over-Temperature	T_{OT}	Rising Temperature		165		°C
OT Hysteresis	T_{OT-HYS}			25		°C
Digital Logic Pins — ENM, ENS, BANK2, AND BANK1						
Input High Threshold	V_{IH}	V_{IN} = 5.5V	1.4			V
Input Low Threshold	V_{IL}	V_{IN} = 2.9V			0.4	V
Input High Current	I_{IH}	V_{IN} = 5.5V			1	µA
Input Low Current	I_{IL}	V_{IN} = 5.5V			1	µA

Notes:

(1) Guaranteed by design

(2) Current matching equals ± [$I_{BL(MAX)}$ - $I_{BL(MIN}$] / [$I_{BL(MAX)}$ + $I_{BL(MIN)}$].

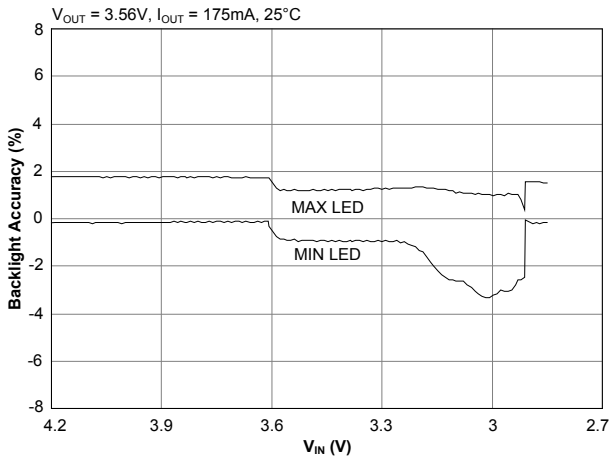
(3) Test voltage is V_{OUT} = 4.0V — a relatively extreme LED voltage used to force a transition during test. Typically V_{OUT} = 3.2V for white LEDs.

(4) The settling time is affected by the magnitude of change in the PWM duty cycle.

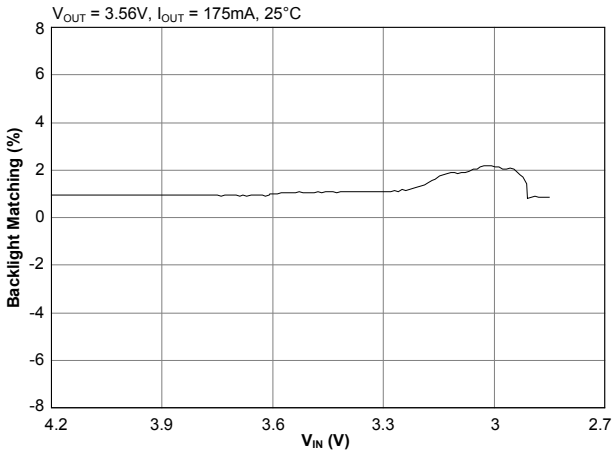
Typical Characteristics

$C_{IN} = C_{OUT} = C_1 = C_2 = 2.2\mu F$ — 0603 size (1608 metric)

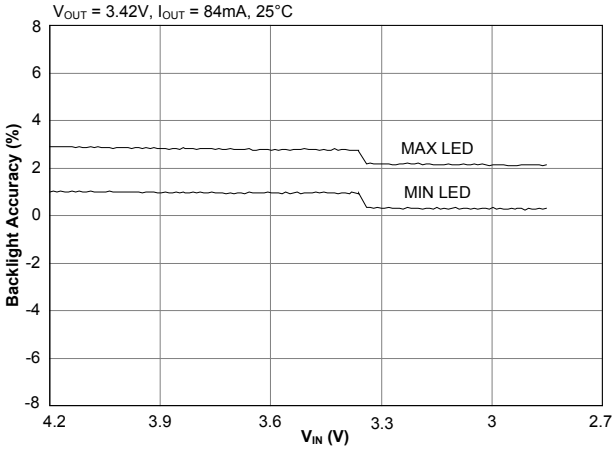
Backlight Accuracy (7 LEDs) — 25mA Each



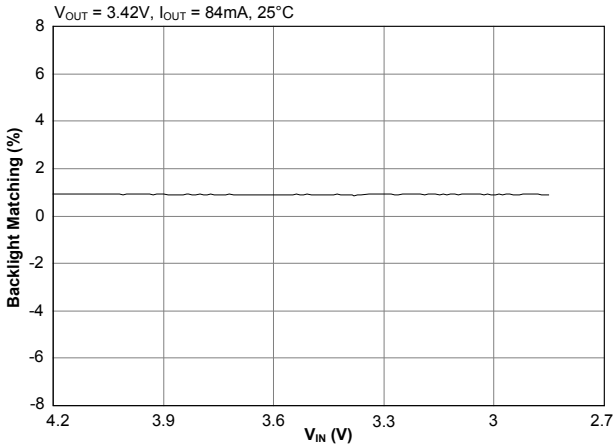
Backlight Matching (7 LEDs) — 25mA Each



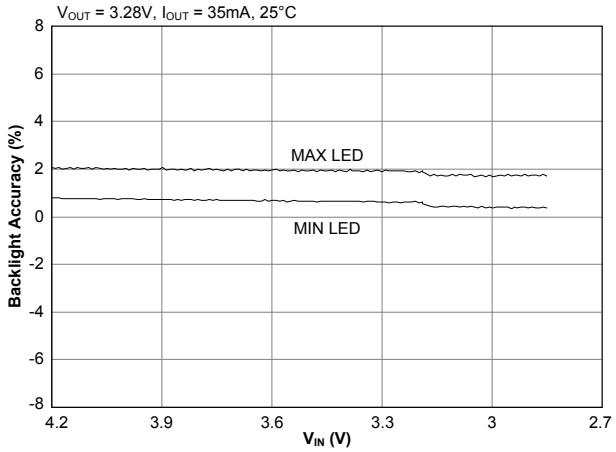
Backlight Accuracy (7 LEDs) — 12mA Each



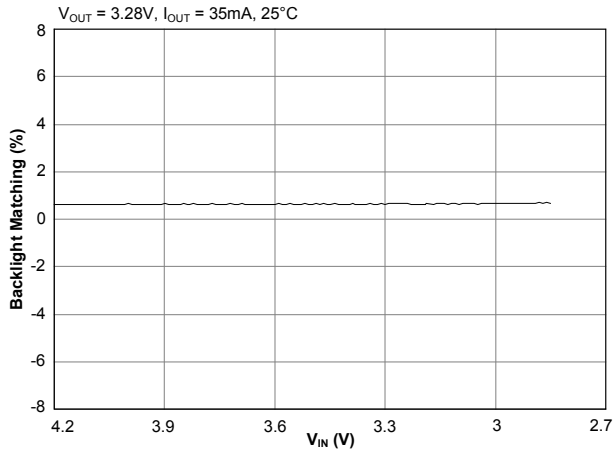
Backlight Matching (7 LEDs) — 12mA Each



Backlight Accuracy (7 LEDs) — 5mA Each

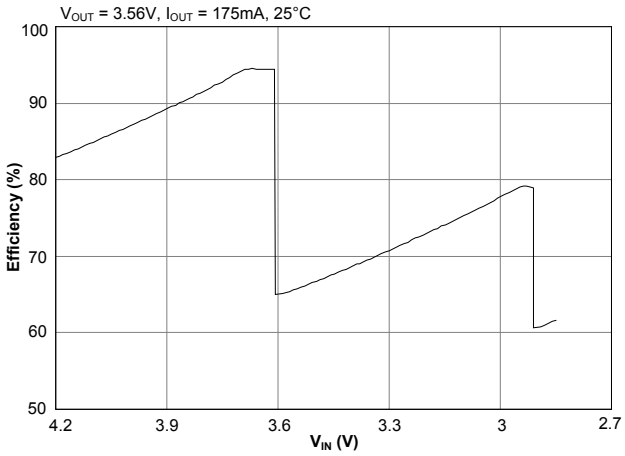


Backlight Matching (7 LEDs) — 5mA Each

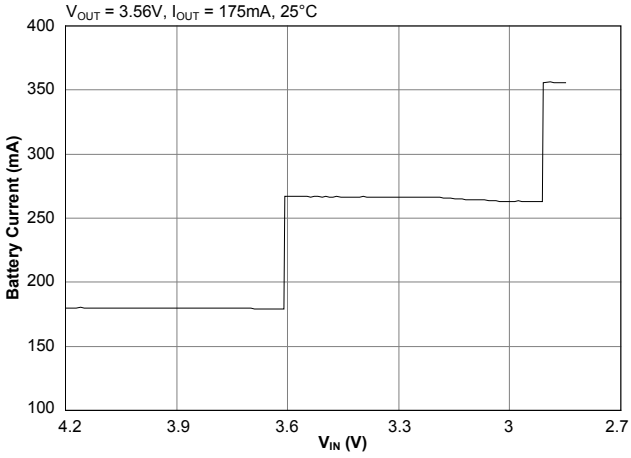


Typical Characteristics (continued)

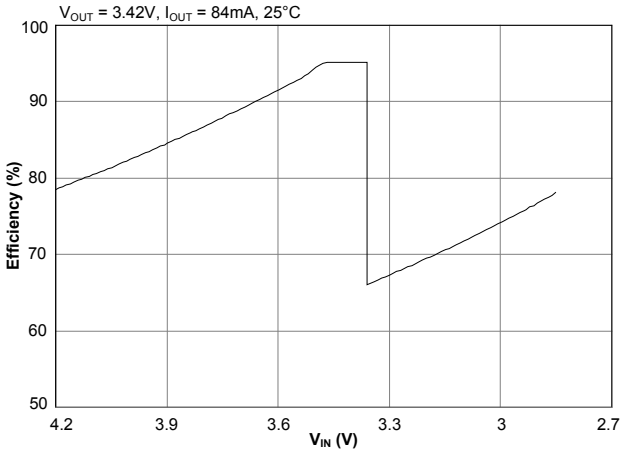
Charge Pump Efficiency (7 LEDs) — 25mA Each



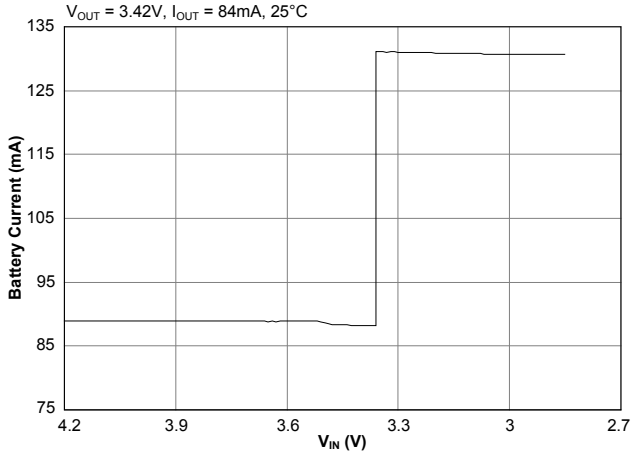
Backlight Current (7 LEDs) — 25mA Each



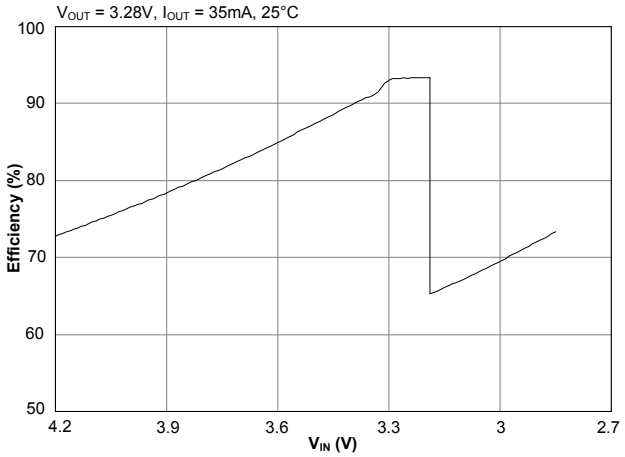
Charge Pump Efficiency (7 LEDs) — 12mA Each



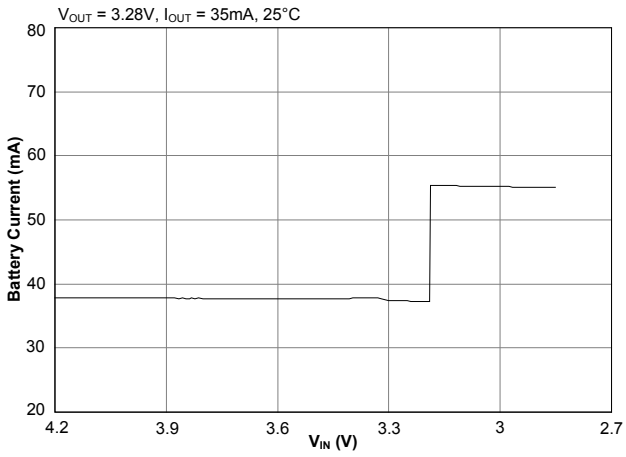
Backlight Current (7 LEDs) — 12mA Each



Charge Pump Efficiency (7 LEDs) — 5mA Each

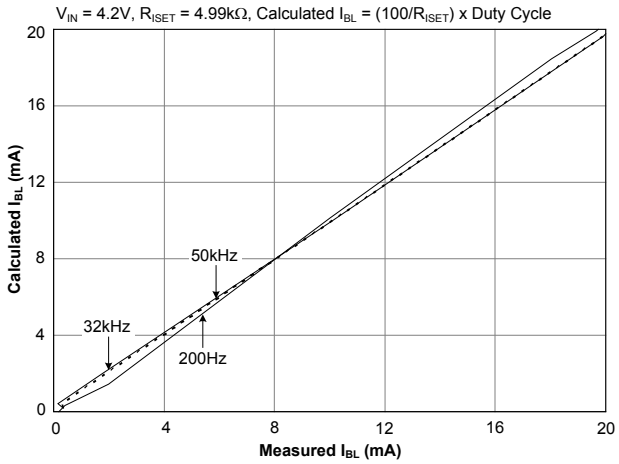


Backlight Current (7 LEDs) — 5mA Each

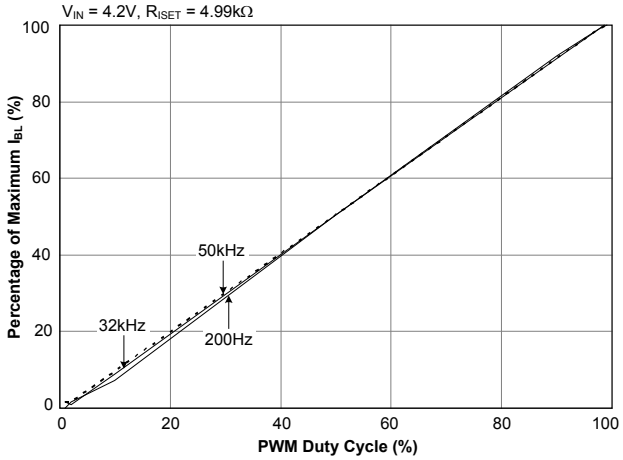


Typical Characteristics (continued)

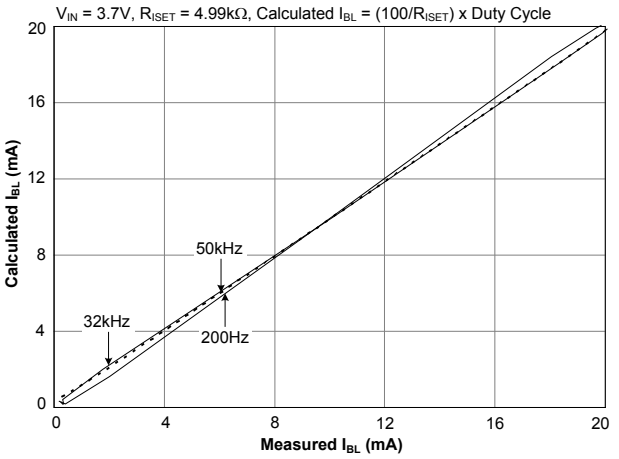
PWM Accuracy — 4.2V



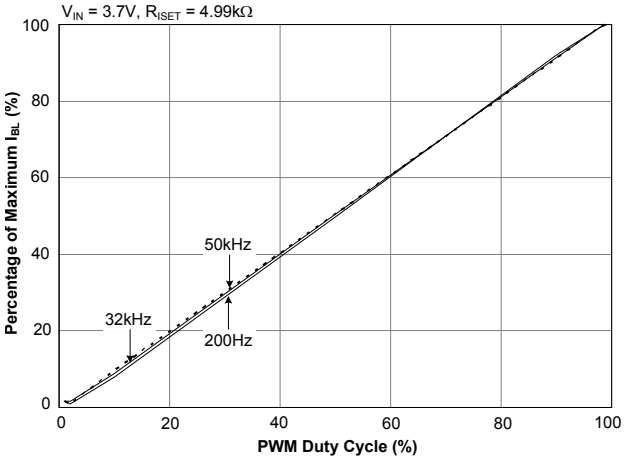
Percentage of Maximum I_{BL} — 4.2V



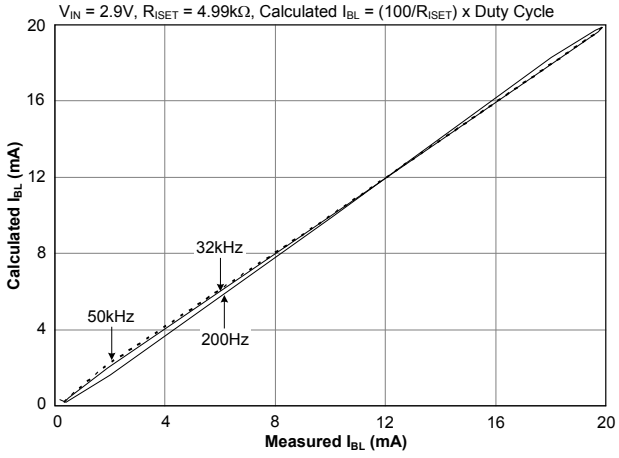
PWM Accuracy — 3.7V



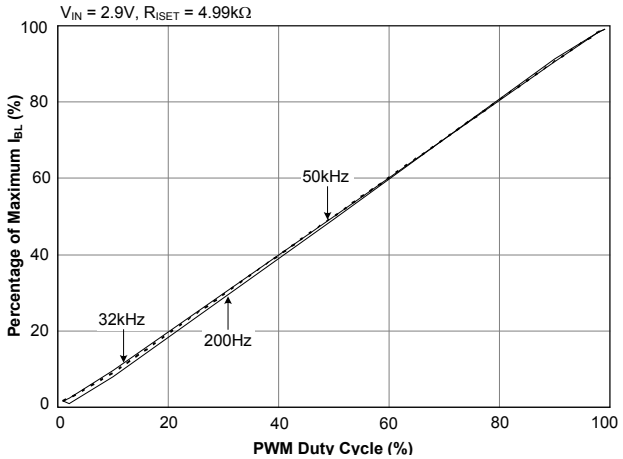
Percentage of Maximum I_{BL} — 3.7V



PWM Accuracy — 2.9V



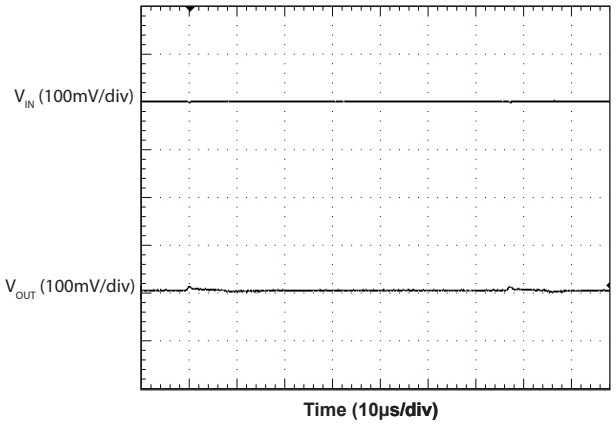
Percentage of Maximum I_{BL} — 2.9V



Typical Characteristics (continued)

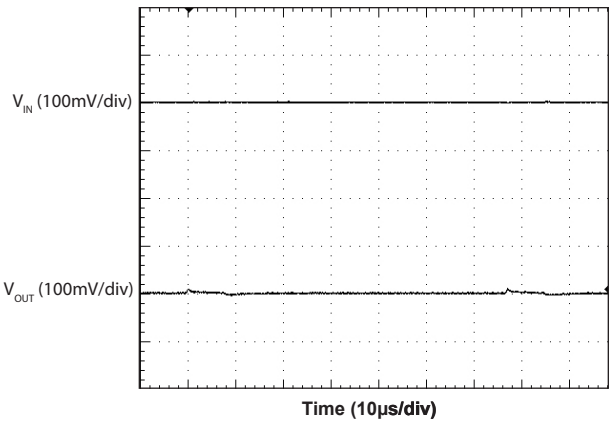
Ripple — 1X Mode

V_{IN}=4.2V, R_{ISET} = 4kΩ, 7 Backlights — 25 mA each, 25°C



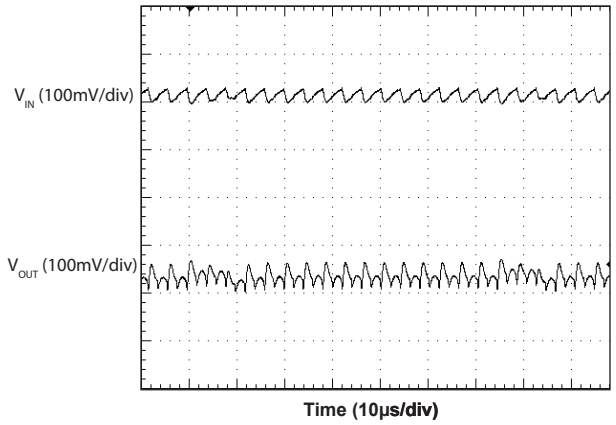
Ripple — 1X Mode

V_{IN}=4.2V, R_{ISET} = 5.56kΩ, 7 Backlights — 18 mA each, 25°C



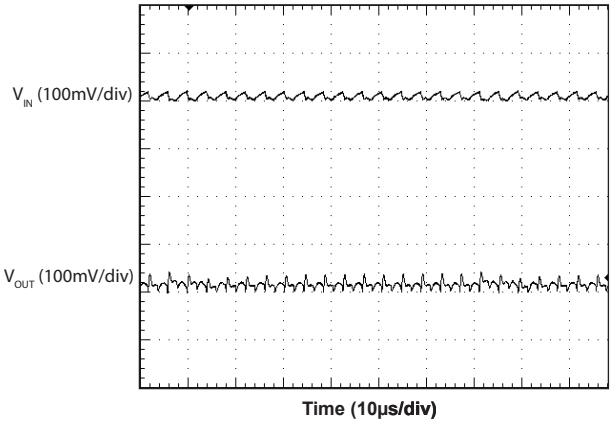
Ripple — 1.5X Mode

V_{IN}=3.2V, R_{ISET} = 4kΩ, 7 Backlights — 25 mA each, 25°C



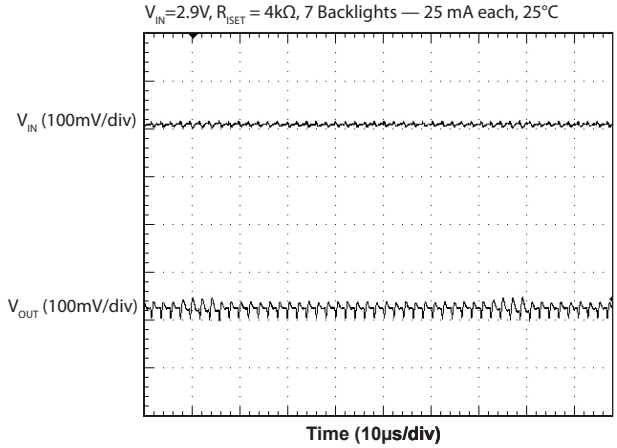
Ripple — 1.5X Mode

V_{IN}=3.2V, R_{ISET} = 5.56kΩ, 7 Backlights — 18 mA each, 25°C



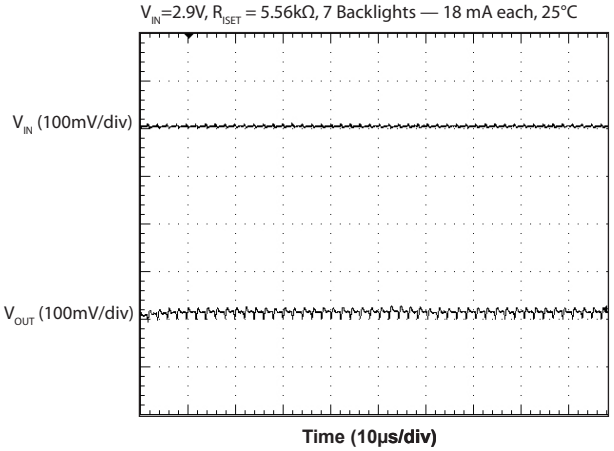
Ripple — 2X Mode

V_{IN}=2.9V, R_{ISET} = 4kΩ, 7 Backlights — 25 mA each, 25°C



Ripple — 2X Mode

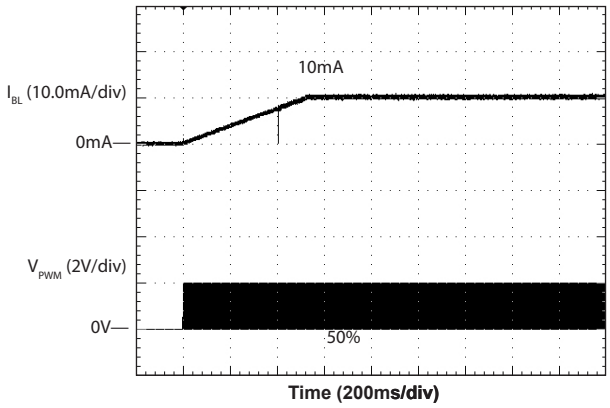
V_{IN}=2.9V, R_{ISET} = 5.56kΩ, 7 Backlights — 18 mA each, 25°C



Typical Characteristics (continued)

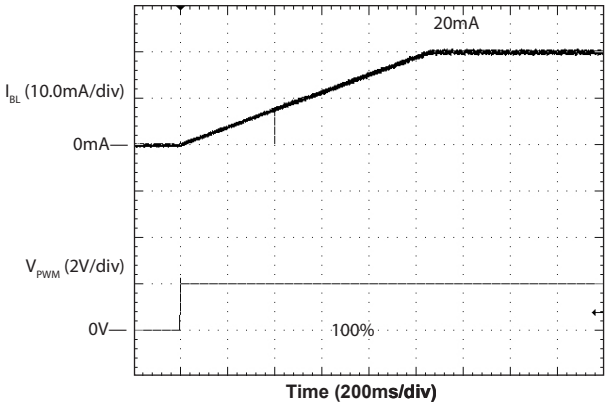
Start-up — 0% to 50%

V_{IN} = 3.7V, 0 to 50% duty cycle, R_{ISET} = 4.99kΩ, f_{PWM} = 32kHz



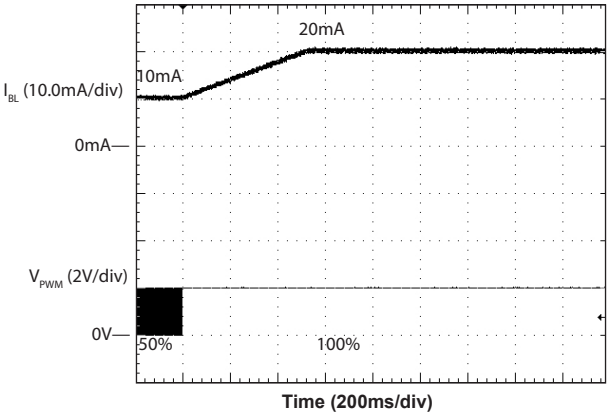
Start-up — 0% to 100%

V_{IN} = 3.7V, 0 to 100% duty cycle, R_{ISET} = 4.99kΩ, no PWM



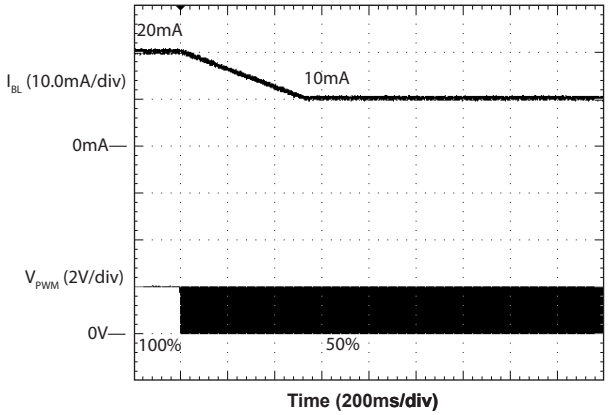
I_{BL} Settling Time — 50% to 100%

V_{IN} = 3.7V, R_{ISET} = 4.99kΩ, f_{PWM} = 32kHz



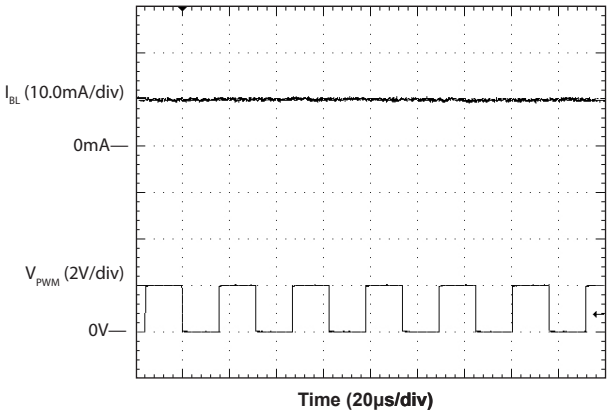
I_{BL} Settling Time — 100% to 50%

V_{IN} = 3.7V, R_{ISET} = 4.99kΩ, f_{PWM} = 32kHz



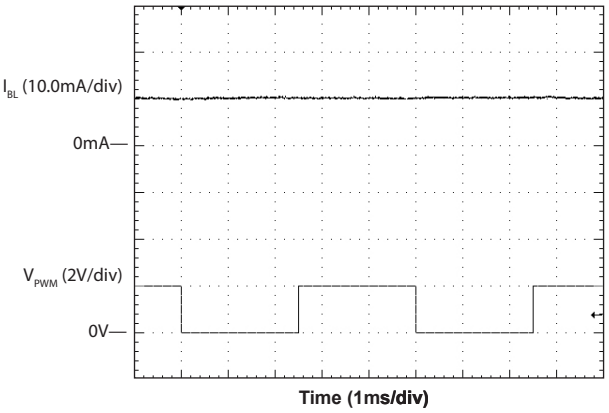
DC Backlight Current — 32kHz PWM

V_{IN} = 3.7V, 50% duty cycle, R_{ISET} = 4.99kΩ, I_{BL} = 10mA



DC Backlight Current — 200Hz PWM

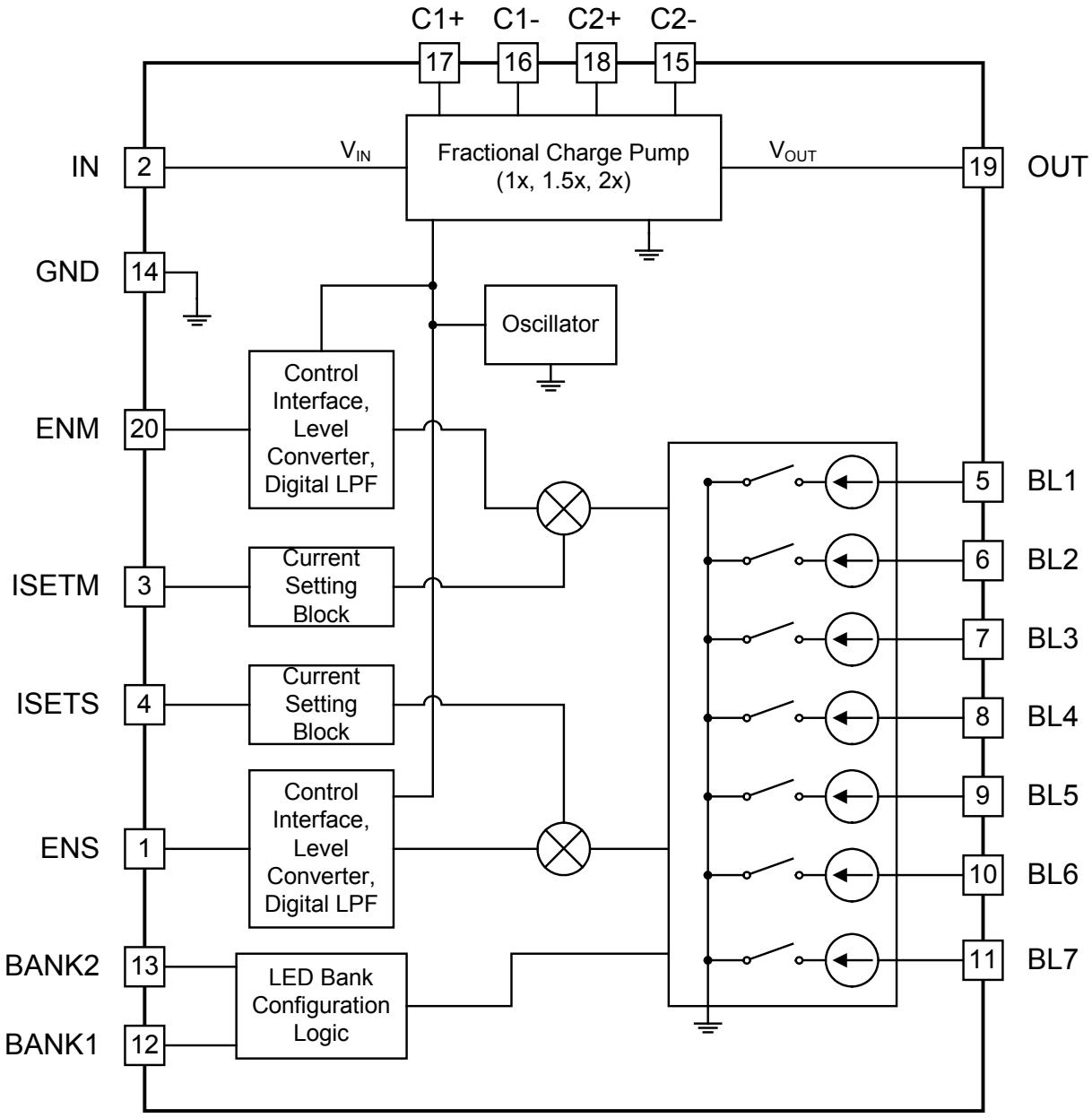
V_{IN} = 3.7V, 50% duty cycle, R_{ISET} = 4.99kΩ, I_{BL} = 10mA



Pin Descriptions

Pin #	Pin Name	Pin Function
1	ENS	Enable pin for sub display LED bank — also used as the PWM dimming control input for this bank
2	IN	Battery voltage input
3	ISETM	Current setting pin — connect a resistor between ISETM and IN to set the main bank LED current.
4	ISETS	Current setting pin — connect a resistor between ISETS and IN to set the sub bank LED current.
5	BL1	Current sink output for backlight LED 1 — leave this pin open if unused
6	BL2	Current sink output for backlight LED 2 — leave this pin open if unused
7	BL3	Current sink output for main backlight LED 3 — leave this pin open if unused
8	BL4	Current sink output for main backlight LED 4 — leave this pin open if unused
9	BL5	Current sink output for main backlight LED 5 — leave this pin open if unused
10	BL6	Current sink output for main backlight LED 6 — leave this pin open if unused
11	BL7	Current sink output for main backlight LED 7 — leave this pin open if unused
12	BANK 1	Logic input that, along with BANK 2, controls the configuration of the main and sub bank functions. See application information section for details.
13	BANK 2	Logic input that, along with BANK 1, controls the configuration of the main and sub bank functions. See application information section for details.
14	GND	Ground pin
15	C2-	Negative connection to bucket capacitor 2
16	C1-	Negative connection to bucket capacitor 1
17	C1+	Positive connection to bucket capacitor 1
18	C2+	Positive connection to bucket capacitor 2
19	OUT	Charge pump output — all LED anode pins are connected to this pin.
20	ENM	Enable pin for the main display LED bank — also used as the PWM dimming control input for this bank

Block Diagram



SEMTECH

Applications Information

General Description

This design is optimized for handheld applications supplied from a single Li-Ion cell and includes the following key features:

- A high efficiency fractional charge pump that supplies power to all LEDs
- Seven matched current sinks that control LED backlighting current, providing 500µA to 25mA per LED
- Two LED bank options with independent current settings and enable pins with PWM control of LED brightness.

High Current Fractional Charge Pump

The backlight outputs are supported by a high efficiency, high current fractional charge pump output at the OUT pin. The charge pump multiplies the input voltage by 1, 1.5, or 2 times. The charge pump switches at a fixed frequency of 250kHz in 1.5x and 2x modes and is disabled in 1x mode to save power and improve efficiency.

The mode selection circuit automatically selects the 1x, 1.5x, or 2x mode based on circuit conditions such as LED voltage, input voltage, and load current. The 1x mode is the most efficient mode, followed by 1.5x and 2x modes. Circuit conditions such as low input voltage, high output current, or high LED voltage place a higher demand on the charge pump output. A higher numerical mode (1.5x or 2x) may be needed momentarily to maintain regulation at the OUT pin during intervals of high demand. The charge pump responds to momentary high demands, setting the charge pump to the optimum mode to deliver the output voltage and load current while optimizing efficiency. Hysteresis is provided to prevent mode toggling.

The charge pump requires two bucket capacitors for proper operation. One capacitor must be connected between the C1+ and C1- pins and the other must be connected between the C2+ and C2- pins as shown in the Typical Application Circuit diagram. These capacitors should be equal in value, with a minimum capacitance of 1µF to support the charge pump current requirements. The device also requires at least 1µF capacitance on the IN pin and at least 1µF capacitance on the OUT pin to minimize noise and support the output drive requirements of I_{OUT} up to 90mA. For output currents higher than 90mA, a nominal value of 2.2µF is recommended for C_{OUT} and C_{IN}.

Capacitors with X7R or X5R ceramic dielectric are strongly recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application.

Capacitor Recommendations

The full rated output of 175mA is achieved using 2.2µF 0603 size capacitors for input, output, and bucket capacitors.

For applications which do not require the full 175mA output capability of the SC656 , a lower cost and smaller size capacitor option may be used. The 1µF capacitor in Table 1 may be used with no loss in accuracy, for up to 90mA of output current.

Table 1 — Capacitor Recommendations

Capacitance Value of $C_{IN} = C_{OUT} = C_1 = C_2$	Size Code EIA (JIS)	Application I_{OUT} Limit
2.2µF	0603 (1608)	up to I_{OUT} = 175mA(1)
1.0µF	0402 (1005)	up to I_{OUT} = 90mA(2)(3)

Notes:

(1) Note that 2.2µF in the 0402 size is not equivalent to 2.2µF in the 0603 size, so 0402 may not be substituted for this application.

(2) Larger size capacitors may be substituted.

(3) Exceeding 90mA, or using less than 1.0µF, may cause excessive peak-to-peak output ripple, (>120mV), and some loss of accuracy in 1.5x mode.

Bank Control Options

The backlight drivers can be configured as a single bank or as two independently controlled banks. The configuration of the banks is determined by the BANK2 and BANK1 pins as described in Table 2. The ENM and ISETM pins control the brightness of LEDs assigned to the main bank, and the ENS and ISETS pins allow the sub bank current to be set independently as described in the following section. Note that when both BANK2 and BANK1 are set to 0, the sub bank feature is disabled. In this case, both ENS and ISETS should be tied to GND.

Applications Information (continued)

Table 2 — Backlight Bank Configuration Settings

Bank 2	Bank 1	Main Bank	Sub Bank
0	0	BL1 — BL7	none
0	1	BL2 — BL7	BL1
1	0	BL3 — BL7	BL1 — BL2
1	1	BL4 — BL7	BL1 — BL3

LED Backlight Current Sinks

The full scale backlight current (I_{FS_BL}) is set via the current through the ISET pin controlling the corresponding LED bank (ISETM or ISETS) . The I_{FS_BL} is regulated to the value of the ISETM or ISETS pin current multiplied by an internal gain of 100A/A. R_{ISETM} and R_{ISETS} are used to control the current into the ISETM and ISETS pins. The relationship between each resistance R_{ISETx} and the full scale backlight current is:

$$R_{ISETx} = 100/I_{FS\_BL}$$

All backlight current sinks have matched currents, even when there is a variation in the forward voltages (ΔV_F) of the LEDs. A ΔV_F of 1.0V is supported when the input voltage is at 2.9V. Higher ΔV_F LED mis-match is supported when V_{IN} is higher than 2.9V. All current sink outputs are compared and the lowest output is used for setting the voltage regulation at the OUT pin. This is done to ensure that sufficient bias exists for all LEDs.

Any unused LED driver outputs must be left open for normal operation.

PWM Operation

A PWM signal on the ENM or ENS pin can be used to adjust the DC current through the LEDs. When the duty cycle is 100%, the backlight current through each LED (I_{BL}) equals the full scale current set by the corresponding ISET pin. As the duty cycle decreases, the ENM or ENS input samples the control signal and converts the duty cycle to a DC current level. In conventional PWM controlled systems, the output current pulses on and off with the PWM input to achieve an average output current. Providing a DC current through the LEDs instead of a pulsed current provides an efficiency advantage over other PWM controlled systems by allowing the charge pump to remain in 1x mode longer since the maximum current is equal to the average current.

PWM Sampling

The sampling system that translates the PWM signal to a DC current requires the ENM and ENS pins to have a minimum high time t_{HIGH_MIN} to set the DC level. High time less than t_{HIGH_MIN} impacts the accuracy of the target I_{BL}. The minimum duty cycle needed to support the minimum high time specification varies with the applied PWM frequency (see figure 1). Note that use of a lower PWM frequency, from 200Hz to 10kHz, will support lower minimum duty cycle and an extended backlight dimming range.

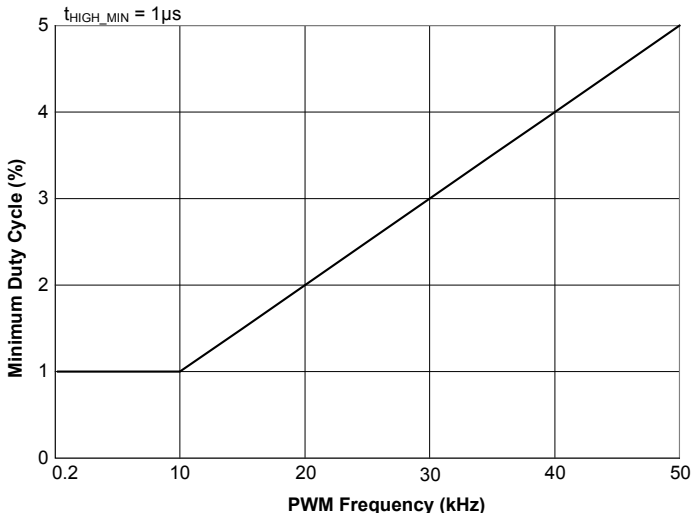


Figure 1 — Minimum Duty Cycle

Shutdown Mode

Shutdown occurs after ENM and ENS are both held low for an interval of 15ms or more. When the ENM and ENS pins are both held low for 5ms or less, the device will not shutdown.

Protection Features

The SC656 provides several protection features to safe-guard the device from catastrophic failures. These features include:

- Output Open Circuit Protection
- Over-Temperature Protection
- Charge Pump Output Current Limit
- LED Float Detection

Applications Information (continued)

Output Open Circuit Protection

Over-Voltage Protection (OVP) at the OUT pin prevents the charge pump from producing an excessively high output voltage. In the event of an open circuit between the OUT pin and all current sinks (no loads connected), the charge pump runs in open loop and the voltage rises up to the OVP limit. OVP operation is hysteretic, meaning the charge pump will momentarily turn off until V_{OUT} is sufficiently reduced. The maximum OVP threshold is 6.0V, allowing the use of a ceramic output capacitor rated at 6.3V.

Over-Temperature Protection

The Over-Temperature (OT) protection circuit prevents the device from overheating and experiencing a catastrophic failure. When the junction temperature exceeds 165°C, the device goes into thermal shutdown with all outputs disabled until the junction temperature is reduced. All register information is retained during thermal shutdown. Hysteresis of 20°C is provided to ensure that the device cools sufficiently before re-enabling.

Charge Pump Output Current Limit

The device limits the charge pump current at the OUT pin. If the OUT pin is shorted to ground, or V_{OUT} is lower than 2.5V, the typical output current limit is 70mA. The output current is limited to 225mA when over loaded resistively with V_{OUT} greater than 2.5.

LED Float Detection

Float detect is a fault detection feature of the LED backlight outputs. If an output is programmed to be enabled and an open circuit fault occurs at any backlight output, that output will be disabled to prevent a sustained output OVP condition from occurring due to the resulting open loop. Float detect ensures device protection but does not ensure optimum performance.

PCB Layout Considerations

The layout diagram in Figure 2 illustrates a proper two layer PCB layout for the SC656 and supporting components. Following fundamental layout rules is critical for achieving the performance specified in the Electrical Characteristics table. The following guidelines are recommended when developing a PCB layout:

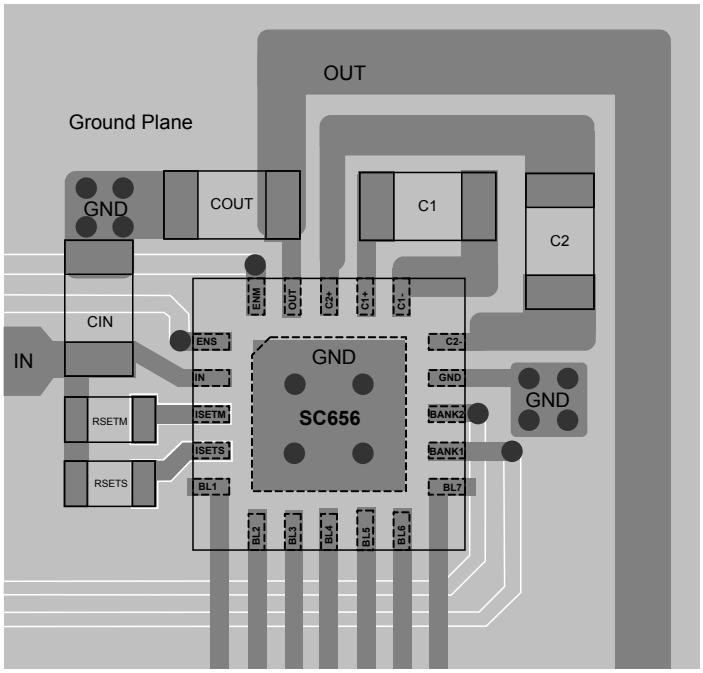


Figure 2 — Recommended Layout

Applications Information (continued)

- Place all bucket and decoupling capacitors — C1, C2, C_{IN}, and C_{OUT} — as close to the device as possible.
- All charge pump current passes through pins IN, OUT, C1+, C2+, C1-, and C2-. Therefore, ensure that all connections to these pins make use of wide traces so that the voltage drop on each connection is minimized.
- The GND pin should be connected to a ground plane using multiple vias to ensure proper thermal connection for optimal heat transfer.
- Make solid ground connections between the grounds of the C_{OUT}, C_{IN}, and the GND pin on the device.
- Resistors R_{SETM} and R_{SETS} should be connected as shown in Figure 2, close to pins IN and ISET. The placement and routing shown minimizes parasitic capacitance at the ISET pin.
- Figure 3 shows the pads on layer 1 that should be connected with vias to layer 2. C_{IN}, C_{OUT} and the GND pin all use vias to connect to the ground plane.
- Figure 4 shows layer 2, which functions as the ground plane. Layer 2 is also used for routing signals to pins ENM, ENS, BANK1, and BANK2. A void in the copper beneath the ISETM and ISETS pins serves to reduce capacitance coupled from these pins to ground.
- Avoid coupling noise to the ENM and ENS pins. This will help prevent unintended clocking of the PWM. The layout should be routed to achieve the least possible trace to trace capacitance between ENM and ENS. Also, minimize trace capacitance between ENM or ENS and any high speed signals.

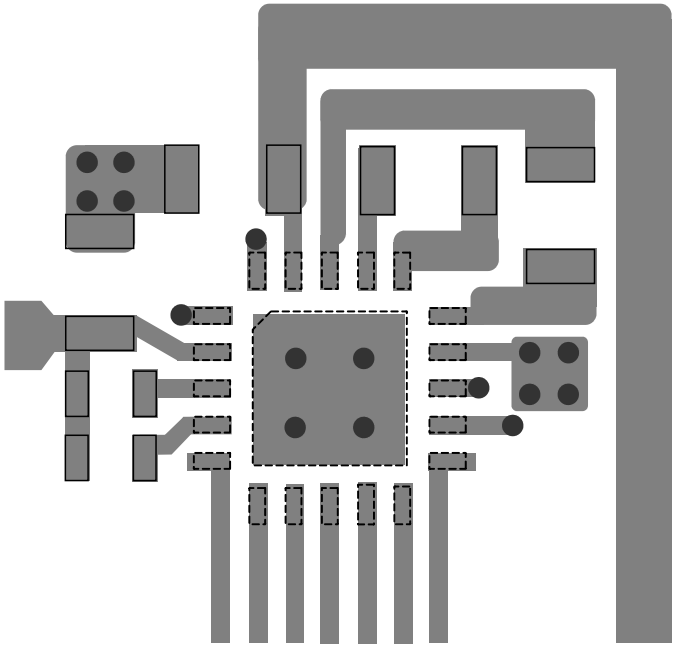


Figure 3 — Layer 1

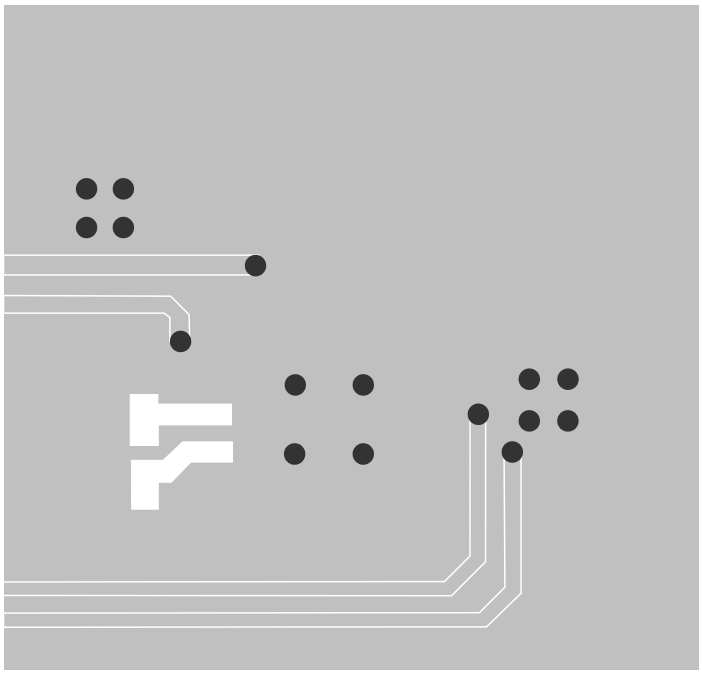
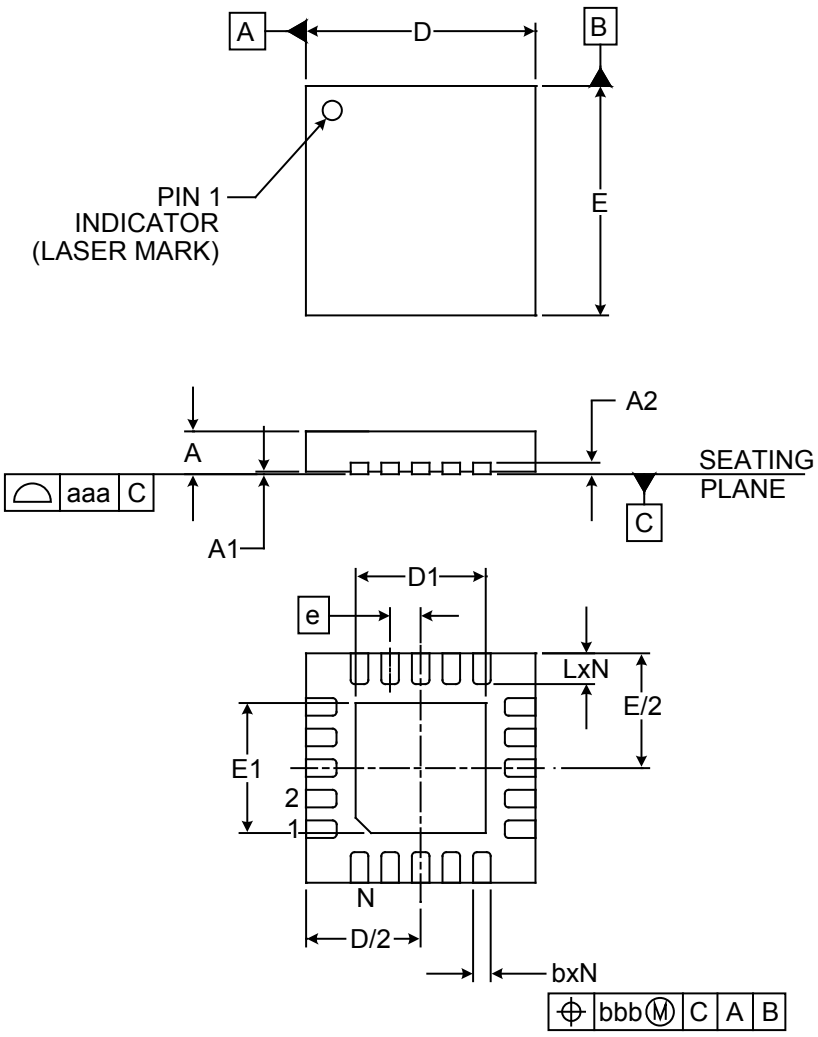


Figure 4 — Layer 2

Outline Drawing — MLPQ-UT-20 3x3

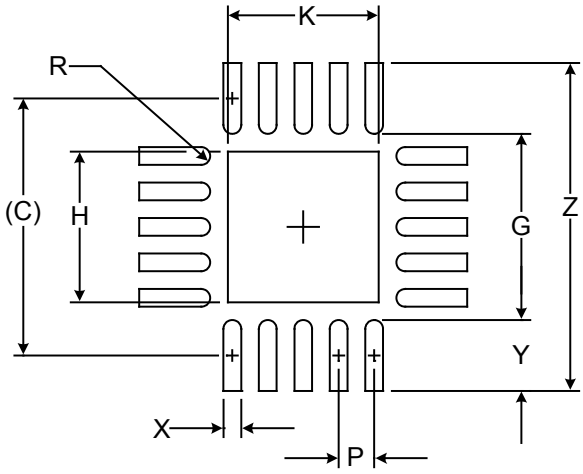


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(0.152)	
b	.006	.008	.010	0.15	0.20	0.25
D	.114	.118	.122	2.90	3.00	3.10
D1	.061	.067	.071	1.55	1.70	1.80
E	.114	.118	.122	2.90	3.00	3.10
E1	.061	.067	.071	1.55	1.70	1.80
e		.016 BSC			0.40 BSC	
L	.012	.016	.020	0.30	0.40	0.50
N		20			20	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP IS 1.90 x 1.90mm.

Land Pattern — MLPQ-UT-20 3x3



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.114)	(2.90)
G	.083	2.10
H	.067	1.70
K	.067	1.70
P	.016	0.40
R	.004	0.10
X	.008	0.20
Y	.031	0.80
Z	.146	3.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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