MAAD-008866

75 Ω Digital Attenuator, 6-Bit, Serial / Parallel Control
31.5 dB, 0.005 - 1.0 GHz

Rev.V2

Features

- 75 Ω Impedance
- Integrated TTL/CMOS Compatible Driver
- Parallel & Serial (P/S) Control with power-up state selection
- 0.5-dB Attenuation Steps to 31.5 dB
- Low DC Power Consumption
- Lead-Free 4mm PQFN-24LD Plastic Package
- Halogen-Free "Green" Mold Compound
- RoHS* Compliant and 260°C Re-flow Compatible

Description

The MAAD-008866 is a 6-bit, 0.5-dB step GaAs digital attenuator in a lead-free 4mm PQFN-24LD surface mount plastic package.

This device is ideally suited for use where high accuracy, very low power consumption and low intermodulation products are required. This part can be used in all 75 Ω systems operating up to 1 GHz.

Ordering Information[1,2]

Part Number	Package
MAAD-008866-TR3000	3000 piece reel
MAAD-008866-001SMB	Sample Board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 5 loose parts.

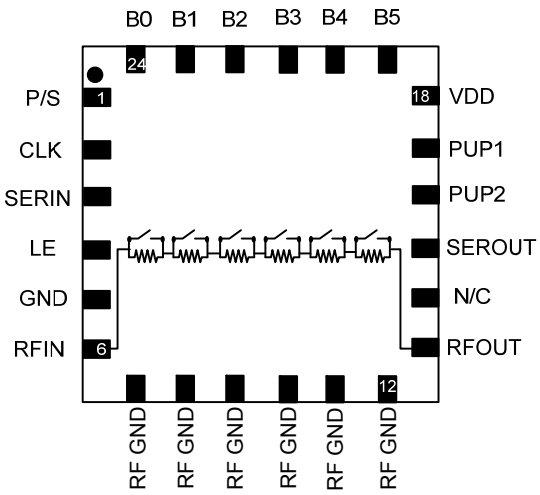
Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices. An external protection circuit using an inexpensive anti-parallel diode pair can be used to protect the IC.
Please reference application note AN3028 on http://www.macomtech.com for further detail.

Functional Schematic[3]



3. Blocking capacitors are required on all RF ports

Pin Configuration

Pin No.	Function	Pin No.	Function
1	Parallel / Serial Select	13	RF Output
2	Clock	14	No Connection
3	Serial Data In	15	Serial Data Out
4	Latch Enable	16	Power Up State 2
5	Ground	17	Power Up State 1
6	RF Input	18	Bias Voltage
7	RF Ground	19	B5
8	RF Ground	20	B4
9	RF Ground	21	B3
10	RF Ground	22	B2
11	RF Ground	23	B1
12	RF Ground	24	B0
25	Paddle[4]		

4. The exposed pad centered on the package bottom must be connected to the RF and DC ground.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

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75 Ω Digital Attenuator, 6-Bit, Serial / Parallel Control
31.5 dB, 0.005 - 1.0 GHz

Electrical Specifications[5,6]: T_A = 25°C, Z_0 = 75 Ω, V_{DD} = 5 V, V_C = 5 V

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Reference Insertion Loss	5 MHz 50 MHz 500 MHz 1000 MHz	dB	— — — —	1.3 1.35 1.6 1.8	— — — 2.3
Attenuation Accuracy	Any Bit or combination 5 - 1000 MHz	± (0.15 dB + 4% of attenuation setting in dB)			
Return Loss	5 - 1000 MHz	dB	—	18	—
Trise, Tfall	10% to 90% RF, 90% to 10% RF	ns	—	320	—
Ton, Toff	50% Control to 90 / 10% RF	ns	—	340	—
Transients	In Band	mV	—	88	—
Input P1dB	50 MHz 1000 MHz	dBm	—	12 25.6	—
IIP3	0 dBm/tone at Input, 6 MHz Spacing 50 MHz 1000 MHz	dBm	—	33 43	—
IIP2	0 dBm/tone at Input, 6 MHz Spacing 50 MHz 1000 MHz	dBm	—	51 74	—
Composite Triple Beat, CTB	132 channels, +30 dBmV/channel at the input	dBc	—	-88	—
Composite Second Order, CSO	132 channels, +30 dBmV/channel at the input	dBc	—	-69	—
Steady State I_{DD}	V_{DD} = +5 V	µA	—	4	—

5. External DC blocking capacitors are required on all RF ports. Loss varies at 0.003 dB/°C.
6. Low frequency is determined by DC block and RF GND capacitor value.

Absolute Maximum Ratings[7,8]

Parameter	Absolute Maximum
Input Power 50 MHz 1000 MHz	 +15 dBm +27 dBm
Operating Voltage	+8.5 V
Control Voltage	-0.5 V ≤ V_C ≤ 5.5 V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

7. Exceeding any one or combination of these limits may cause permanent damage to this device.
8. M/A-COM Technology Solutions does not recommend sustained operation near these survivability limits.

Truth Table[9]

B5	B4	B3	B2	B1	B0	Attenuation (dB)
1	1	1	1	1	1	Reference IL
1	1	1	1	1	0	0.5
1	1	1	1	0	1	1
1	1	1	0	1	1	2
1	1	0	1	1	1	4
1	0	1	1	1	1	8
0	1	1	1	1	1	16
0	0	0	0	0	0	31.5

9. Logic “0” = 0 to +0.8 V, Logic “1” = +2 to +5 V.

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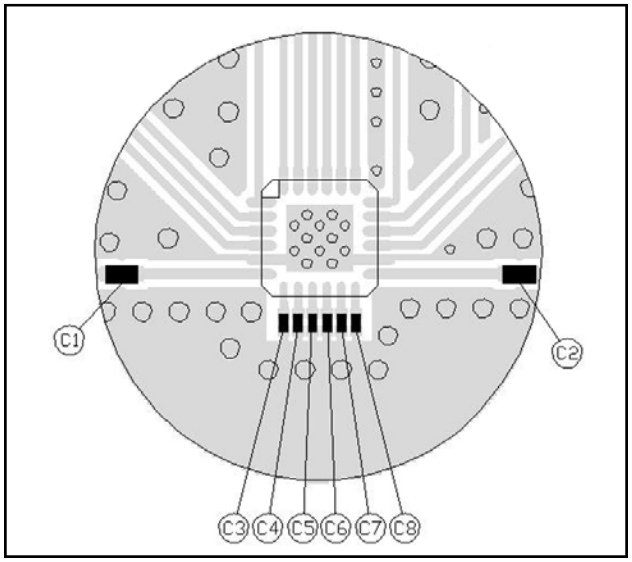
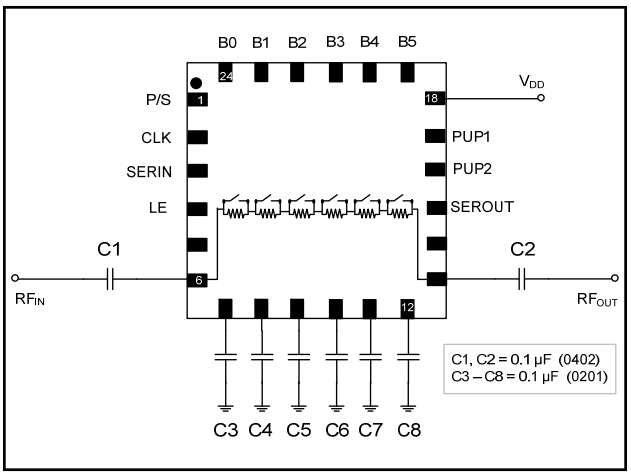
Recommended PCB



Application[10]

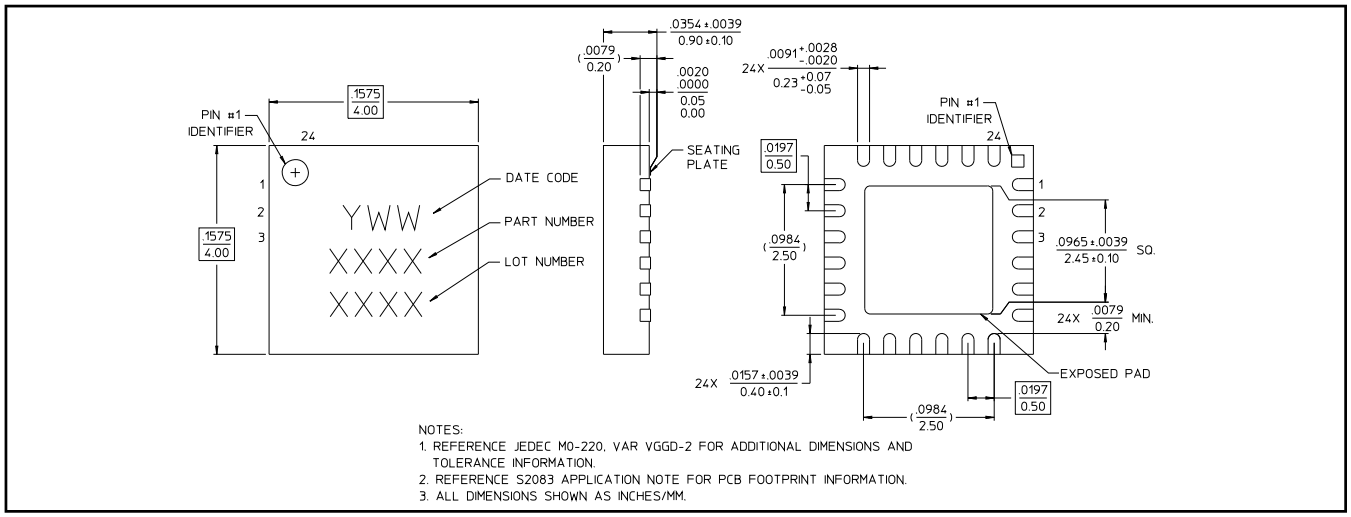


10. Capacitors C3 - C8 should be as close to package pins as possible.

Off-Chip Component Values

Component	Value	Package
C1 & C2	0.1 µF	0402
C3 - C8	0.1 µF	0201

Lead Free 4 mm 24-Lead PQFN †



† Reference Application Note M538 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is 100% matte tin over copper.

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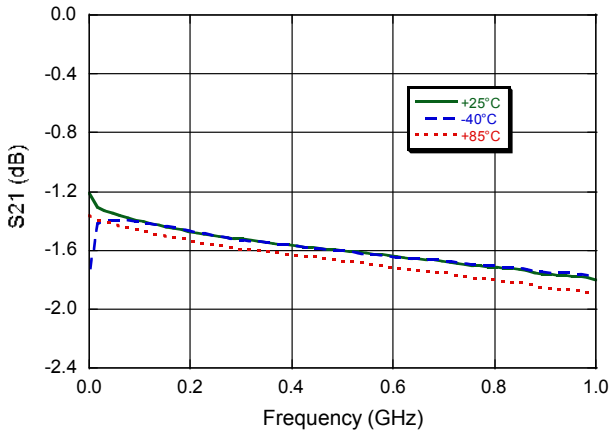
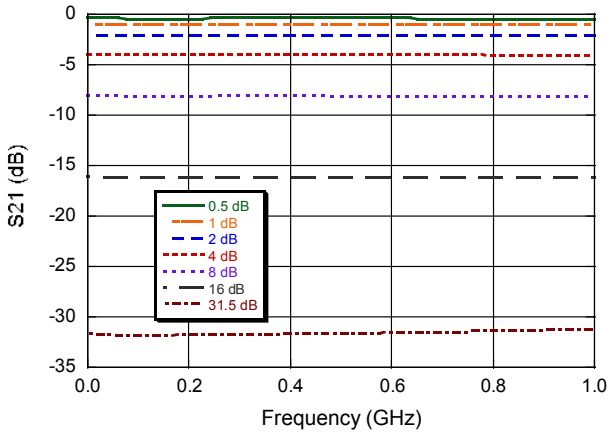
Typical Performance Curves

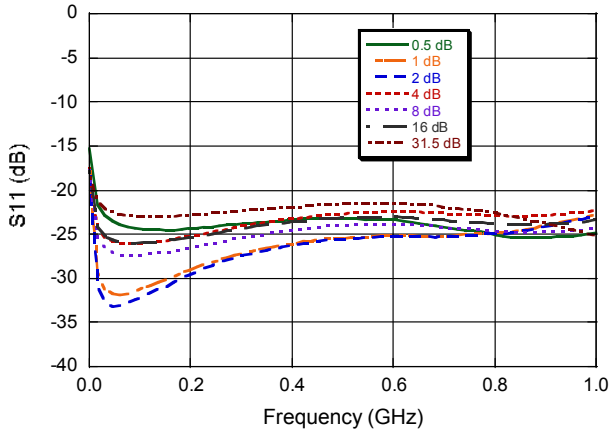
Insertion Loss



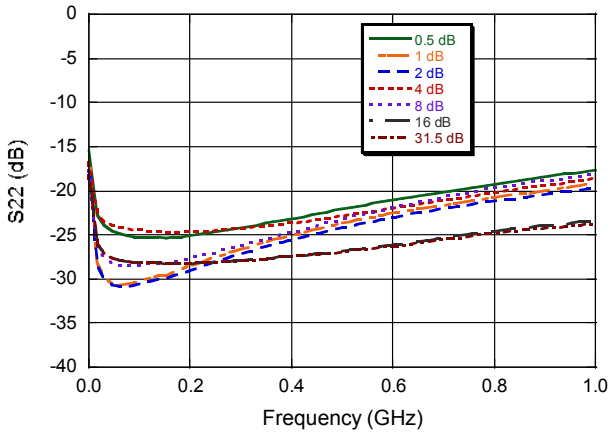
Relative Attenuation across all major states



Input Return Loss, across all attenuation states



Output Return Loss, across all attenuation states



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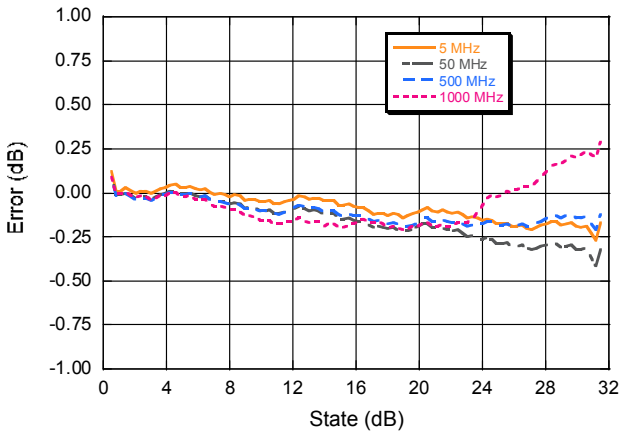
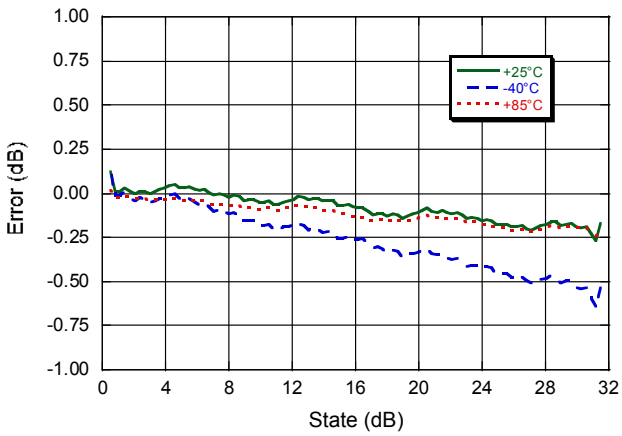
Typical Performance Curves @ 5 Volts

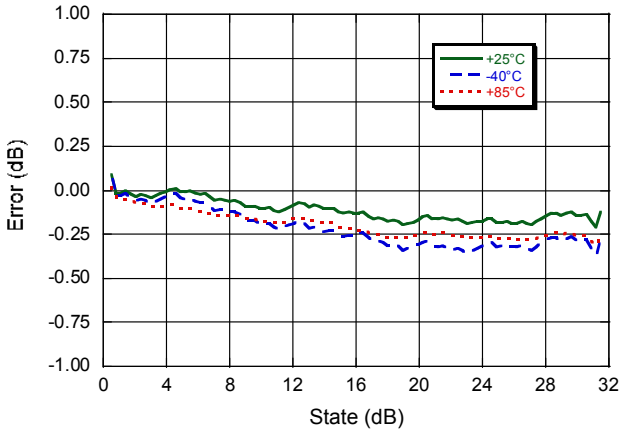
Step Error vs. State over Frequency



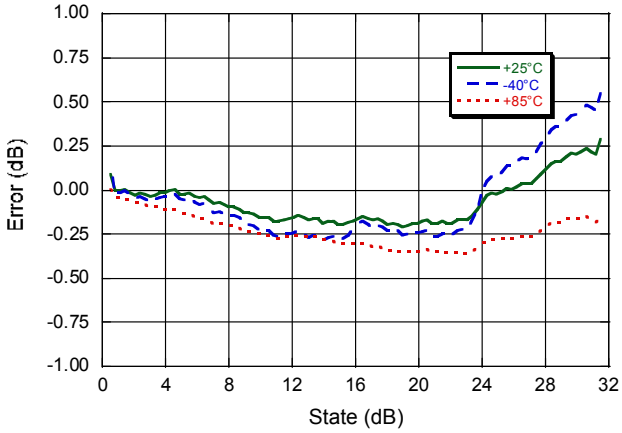
Step Error vs. State over Temp @ 5 MHz



Step Error vs. State over Temp @ 500 MHz



Step Error vs. State over Temp @ 1000 MHz



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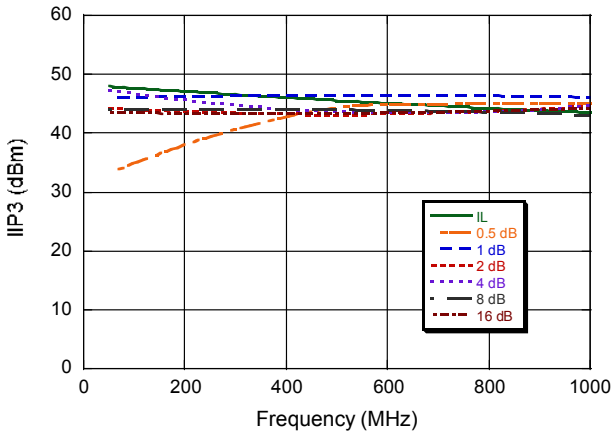
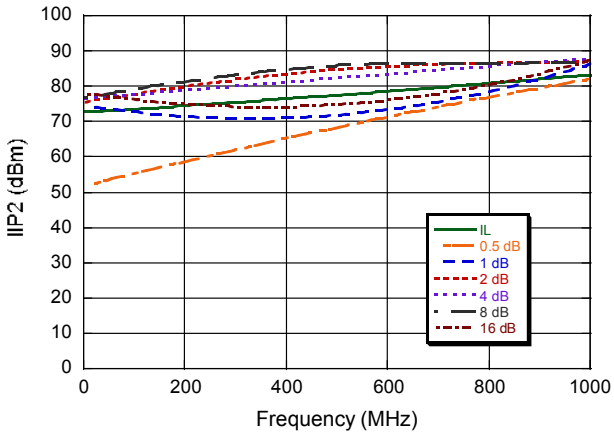
Typical Performance Curves @ 5 Volts

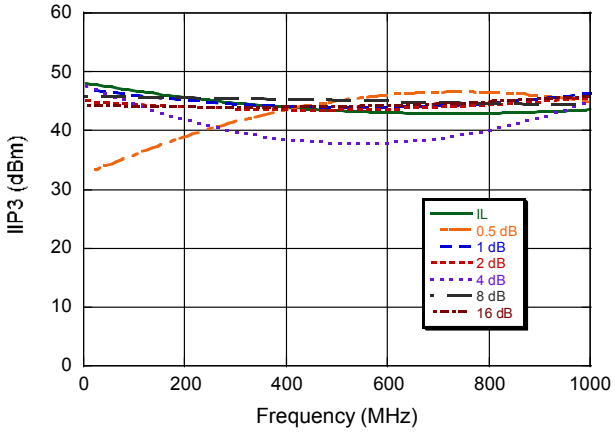
IIP3 vs. Frequency @ 25°C



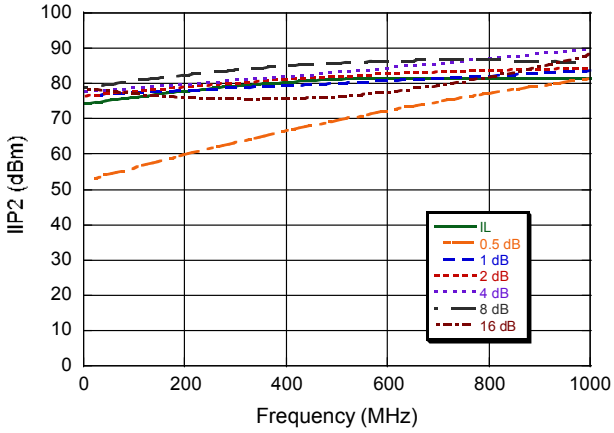
IIP2 vs. Frequency @ 25°C



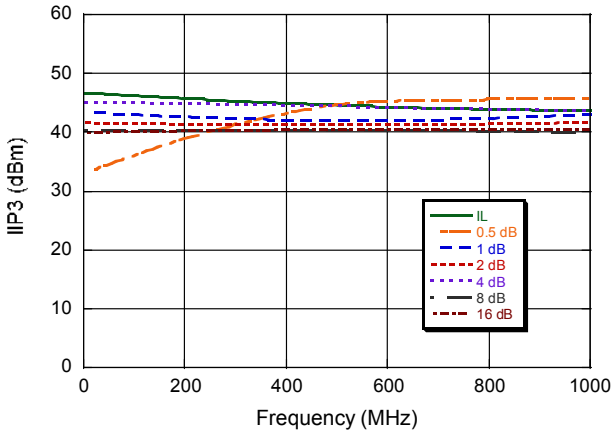
IIP3 vs. Frequency @ -40°C



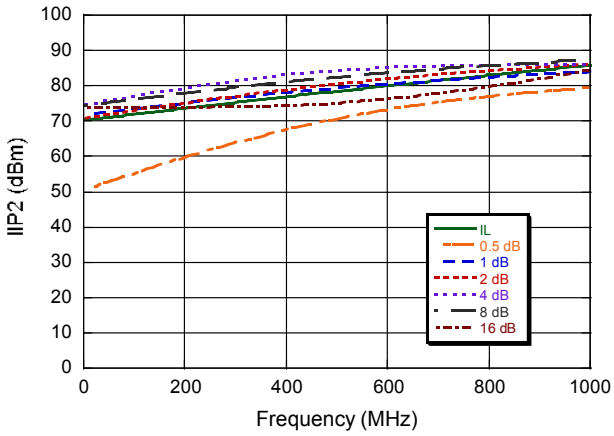
IIP2 vs. Frequency @ -40°C



IIP3 vs. Frequency @ +85°C



IIP2 vs. Frequency @ +85°C



Functionality
Modes of Operation: Serial, Direct Parallel, and Latched Parallel

Mode Truth Table

P/S	LE	Mode
1	X	Serial
0	Constant High	Direct Parallel
0	Pulsed	Latched Parallel

Serial Mode

The serial control interface (SERIN, CLK, LE, SEROUT) is compatible with the SPI protocol. SPI mode is activated when P/S is kept high. The 6-bit serial word must be loaded with MSB first. After shifting in the 6 bit word, bringing LE high will set the attenuator to the desired state. While LE is high the CLK is masked to protect the data while implementing the change . SEROUT is the SERIN delayed by 6 clock cycles.

When P/S is low, the serial control interface is disabled and the serial input register is loaded asynchronously with parallel digital inputs.

Direct Parallel Mode

The parallel mode is enabled when P/S is set to low. In the direct parallel mode, the attenuator is controlled by the parallel control inputs directly. The LE must be at logic high to control the attenuator in this mode.

Latched Parallel Mode

In the latched parallel mode, the parallel control inputs will be buffered by registers, and loaded to the outputs when LE is high. The outputs shall not change states when LE is low.

Power-up States

The power-up (PUP) states will work in both serial and parallel modes, and initiate the attenuator according to the PUP truth table. During power up, the digital inputs shall be held constant for at least 1 µs after V_{DD} reaches 90% of final value. For serial mode, the PUP states will only work when LE is held low. The PUP state shall be locked out after the first LE pulse.

Functionality
Modes of Operation: Serial, Direct Parallel, and Latched Parallel

PUP Truth Table*

Inputs				Gain Relative to Max. Gain	Notes
PS	LE	PUP2	PUP1		
0	0	0	0	-31.5 dB	Parallel Mode
0	0	0	1	-24 dB	
0	0	1	0	-16 dB	
0	0	1	1	Insertion Loss	
0	1	X	X	0 to –31.5 dB (Set VC0.5 - VC16)	
1	0	X	X	0 to –31.5 dB (Set VC0.5 - VC16)	Serial Mode
1	1	X	X	No Definition	

*V_{DD} T_{RISE} must be <= 125 ns

Serial Interface Timing Characteristics

Symbol	Parameter	Typical Performance			Units
		-40°C	25°C	+85°C	
t_{SCK}	Min. Serial Clock Period	100	100	100	ns
t_{CS}	Min. Control Set-up Time	20	20	20	ns
t_{CH}	Min. Control Hold Time	20	20	20	ns
t_{LS}	Min. LE Set-up Time	10	10	10	ns
t_{LEW}	Min. LE Pulse Width	10	10	10	ns
t_{LH}	Min. Serial Clock Hold Time from LE	10	10	10	ns
t_{LES}	Min. LE Pulse Spacing	630	630	630	ns

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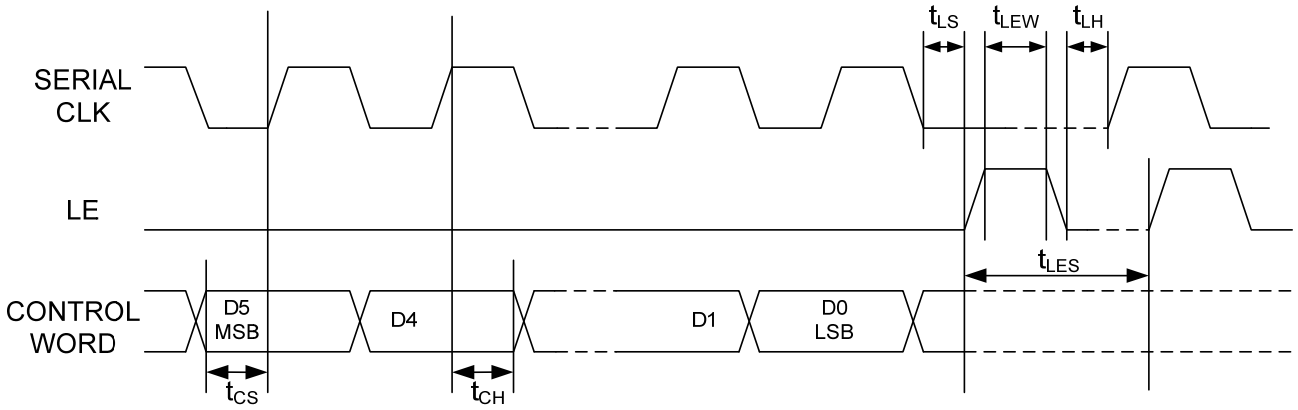
Functionality
Modes of Operation: Serial, Direct Parallel, and Latched Parallel

Serial Input Interface Timing Diagram



Parallel Control Word