

# ITS42k5D-LD-F

Dual Channel High-Side PMOS Power Switch with Integrated Freewheeling Diodes

## Data Sheet

Rev 1.0, 2015-04-28

Standard Power



## 1 Overview

### Features

- Two channel power PMOS high-side switch
- Integrated freewheeling diode
- Output current capability: up to 250mA per channel
- Wide operating voltage range: 4.5V to 42V
- Very low quiescent current in OFF state
- High current limit accuracy
- 3.3V and 5V compatible logic inputs
- Optimized EMC behavior
- Overload, short circuit, open load and overtemperature diagnosis
- ESD, short circuit, safe operation area and overtemperature protection
- Undervoltage lockout (UVLO)
- Green and robust product (RoHS compliant)



**PG-TSON-10**

### Description

The ITS42k5D-LD-F, which is available in a very small leadless PG-TSON-10 package, is a 2.5Ω dual channel high-side PMOS power switch with integrated freewheeling diodes including protection and diagnostic functions. The ITS42k5D-LD-F has two diagnostic status output pins, one for each channel.

The diagnosis can be read out from two separate open drain outputs in order to indicate overload, short circuit, open load and overtemperature conditions. The device controls the respective channel one or two by the two separate input pins i.e. IN1 and IN2. When both inputs are low the device is in OFF condition. Each channel of the device is able to drive loads up to 250mA.

### Application range

The ITS42k5D-LD-F is capable of switching resistive, capacitive and inductive loads (e.g. sensor units, LEDs, relays, valves) in harsh industrial environments. An integrated freewheeling diode enables driving of inductive loads. The ITS42k5D-LD-F is suitable for switching small loads such as sensors. For sensor supplies please refer to Infineon's industrial linear voltage regulator products.

The qualification of this product is based on JEDEC JESD47 and may reference existing qualification results of similar products. Such referencing is justified by the structural similarity of the products. The product is not qualified and manufactured according to the requirements of Infineon Technologies with regard to automotive and/or transportation applications.

Type	Package	Marking
ITS42k5D-LD-F	PG-TSON-10	I2k5DF

Infineon Technologies administrates a comprehensive quality management system according to the latest version of the ISO9001 and ISO/TS 16949.

The most updated certificates of the aforesaid ISO9001 and ISOTS 16949 are available on the Infineon Technologies web page <http://www.infineon.com/cms/en/product/technology/quality/>

## 2 Pin Configuration

### 2.1 Pin Assignment

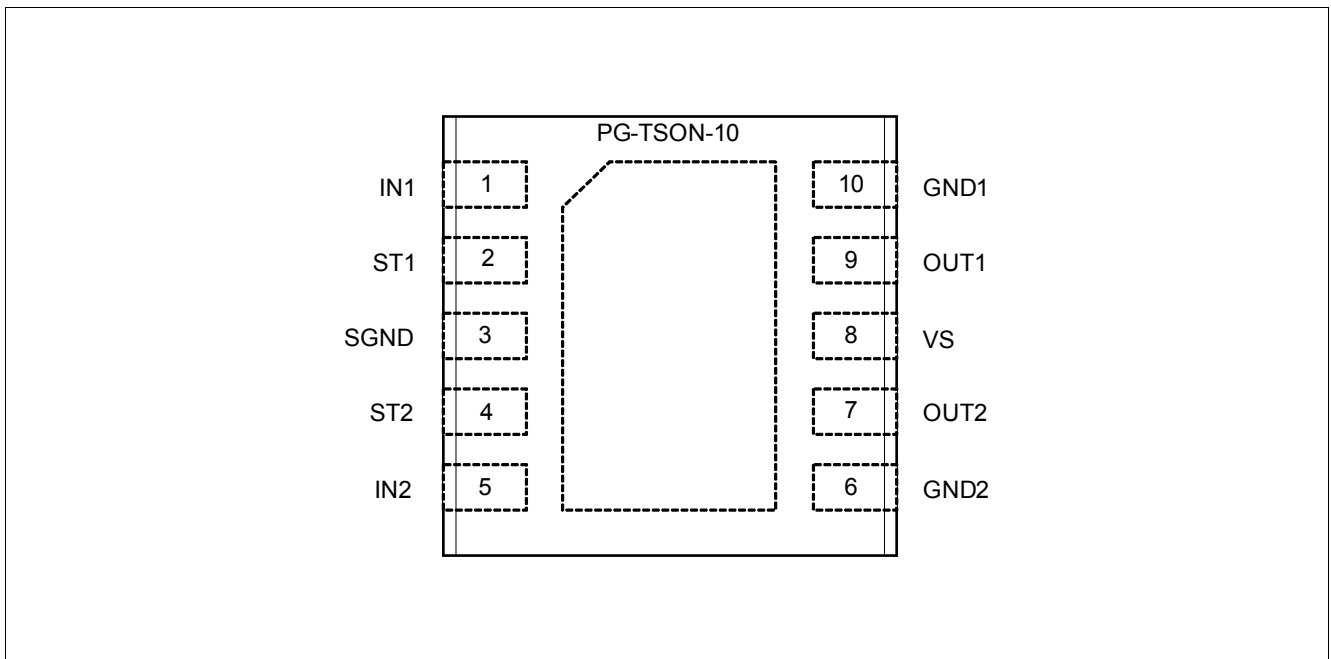


Figure 1 Pin configuration top view, PG-TSON-10

### 2.2 Pin Definitions and Functions

Table 1 Pin Definition

Pin	Symbol	Function
1	IN1	<b>INPUT 1</b> ; Control Input for Channel 1, Active High
2	ST1	<b>STATUS 1</b> ; Status Flag for Channel 1; Open Drain Output
3	SGND	<b>SIGNAL GND</b> ; connect to all GNDs and to exposed GND pad
4	ST2	<b>STATUS 2</b> ; Status Flag for Channel 2; Open Drain Output
5	IN2	<b>INPUT 2</b> ; Control Input for Channel 2; Active High
6	GND2	<b>Ground Channel 2</b> ; Connect to all GNDs and to exposed GND pad
7	OUT2	<b>OUTPUT 2</b> ; drain of the power-PMOS Channel 2; power freewheeling diode to GND
8	VS	<b>Supply Voltage</b> ; block to GND with a capacitor near the IC
9	OUT1	<b>OUTPUT 1</b> ; drain of the power-PMOS Channel 1; power freewheeling diode to GND
10	GND1	<b>Ground Channel 1</b> ; Connect to all GNDs and to exposed GND pad
Exposed pad	–	Connect externally to all GNDs i.e. GND1, GND2 and SGND

### 3 Block Diagram

#### 3.1 ITS42k5D-LD-F in the PG-TSON-10 package

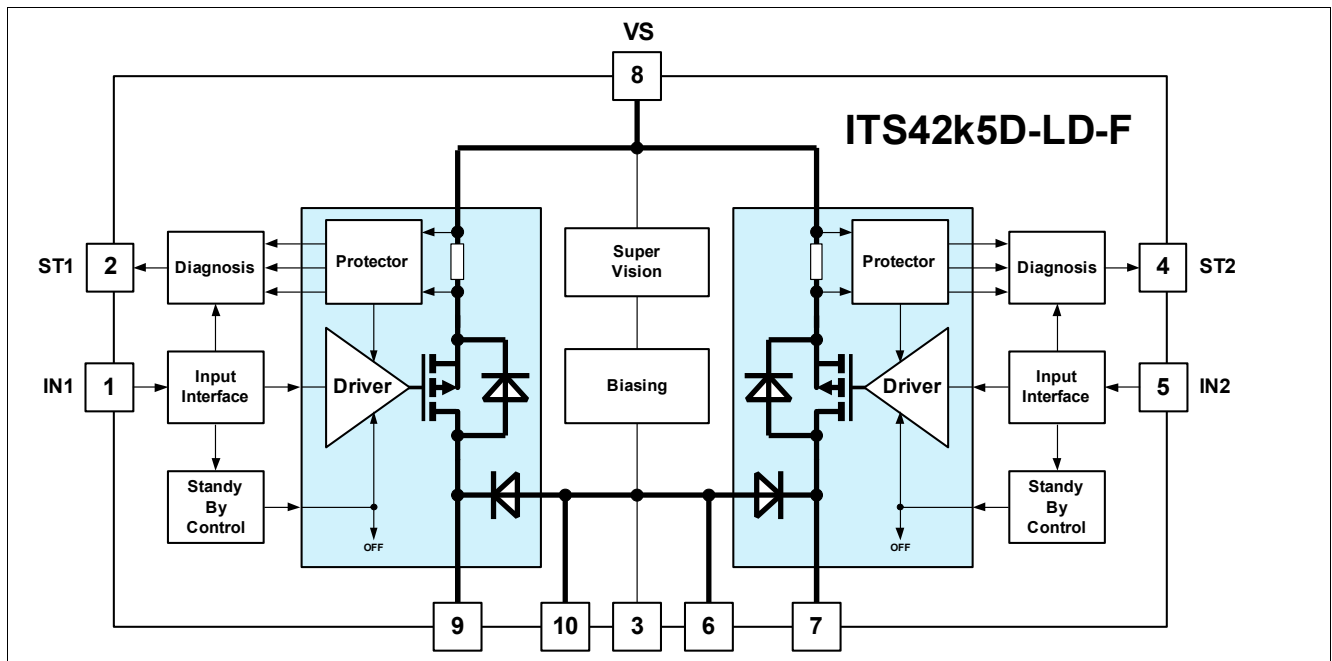


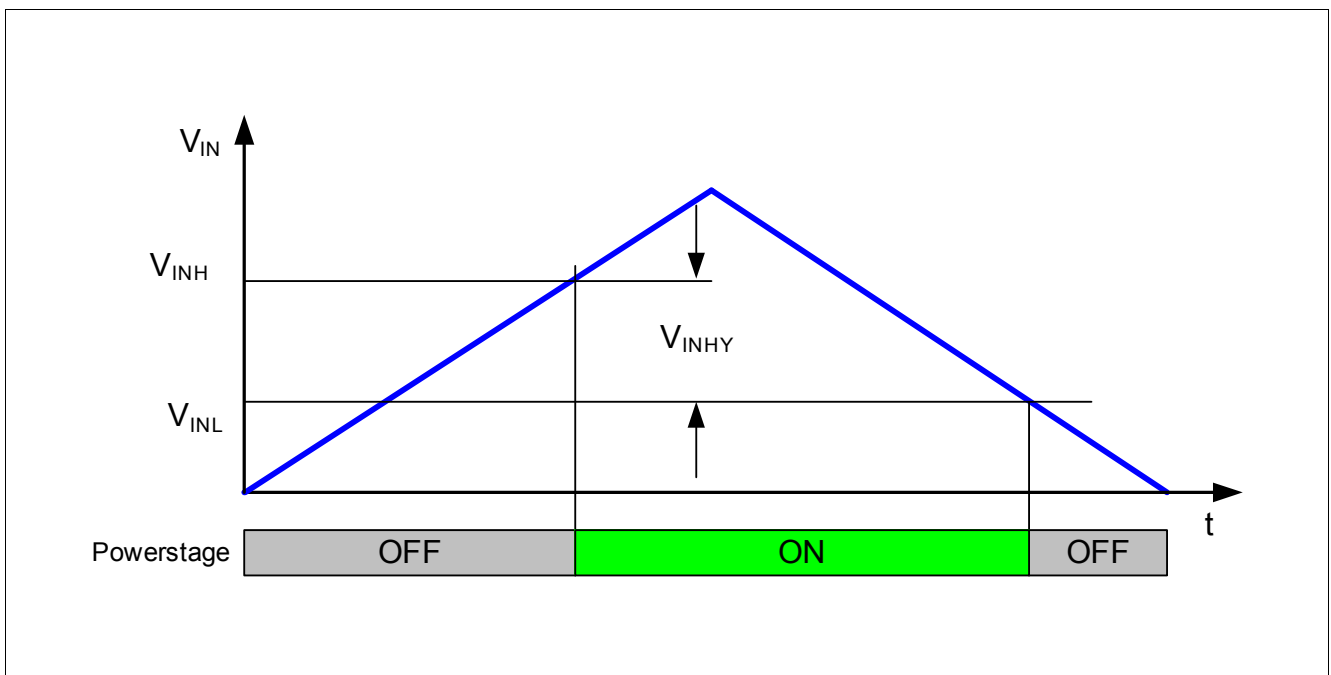
Figure 2 Block diagram ITS42k5D-LD-F

## 4 Functional Description

### 4.1 Input Circuit

The two inputs i.e. IN1 and IN2 control the outputs of channel 1 and channel 2 respectively.

When both inputs IN1 and IN2 are low the device is switched OFF. In OFF state, the current consumption of the device is very low. For more details on current consumption in ON and OFF states please refer to electrical characteristics. The logic input levels are compatible with 3.3V and 5V microcontrollers. To avoid switching noise all inputs have hysteresis. Logic level definitions are shown in [Figure 3](#)



**Figure 3** Function and Thresholds of the inputs IN1 and IN2

The input pins are optimized in terms of ESD protection, withstanding overvoltage scenarios like surge pulses. Overvoltage transient levels higher than the maximum ratings of 45V must be avoided.

*Note: Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" the normal operating range. Protection functions are neither designed for continuous nor repetitive operation.*

### 4.2 Powerstage

The two outputs are designed as high-side switches with integrated freewheeling diodes from OUT to GND. The high side switch is a power P-channel MOSFET. The integrated freewheeling diodes enable the device to switch inductive loads on each channel.

A built-in high accuracy current limiter ensures that the Power P-channel MOSFET is protected against overload when driving heavy capacitive loads.

[Figure 4](#) shows the output voltage  $V_{OUT1}$  and  $V_{OUT2}$  controlled by the input interfaces IN1, IN2

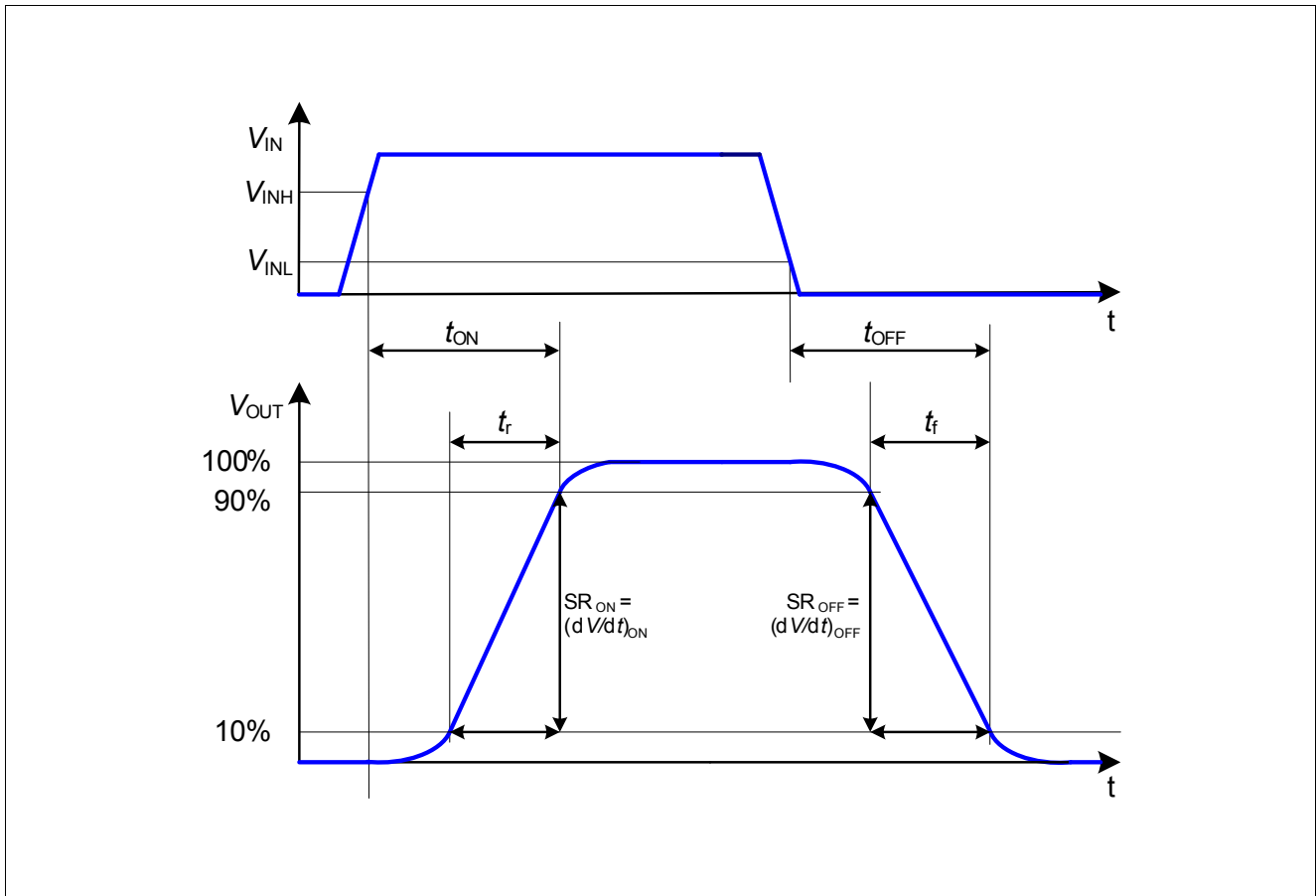


Figure 4 Input / output timings when switching a resistive load.

### 4.3 Protection Functions

*Note: Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” the normal operating range. Protection functions are neither designed for continuous nor repetitive operation.*

#### 4.3.1 Short Circuit Protection

Short circuit is a special case of overload. The device is protected within the supply voltage range from  $V_S = 4.5$  V to 42 V. If the device stays in short circuit condition for a longer time the integrated temperature protection will switch the device OFF (both channels OFF). For details please look at chapter “Overtemperature Protection”.

#### 4.3.2 Protection by Overtemperature Shutdown

This circuit monitors the junction temperature  $T_j$ . When the device is ON, the junction temperature  $T_j$  increases proportional to the power loss. The temperature protector is equipped with two temperature sensors, one for each one of the powerstages. When the thermal shutdown trip point  $T_{SDOFF}$  is reached, the in-built protector switches OFF the respective channel. This overtemperature shutdown is reported via diagnosis to the respective status flag i.e. either ST1 and ST2. The output remains OFF until the junction is cooled down to the thermal shutdown release point  $T_{SDON}$ . If the overload condition remains the device will toggle between both junction temperature values. It is not recommended for the device to stay in an overload condition as this will degrade its lifetime.

### 4.4 Diagnosis

For diagnostic purposes the device provides two digital output pins ST1 and ST2 in order to indicate fault conditions.

The status flag ST1 indicates the status of channel 1 and flag ST2 indicates the status of channel 2.

Each status output (ST1, ST2) of the ITS42k5D-LD-F is a high voltage open drain output.

In “normal” operation mode the NMOS open drain transistors are switched OFF. The following truth table (Table 2) defines the status output of the device under various conditions.

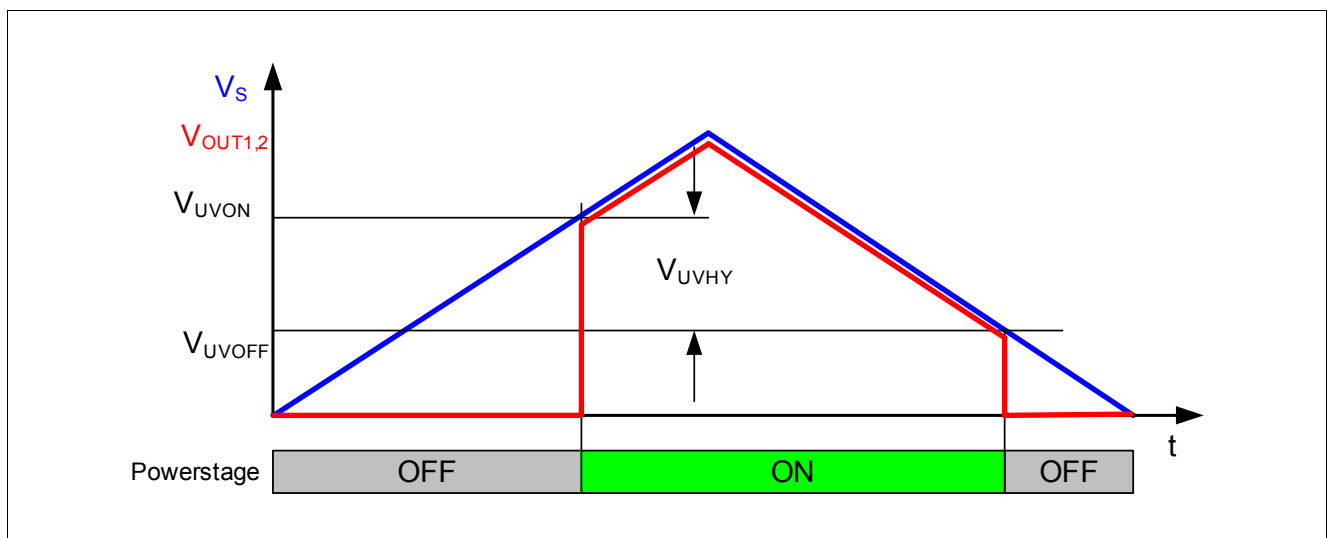
**Table 2 Truth table of diagnosis feature**

Device Operation	IN1	IN2	ST1	ST2	Comment
Normal Operation	H	H	H	H	–
Overload	H	H	L	L	Respective flag is low; latched
Short Circuit to GND	H	H	L	L	Respective flag is low; latched
Overtemperature	H	H	L	L	Respective flag is low; latched
Overtemperature	L	L	H	H	Device in OFF mode; no internal heat source
Open Load	H	H	L	L	Respective flag is low

### 4.5 Undervoltage Lockout

In order to avoid an application malfunction caused by an undervoltage condition at the load (e.g. a relay can not keep the contact closed properly) an undervoltage lockout (UVLO) supervises the supply voltage  $V_s$ .

The UVLO circuit switches the power stages off if the supply voltage is below the functional operating voltage range



**Figure 5 Under Voltage Lockout (UVLO) function and thresholds**



### 4.6 Protection Behavior

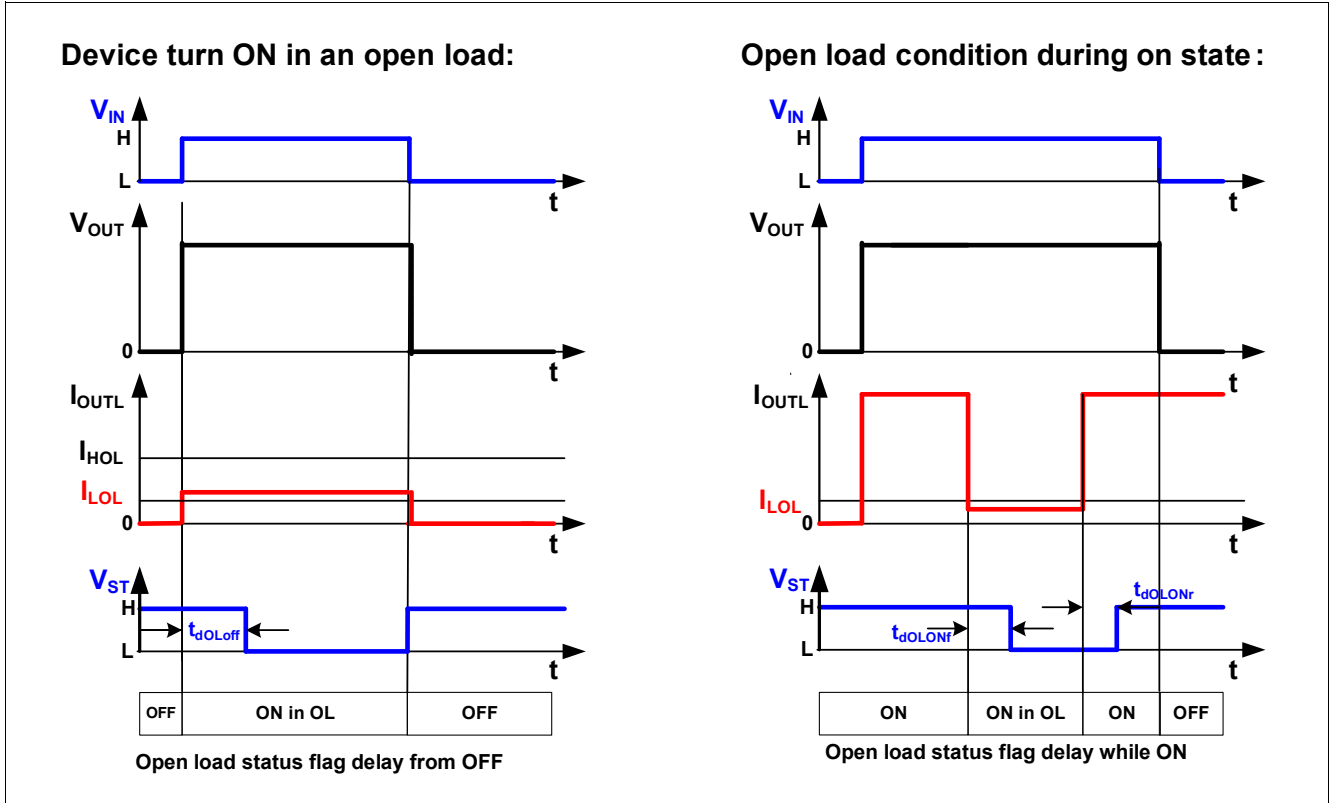


Figure 6 Protection mechanism of the ITS42k5D-LD-F

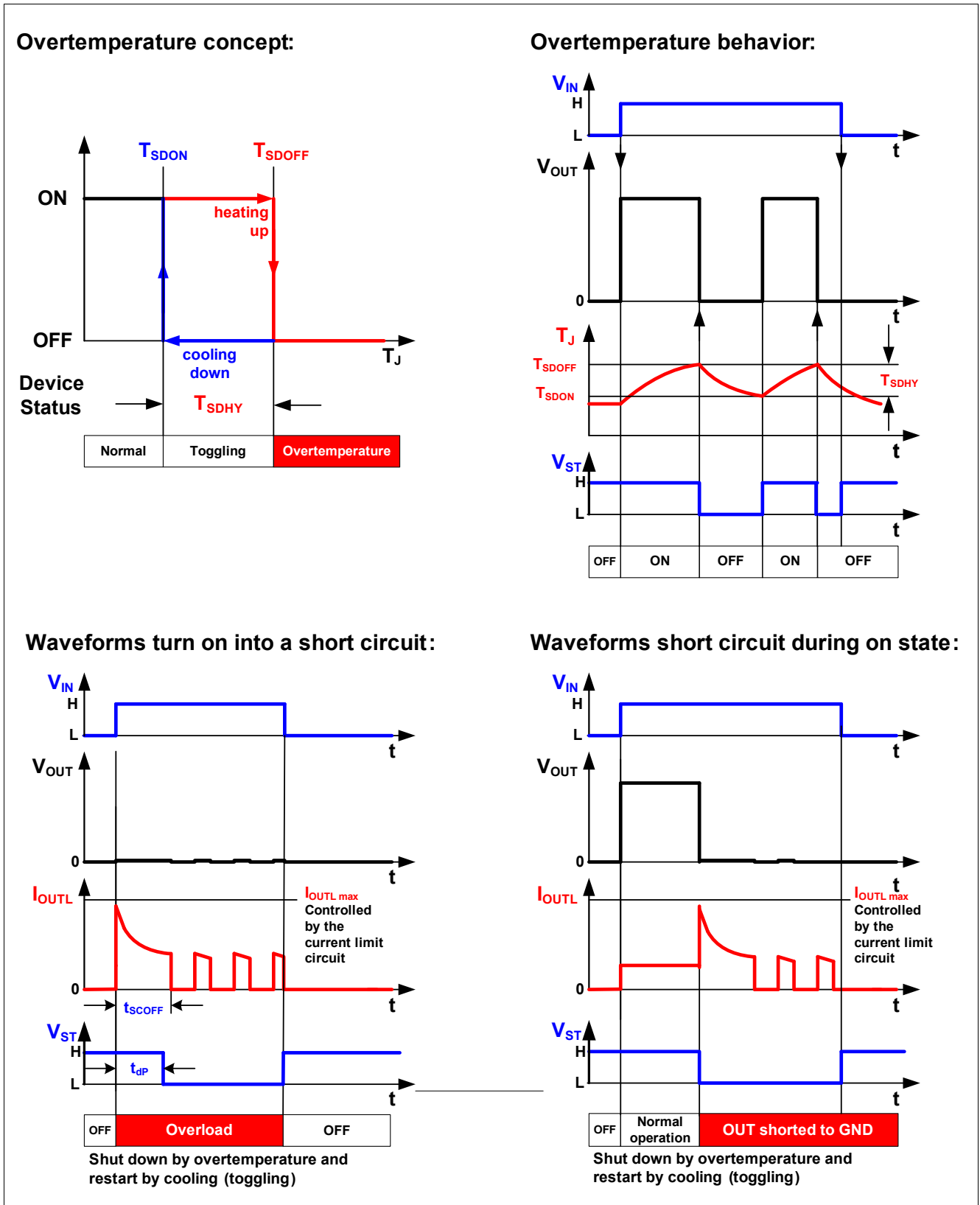


Figure 7 Protection behavior of the ITS42k5D-LD-F

## 4.7 Application Waveforms

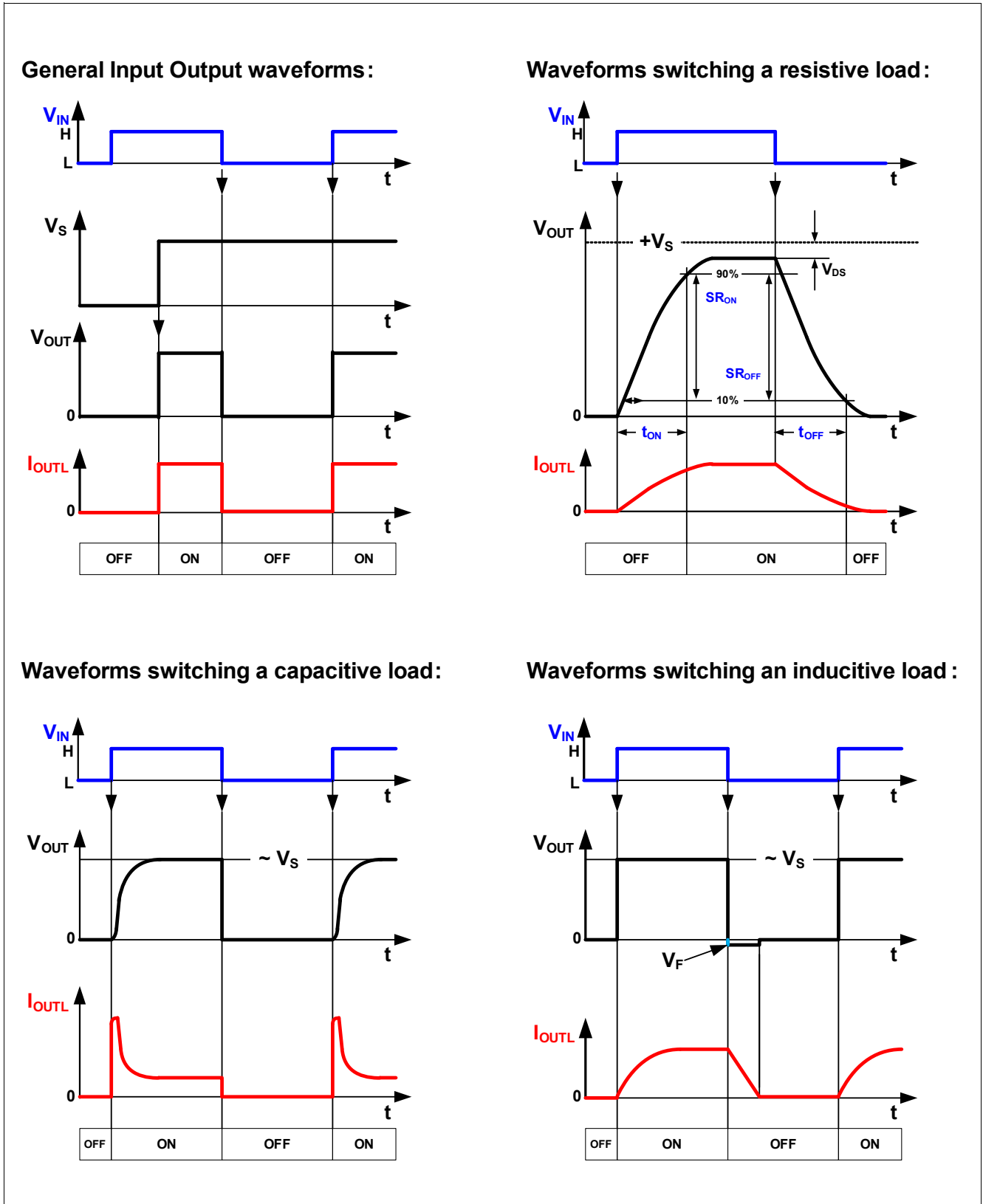


Figure 8 Protection behavior of the ITS42k5D-LD-F

## 5 General Product Characteristics

### 5.1 Absolute Maximum Ratings

**Table 3 Absolute maximum ratings<sup>1)</sup>  $T_j = -40^\circ\text{C}$  to  $+125^\circ$  unless otherwise specified; all voltages with respect to ground unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
<b>Supply voltage <math>V_S</math></b>							
Voltage	$V_S$	-0.3	–	45	V	–	5.1.1
Current	$I_S$	-10	–	–	mA	Internally limited	5.1.2
<b>Input IN1 and IN2</b>							
Input Voltage	$V_{IN1,2}$	-0.3	–	45	V	–	5.1.3
Current	$I_{IN1,2}$	–	–	–	mA	Internally limited	5.1.4
<b>Output ST</b>							
Voltage	$V_{ST1,2}$	-0.3	–	45	V	–	5.1.5
Current	$I_{ST1,2}$	–	–	5	mA	–	5.1.6
<b>Ground GND1, GND2, SGND</b>							
Current	$I_{GND1,2}$	–	–	600	mA	Internally limited	5.1.7
Current	$I_{SGND}$	–	–	10	mA	Internally limited	5.1.8
<b>Output stage OUT1, OUT2</b>							
Voltage	$V_{OUT1,2}$	–	–	$V_S + 0.3$	V	Internally limited	5.1.9
<b>Temperatures</b>							
Junction Temperature	$T_j$	-40	–	150	$^\circ\text{C}$	–	5.1.11
Storage Temperature	$T_{stg}$	-55	–	150	$^\circ\text{C}$	–	5.1.12
<b>Power Dissipation</b>							
Power dissipation	$P_{tot}$	–	0.66	–	W	PCB <sup>2)</sup> is vertical without blown air	5.1.13
<b>ESD Susceptibility</b>							
ESD susceptibility (all pins)	$V_{ESD}$	-2	–	2	kV	HBM <sup>3)</sup>	5.1.14
ESD susceptibility OUT pins vs. GND pin	$V_{ESD}$	-2	–	2	kV		5.1.15
ESD susceptibility (all pins)	$V_{ESD}$	-1	–	1	kV	CDM <sup>4)</sup>	5.1.15

1) Not subject to production test, specified by design

2) See Thermal Resistance Footnote <sup>2)</sup>

3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5k $\Omega$ , 100pF)

4) ESD susceptibility, Charged Device Model "CDM" JEDEC JESD22-C101

*Note: Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" the normal operating range. Protection functions are neither designed for continuous nor repetitive operation.*

## 5.2 Functional Range

**Table 4 Functional Range<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Nominal Operating Voltage	$V_S$	$V_{UVON}$	–	42	V	$V_S$ increasing	5.2.1
Nominal Operating Voltage	$V_S$	$V_{UVOFF}$	–	42	V	$V_S$ decreasing	5.2.2
Nominal Operating Voltage	$V_{IN1,2}$	-0.3	–	7	V	–	5.2.3
Nominal Operating Voltage	$V_{ST1,2}$	-0.3	–	7	V	–	5.2.4
Junction Temperature	$T_J$	-40	–	125	°C	–	5.2.5

1) Not subject to production test, specified by design

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 5.3 Thermal Resistance

This thermal data was generated in accordance with JEDEC JESD51 standards.

More information on [www.jedec.org](http://www.jedec.org)

**Table 5 Thermal Resistance<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
<b>PG-TSON-10</b>							
Junction to Case, exposed pad	$R_{thjc}$	–	12	–	K/W		5.3.1
Junction to ambient	$R_{thJA\_1s0p}$	–	140	–	K/W	<sup>2)</sup>	5.3.2
Junction to ambient	$R_{thJA\_1s0p\_300mm}$	–	70	–	K/W	<sup>3)</sup>	5.3.3
Junction to ambient	$R_{thJA\_1s0p\_600mm}$	–	60	–	K/W	<sup>4)</sup>	5.3.4
Junction to ambient	$R_{thJA\_2s2p}$	–	67	–	K/W	<sup>5)</sup>	5.3.5
Junction to ambient	$R_{thJA\_2s2pvia}$	–	55	–	K/W	<sup>6)</sup>	5.3.6

1) Not subject to production test, specified by design

2) Specified  $R_{thJA}$  value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, footprint; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.

3) Specified  $R_{thJA}$  value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, Cu, 300mm<sup>2</sup>; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.

4) Specified  $R_{thJA}$  value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, 600mm<sup>2</sup>; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.

5) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu).

6) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board with two thermal vias; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). The diameter of the two vias are equal 0.3mm and have a plating of 25µm with a copper heatsink area of 3mm x 2mm). JEDEC51-7: The two plated-through hole vias should have a solder land of no less than 1.25 mm diameter with a drill hole of no less than 0.85 mm diameter.

## 6 Electrical Characteristics

**Table 6**  $V_S = 4.5\text{ V to }42\text{ V}$  ;  $T_j = -40^\circ\text{C to }+125^\circ$ , all voltages with respect to ground, currents flowing into the device unless otherwise specified ; typical values are given at  $V_S = 13.5\text{ V}$ ,  $T_j = 25^\circ\text{C}$

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
<b>Input</b>							
ON Threshold	$V_{INH1,2}$	2	–	–	V	–	6.1.1
OFF Threshold	$V_{INL1,2}$	–	–	0.8	V	–	6.1.2
Input Hysteresis	$V_{INH1,2}$	0.1	0.4	–	V	$V_{INH1,2} = V_{INH} - V_{INL}$	6.1.3
Input Current - ON state	$I_{INON1,2}$	10	25	50	$\mu\text{A}$	$V_{IN} = 5\text{V}$	6.1.4
Input Pull Down Resistor; IN1,2 to SGND	$R_{IN1,2}$	100	200	300	k $\Omega$	–	6.1.5
<b>Powerstage</b>							
PMOS ON Resistance	$R_{DSON1,2}$	–	2.5	8	$\Omega$	$I_{OUT1,2} = 250\text{mA}$	6.1.6
PMOS ON Resistance	$R_{DSON1,2}$	–	2.5	4	$\Omega$	$I_{OUT1,2} = 250\text{mA}$ ; $T_j = 25^\circ\text{C}$ ;	6.1.7
Freewheeling Diode Forward Voltage	$V_{F1,2}$	–	–	1.5	V	$I_{F1,2} = 250\text{mA}$	6.1.8
Freewheeling Diode Forward Voltage	$V_{F1,2}$	–	1.0	1.2	V	$I_{F1,2} = 250\text{mA}$ ; $T_j = 25^\circ\text{C}$ ;	6.1.9
Output Leakage Current (PMOS)	$I_{OUTLK1,2}$	–	–	2	$\mu\text{A}$	$V_{IN1} = V_{IN2} = 0\text{V}$ ; $V_{OUT1,2} = 0\text{V}$ ; $T_j = -40^\circ\text{C to }105^\circ\text{C}$	6.1.10
Output Leakage Current (Diode)	$I_{OUTLK1,2}$	-2	–	–	$\mu\text{A}$	$V_{IN1} = V_{IN2} = 0\text{V}$ ; $V_{OUT1,2} = V_S$ ; $T_j = -40^\circ\text{C to }105^\circ\text{C}$	6.1.11
Turn ON Time (to 90% of $V_{OUT}$ )	$t_{ON1,2}$	6	12	25	$\mu\text{s}$	$V_S = 13.5\text{V}$ ; $R_{L1,2} = 51\Omega$	6.1.12
Turn OFF Time (to 10% of $V_{OUT}$ )	$t_{OFF1,2}$	8	16	30	$\mu\text{s}$	$V_S = 13.5\text{V}$ ; $R_{L1,2} = 51\Omega$	6.1.13
Rise Time (from 10% to 90% of $V_{OUT}$ )	$t_{r1,2}$	3	6	15	$\mu\text{s}$	$V_S = 13.5\text{V}$ ; $R_{L1,2} = 51\Omega$	6.1.14
Fall Time (from 90% to 10% of $V_{OUT}$ )	$t_{f1,2}$	3	6	15	$\mu\text{s}$	$V_S = 13.5\text{V}$ ; $R_{L1,2} = 51\Omega$	6.1.15
Slew Rate ON = $dV/dt$ (10% to 90% of $V_{OUT}$ )	$SR_{ON1,2}$	0.7	1.7	3.5	V/ $\mu\text{s}$	$V_S = 13.5\text{V}$ ; $R_{L1,2} = 51\Omega$	6.1.16
Slew Rate OFF = $-dV/dt$ (10% to 90% of $V_{OUT}$ )	$SR_{OFF1,2}$	0.7	1.7	3.5	V/ $\mu\text{s}$	$V_S = 13.5\text{V}$ ; $R_{L1,2} = 51\Omega$	6.1.17
<b>Current consumption</b>							
Quiescent Current in OFF Mode	$I_{SOFF}$	–	–	1	$\mu\text{A}$	$T_j = -40^\circ\text{C to }85^\circ\text{C}$ ; $V_{IN1} = V_{IN2} = 0\text{V}$ ; $R_{L1,2} = 51\Omega$	6.1.18

**Electrical Characteristics**
**Table 6**  $V_S = 4.5\text{ V to }42\text{ V}$  ;  $T_j = -40^\circ\text{C to }+125^\circ\text{C}$ , all voltages with respect to ground, currents flowing into the device unless otherwise specified ; typical values are given at  $V_S = 13.5\text{ V}$ ,  $T_j = 25^\circ\text{C}$ 

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Quiescent Current in OFF Mode	$I_{\text{SOFF}}$	–	–	5	$\mu\text{A}$	$T_j = -40^\circ\text{C to }105^\circ\text{C}$ ; $V_{\text{IN}1} = V_{\text{IN}2} = 0\text{V}$ ; $R_{\text{L}1,2} = 51\Omega$	6.1.19
Current Consumption in ON Mode without load	$I_{\text{SON}}$	–	3	5	$\text{mA}$	$V_{\text{IN}1} = V_{\text{IN}2} = 5\text{V}$ ; OUT1, 2 open	6.1.20
Current Consumption in ON Mode without load	$I_{\text{SON}}$	–	3	4	$\text{mA}$	$V_{\text{IN}1} = V_{\text{IN}2} = 5\text{V}$ ; $T_j = 25^\circ\text{C}$ ; OUT1, 2 open	6.1.21
Current Consumption in ON Mode; with resistive nominal loads $I_{\text{SON}} = I_S - I_{\text{OUT}1} - I_{\text{OUT}2}$	$I_{\text{SON}}$	–	3	5	$\text{mA}$	$V_{\text{IN}1} = V_{\text{IN}2} = 5\text{V}$ ; $R_{\text{L}1} = R_{\text{L}2} = 51\Omega$ ; $V_S = 13.5\text{ V}$	6.1.22
<b>Overload Protection Current Limit<sup>1)</sup></b>							
Output Current Limitation	$I_{\text{OUTL}1,2}$	250	400	600	$\text{mA}$	$4.5\text{V} < V_{\text{DS}1,2} < 20\text{V}$	6.1.23
Output Current Limitation	$I_{\text{OUTL}1,2}$	200	300	–	$\text{mA}$	$V_{\text{DS}1,2} = 30\text{V}$	6.1.24
Output Current Limitation	$I_{\text{OUTL}1,2}$	50	150	–	$\text{mA}$	$V_{\text{DS}1,2} = 42\text{V}$	6.1.25
Status flag time after positive input slope <sup>2)</sup>	$t_{\text{dP}1,2}$	–	60	–	$\mu\text{s}$	–	6.1.26
<b>Overtemperature Protection<sup>1)</sup></b>							
Thermal Shutdown Trip Point	$T_{\text{SDOFF}}$	150	175	200	$^\circ\text{C}$	–	6.1.27
Thermal Shutdown Release Point	$T_{\text{SDON}}$	125	150	175	$^\circ\text{C}$	–	6.1.28
Thermal Shutdown Hysteresis	$T_{\text{SDHY}}$	–	25	–	$^\circ\text{C}$	–	6.1.29
<b>Open Load Diagnosis</b>							
Open Load Detection Threshold in ON state; ST going from high to low	$I_{\text{LOL}}$	0.2	3.5	8	$\text{mA}$	$V_S = 13.5\text{V}$ $T_j = 25^\circ\text{C}$	6.1.30
Open Load Detection Threshold in ON state; ST going from low to high	$I_{\text{HOL}}$	1	5	9.5	$\text{mA}$	$V_S = 13.5\text{V}$ $T_j = 25^\circ\text{C}$	6.1.31
Open Load Detection Threshold Hysteresis in ON state	$I_{\text{LOLHYS}}$	0.2	1.5	–	$\text{mA}$	$V_S = 13.5\text{V}$ $T_j = 25^\circ\text{C}$	6.1.32
Status flag time after positive input slope while in Open Load	$t_{\text{dOLOFF}1,2}$	–	18	–	$\mu\text{s}$	$V_S = 13.5\text{V}$ $T_j = 25^\circ\text{C}$	6.1.33
Status flag time while ON after Open Load event	$t_{\text{dOLONF}1,2}$	–	42	–	$\mu\text{s}$	$V_S = 13.5\text{V}$ $T_j = 25^\circ\text{C}$	6.1.34
Status flag time while ON going out of Open Load	$t_{\text{dOLONR}1,2}$	–	10	–	$\mu\text{s}$	$V_S = 13.5\text{V}$ $T_j = 25^\circ\text{C}$	6.1.35
<b>Status Flag</b>							
Status Drop Voltage when L	$V_{\text{STL}1,2}$	–	200	400	$\text{mV}$	$I_{\text{ST}1,2} = 3\text{mA}$	6.1.36
Status Leakage Current when H	$I_{\text{STLK}1,2}$	–	–	10	$\mu\text{A}$	$V_{\text{ST}1,2} = 7\text{V}$	6.1.37
<b>Undervoltage Lockout</b>							
UV Switch ON Voltage	$V_{\text{UVON}}$	3.75	4.25	4.5	$\text{V}$	$V_S$ increasing	6.1.38
UV Switch OFF Voltage	$V_{\text{UVOFF}}$	3.25	3.75	4.25	$\text{V}$	$V_S$ decreasing	6.1.39
UV ON/OFF Hysteresis	$V_{\text{UVHY}}$	0.2	0.5	–	$\text{V}$	$V_{\text{UVON}} - V_{\text{UVOFF}}$	6.1.40

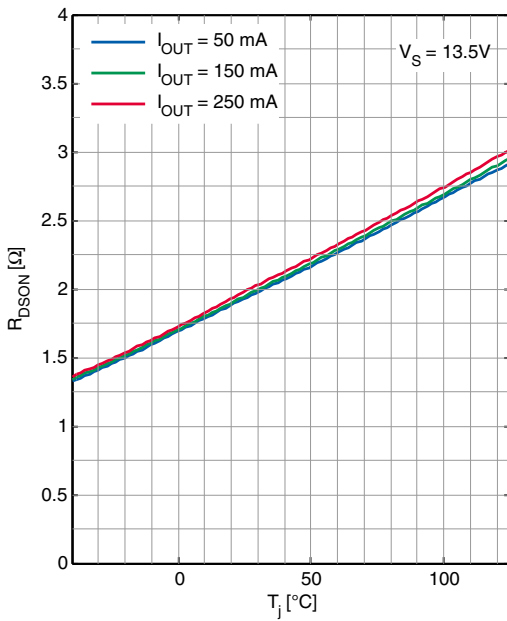
- 1) Please refer to chapter **"Protection Functions" on Page 7**
- 2) No delay time after overtemperature switch off and short circuit in on-state.



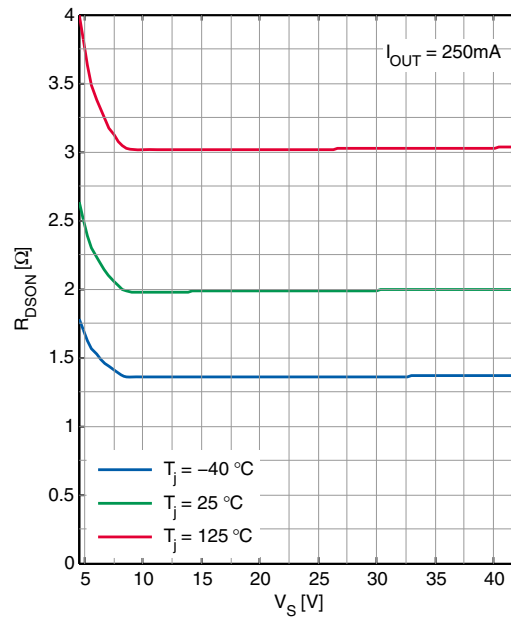
## 7 Typical Performance Graphs

### Typical Performance Characteristics

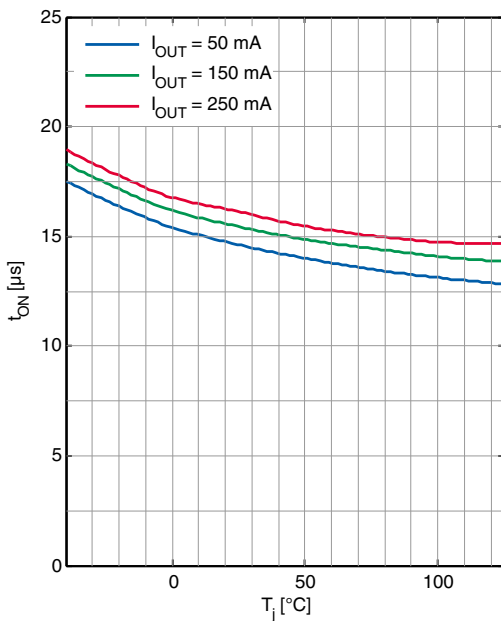
**On-Resistance  $R_{DSON}$  versus Junction Temperature  $T_j$**



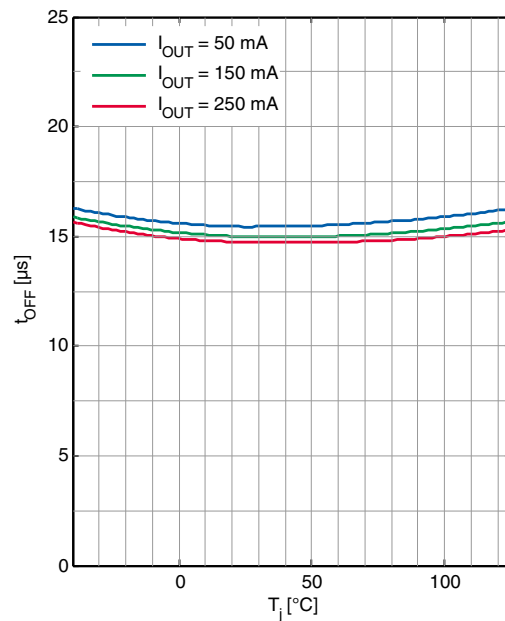
**On-Resistance  $R_{DSON}$  versus Supply Voltage  $V_S$**



**Switch ON Time  $t_{ON}$  versus Junction Temperature  $T_j$**

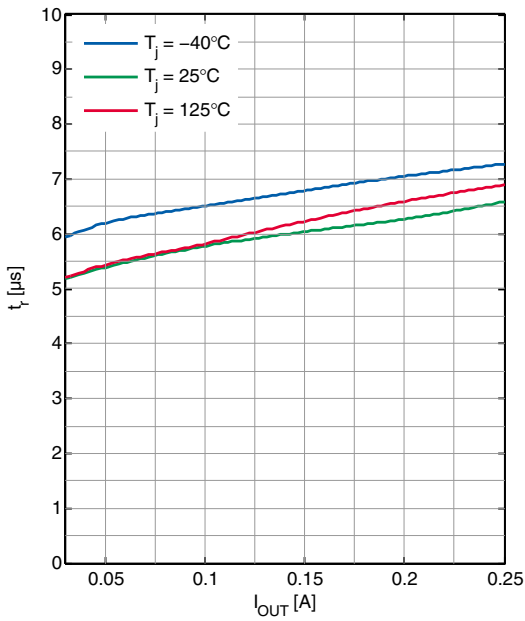


**Switch OFF Time  $t_{OFF}$  versus Junction Temperature  $T_j$**

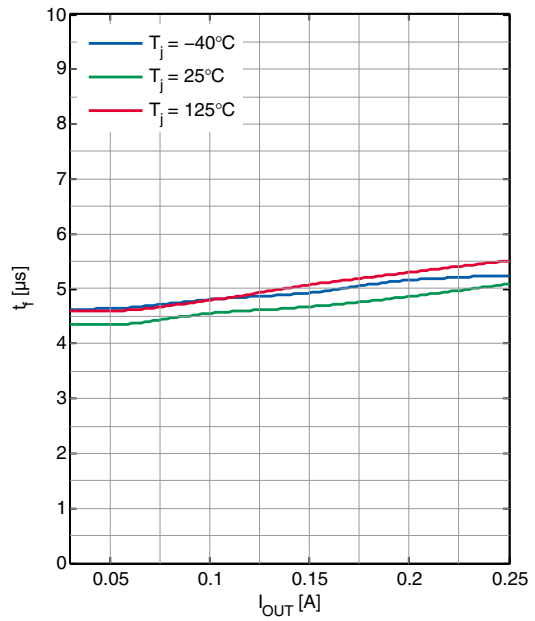


Typical Performance Characteristics

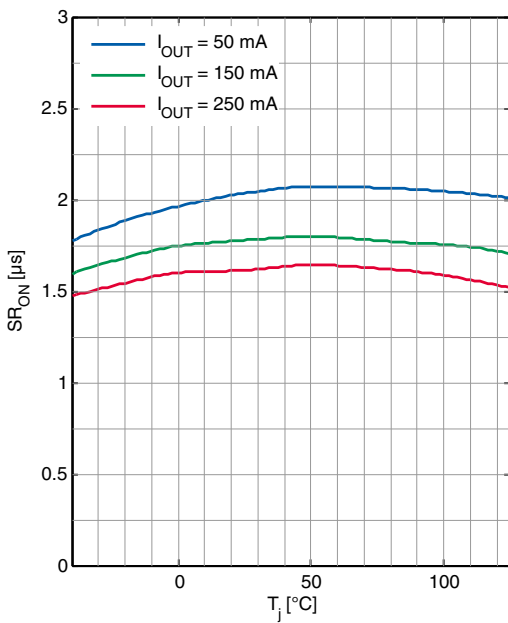
Output Rise Time  $t_r$  versus Load Current  $I_{OUT}$



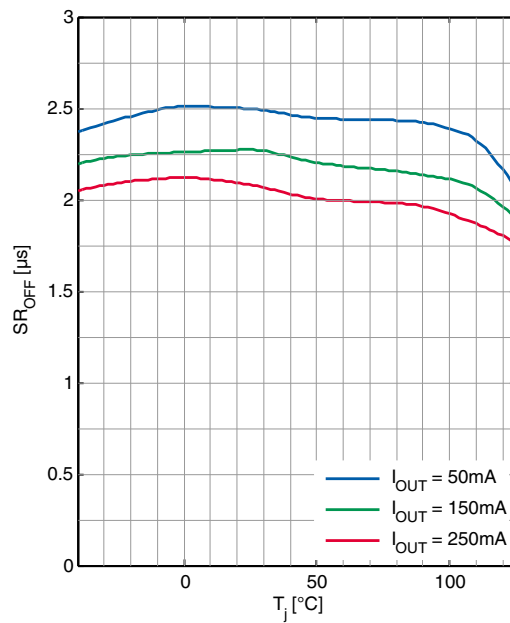
Output Fall Time  $t_f$  versus Load Current  $I_{OUT}$



ON Slewrate  $SR_{ON}$  versus Junction Temperature  $T_j$

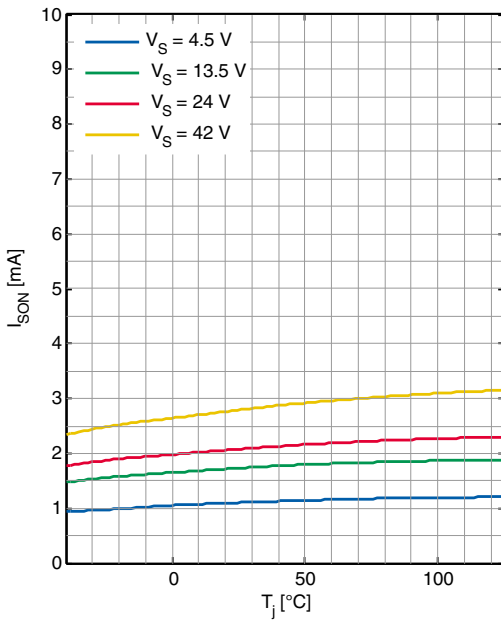


OFF Slewrate  $SR_{OFF}$  versus Junction Temperature  $T_j$

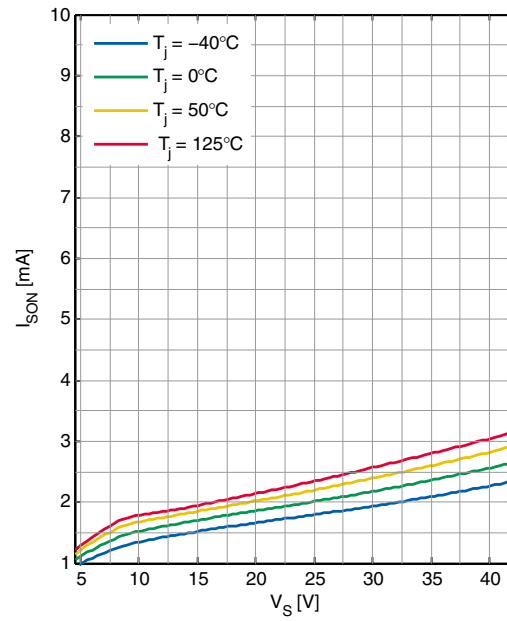


Typical Performance Characteristics

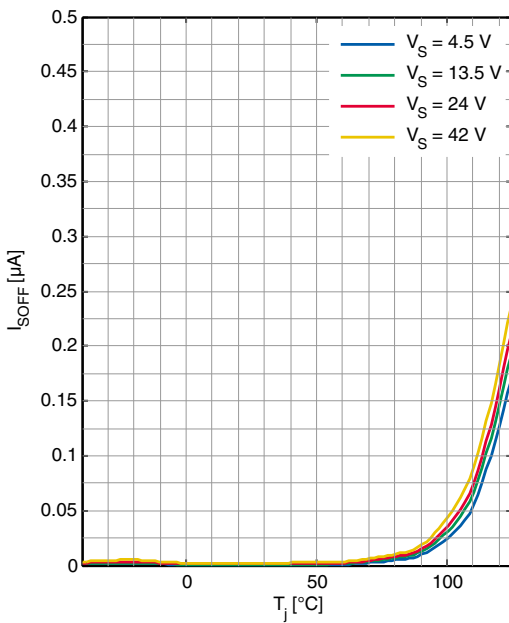
ON Supply Current  $I_{SON}$  versus Junction Temperature  $T_j$



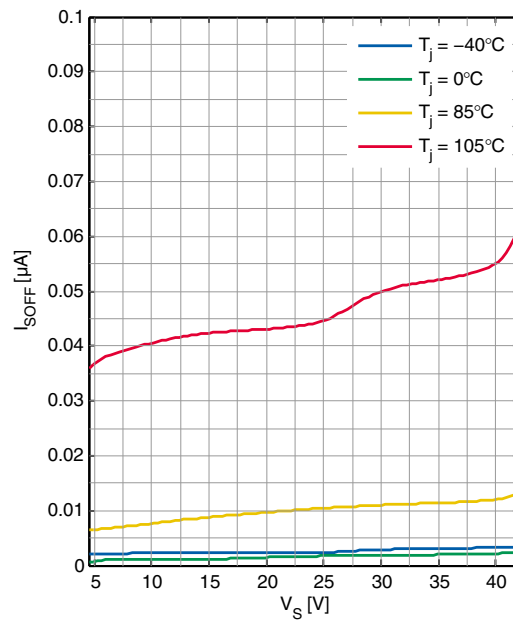
ON Supply Current  $I_{SON}$  versus Supply Voltage  $V_S$



Quiescent Current in OFF mode  $I_{SOFF}$  versus Junction Temperature  $T_j$

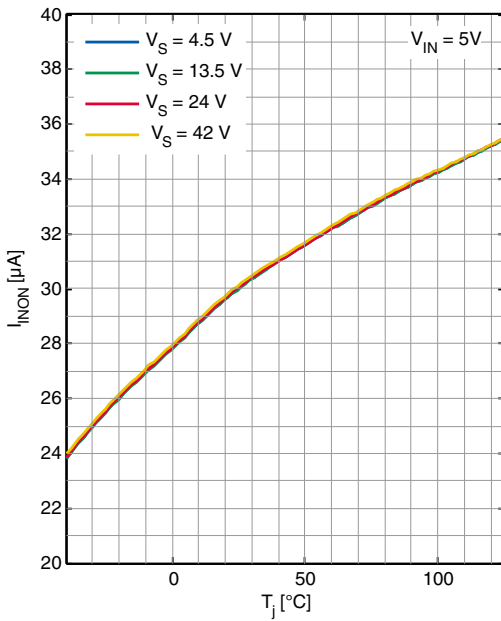


Quiescent Current in OFF mode  $I_{SOFF}$  versus Supply Voltage  $V_S$

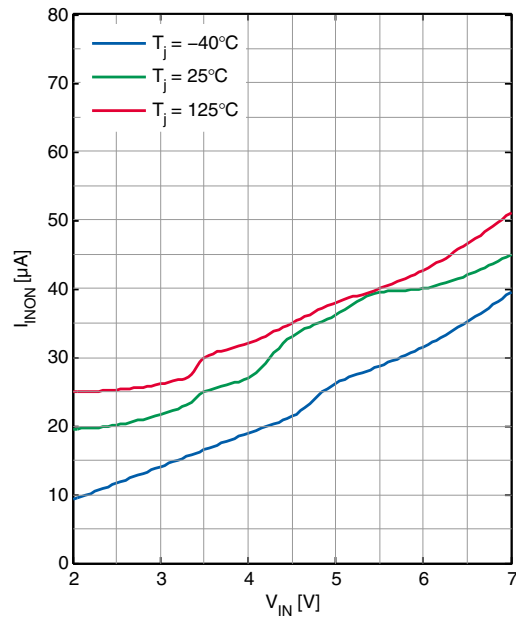


Typical Performance Characteristics

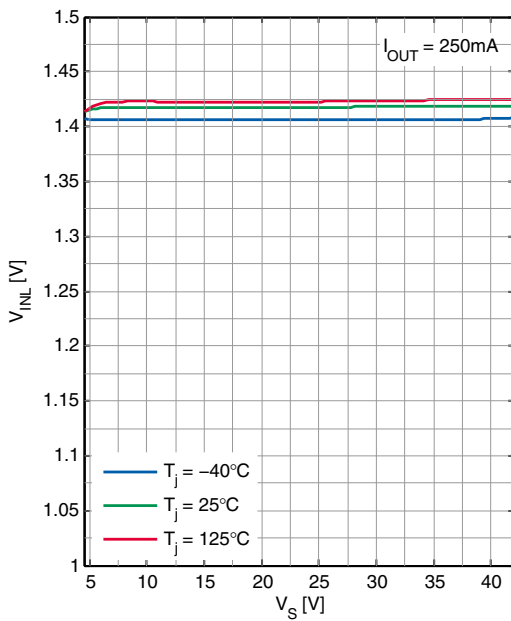
Input Current Consumption  $I_{IN}$  versus Junction Temperature  $T_j$



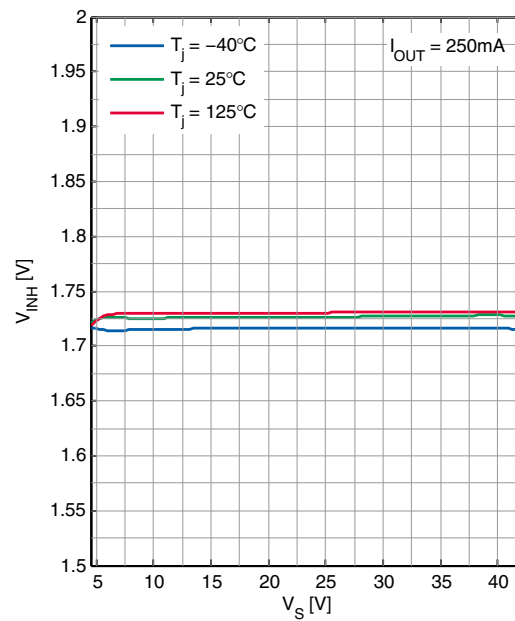
Input Current Consumption  $I_{IN}$  versus Input voltage  $V_{IN}$



Input Threshold voltage  $V_{INL}$  versus Supply Voltage  $V_S$

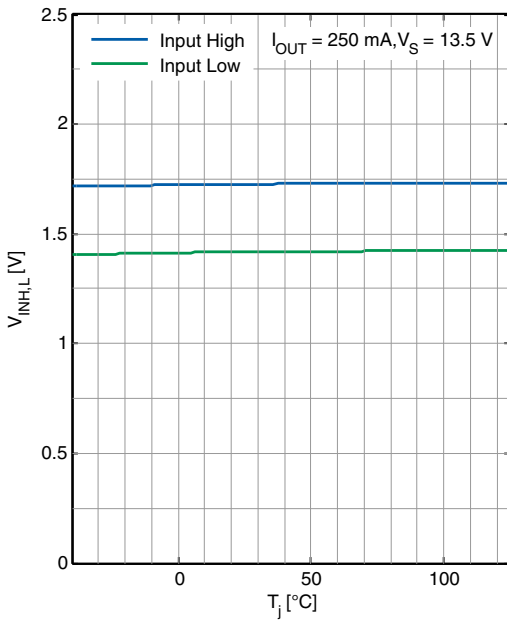


Input Threshold voltage  $V_{INH}$  versus Supply Voltage  $V_S$

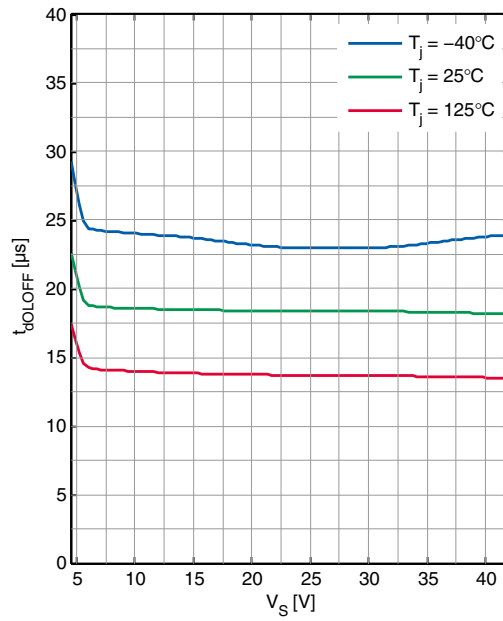


Typical Performance Characteristics

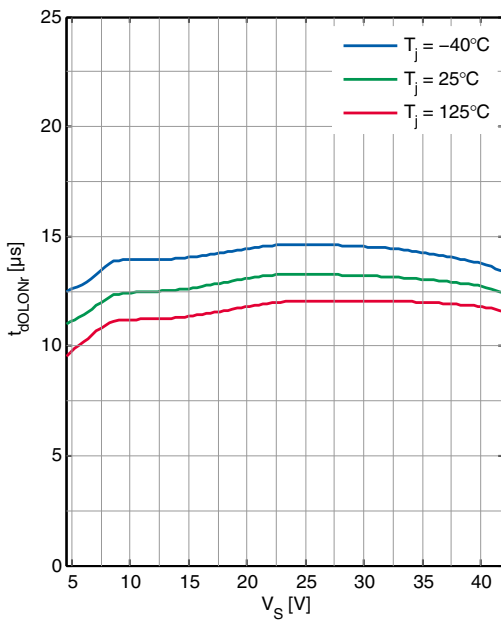
Input Threshold voltage  $V_{IN,H,L}$  versus Junction Temperature  $T_j$



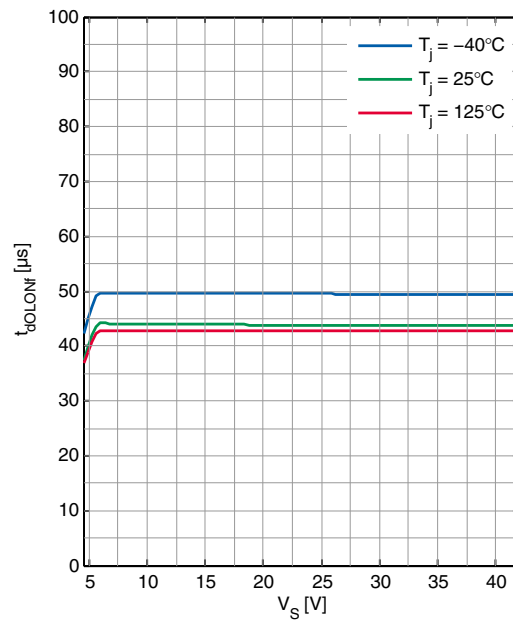
Status Flag Delay time in Open Load condition  $t_{dO,OFF}$  versus Supply Voltage  $V_S$



Status Flag Delay time while ON going out of Open Load condition  $t_{dO,ONr}$  versus Supply Voltage  $V_S$

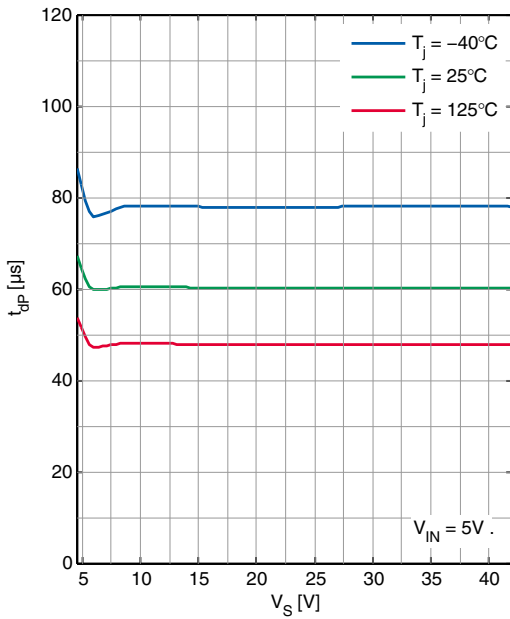


Status Flag Delay time while ON after Open Load event  $t_{dO,ONf}$  versus Supply Voltage  $V_S$

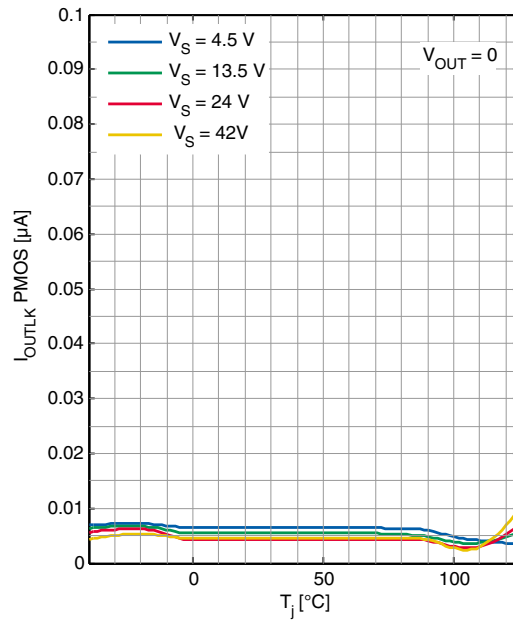


Typical Performance Characteristics

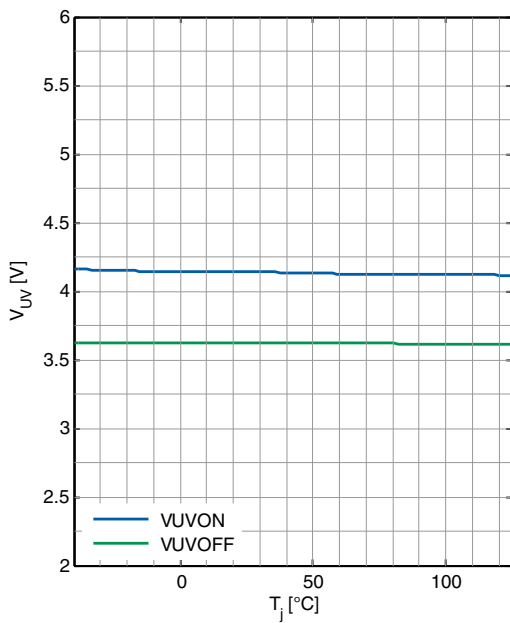
Status Flag Delay time after positive slope  $t_{dp}$  versus Supply Voltage  $V_S$



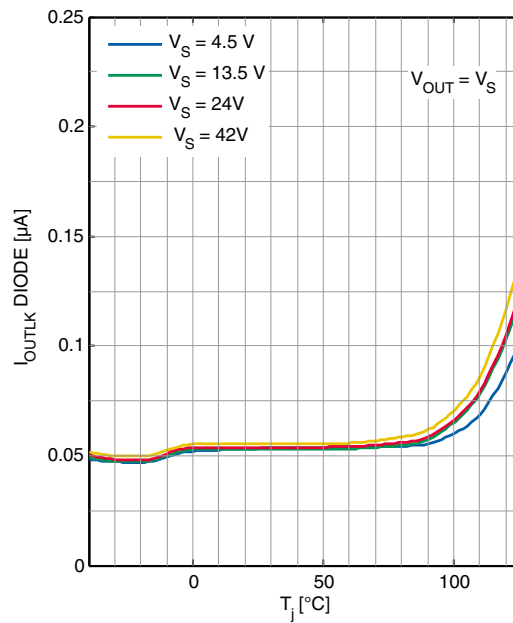
Output Leakage current  $I_{OUTLK}$  (PMOS) versus Junction Temperature  $T_j$



Under Voltage Lockout  $V_{UVON}$ ,  $V_{UVOFF}$  versus Junction Temperature  $T_j$

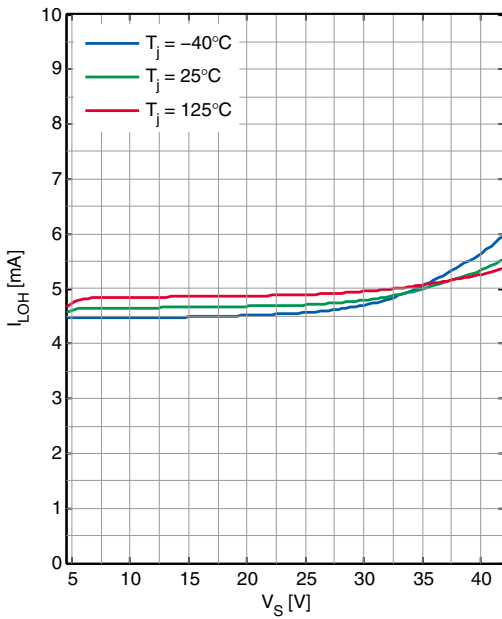


Output Leakage current  $I_{OUTLK}$  (Diode) versus Junction Temperature  $T_j$

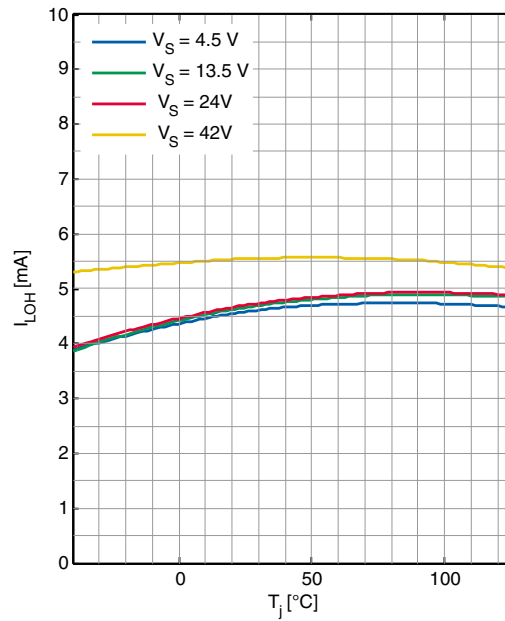


Typical Performance Characteristics

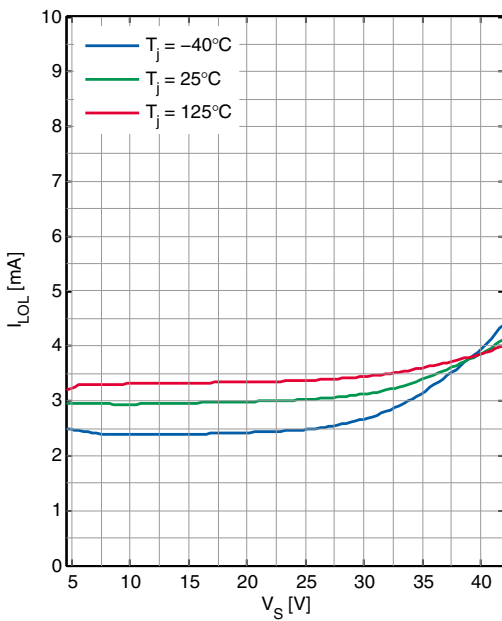
Open Load Current Threshold  $I_{LOH}$  versus Supply Voltage  $V_S$



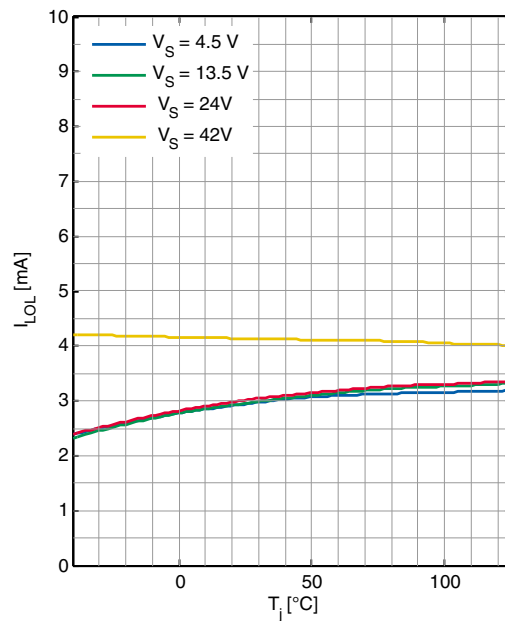
Open Load Current Threshold  $I_{LOH}$  versus Junction Temperature  $T_j$



Open Load Current Threshold  $I_{LOL}$  versus Supply Voltage  $V_S$

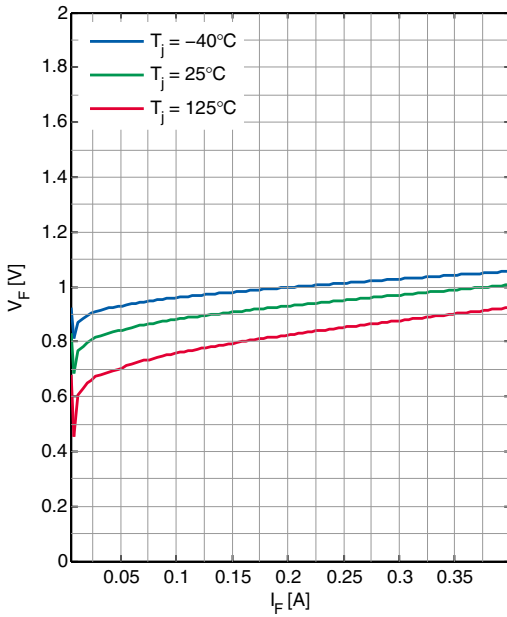


Open Load Current Threshold  $I_{LOL}$  versus Junction Temperature  $T_j$

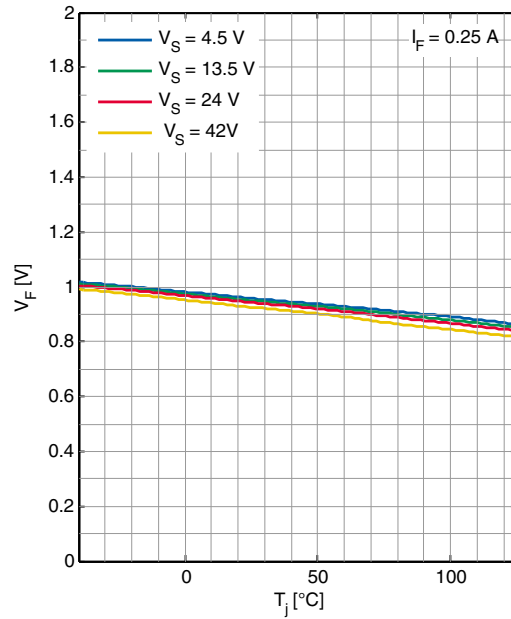


Typical Performance Characteristics

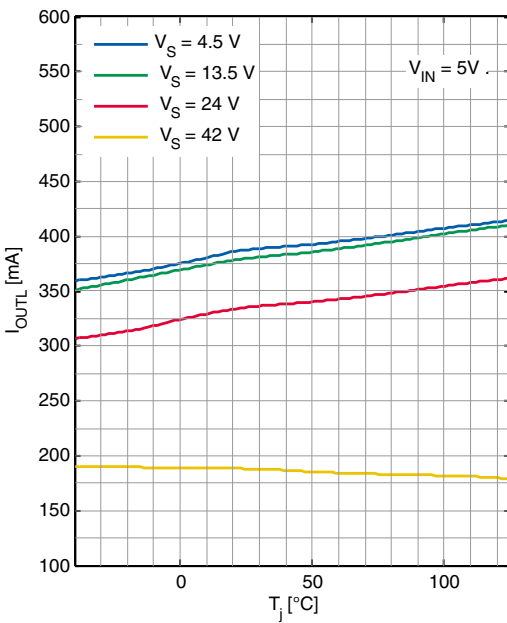
Freewheeling diode forward voltage  $V_F$  versus Current  $I_F$



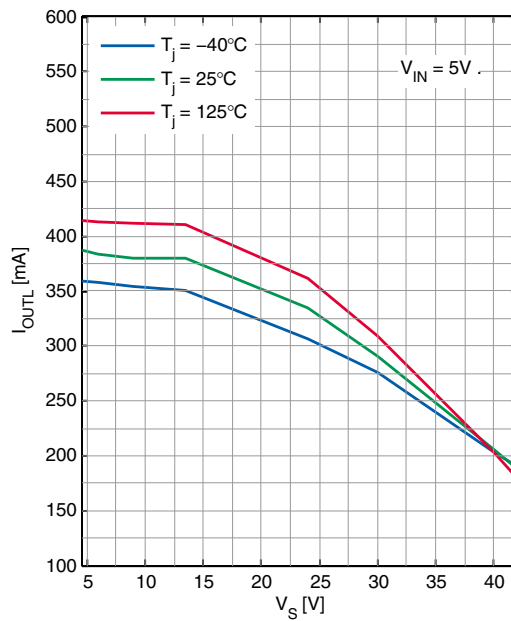
Freewheeling diode forward voltage  $V_F$  versus Junction Temperature  $T_j$



Output Current Limitation  $I_{OUTL}$  versus Junction Temperature  $T_j$



Output Current Limitation  $I_{OUTL}$  versus Supply Voltage  $V_S$





## 8 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

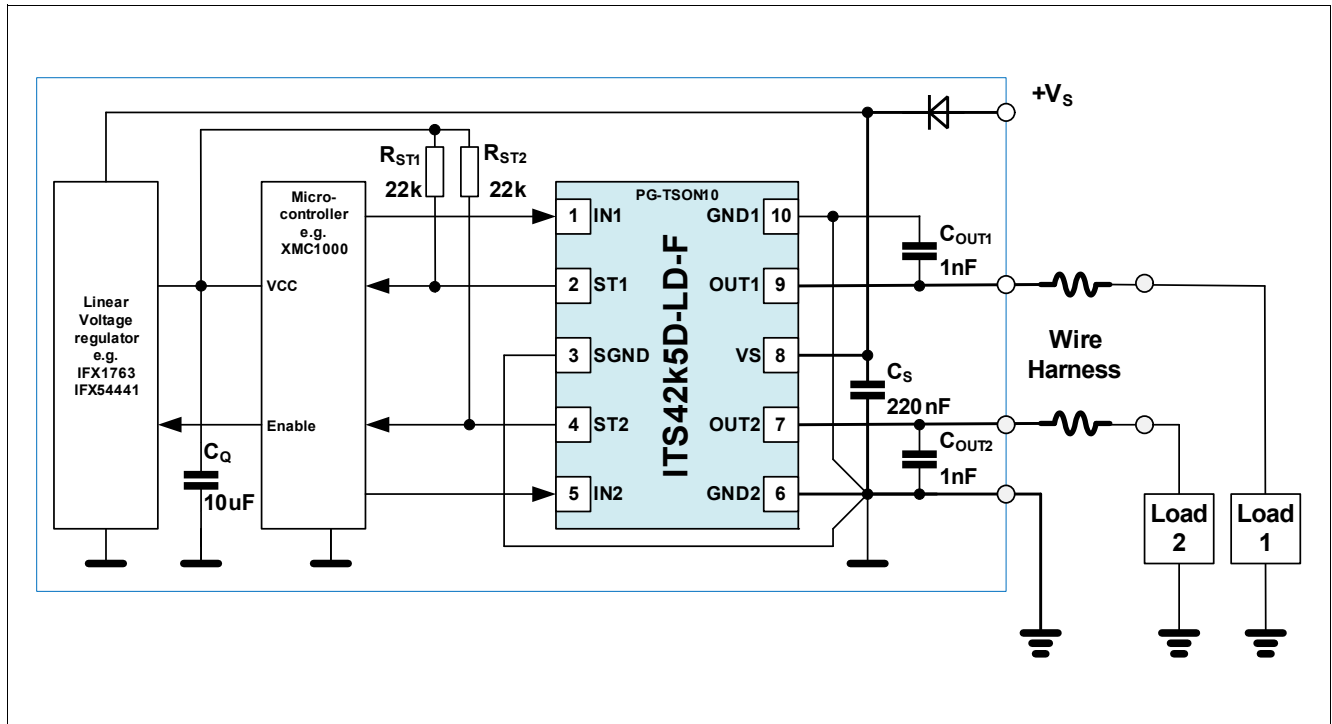


Figure 9 Application diagram ITS42k5D-LD-F

The ITS42k5D-LD-F can be connected via a reverse polarity diode to a supply network. It is recommended to place a ceramic capacitor (e.g.  $C_s = 220\text{nF}$ ) between supply voltage VS and GND of the module to avoid line disturbances. Wire harness inductors/resistors are sketched in the application circuit above.

The complex loads (resistive, capacitive or inductive) must be connected to the output pins OUT1 and OUT2.

A built-in current limit protects the device against destruction.

The ITS42k5D-LD-F can be switched on and off with standard logic ground related logic signals at pin IN1 and IN2. In standby mode ( $\text{IN1}=\text{IN2}=\text{L}$ ) the ITS42k5D-LD-F is deactivated with very low current consumption.

The output voltage slope is controlled during on and off transition to minimize emissions. Only a small ceramic capacitor  $\text{COUT}_{1,2} = 1\text{nF}$  is recommended to attenuate RF noise.

An evaluation board is available for the easy evaluation of the ITS42k5D-LD-F. Please refer to the Evaluation Board Finder under Tools on the Infineon webpage.

## 8.1 Thermal Considerations

The kind of PCB required for an application can be easily derived if the ambient temperature of the application, in which the ITS42k5D-LD-F is being used, is known.

Let us assume the following application conditions with both channels active:

$I_{OUT} = 250 \text{ mA}$  (Given by application, load dependent)

$R_{DSON,Max} = 8 \Omega$  (Worst case scenario considered)

$T_A = 60 \text{ }^\circ\text{C}$  (Ambient Temperature, given by application)

$T_{j,max} = 125^\circ\text{C}$  as given under **“Functional Range” on Page 13**

(1)

$$P_D = I_{OUT}^2 \times R_{DSON}$$

Applying the formula given above, one can calculate the power dissipation  $P_D$  in the application, which for our application scenario i.e. 0.5W for one channel active and 1W for both channels active.

Furthermore, we know that

(2)

$$R_{thJA, Max} = \frac{T_{j, max} - T_A}{P_D}$$

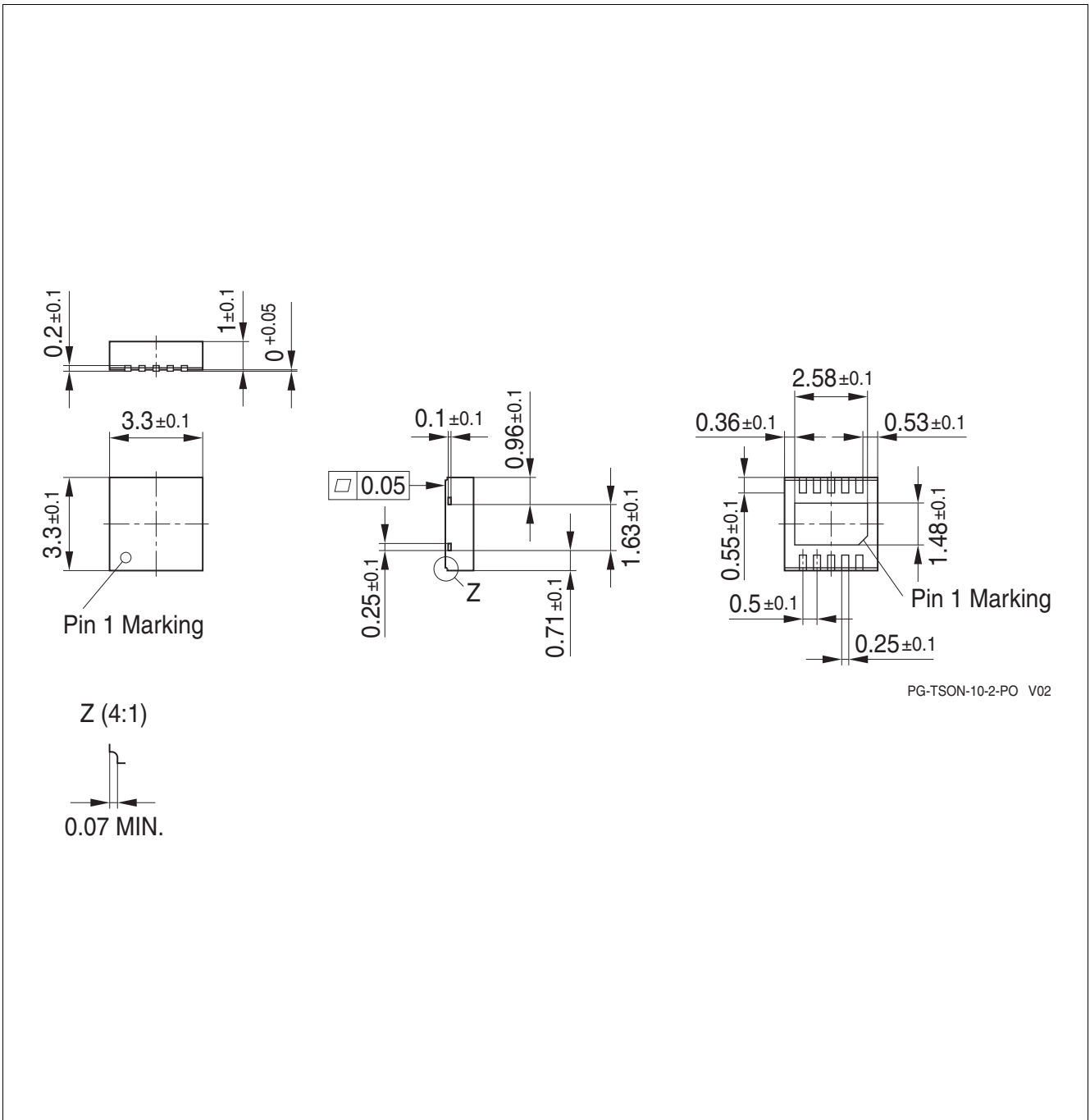
Hence we can calculate  $R_{thJA,Max}$ , which for this application scenario is 65K/W. As a result, the PCB design must ensure a thermal resistance of lower than 65K/W for the above mentioned application assumption. According to **“Thermal Resistance” on Page 13**, at least a 300mm<sup>2</sup> heatsink area is needed on a FR4 1s0p PCB or the FR4 2s2p board with thermal vias could be used for this application.

For support regarding thermal considerations, please contact us via our support webpage [www.infineon.com/support](http://www.infineon.com/support).

For further support, please refer to application notes on the Infineon website [www.infineon.com](http://www.infineon.com).

## 9 Package Outlines and Footprint

### 9.1 PG-TSON-10 Package Outline



**Figure 10 PG-TSON-10 (Plastic Dual Small Outline Package, RoHS-Compliant) Package Outline**

9.2 PG-TSON-10 Footprint

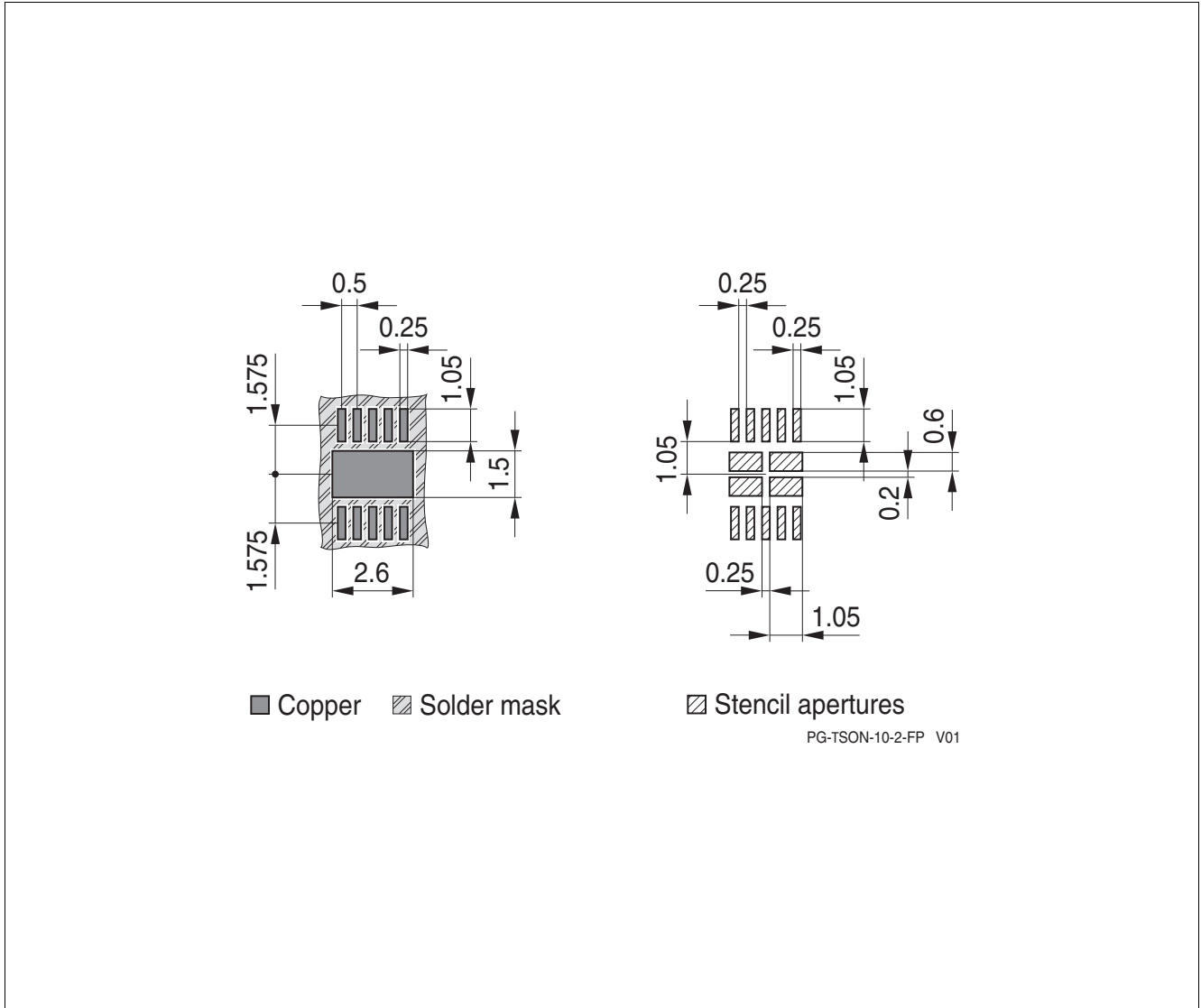


Figure 11 PG-TSON-10 (Plastic Dual Small Outline Package, RoHS-Compliant) Package Footprint

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:  
<http://www.infineon.com/packages>.

Dimensions in mm

## 10 Revision History

Revision	Date	Changes
Rev 1.0	2015-04-28	Datasheet - Initial Version

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