# SC2596
# Low Voltage Integrated DDR Termination Regulator



## Description

The SC2596 is an integrated linear DDR termination device, which provides a complete solution for DDR termination regulator designs; while meeting the JEDEC requirements of SSTL-2 and SSTL-18 specifications for DDR-SDRAM termination.

The SC2596 regulates up to +/- 2.5A for DDR-I and +/- 1.5A for DDR-II application requirements.

$V_{TT}$ is regulated to track the $V_{REF}$ voltage over the entire current range with shoot through protection.

A $V_{SENSE}$ pin is incorporated to provide excellent load regulation, along with a buffered reference voltage for internal use.

The SC2596 also features a disable function which is to tri-state the output during Suspend To Ram (STR) states by pulling the EN pin low.

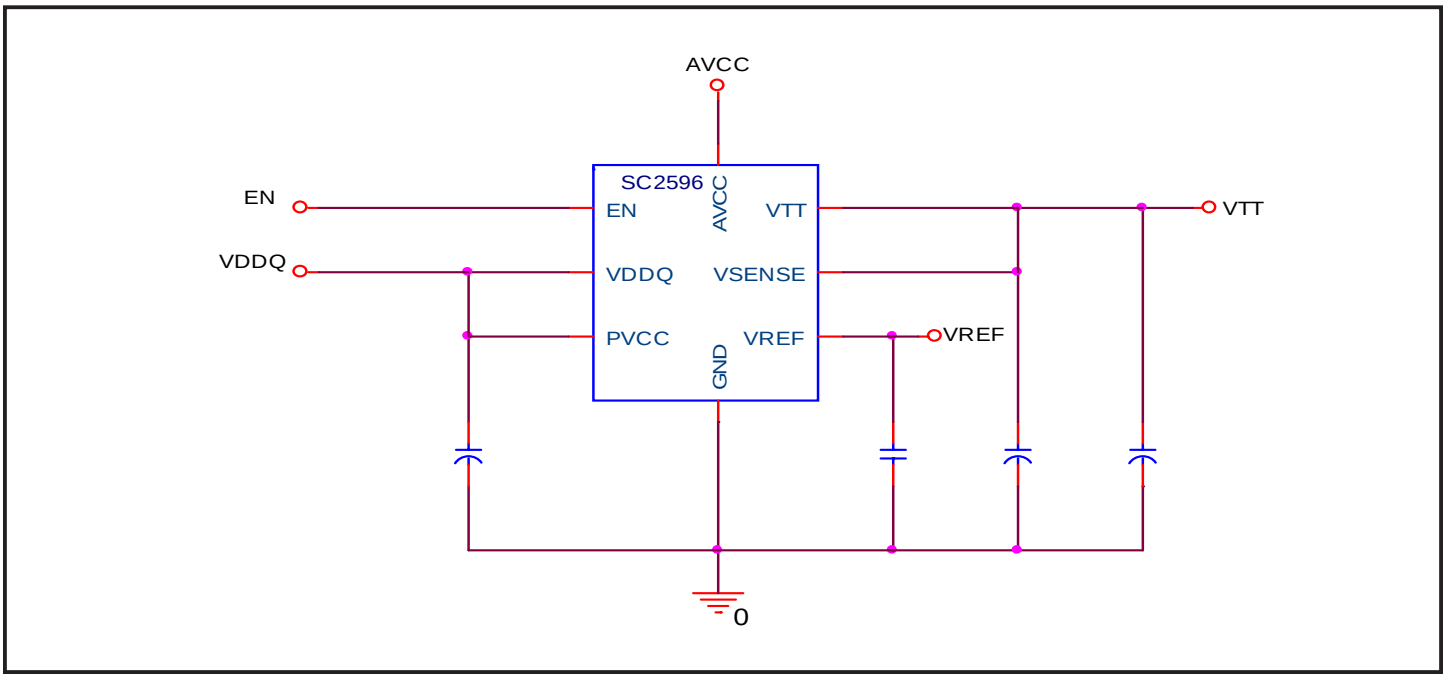
## Features

- Sourcing or sinking 2.5A for DDR-I
- Sourcing or sinking 1.5A for DDR-II
- $AV_{CC}$ undervoltage lockout
- Reference output
- Minimum number of external components
- Accurate internal voltage divider
- Disable function, puts device into sleep mode
- Thermal shutdown
- Over current protection
- Available in SOIC8-EDP package
- Pb-free, Halogen free, and RoHS/WEEE compliant

## Applications

- DDR-I and DDR-II memory termination
- SSTL-2 and SSTL-3 termination
- HSTL termination
- PC motherboards
- Graphics boards
- Disk drives
- CD-ROM drives

## Typical Application Circuit



## Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

| Parameter | Symbol | Maximum | Units |
|---|---|---|---|
| PVCC, AVCC, VDDQ, EN to GND | | -0.3 to +6.0 | V |
| Thermal Resistance Junction to Case | $\theta_{JC}$ | 5.5 | °C/W |
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | 36.5 | °C/W |
| Maximum Junction Temperature Range | $T_J$ | -40 to +125 | °C |
| Storage Temperature Range | $T_{STG}$ | -65 to +150 | °C |
| Peak IR Reflow Temperature 10-40S | $T_{PKG}$ | 260 | °C |
| ESD Rating (Human Body Model) | ESD | 2 | kV |

## Electrical Characteristics (DDR-I)

Unless otherwise specified: $T_J$ = -40°C to +125°C, $AV_{CC}$ = $PV_{CC}$ = 2.5V, $V_{DDQ}$ = 2.5V.

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Reference Voltage | $V_{REF}$ | $I_{REF\_OUT}$ = 0mA | 0.49VDDQ | 0.5VDDQ | 0.51VDDQ | V |
| $V_{REF}$ Output Impedance | $Z_{VREF}$ | $I_{REF}$ = -30uA to +30uA | | 230 | | Ω |
| VTT Output Regulation (1) | ($V_{TT}$ - $V_{REF}$) | $I_{OUT}$ = 0A<br>$I_{OUT}$ = -1.5A<br>$I_{OUT}$ = +1.5A | -25 | 0 | +25 | mV |
| Quiescent Current | $I_Q$ | $I_{LOAD}$ = 0A | | 400 | 700 | uA |
| $AV_{CC}$ Enable Threshold | | | | 2.1 | 2.2 | V |
| VDDQ Input Impedance | $Z_{VDDQ}$ | | | 100 | | kΩ |
| Quiescent Current in Shutdown | $I_{SD}$ | EN = 0 | | 150 | 250 | uA |
| EN Pin Leakage Current | $I_{Q\_SD}$ | EN = 0 | | | 1 | uA |
| EN Threshold Voltage | VH<br>VL | | 2 | | <br>0.8 | V |
| VTT Leakage Current in Shutdown | $I_{VTT\_L}$ | SD = 0V, VTT = 1.25V, at 25 °C | | 6 | | uA |

## Electrical Characteristics (DDR-I Cont.)

Unless otherwise specified: $T_J$ = -40°C to +125°C, $AV_{CC}$ = $PV_{CC}$ = 2.5V, $V_{DDQ}$ = 2.5V.

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| VSENSE Current | $I_{SENSE}$ | | | 50 | 200 | nA |
| Thermal Shutdown | $T_{SD}$ | | | 160 | | °C |
| Thermal Shutdown Hysteresis | $T_{SD\_HYS}$ | | | 10 | | °C |

Note: (1) Regulation is measured by using a load current pulse. (Pulse Width less than 10mS, Duty Cycle less than 2%, $T_A$ = 25°C)

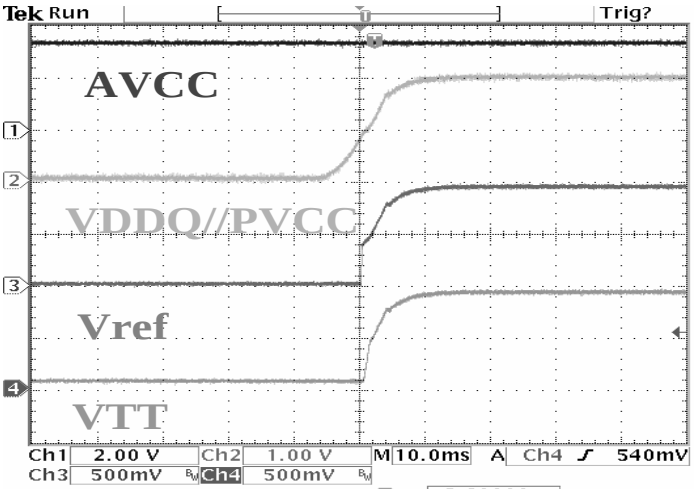
## Electrical Characteristics (DDR-II)

Unless otherwise specified: $T_J$ = -40°C to +125°C, $AV_{CC}$ = 3.3V, $PV_{CC}$ = $V_{DDQ}$ = 1.8V.

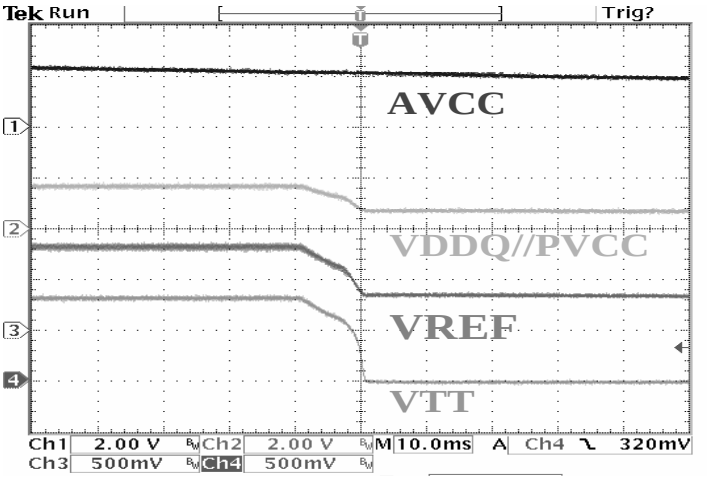
| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Reference Voltage | $V_{REF}$ | $I_{REF\_OUT}$ = 0mA | 0.49VDDQ | 0.5VDDQ | 0.51VDDQ | V |
| $V_{REF}$ Output Impedance | $Z_{VREF}$ | $I_{REF}$ = -30uA to +30uA | | 230 | | Ω |
| VTT Output Regulation (1) | ($V_{TT}$ - $V_{REF}$) | $I_{OUT}$ = 0A<br>$I_{OUT}$ = -1.0A<br>$I_{OUT}$ = +1.0A | -25 | 0 | +25 | mV |
| Quiescent Current | $I_Q$ | $I_{LOAD}$ = 0A | | 400 | 700 | uA |
| $AV_{CC}$ Enable Threshold | | | | 2.1 | 2.2 | V |
| VDDQ Input Impedance | $Z_{VDDQ}$ | | | 100 | | kΩ |
| Quiescent Current in Shutdown | $I_{SD}$ | EN = 0 | | 150 | 250 | uA |
| EN Pin Leakage Current | $I_{Q\_SD}$ | EN = 0 | | 0.5 | | uA |
| EN Threshold Voltage | VH<br>VL | | 2 | | <br>0.8 | V |
| VTT Leakage Current in Shutdown | $I_{VTT\_L}$ | SD = 0V, VTT = 0.9V, at 25 °C | | 6 | | uA |
| VSENSE Current | $I_{SENSE}$ | | | 50 | 200 | nA |
| Thermal Shutdown | $T_{SD}$ | | | 160 | | °C |
| Thermal Shutdown Hysteresis | $T_{SD\_HYS}$ | | | 10 | | °C |

Note: (1) Regulation is measured by using a load current pulse. (Pulse Width less than 10mS, Duty Cycle less than 2%, $T_A$ = 25°C)

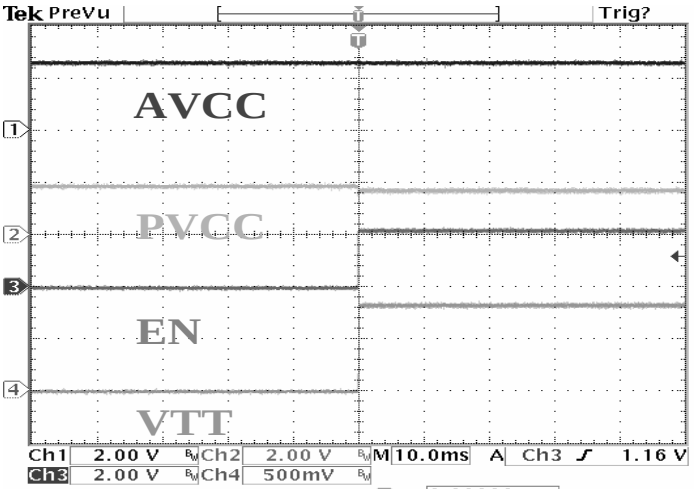
## Waveforms



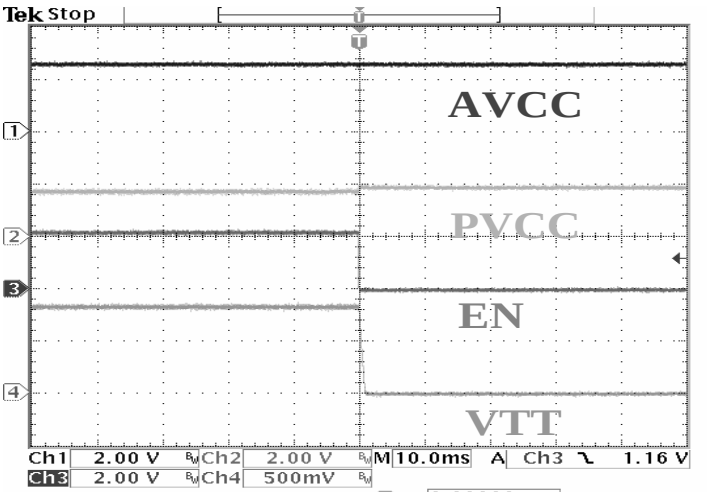

**Start up.**



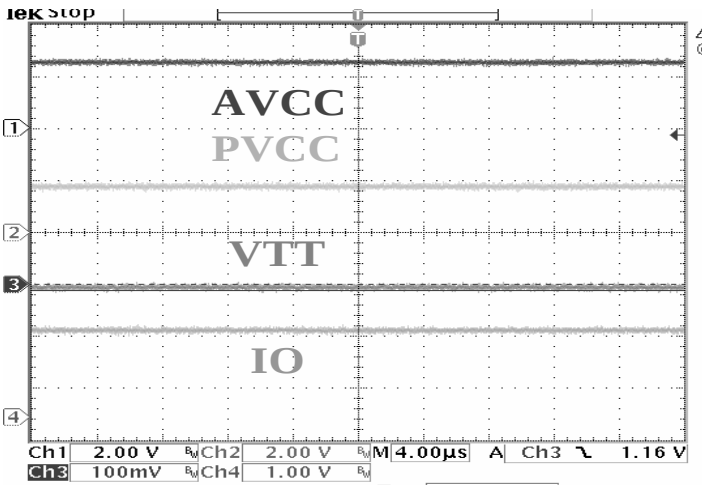

**Shut down.**



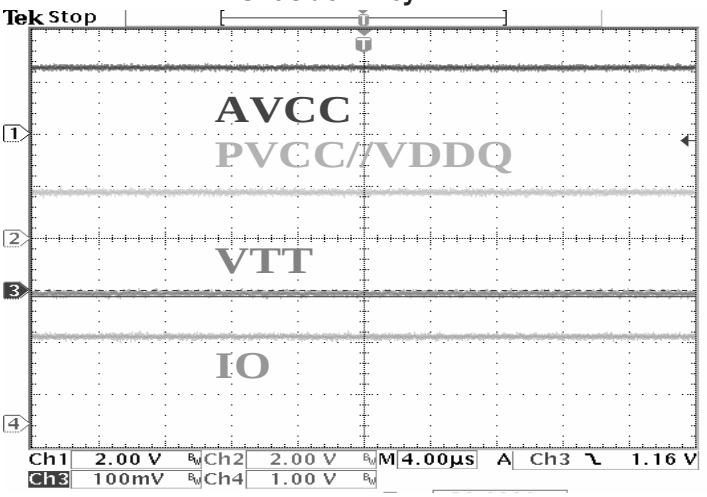

**Start up by EN.**




**Shut down by EN.**

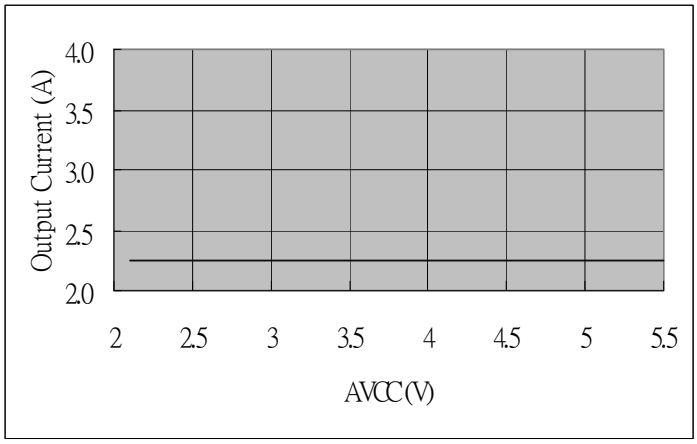



**1A load**

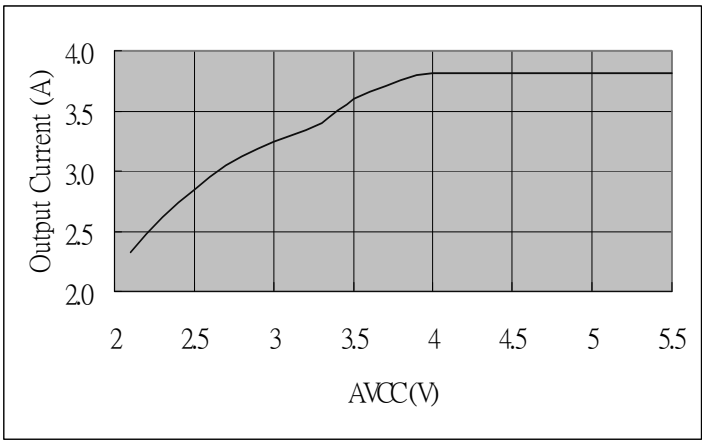



**Transient with +/- 1A load**

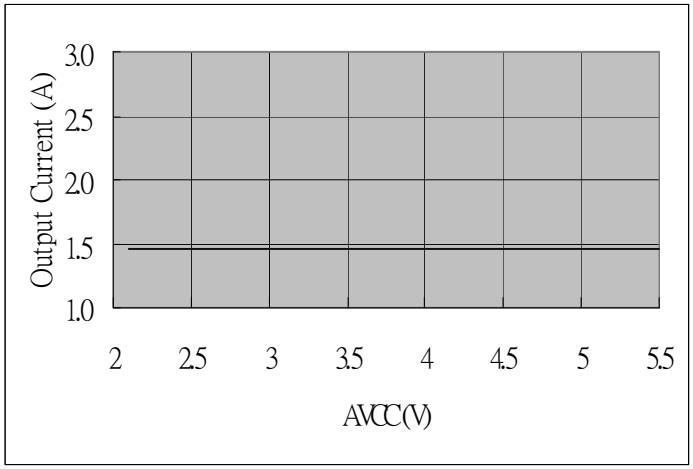
## Waveforms



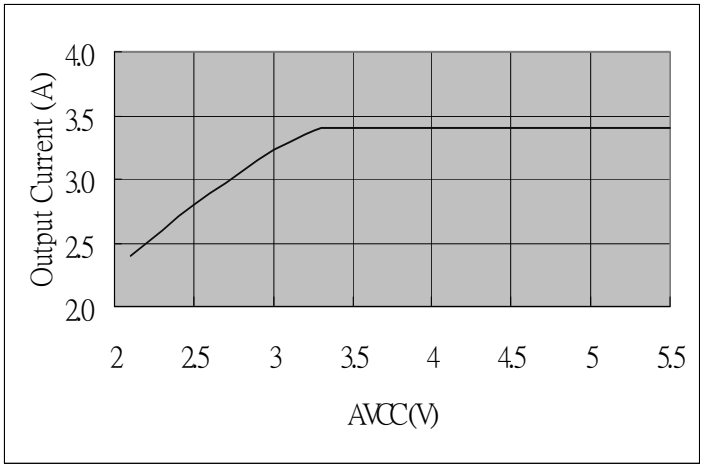

**Maximum Sourcing Current vs AVCC.**
**(VDDQ=1.8V, PVCC=2.5V)**




**Maximum Sinking Current vs AVCC.**
**(VDDQ=1.8V, PVCC=2.5V)**

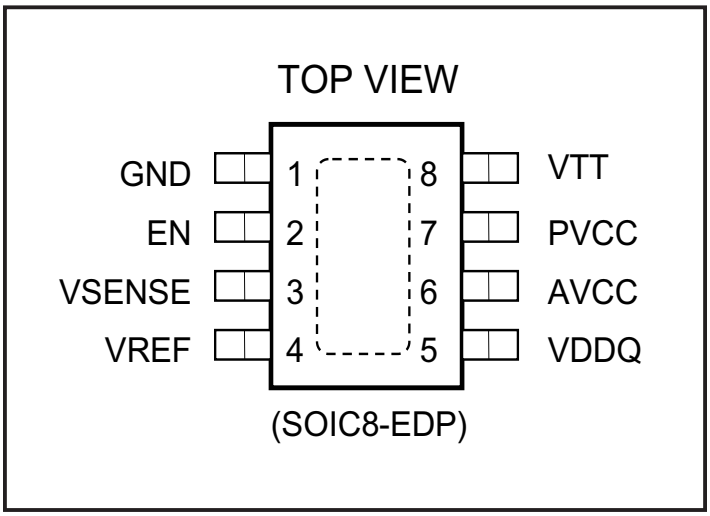



**Maximum Sourcing Current vs AVCC.**
**(VDDQ=1.8V, PVCC=1.8V)**




**Maximum Sinking Current vs AVCC.**
**(VDDQ=1.8V, PVCC=1.8V)**

## Pin Configuration




## Ordering Information

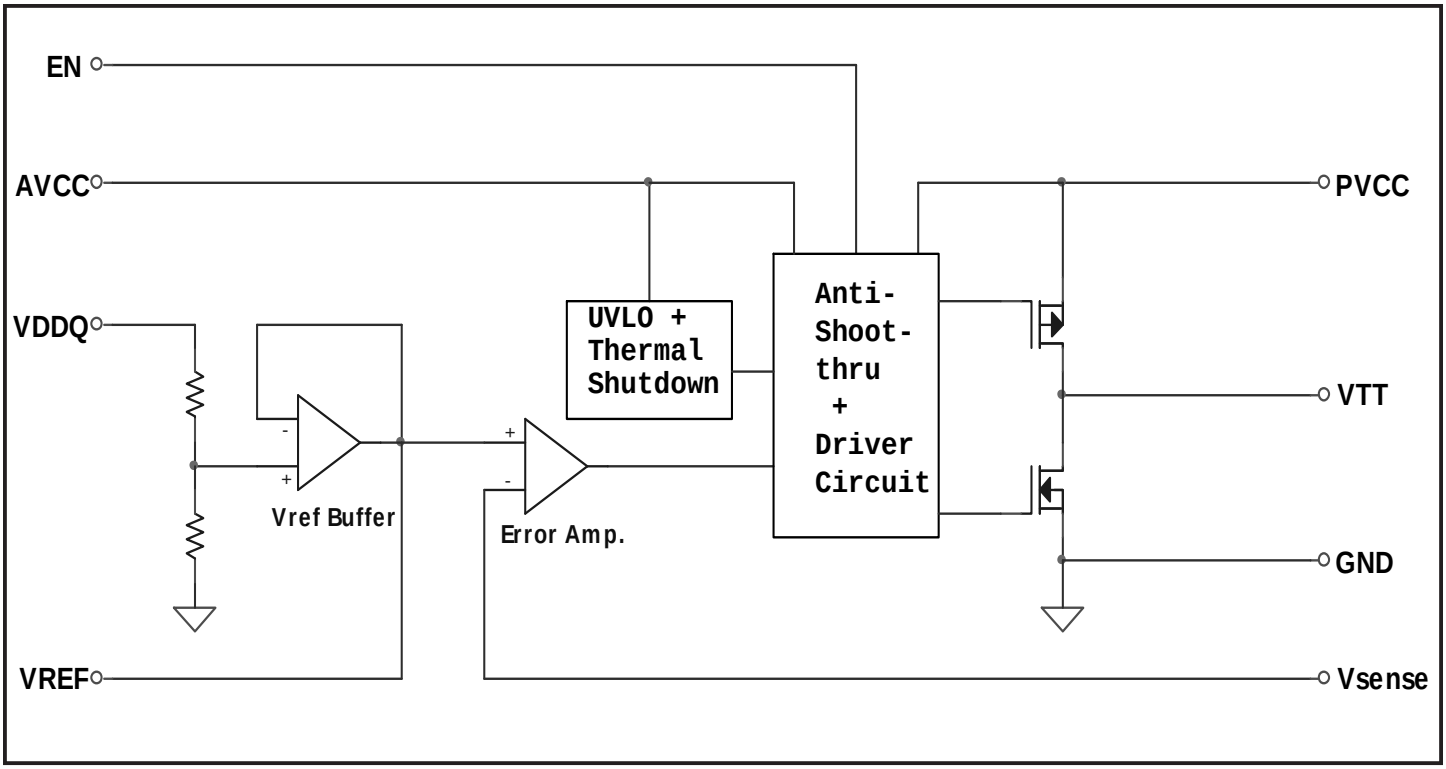
| Part Number | Package(3) | Temp. Range ($T_A$) |
|---|---|---|
| SC2596SETRT(1) | SOIC8-EDP | -40 to +105 °C |
| SC2596EVB (2) | Evaluation Board | |

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices for SOIC8-EDP.
(2) EVB provided with SOIC8-EDP package.
(3) Pb-free, Halogen free, and RoHS/WEEE compliant.

## Pin Descriptions

| Pin # | Pin Name | Pin Function |
|---|---|---|
| 1 | GND | Ground. |
| 2 | EN | Enable pin. SC2596 is disabled when EN pin is low. |
| 3 | VSENSE | VSENSE pin is a feedback pin. Connect a 10nF to 100nF Ceramic capacitor between this pin to ground and place this capacitor close to VSENSE pin is required to avoid oscillation during transient condition. |
| 4 | VREF | VREF pin is an output pin, which provides the buffered output of the internal reference voltage. A 100nF ceramic capacitor should be connected from VREF pin to ground with short trace. |
| 5 | VDDQ | The VDDQ pin is an input pin for creating internal reference voltage to regulate VTT. The VDDQ voltage is connected to an internal resistor divider. The central tap of resistor divider (VDDQ/2) is connected to the internal voltage buffer, which output is connected to VREF pin and the non-inverting input of the error amplifier as the reference voltage. With the feedback loop closed, the V TT output voltage will always track the VDDQ/2 precisely. It is recommended that a 1uF ceramic capacitor should be added next to the VDDQ pin to ground to increase the noise immunity. |
| 6 | AVCC | The AVCC pin is used to supply all of the internal control circuitry. The AVCC voltage has to be greater than its UVLO threshold voltage (2.1V typical) to allow the SC2596 to be in normal operation. If AVCC voltage is lower than the UVLO threshold voltage, the VTT pin should be in high impedance status. |
| 7 | PVCC | The PVCC pin provides the rail voltage from where the VTT pin draws load current. There is a limitation between AVCC and PVCC. The PVCC voltage must be less or equal to AVCC voltage to ensure the correct output voltage regulation. The VTT source current capability is dependent on PVCC voltage. Higher the voltage on PVCC, higher the source current. |
| 8 | VTT | The VTT pin is the output of SC2596. It can sink and source continuous current while keeping excellent load regulation. It is recommended that one should use at least one 220uF low ESR capacitor and a 1uF ceramic capacitor or one 220uF high ESR electrolytic capacitor and a 6.8uF ceramic capacitor, which are placed on the VTT strip plane to ground reducing the voltage spike under load transient condition. |
| | THERMAL PAD | Pad for heatsinking purposes. Connect to ground plane using multiple vias. Not connected internally. |

## Block Diagram




### Description

SC2596 is a low-voltage, low-dropout DDR termination regulator with separate power supply to support both DDR1 and DDR2 applications. AVCC and PVCC can be tied together for DDR1 and can also be separated for DDR2.

SC2596 regulates VTT to the voltage of VREF. VTT will sink or source upto 2.5A. Internal shoot-through protection ensure both top and bottom MOSFET will not conduct while maintaining fast source-to-sink load transient. Thermal shut-down and internal current limit protect SC2596 from shorted load or over-heated

### VREF BUFF

VREF is derived from VDDQ with an accurate divide by op-amps(VREF Buffer). It is capable to sink and source 30uA. It is used as the reference voltage to the Error amp. A 100nF or higher capacitor is recommended for VREF pin to ground; To enhance the noise immunity from board, an additional pull-down resistor (1MΩ) is recomanded as well from VREF pin to ground.

### ERROR AMP

Low input offset op-amp for the main linear regulator. It controls the VTT output voltage and which side of the MOSFET to turn on (or turn off) to achieve zero shoot through current.

### ANTI-Shoot Thought Driver

Buffer stage takes the error voltage to control MOSFET. Internal current limit is incorporated to protect from shorted load.

### THERMAL SHUTDOWN & UVLO

The Thermal shutdown block prevent the junction temperature exceed 165 °C. UVLO circuit to ensure proper power is available for correct operation of the IC.

## Application Information

### Overview

Double Data Rate (DDR) SDRAM was defined by JEDEC 1997. Its clock speed is the same as previous SDRAM but data transfer speed is twice than previous SDRAM. By now, the requirement voltage range is changed from 3.3V to 2.5V or 1.8V; the power dissipation is smaller than SDRAM. For above reasons, it is very popular and widely used in M/B, N/B, Video-cards, CD ROM drives, Disk drives.

Regarding the DDR power management solution, there are two topologies can be selected for system designers. One is switching mode regulator that has bigger sink/source current capability, but the cost is higher and needs more board space. Another solution is linear mode regulator, which costs less, and needs less board space. For two DIMM motherboards, system designers usually choose the linear mode regulator for DDR power management solution.

### Thermal shutdown

The SC2596 has built-in thermal detected circuit to prevent this device from over temperature and damage. The SC2596 goes into shunt down mode when temperature is higher than 165°C. The protection condition will release when the temperature of device drop down by 10°C.

### AVCC and PVCC

AVCC and PVCC are the input supply pins for the SC2596. AVCC is supply voltage for all the internal control circuitry. The AVCC voltage has to be greater than its UVLO threshold voltage (2.1V typical) to allow the SC2596 to be normal operation.

The PVCC pin provides the rail voltage from where the VTT pin draws load current. There is a limitation between AVCC and PVCC. The PVCC voltage must be less or equal to AVCC voltage to ensure the correct VTT output voltage regulation.

### VSENSE

VSENSE pin is a feedback pin from VTT plane. VTT plane is always a narrow and long strip plane in most montherboard applications. This long strip plane will cause a large trace inductance and trace resistance. Consider the load transient condition, a fast load current going through VTT strip plane will create a voltage spike on VTT plane and a DC voltage drop for load current. It is recommanded the VSENSE pin should be connected center of VTT plane to improve regulation and transient response.

A longer trace of VSENSE may pick up noise and cause the error of load regulation. Hence designer should avoid a longer trace between VSENSE to VTT plane. A 100nF ceramic capacitor close to VSENSE pin is required.

### VREF

VREF pin is an output pin to provid internal reference voltage. System designer can use the voltage for Northbridge chipset and memory. It is necessary to add a ceramic capacitor (100nF) from VREF pin to ground with shortest trace.

### Typical Application Circuits & Waveforms

Four different application circuits are shown below in Figure 1, Figure 2, Figure 3 and Figure 4. Each circuit is designed for a specific condition. See Note a. and b. below for recommended power up sequencing.

### Application_1: Standard SSTL-2 Application

The AVCC pin, PVCC pin and the $V_{DDQ}$ pin can be tied together for SSTL-2 application (Figure 1). It only needs a 2.5V power rail for normal operation. System designer can save the PCB space and reduce the cost.

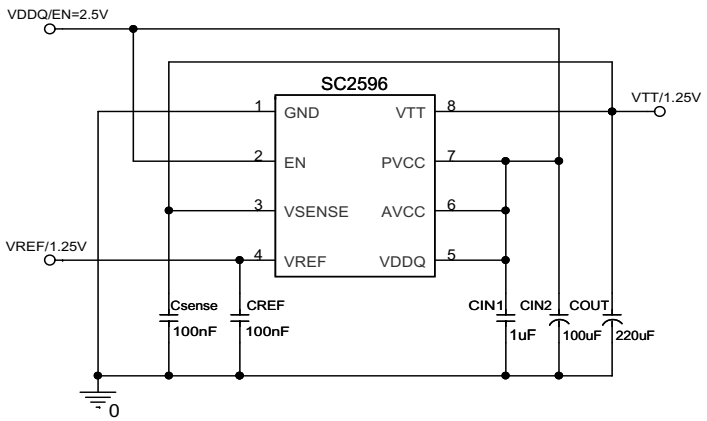



**Figure 1: Standard SSTL-2 application.**

## Application Information (Cont.)

### Application_2: Lower Power Loss Configuration for SSTL-2

If power loss is a major concern, separating the PVCC form AVCC and VDDQ will be a good choice (Figure 2). The PVCC can operate at lower voltage (1.8V to 2.5V) if 2.5V voltage is applied on AVCC and the VDDQ, the source current is lower due to the lower operating voltage applied on the PVCC.

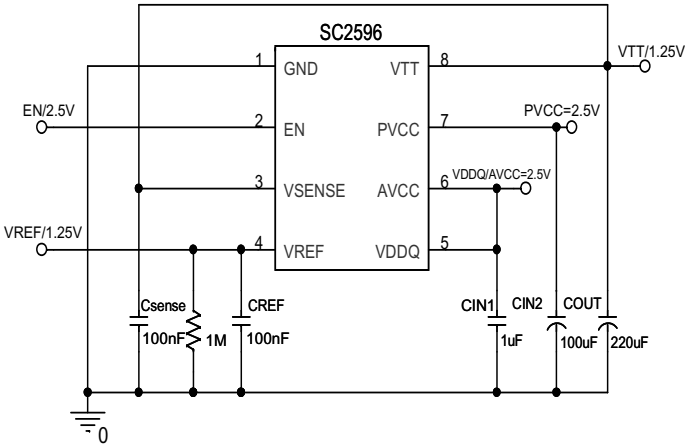



**Figure 2: Lower power loss for SSTL-2(DDR-I).**

### Application_3: Low Power Loss Configuration for SSTL-18(DDR-II)

If power loss is a major concern, setting the PVCC to be 2.5V will be a good choice (Figure 3). The PVCC can operate at lower voltage. if 2.5V voltage is applied on AVCC and PVCC, the source current is lower due to the lower operating voltage applied on the PVCC.

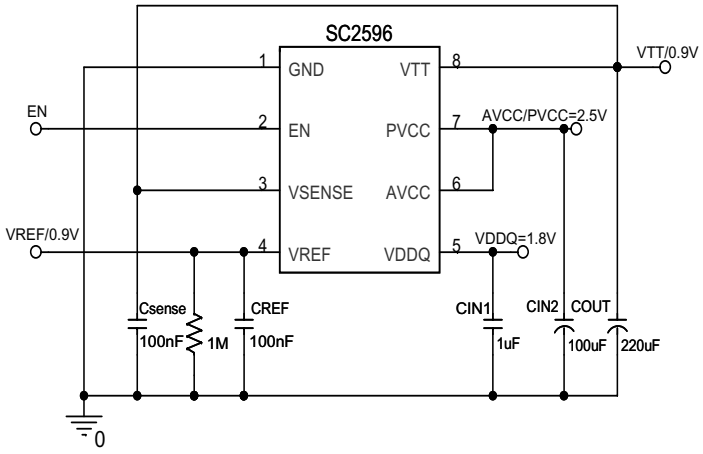



**Figure 3: Lower power loss for SSTL-18(DDR-II).**

### Application_4: High Source Current Configuration

If there is a need for VTT to source more current, especially for DDR-II applications, the system designer can tie the AVCC and PVCC to 3.3V while has the VDDQ tie to 1.8V. This configuration can ensure more than 2A source and sink capability from the VTT rail.

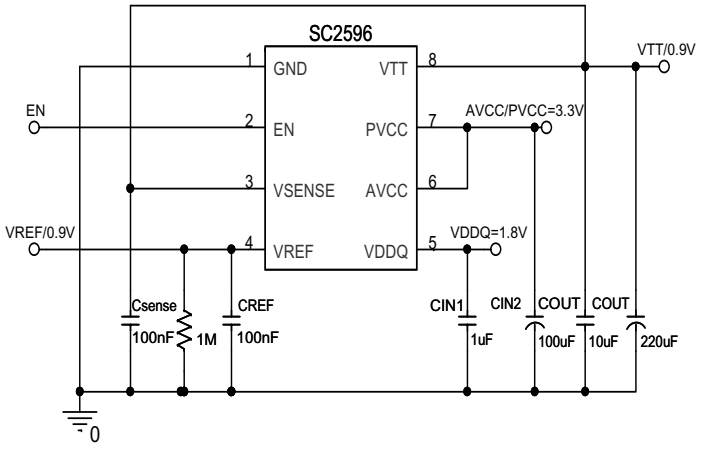



**Figure 4: High current set up for SSTL-18(DDR-II).**

### Application_5: All Ceramic Capacitor Configuration

For some pure ceramic output capacitor designs, one needs to add small ESR in series with the output capacitor in order to enhance stability margin. For example, an 100mohm external ESR is suggested to help improve the phase margin for the circuit in Figure 5. Figure 6 shows the corresponding Bode plot.

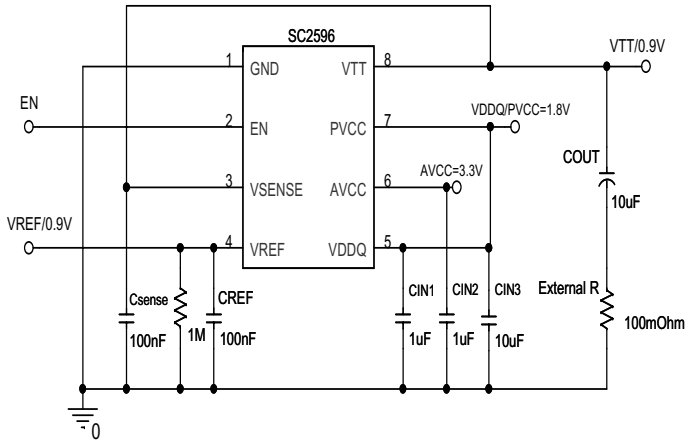



**Figure 5: All ceramic capacitor configuration.**

**Notes:**

(a) The preferred configuration for DDR-I applications is to tie AVCC and PVCC to VDDQ, which is typically 2.5V.

(b) If AVCC and PVCC rails are tied together, then the VDDQ cannot lead the AVCC and PVCC.

**Application_5: Bode Plot of an all ceramic capacitor solution in Figure 5.**

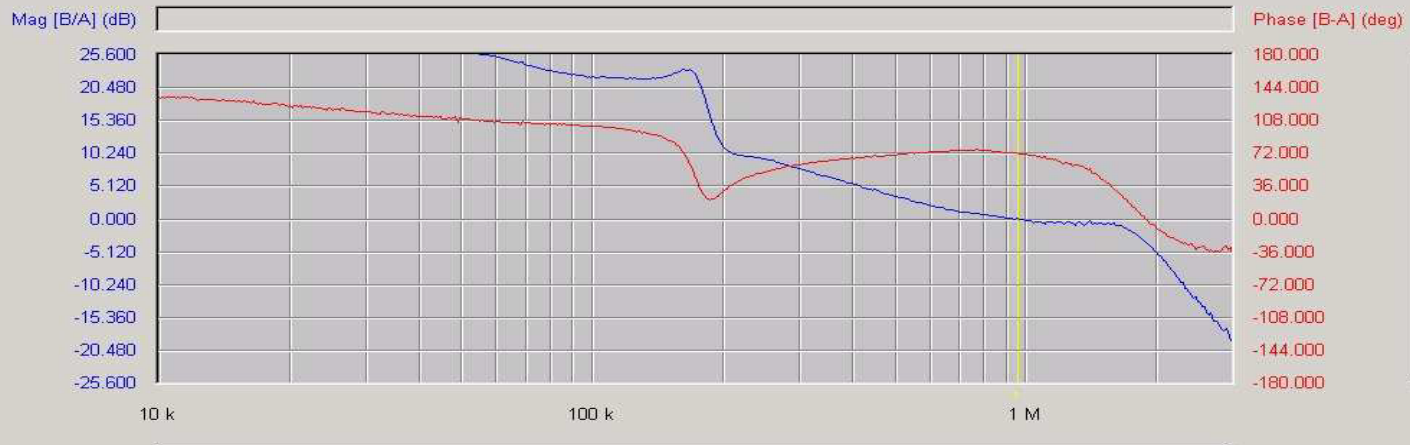



**Figure 6: Bode Plot of an all ceramic capacitor application**

**The phase margin is 72° and the bandwidth is around 1MHz, where: AVCC=3.3V, PVCC=VDDQ=1.8V, VTT=0.9V, IOUT=380mA, COUT=10uF & 100mhom. For this application, we further measured the corresponding phase margins for different output capacitor values and ESR values at designed sourcing and sinking currents in Figure 7.**

**Phase Margin vs External ESR**

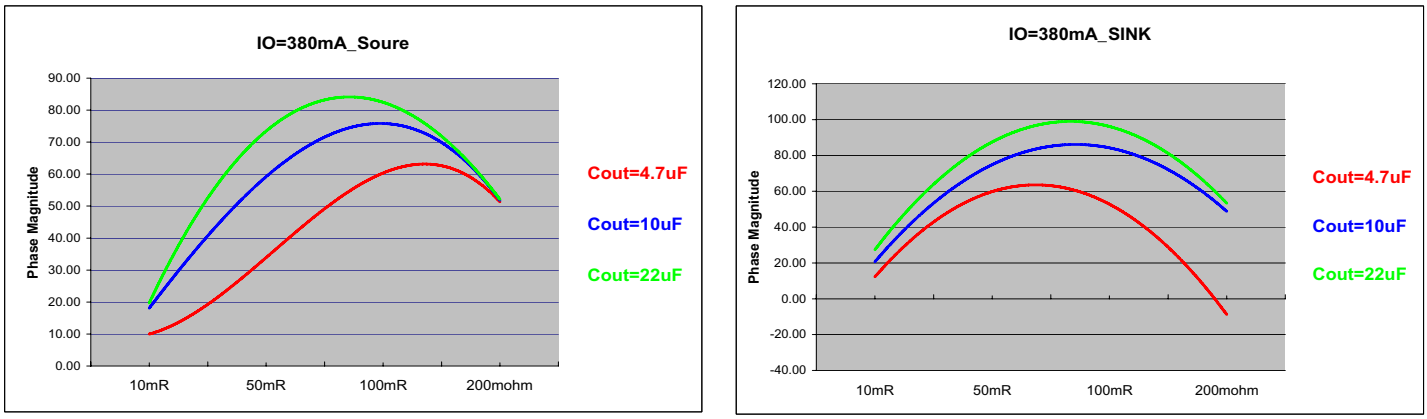
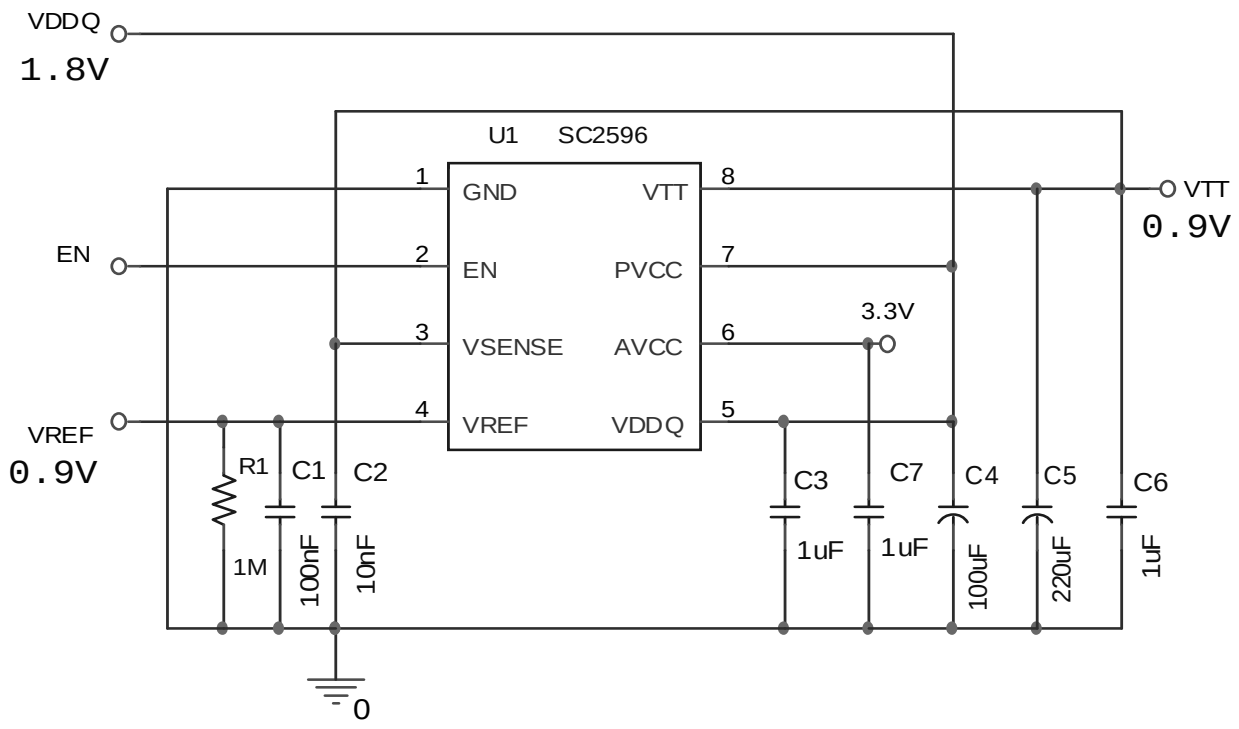



**Figure 7: Phase margin vs external ESR values for different output ceramic capacitor values**

**Layout guidelines**

1) The SOIC8-EDP package of SC2596 can improve the thermal impedance ($\theta_{JC}$) significantly. A suitable thermal pad should be add when PCB layout. Some thermal vias are required to connect the thermal pad to the PCB ground layer. This will improve the thermal performance. Please refer to the recommanded landing pattern.
2) To increase the noise immunity, a ceramic capacitor of 100nF is required to decouple the $V_{REF}$ pin with the shortest connection trace.
3) To reduce the noise on input power rail for standard SSTL-2 application, a 100µF low ESR capacitor and a 1µF ceramic capacitor capacitor have to be used on the input power rail with shortest possible connection.
4) VTT output copper plane should be as large as possible. A 4.7uF to 10µF capacitor have to be used to decouple the VTT pin.
5) The trace between VSENSE pin and VTT rail should be as short as possible and put a 10nF ~100nF capacitor close this vsense pin.

## Typical Application Circuit

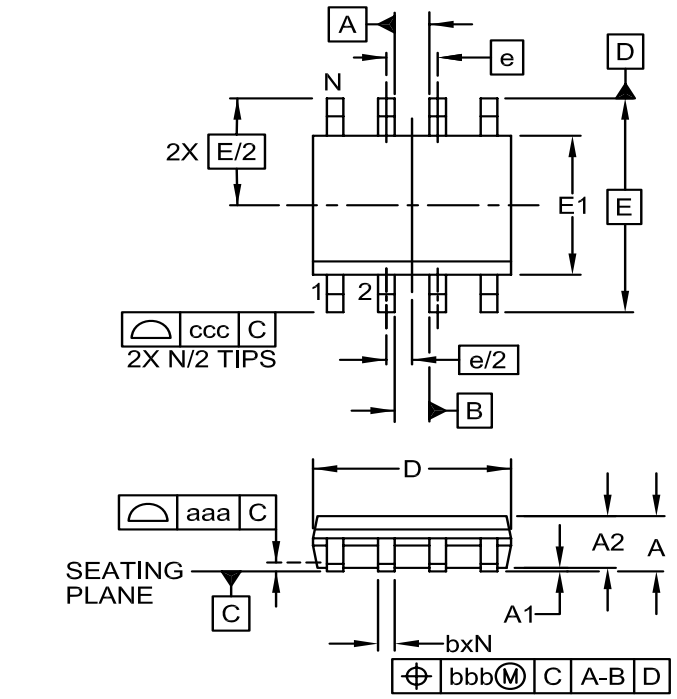



DDR-II VTT Solution

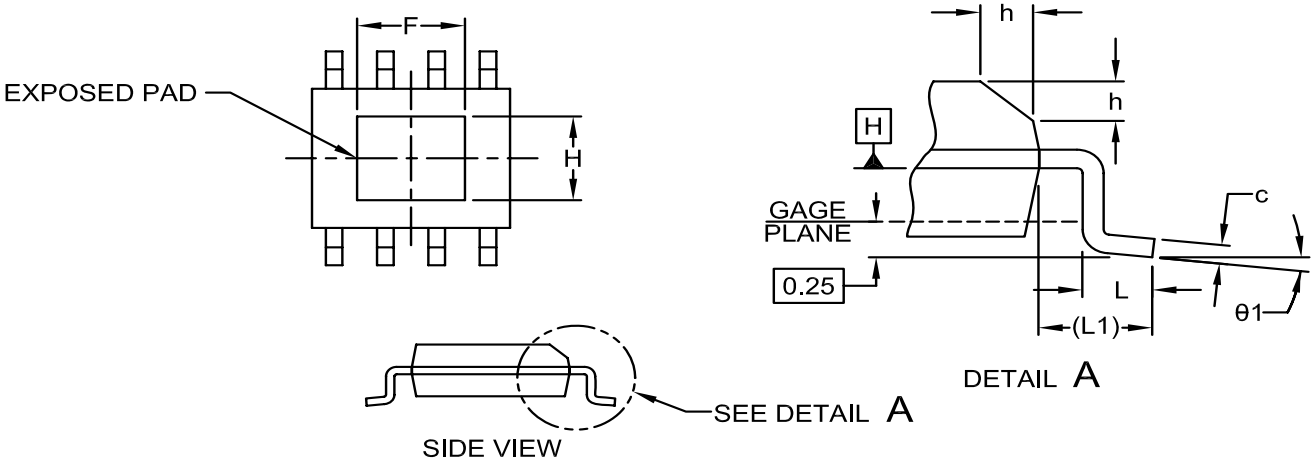
## Bill of Material

| Ref | Qty | Reference | Part Number/Value | Manufacturer |
|---|---|---|---|---|
| 1 | 1 | C1 | 100nF, 25V, X5R,Ceramic, 0603 | Yageo |
| 2 | 1 | C2 | 10nF, 16V, X5R, Ceramic , 0603 | Yageo |
| 3 | 1 | C3 | 1uF, 16V, X5R, Ceramic , 0603 | Yageo |
| 4 | 1 | C6 | 1uF, 16V, X5R, Ceramic , 0603 | Yageo |
| 5 | 1 | C7 | 1uF, 16V, X5R, Ceramic , 0603 | Yageo |
| 6 | 1 | C4 | 100uF, 6.3V, Aluminum | Yageo |
| 7 | 1 | C5 | 220uF, 6.3V, Aluminum | Rubycon |
| 8 | 1 | R1 | 1M OHM | Yageo |
| 9 | 1 | U1 | SC2596 | Semtech |

## Outline Drawing - SOIC8-EDP



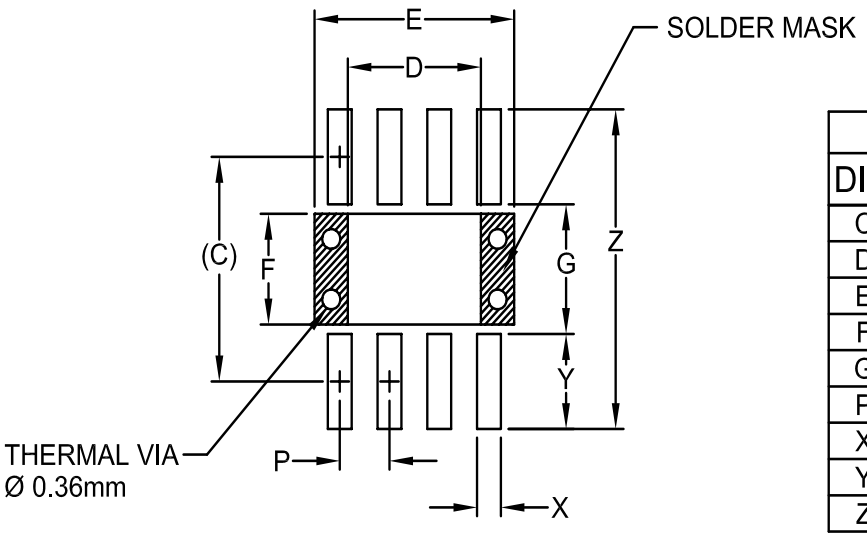

| DIMENSIONS | | | | | | |
|---|---|---|---|---|---|---|
| DIM | INCHES | | | MILLIMETERS | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | .053 | - | .069 | 1.35 | - | 1.75 |
| A1 | .000 | - | .005 | 0.00 | - | 0.13 |
| A2 | .049 | - | .065 | 1.25 | - | 1.65 |
| b | .012 | - | .020 | 0.31 | - | 0.51 |
| c | .007 | - | .010 | 0.17 | - | 0.25 |
| D | .189 | .193 | .197 | 4.80 | 4.90 | 5.00 |
| E1 | .150 | .154 | .157 | 3.80 | 3.90 | 4.00 |
| E | .236 BSC | | | 6.00 BSC | | |
| e | .050 BSC | | | 1.27 BSC | | |
| F | .086 | - | .130 | 2.19 | - | 3.30 |
| H | .085 | - | .099 | 2.15 | - | 2.51 |
| h | .010 | - | .020 | 0.25 | - | 0.50 |
| L | .016 | .028 | .041 | 0.40 | 0.72 | 1.04 |
| L1 | (.041) | | | (1.05) | | |
| N | 8 | | | 8 | | |
| θ1 | 0° | - | 8° | 0° | - | 8° |
| aaa | .004 | | | 0.10 | | |
| bbb | .010 | | | 0.25 | | |
| ccc | .008 | | | 0.20 | | |




NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

## Land Pattern - SOIC8-EDP




| DIMENSIONS | | |
|---|---|---|
| DIM | INCHES | MILLIMETERS |
| C | (.205) | (5.20) |
| D | .134 | 3.40 |
| E | .201 | 5.10 |
| F | .101 | 2.56 |
| G | .118 | 3.00 |
| P | .050 | 1.27 |
| X | .024 | 0.60 |
| Y | .087 | 2.20 |
| Z | .291 | 7.40 |

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. REFERENCE IPC-SM-782A, RLP NO. 300A.
4. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

## Contact Information

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