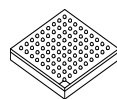
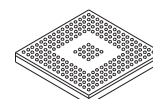




MCF54455



MAPBGA-256
17mm x 17mm



TEPBGA-360
23mm x 23mm

MCF5445x ColdFire Microprocessor Data Sheet

Features

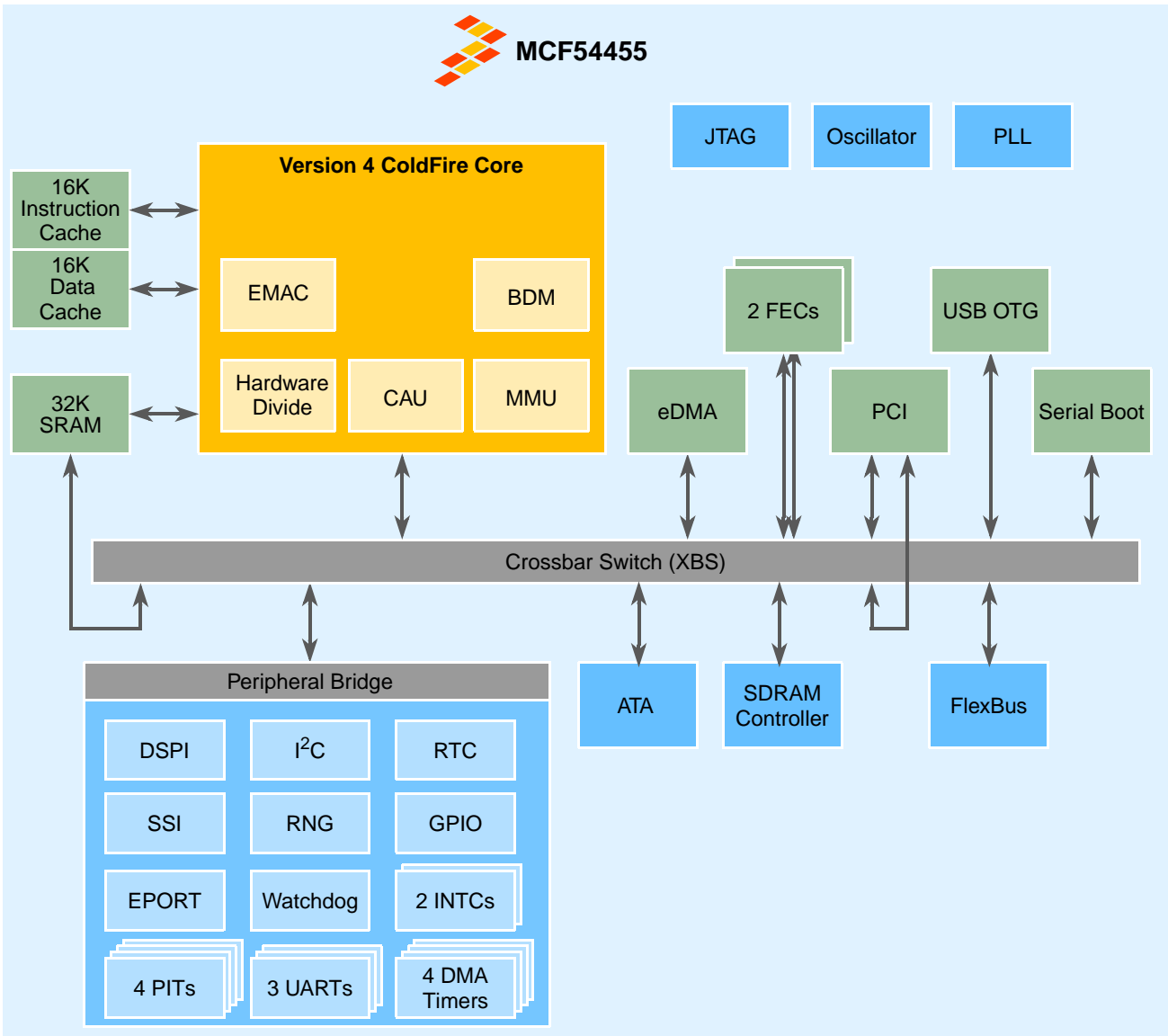
- Version 4 ColdFire Core with MMU and EMAC
- Up to 410 Dhrystone 2.1 MIPS @ 266 MHz
- 16-KBytes instruction cache and 16-KBytes data cache
- 32-KBytes internal SRAM
- Support for booting from SPI-compatible flash, EEPROM, and FRAM devices
- Crossbar switch technology (XBS) for concurrent access to peripherals or RAM from multiple bus masters
- 16-channel DMA controller
- 16-bit 133-MHz DDR/mobile-DDR/DDR2 controller
- USB 2.0 On-the-Go controller with ULPI support
- 32-bit PCI controller @ 66MHz
- ATA/ATAPI controller
- 2 10/100 Ethernet MACs
- Coprocessor for acceleration of the DES, 3DES, AES, MD5, and SHA-1 algorithms
- Random number generator
- Synchronous serial interface (SSI)
- 4 periodic interrupt timers (PIT)
- 4 32-bit timers with DMA support
- DMA-supported serial peripheral interface (DSPI)
- 3 UARTs
- I²C bus interface

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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LEGEND

- | | | | |
|-----------------------|---|----------------|---|
| ATA | – Advanced Technology Attachment Controller | INTC | – Interrupt controller |
| BDM | – Background debug module | JTAG | – Joint Test Action Group interface |
| CAU | – Cryptography acceleration unit | MMU | – Memory management unit |
| DSPI | – DMA serial peripheral interface | PCI | – Peripheral Component Interconnect |
| eDMA | – Enhanced direct memory access | PIT | – Programmable interrupt timers |
| EMAC | – Enhance multiply-accumulate unit | PLL | – Phase locked loop module |
| EPORT | – Edge port module | RNG | – Random Number Generator |
| FEC | – Fast Ethernet controller | RTC | – Real time clock |
| GPIO | – General Purpose Input/Output | SSI | – Synchronous Serial Interface |
| I²C | – Inter-Integrated Circuit | USB OTG | – Universal Serial Bus On-the-Go controller |

Figure 1. MCF54455 Block Diagram

1 MCF5445x Family Comparison

The following table compares the various device derivatives available within the MCF5445x family.

Table 1. MCF5445x Family Configurations

| Module | MCF54450 | MCF54451 | MCF54452 | MCF54453 | MCF54454 | MCF54455 |
|---|----------------|----------|---------------|----------|----------|----------|
| ColdFire Version 4 Core with EMAC (Enhanced Multiply-Accumulate Unit) | • | • | • | • | • | • |
| Core (System) Clock | up to 240 MHz | | up to 266 MHz | | | |
| Peripheral Bus Clock (Core clock ÷ 2) | up to 120 MHz | | up to 133 MHz | | | |
| External Bus Clock (Core clock ÷ 4) | up to 60 MHz | | up to 66 MHz | | | |
| Performance (Dhrystone/2.1 MIPS) | up to 370 | | up to 410 | | | |
| Independent Data/Instruction Cache | 16 Kbytes each | | | | | |
| Static RAM (SRAM) | 32 Kbytes | | | | | |
| PCI Controller | — | — | • | • | • | • |
| Cryptography Acceleration Unit (CAU) | — | • | — | • | — | • |
| ATA Controller | — | — | — | — | • | • |
| DDR SDRAM Controller | • | • | • | • | • | • |
| FlexBus External Interface | • | • | • | • | • | • |
| USB 2.0 On-the-Go | • | • | • | • | • | • |
| UTMI+ Low Pin Interface (ULPI) | • | • | • | • | • | • |
| Synchronous Serial Interface (SSI) | • | • | • | • | • | • |
| Fast Ethernet Controller (FEC) | 1 | 1 | 2 | 2 | 2 | 2 |
| UARTs | 3 | 3 | 3 | 3 | 3 | 3 |
| I ² C | • | • | • | • | • | • |
| DSPI | • | • | • | • | • | • |
| Real Time Clock | • | • | • | • | • | • |
| 32-bit DMA Timers | 4 | 4 | 4 | 4 | 4 | 4 |
| Watchdog Timer (WDT) | • | • | • | • | • | • |
| Periodic Interrupt Timers (PIT) | 4 | 4 | 4 | 4 | 4 | 4 |
| Edge Port Module (EPORT) | • | • | • | • | • | • |
| Interrupt Controllers (INTC) | 2 | 2 | 2 | 2 | 2 | 2 |
| 16-channel Direct Memory Access (DMA) | • | • | • | • | • | • |
| General Purpose I/O (GPIO) | • | • | • | • | • | • |
| JTAG - IEEE [®] 1149.1 Test Access Port | • | • | • | • | • | • |
| Package | 256 MAPBGA | | 360 TEPBGA | | | |

2 Ordering Information

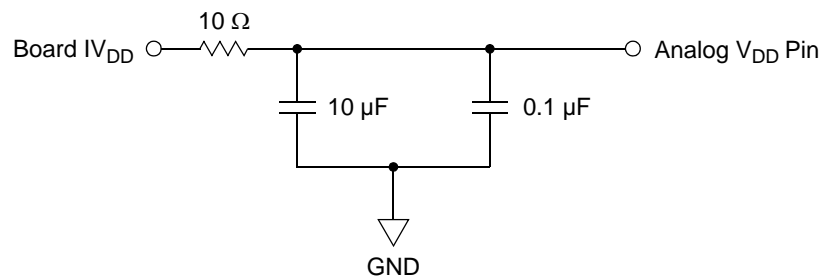
Table 2. Orderable Part Numbers

| Freescle Part Number | Description | Package | Speed | Temperature |
|----------------------|-------------------------|------------|---------|-----------------|
| MCF54450CVM180 | MCF54450 Microprocessor | 256 MAPBGA | 180 MHz | -40° to +85° C |
| MCF54450VM240 | | | 240 MHz | 0° to +70° C |
| MCF54451CVM180 | MCF54451 Microprocessor | | 180 MHz | -40° to +85° C |
| MCF54451VM240 | | | 240 MHz | 0° to +70° C |
| MCF54452CVR200 | MCF54452 Microprocessor | 360 TEPBGA | 200 MHz | -40° to +85° C |
| MCF54452YVR200 | | | 200 MHz | -40° to +105° C |
| MCF54452VR266 | | | 266 MHz | 0° to +70° C |
| MCF54453CVR200 | MCF54453 Microprocessor | | 200 MHz | -40° to +85° C |
| MCF54453VR266 | | | 266 MHz | 0° to +70° C |
| MCF54454CVR200 | MCF54454 Microprocessor | | 200 MHz | -40° to +85° C |
| MCF54454VR266 | | | 266 MHz | 0° to +70° C |
| MCF54455CVR200 | MCF54455 Microprocessor | | 200 MHz | -40° to +85° C |
| MCF54455VR266 | | | 266 MHz | 0° to +70° C |

3 Hardware Design Considerations

3.1 Analog Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for the analog V_{DD} pins ($V_{DD_A_PLL}$, V_{DD_RTC}). The filter shown in Figure 2 should be connected between the board IV_{DD} and the analog pins. The resistor and capacitors should be placed as close to the dedicated analog V_{DD} pin as possible. The 10- Ω resistor in the given filter is required. Do not implement the filter circuit using only capacitors. The analog power pins draw very little current. Concerns regarding voltage loss across the 10-ohm resistor are not valid.


 Figure 2. System Analog V_{DD} Power Filter

3.2 Oscillator Power Filtering

Figure 3 shows an example for isolating the oscillator power supply from the I/O supply (EVDD) and ground.

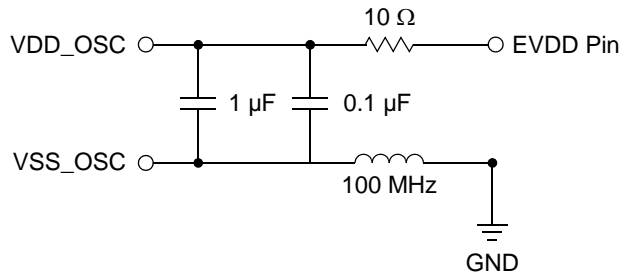
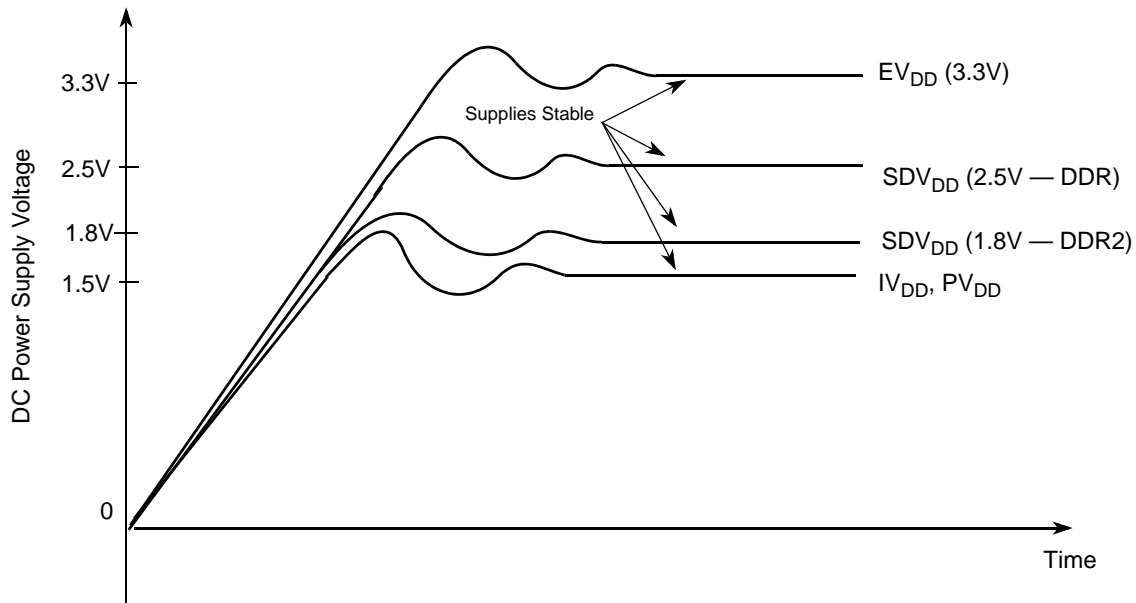


Figure 3. Oscillator Power Filter

3.3 Supply Voltage Sequencing

Figure 4 shows situations in sequencing the I/O V_{DD} (EV_{DD}), SDRAM V_{DD} (SDV_{DD}), PLL V_{DD} (PV_{DD}), and internal logic/core V_{DD} (IV_{DD}).



Notes:

- 1 Input voltage must not be greater than the supply voltage (EV_{DD} , SDV_{DD} , IV_{DD} , or PV_{DD}) by more than 0.5V at any time, including during power-up.
- 2 Use 50 V/millisecond or slower rise time for all supplies.

Figure 4. Supply Voltage Sequencing and Separation Cautions

The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. SDV_{DD} (2.5V or 1.8V) and EV_{DD} are specified relative to IV_{DD} .

3.3.1 Power-Up Sequence

If EV_{DD}/SDV_{DD} are powered up with the IV_{DD} at 0 V, the sense circuits in the I/O pads cause all pad output drivers connected to the EV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SDV_{DD} powers up before IV_{DD} must power up. The rise times on the power supplies should be slower than 50 V/millisecond to avoid turning on the internal ESD protection clamp diodes.

3.3.2 Power-Down Sequence

If IV_{DD}/PV_{DD} are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and PV_{DD} power down before EV_{DD} or SDV_{DD} must power down. There are no requirements for the fall times of the power supplies.

4 Pin Assignments and Reset States

4.1 Signal Multiplexing

The following table lists all the MCF5445x pins grouped by function. The Dir column is the direction for the primary function of the pin only. Refer to [Section 4, “Pin Assignments and Reset States,”](#) for package diagrams. For a more detailed discussion of the MCF5445x signals, consult the *MCF54455 Reference Manual* (MCF54455RM).

NOTE

In this table and throughout this document, a single signal within a group is designated without square brackets (i.e., FB_AD23), while designations for multiple signals within a group use brackets (i.e., FB_AD[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Most pins that are muxed with GPIO default to their GPIO functionality. See [Table 3](#) for a list of the exceptions.

Table 3. Special-Case Default Signal Functionality

| Pin | 256 MAPBGA | 360 TEPBGA |
|-----------------------------|---|------------|
| FB_AD[31:0] | FB_AD[31:0] except when serial boot selects 0-bit boot port size. | |
| FB_BE/BWE[3:0] | $\overline{\text{FB_BE/BWE}}[3:0]$ | |
| FB_CS[3:1] | $\overline{\text{FB_CS}}[3:1]$ | |
| FB_OE | $\overline{\text{FB_OE}}$ | |
| FB_R/ $\overline{\text{W}}$ | FB_R/ $\overline{\text{W}}$ | |
| $\overline{\text{FB_TA}}$ | $\overline{\text{FB_TA}}$ | |
| $\overline{\text{FB_TS}}$ | $\overline{\text{FB_TS}}$ | |

Table 3. Special-Case Default Signal Functionality (continued)

| Pin | 256 MAPBGA | 360 TEPBGA |
|-----------------------------------|------------|---|
| $\overline{\text{PCI_GNT}}[3:0]$ | GPIO | $\overline{\text{PCI_GNT}}[3:0]$ |
| $\overline{\text{PCI_REQ}}[3:0]$ | GPIO | $\overline{\text{PCI_REQ}}[3:0]$ |
| IRQ1 | GPIO | $\overline{\text{PCI_INTA}}$ and configured as an agent. |
| ATA_RESET | GPIO | ATA reset |

Table 4. MCF5445x Signal Information and Muxing

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Pull-up (U) ¹ Pull-down (D) | Direction ² | Voltage Domain | MCF54450 MCF54451 256 MAPBGA | MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA |
|-------------------------------------|---------------------------|--------------|-------------|---|------------------------|----------------|--|--|
| Reset | | | | | | | | |
| $\overline{\text{RESET}}$ | — | — | — | U | I | EVDD | L4 | Y18 |
| $\overline{\text{RSTOUT}}$ | — | — | — | — | O | EVDD | M15 | B17 |
| Clock | | | | | | | | |
| EXTAL/PCI_CLK | — | — | — | — | I | EVDD | M16 | A16 |
| XTAL | — | — | — | U ³ | O | EVDD | L16 | A17 |
| Mode Selection | | | | | | | | |
| BOOTMOD[1:0] | — | — | — | — | I | EVDD | M5, M7 | AB17, AB21 |
| FlexBus | | | | | | | | |
| FB_AD[31:24] | PFBADH[7:0] ⁴ | FB_D[31:24] | — | — | I/O | EVDD | A14, A13, D12, C12, B12, A12, D11, C11 | J2, K4, J1, K1–3, L1, L4 |
| FB_AD[23:16] | PFBADMH[7:0] ⁴ | FB_D[23:16] | — | — | I/O | EVDD | B11, A11, D10, C10, B10, A10, D9, C9 | L2, L3, M1–4, N1–2 |
| FB_AD[15:8] | PFBADML[7:0] ⁴ | FB_D[15:8] | — | — | I/O | EVDD | B9, A9, D8, C8, B8, A8, D7, C7 | P1–2, R1–3, P4, T1–2 |
| FB_AD[7:0] | PFBADL[7:0] ⁴ | FB_D[7:0] | — | — | I/O | EVDD | B7, A7, D6, C6, B6, A6, D5, C5 | T3–4, U1–3, V1–2, W1 |
| $\overline{\text{FB_BE/BWE}}[3:2]$ | PBE[3:2] | FB_TSIZ[1:0] | — | — | O | EVDD | B5, A5 | Y1, W2 |
| $\overline{\text{FB_BE/BWE}}[1:0]$ | PBE[1:0] | — | — | — | O | EVDD | B4, A4 | W3, Y2 |
| FB_CLK | — | — | — | — | O | EVDD | B13 | J3 |
| $\overline{\text{FB_CS}}[3:1]$ | PCS[3:1] | — | — | — | O | EVDD | C2, D4, C3 | W5, AA4, AB3 |
| $\overline{\text{FB_CS0}}$ | — | — | — | — | O | EVDD | C4 | Y4 |
| $\overline{\text{FB_OE}}$ | PFBCTL3 | — | — | — | O | EVDD | A2 | AA1 |
| FB_R $\overline{\text{W}}$ | PFBCTL2 | — | — | — | O | EVDD | B2 | AA3 |
| $\overline{\text{FB_TA}}$ | PFBCTL1 | — | — | U | I | EVDD | B1 | AB2 |

Table 4. MCF5445x Signal Information and Muxing (continued)

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Pull-up (U) ¹ Pull-down (D) | Direction ² | Voltage Domain | MCF54450 MCF54451 256 MAPBGA | MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA |
|---|-----------|--------------------------------|------------------------------|---|------------------------|----------------|--|---|
| $\overline{\text{FB_TS}}$ | PFBCTL0 | FB_ALE | $\overline{\text{FB_TBST}}$ | — | O | EVDD | A3 | Y3 |
| PCI Controller⁵ | | | | | | | | |
| PCI_AD[31:0] | — | FB_A[31:0] | — | — | I/O | EVDD | — | C11, D11, A10, B10, J4, G2, G3, F1, D12, C12, B12, A11, B11, B9, D9, D10, A8, B8, A5, B5, A4, A3, B3, D4, D3, E3–E1, F3, C2, D2, C1 |
| — | — | FB_A[23:0] | — | — | I/O | EVDD | K14–13, J15–13, H13–15, G15–13, F14–13, E15–13, D16, B16, C15, B15, C14, D15, C16, D14 | — |
| $\overline{\text{PCI_CBE}}[3:0]$ | — | — | — | — | I/O | EVDD | — | G4, E4, D1, B1 |
| PCI_DEVSEL | — | — | — | — | O | EVDD | — | F2 |
| $\overline{\text{PCI_FRAME}}$ | — | — | — | — | I/O | EVDD | — | B2 |
| $\overline{\text{PCI_GNT3}}$ | PPCI7 | $\overline{\text{ATA_DMACK}}$ | — | — | O | EVDD | — | B7 |
| $\overline{\text{PCI_GNT}}[2:1]$ | PPCI[6:5] | — | — | — | O | EVDD | — | C8, C9 |
| $\overline{\text{PCI_GNT0}}/$ $\overline{\text{PCI_EXTREQ}}$ | PPCI4 | — | — | — | O | EVDD | — | A9 |
| PCI_IDSEL | — | — | — | — | I | EVDD | — | D5 |
| $\overline{\text{PCI_IRDY}}$ | — | — | — | — | I/O | EVDD | — | C3 |
| PCI_PAR | — | — | — | — | I/O | EVDD | — | C4 |
| $\overline{\text{PCI_PERR}}$ | — | — | — | — | I/O | EVDD | — | B4 |
| $\overline{\text{PCI_REQ3}}$ | PPCI3 | ATA_INTRQ | — | — | I | EVDD | — | C7 |
| $\overline{\text{PCI_REQ}}[2:1]$ | PPCI[2:1] | — | — | — | I | EVDD | — | D7, C5 |
| $\overline{\text{PCI_REQ0}}/$ $\overline{\text{PCI_EXTGNT}}$ | PPCI0 | — | — | — | I | EVDD | — | A2 |
| PCI_RST | — | — | — | — | O | EVDD | — | B6 |
| $\overline{\text{PCI_SERR}}$ | — | — | — | — | I/O | EVDD | — | A6 |
| $\overline{\text{PCI_STOP}}$ | — | — | — | — | I/O | EVDD | — | A7 |
| $\overline{\text{PCI_TRDY}}$ | — | — | — | — | I/O | EVDD | — | C10 |
| SDRAM Controller | | | | | | | | |
| SD_A[13:0] | — | — | — | — | O | SDVDD | R1, P1, N2, P2, R2, T2, M4, N3, P3, R3, T3, T4, R4, N4 | V22, U20–22, T19–22, R20–22, N19, P20–21 |

Table 4. MCF5445x Signal Information and Muxing (continued)

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Pull-up (U) ¹ Pull-down (D) | Direction ² | Voltage Domain | MCF54450 MCF54451 256 MAPBGA | MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA |
|---|-------------|----------------------|----------------|---|------------------------|----------------|---|--|
| SD_BA[1:0] | — | — | — | — | O | SDVDD | P4, T5 | P22, P19 |
| SD_CAS | — | — | — | — | O | SDVDD | T6 | L19 |
| SD_CKE | — | — | — | — | O | SDVDD | N5 | N22 |
| SD_CLK | — | — | — | — | O | SDVDD | T9 | L22 |
| SD_CLK | — | — | — | — | O | SDVDD | T8 | M22 |
| SD_CS[1:0] | — | — | — | — | O | SDVDD | P6, R6 | L20, M20 |
| SD_D[31:16] | — | — | — | — | I/O | SDVDD | N6, T7, N7, P7, R7, R8, P8, N8, N9, T10, R10, P10, N10, T11, R11, P11 | L21, K22, K21, K20, J20, J19, J21, J22, H20, G22, G21, G20, G19, F22, F21, F20 |
| SD_DM[3:2] | — | — | — | — | O | SDVDD | P9, N12 | H21, E21 |
| SD_DQS[3:2] | — | — | — | — | O | SDVDD | R9, N11 | H22, E22 |
| SD_RAS | — | — | — | — | O | SDVDD | P5 | N21 |
| SD_VREF | — | — | — | — | I | SDVDD | M8 | M21 |
| SD_WE | — | — | — | — | O | SDVDD | R5 | N20 |
| External Interrupts Port⁶ | | | | | | | | |
| IRQ7 | PIRQ7 | — | — | — | I | EVDD | L1 | ABB13 |
| IRQ4 | PIRQ4 | — | SSI_CLKIN | — | I | EVDD | L2 | ABB13 |
| IRQ3 | PIRQ3 | — | — | — | I | EVDD | L3 | AB14 |
| IRQ1 | PIRQ1 | PCI_INTA | — | — | I | EVDD | F15 | C6 |
| FEC0 | | | | | | | | |
| FEC0_MDC | PFECI2C3 | — | — | — | O | EVDD | F3 | AB8 |
| FEC0_MDIO | PFECI2C2 | — | — | — | I/O | EVDD | F2 | Y7 |
| FEC0_COL | PFEC0H4 | — | ULPI_DATA7 | — | I | EVDD | E1 | AB7 |
| FEC0_CRS | PFEC0H0 | — | ULPI_DATA6 | — | I | EVDD | F1 | AA7 |
| FEC0_RXCLK | PFEC0H3 | — | ULPI_DATA1 | — | I | EVDD | G1 | AA8 |
| FEC0_RXDV | PFEC0H2 | FEC0_RMII_ CRS_DV | — | — | I | EVDD | G2 | Y8 |
| FEC0_RXD[3:2] | PFEC0L[3:2] | — | ULPI_DATA[5:4] | — | I | EVDD | G3, G4 | AB9, Y9 |
| FEC0_RXD1 | PFEC0L1 | FEC0_RMII_RXD1 | — | — | I | EVDD | H1 | W9 |
| FEC0_RXD0 | PFEC0H1 | FEC0_RMII_RXD0 | — | — | I | EVDD | H2 | AB10 |
| FEC0_RXER | PFEC0L0 | FEC0_RMII_RXER | — | — | I | EVDD | H3 | AA10 |

Table 4. MCF5445x Signal Information and Muxing (continued)

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Pull-up (U) ¹ Pull-down (D) | Direction ² | Voltage Domain | MCF54450 MCF54451 256 MAPBGA | MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA |
|----------------------|-------------|-------------------|----------------|---|------------------------|----------------|------------------------------------|--|
| FEC0_TXCLK | PFEC0H7 | FEC0_RMII_REF_CLK | — | — | I | EVDD | H4 | Y10 |
| FEC0_TXD[3:2] | PFEC0L[7:6] | — | ULPI_DATA[3:2] | — | O | EVDD | J1, J2 | W10, AB11 |
| FEC0_TXD1 | PFEC0L5 | FEC0_RMII_TXD1 | — | — | O | EVDD | J3 | AA11 |
| FEC0_TXD0 | PFEC0H5 | FEC0_RMII_TXD0 | — | — | O | EVDD | J4 | Y11 |
| FEC0_TXEN | PFEC0H6 | FEC0_RMII_TXEN | — | — | O | EVDD | K1 | W11 |
| FEC0_TXER | PFEC0L4 | — | ULPI_DATA0 | — | O | EVDD | K2 | AB12 |
| FEC1 | | | | | | | | |
| FEC1_MDC | PFEC1C5 | — | ATA_DIOR | — | O | EVDD | — | W20 |
| FEC1_MDIO | PFEC1C4 | — | ATA_DIOW | — | I/O | EVDD | — | Y22 |
| FEC1_COL | PFEC1H4 | — | ATA_DATA7 | — | I | EVDD | — | AB18 |
| FEC1_CRS | PFEC1H0 | — | ATA_DATA6 | — | I | EVDD | — | AA18 |
| FEC1_RXCLK | PFEC1H3 | — | ATA_DATA5 | — | I | EVDD | — | W14 |
| FEC1_RXDV | PFEC1H2 | FEC1_RMII_CRS_DV | ATA_DATA15 | — | I | EVDD | — | AB15 |
| FEC1_RXD[3:2] | PFEC1L[3:2] | — | ATA_DATA[4:3] | — | I | EVDD | — | AA15, Y15 |
| FEC1_RXD1 | PFEC1L1 | FEC1_RMII_RXD1 | ATA_DATA14 | — | I | EVDD | — | AA17 |
| FEC1_RXD0 | PFEC1H1 | FEC1_RMII_RXD0 | ATA_DATA13 | — | I | EVDD | — | Y17 |
| FEC1_RXER | PFEC1L0 | FEC1_RMII_RXER | ATA_DATA12 | — | I | EVDD | — | W17 |
| FEC1_TXCLK | PFEC1H7 | FEC1_RMII_REF_CLK | ATA_DATA11 | — | I | EVDD | — | AB19 |
| FEC1_TXD[3:2] | PFEC1L[7:6] | — | ATA_DATA[2:1] | — | O | EVDD | — | Y19, W18 |
| FEC1_TXD1 | PFEC1L5 | FEC1_RMII_TXD1 | ATA_DATA10 | — | O | EVDD | — | AA19 |
| FEC1_TXD0 | PFEC1H5 | FEC1_RMII_TXD0 | ATA_DATA9 | — | O | EVDD | — | Y20 |
| FEC1_TXEN | PFEC1H6 | FEC1_RMII_TXEN | ATA_DATA8 | — | O | EVDD | — | AA21 |
| FEC1_TXER | PFEC1L4 | — | ATA_DATA0 | — | O | EVDD | — | AA22 |
| USB On-the-Go | | | | | | | | |
| USB_DM | — | — | — | — | O | USB VDD | F16 | A14 |
| USB_DP | — | — | — | — | O | USB VDD | E16 | A15 |
| USB_VBUS_EN | PUSB1 | USB_PULLUP | ULPI_NXT | — | O | USB VDD | E5 | AA2 |
| USB_VBUS_OC | PUSB0 | — | ULPI_STP | UD ⁷ | I | USB VDD | B3 | V4 |

Table 4. MCF5445x Signal Information and Muxing (continued)

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Pull-up (U) ¹ Pull-down (D) | Direction ² | Voltage Domain | MCF54450 MCF54451 256 MAPBGA | MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA |
|-------------------------------------|------------|-----------------------------|-------------|---|------------------------|----------------|------------------------------------|--|
| ATA | | | | | | | | |
| ATA_BUFFER_EN | PATAH5 | — | — | — | O | EVDD | — | Y13 |
| $\overline{\text{ATA_CS}}[1:0]$ | PATAH[4:3] | — | — | — | O | EVDD | — | W21, W22 |
| ATA_DA[2:0] | PATAH[2:0] | — | — | — | O | EVDD | — | V19–21 |
| $\overline{\text{ATA_RESET}}$ | PATAL2 | — | — | — | O | EVDD | — | W13 |
| ATA_DMARQ | PATAL1 | — | — | — | I | EVDD | — | AA14 |
| ATA_IORDY | PATAL0 | — | — | — | I | EVDD | — | Y14 |
| Real Time Clock | | | | | | | | |
| EXTAL32K | — | — | — | — | I | EVDD | J16 | A13 |
| XTAL32K | — | — | — | — | O | EVDD | H16 | A12 |
| SSI | | | | | | | | |
| SSI_MCLK | PSSI4 | — | — | — | O | EVDD | T13 | D20 |
| SSI_BCLK | PSSI3 | $\overline{\text{U1CTS}}$ | — | — | I/O | EVDD | R13 | E19 |
| SSI_FS | PSSI2 | $\overline{\text{U1RTS}}$ | — | — | I/O | EVDD | P12 | E20 |
| SSI_RXD | PSSI1 | U1RXD | — | UD | I | EVDD | T12 | D21 |
| SSI_TXD | PSSI0 | U1TXD | — | UD | O | EVDD | R12 | D22 |
| I²C | | | | | | | | |
| I2C_SCL | PFECI2C1 | — | U2TXD | U | I/O | EVDD | K3 | AA12 |
| I2C_SDA | PFECI2C0 | — | U2RXD | U | I/O | EVDD | K4 | Y12 |
| DMA | | | | | | | | |
| $\overline{\text{DACK1}}$ | PDMA3 | — | ULPI_DIR | — | O | EVDD | M14 | C17 |
| $\overline{\text{DREQ1}}$ | PDMA2 | — | USB_CLKIN | U | I | EVDD | P16 | C18 |
| $\overline{\text{DACK0}}$ | PDMA1 | DSPI_PCS3 | — | — | O | EVDD | N15 | A18 |
| $\overline{\text{DREQ0}}$ | PDMA0 | — | — | U | I | EVDD | N16 | B18 |
| DSPI | | | | | | | | |
| DSPI_PCS5/ $\overline{\text{PCS5}}$ | PDSP16 | — | — | — | O | EVDD | N14 | D18 |
| DSPI_PCS2 | PDSP15 | — | — | — | O | EVDD | L13 | A19 |
| DSPI_PCS1 | PDSP14 | $\overline{\text{SBF_CS}}$ | — | — | O | EVDD | P14 | B20 |
| DSPI_PCS0/ $\overline{\text{SS}}$ | PDSP13 | — | — | U | I/O | EVDD | R16 | D17 |
| DSPI_SCK | PDSP12 | SBF_CK | — | — | I/O | EVDD | R15 | A20 |

Table 4. MCF5445x Signal Information and Muxing (continued)

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Pull-up (U) ¹ Pull-down (D) | Direction ² | Voltage Domain | MCF54450 MCF54451 256 MAPBGA | MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA |
|---|---------|-------------------|--------------------|---|------------------------|----------------|------------------------------------|--|
| DSPI_SIN | PDSP11 | SBF_DI | — | 8 | I | EVDD | P15 | B19 |
| DSPI_SOUT | PDSP10 | SBF_DO | — | — | O | EVDD | N13 | C20 |
| UARTs | | | | | | | | |
| $\overline{U1CTS}$ | PUART7 | — | — | — | I | EVDD | — | V3 |
| $\overline{U1RTS}$ | PUART6 | — | — | — | O | EVDD | — | U4 |
| U1RXD | PUART5 | — | — | — | I | EVDD | — | P3 |
| U1TXD | PUART4 | — | — | — | O | EVDD | — | N3 |
| $\overline{U0CTS}$ | PUART3 | — | — | — | I | EVDD | M3 | Y16 |
| $\overline{U0RTS}$ | PUART2 | — | — | — | O | EVDD | M2 | AA16 |
| U0RXD | PUART1 | — | — | — | I | EVDD | N1 | AB16 |
| U0TXD | PUART0 | — | — | — | O | EVDD | M1 | W15 |
| Note: The UART1 and UART 2 signals are multiplexed on the DMA timers and I2C pins. | | | | | | | | |
| DMA Timers | | | | | | | | |
| DT3IN | PTIMER3 | DT3OUT | U2RXD | — | I | EVDD | C13 | H2 |
| DT2IN | PTIMER2 | DT2OUT | U2TXD | — | I | EVDD | D13 | H1 |
| DT1IN | PTIMER1 | DT1OUT | $\overline{U2CTS}$ | — | I | EVDD | B14 | H3 |
| DT0IN | PTIMER0 | DT0OUT | $\overline{U2RTS}$ | — | I | EVDD | A15 | G1 |
| BDM/JTAG⁹ | | | | | | | | |
| PSTDDATA[7:0] | — | — | — | — | O | EVDD | E2, D1, F4, E3, D2, C1, E4, D3 | AA6, AB6, AB5, W6, Y6, AA5, AB4, Y5 |
| JTAG_EN | — | — | — | D | I | EVDD | M11 | C21 |
| PSTCLK | — | TCLK | — | — | I | EVDD | P13 | C22 |
| DSI | — | TDI | — | U | I | EVDD | T15 | C19 |
| DSO | — | TDO | — | — | O | EVDD | T14 | A21 |
| \overline{BKPT} | — | TMS | — | U | I | EVDD | R14 | B21 |
| DSCLK | — | \overline{TRST} | — | U | I | EVDD | M13 | B22 |
| Test | | | | | | | | |
| TEST | — | — | — | D | I | EVDD | M6 | AB20 |
| PLLTEST | — | — | — | — | O | EVDD | K16 | D15 |

Table 4. MCF5445x Signal Information and Muxing (continued)

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Pull-up (U) ¹ Pull-down (D) | Direction ² | Voltage Domain | MCF54450 MCF54451 256 MAPBGA | MCF54452 MCF54453 MCF54454 MCF54455 360 TEPBGA |
|-----------------------|------|-------------|-------------|---|------------------------|----------------|---|---|
| Power Supplies | | | | | | | | |
| IVDD | — | — | — | — | — | — | E6–12, F5, F12 | D6, D8, D14, F4, H4, N4, R4, W4, W7, W8, W12, W16, W19 |
| EVDD | — | — | — | — | — | — | G5, G12, H5, H12, J5, J12, K5, K12, L5–6, L12 | D13, D19, G8, G11, G14, G16, J7, J16, L7, L16, N16, P7, R16, T8, T12, T14, T16 |
| SD_VDD | — | — | — | — | — | — | L7–11, M9, M10 | F19, H19, K19, M19, R19, U19 |
| VDD_OSC | — | — | — | — | — | — | L14 | B16 |
| VDD_A_PLL | — | — | — | — | — | — | K15 | C14 |
| VDD_RTC | — | — | — | — | — | — | M12 | C13 |
| VSS | — | — | — | — | — | — | A1, A16, F6–11, G6–11, H6–11, J6–11, K6–11, T1, T16 | A1, A22, B14, G7, G9–10, G12–13, G15, H7, H16, J9–14, K7, K9–14, K16, L9–14, M7, M9–M14, M16, N7, N9–14, P9–14, P16, R7, T7, T9–11, T13, T15, AB1, AB22 |
| VSS_OSC | — | — | — | — | — | — | L15 | C16 |

¹ Pull-ups are generally only enabled on pins with their primary function, except as noted.

² Refers to pin's primary function.

³ Enabled only in oscillator bypass mode (internal crystal oscillator is disabled).

⁴ Serial boot must select 0-bit boot port size to enable the GPIO mode on these pins.

⁵ When the PCI is enabled, all PCI bus pins come up configured as such. This includes the PCI_GNT and PCI_REQ lines, which have GPIO. The IRQ1/ $\overline{\text{PCI_INTA}}$ signal is a special case. It comes up as $\overline{\text{PCI_INTA}}$ when booting as a PCI agent and as GPIO when booting as a PCI host.

For the 360 TEPBGA, booting with PCI disabled results in all dedicated PCI pins being safe-stated. The $\overline{\text{PCI_GNT}}$ and $\overline{\text{PCI_REQ}}$ lines and IRQ1/ $\overline{\text{PCI_INTA}}$ come up as GPIO.

⁶ GPIO functionality is determined by the edge port module. The pin multiplexing and control module is only responsible for assigning the alternate functions.

⁷ Depends on programmed polarity of the USB_VBUS_OC signal.

⁸ Pull-up when the serial boot facility (SBF) controls the pin

⁹ If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The pin multiplexing and control module is not responsible for assigning these pins.

4.2 Pinout—256 MAPBGA

The pinout for the MCF54450 and MCF54451 packages are shown below.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | | |
|---|------------|------------|-------------|------------|-------------|---------|-----------|----------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|--------|---|
| A | VSS | FB_OE | FB_TS | FB_BE/BWE0 | FB_BE/BWE2 | FB_AD 2 | FB_AD 6 | FB_AD 10 | FB_AD 14 | FB_AD 18 | FB_AD 22 | FB_AD 26 | FB_AD 30 | FB_AD 31 | T0IN | VSS | A | |
| B | FB_TA | FB_R/W | USB_VBUS_OC | FB_BE/BWE1 | FB_BE/BWE3 | FB_AD 3 | FB_AD 7 | FB_AD 11 | FB_AD 15 | FB_AD 19 | FB_AD 23 | FB_AD 27 | FB_CLK | T1IN | FB_A 4 | FB_A 6 | B | |
| C | PST_DDATA2 | FB_CS3 | FB_CS1 | FB_CS0 | FB_AD 0 | FB_AD 4 | FB_AD 8 | FB_AD 12 | FB_AD 16 | FB_AD 20 | FB_AD 24 | FB_AD 28 | T3IN | FB_A 3 | FB_A 5 | FB_A 1 | C | |
| D | PST_DDATA6 | PST_DDATA3 | PST_DDATA0 | FB_CS2 | FB_AD 1 | FB_AD 5 | FB_AD 9 | FB_AD 13 | FB_AD 17 | FB_AD 21 | FB_AD 25 | FB_AD 29 | T2IN | FB_A 0 | FB_A 2 | FB_A 7 | D | |
| E | FEC0_COL | PST_DDATA7 | PST_DDATA4 | PST_DDATA1 | USB_VBUS_EN | IVDD | IVDD | IVDD | IVDD | IVDD | IVDD | IVDD | IVDD | FB_A 8 | FB_A 9 | FB_A 10 | USB_DP | E |
| F | FEC0_CRS | FEC0_MDIO | FEC0_MDC | PST_DDATA5 | IVDD | VSS | VSS | VSS | VSS | VSS | VSS | IVDD | FB_A 11 | FB_A 12 | IRQ_1 | USB_DM | F | |
| G | FEC0_RXCLK | FEC0_RXDV | FEC0_RXD3 | FEC0_RXD2 | EVDD | VSS | VSS | VSS | VSS | VSS | VSS | EVDD | FB_A 13 | FB_A 14 | FB_A 15 | NC | G | |
| H | FEC0_RXD1 | FEC0_RXD0 | FEC0_RXER | FEC0_TXCLK | EVDD | VSS | VSS | VSS | VSS | VSS | VSS | EVDD | FB_A 18 | FB_A 17 | FB_A 16 | XTAL 32K | H | |
| J | FEC0_TXD3 | FEC0_TXD2 | FEC0_TXD1 | FEC0_TXD0 | EVDD | VSS | VSS | VSS | VSS | VSS | VSS | EVDD | FB_A 19 | FB_A 20 | FB_A 21 | EXTAL 32K | J | |
| K | FEC0_TXEN | FEC0_TXER | I2C_SCL | I2C_SDA | EVDD | VSS | VSS | VSS | VSS | VSS | VSS | EVDD | FB_A 22 | FB_A 23 | VDD_A_PLL | PLL TEST | K | |
| L | IRQ_7 | IRQ_4 | IRQ_3 | RESET | EVDD | EVDD | SDVDD | SDVDD | SDVDD | SDVDD | SDVDD | EVDD | DSPI_PCS2 | VDD_OSC | VSS_OSC | XTAL | L | |
| M | U0TXD | U0RTS | U0CTS | SD_A7 | BOOT_MOD1 | TEST | BOOT_MOD0 | SD_VREF | SDVDD | SDVDD | JTAG_EN | VDD_RTC | TRST | DACK1 | RST_OUT | EXTAL | M | |
| N | U0RXD | SD_A11 | SD_A6 | SD_A0 | SD_CKE | SD_D31 | SD_D29 | SD_D24 | SD_D23 | SD_D19 | SD_DQS2 | SD_DM2 | DSPI_SOUT | DSPI_PCS5 | DACK0 | DREQ0 | N | |
| P | SD_A12 | SD_A10 | SD_A5 | SD_BA1 | SD_RAS | SD_CS1 | SD_D28 | SD_D25 | SD_DM3 | SD_D20 | SD_D16 | SSI_FS | TCLK | DSPI_PCS1 | DSPI_SIN | DREQ1 | P | |
| R | SD_A13 | SD_A9 | SD_A4 | SD_A1 | SD_WE | SD_CS0 | SD_D27 | SD_D26 | SD_DQS3 | SD_D21 | SD_D17 | SSI_TXD | SSI_BCLK | TMS | DSPI_SCK | DSPI_PCS0 | R | |
| T | VSS | SD_A8 | SD_A3 | SD_A2 | SD_BA0 | SD_CAS | SD_D30 | SD_CLK | SD_CLK | SD_D22 | SD_D18 | SSI_RXD | SSI_MCLK | TDO | TDI | VSS | T | |

Figure 5. MCF54450 and MCF54451 Pinout (256 MAPBGA)

4.3 Pinout—360 TEPBGA

The pinout for the MCF54452, MCF54453, MCF54454, and MCF54455 packages are shown below.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | | |
|----|------------|-------------|------------|-------------|------------|------------|-----------|------------|-----------|------------|-----------|-----------|---------------|------------|-----------|---------|-----------|-----------|------------|-----------|-----------|-----------|---------|---|
| A | GND | PCI_REQ0 | PCI_AD10 | PCI_AD11 | PCI_AD13 | PCI_SERR | PCI_STOP | PCI_AD15 | PCI_GNT0 | PCI_AD20 | XTAL_32K | EXTAL_32K | USB_DM | USB_DP | EXTAL | XTAL | DACK0 | DSPL_PCS2 | DSPL_SCK | TDO | GND | A | | |
| B | PCI_CBE0 | PCI_FRAME | PCI_AD9 | PCI_PERR | PCI_AD12 | PCI_RST | PCI_GNT3 | PCI_AD14 | PCI_AD18 | PCI_AD28 | PCI_AD19 | PCI_AD21 | NC | GND | NC | VDD_OSC | RST_OUT | DREQ0 | DSPL_SIN | DSPL_PCS1 | TMS | TRST | B | |
| C | PCI_AD0 | PCI_AD2 | PCI_IRDY | PCI_PAR | PCI_REQ1 | IRQT | PCI_REQ3 | PCI_GNT2 | PCI_GNT1 | PCI_TRDY | PCI_AD31 | PCI_AD22 | VDD_RTC | VDD_A_PLL | NC | VSS_OSC | DACK1 | DREQ1 | TDI | DSPL_SOUT | JTAG_EN | TCLK | C | |
| D | PCI_CBE1 | PCI_AD1 | PCI_AD7 | PCI_AD8 | PCI_IDSEL | IVDD | PCI_REQ2 | IVDD | PCI_AD17 | PCI_AD16 | PCI_AD30 | PCI_AD23 | EVDD | IVDD | PLL_TEST | NC | DSPL_PCS0 | DSPL_PCS5 | EVDD | SSL_MCLK | SSL_RXD | SSL_TXD | D | |
| E | PCI_AD4 | PCI_AD5 | PCI_AD6 | PCI_CBE2 | | | | | | | | | | | | | | | SSL_BCLK | SSL_FS | SD_DM2 | SD_DQS2 | E | |
| F | PCI_AD24 | PCI_DE_VSEL | PCI_AD3 | IVDD | | | | | | | | | | | | | | | SDVDD | SD_D16 | SD_D17 | SD_D18 | F | |
| G | T0IN | PCI_AD26 | PCI_AD25 | PCI_CBE3 | | | | | | | | | | | | | | | | SD_D19 | SD_D20 | SD_D21 | SD_D22 | G |
| H | T2IN | T3IN | T1IN | IVDD | | | | | | | | | | | | | | | | SDVDD | SD_D23 | SD_DM3 | SD_DQS3 | H |
| J | FB_AD_29 | FB_AD_31 | FB_CLK | PCI_AD27 | | | | | | | | | | | | | | | | SD_D26 | SD_D27 | SD_D25 | SD_D24 | J |
| K | FB_AD_28 | FB_AD_27 | FB_AD_26 | FB_AD_30 | | | | | | | | | | | | | | | | SDVDD | SD_D28 | SD_D29 | SD_D30 | K |
| L | FB_AD_25 | FB_AD_23 | FB_AD_22 | FB_AD_24 | | | | | | | | | | | | | | | | SD_CAS | SD_CST | SD_D31 | SD_CLK | L |
| M | FB_AD_21 | FB_AD_20 | FB_AD_19 | FB_AD_18 | | | | | | | | | | | | | | | | SDVDD | SD_CS0 | SD_VREF | SD_CLK | M |
| N | FB_AD_17 | FB_AD_16 | U1TXD | IVDD | | | | | | | | | | | | | | | | SD_A2 | SD_WE | SD_RAS | SD_CKE | N |
| P | FB_AD_15 | FB_AD_14 | U1RXD | FB_AD_10 | | | | | | | | | | | | | | | | SD_BA0 | SD_A1 | SD_A0 | SD_BA1 | P |
| R | FB_AD_13 | FB_AD_12 | FB_AD_11 | IVDD | | | | | | | | | | | | | | | | SDVDD | SD_A5 | SD_A4 | SD_A3 | R |
| T | FB_AD_9 | FB_AD_8 | FB_AD_7 | FB_AD_6 | | | | | | | | | | | | | | | | SD_A9 | SD_A8 | SD_A7 | SD_A6 | T |
| U | FB_AD_5 | FB_AD_4 | FB_AD_3 | U1RTS | | | | | | | | | | | | | | | | SDVDD | SD_A12 | SD_A11 | SD_A10 | U |
| V | FB_AD_2 | FB_AD_1 | U1CTS | USB_VBUS_OC | | | | | | | | | | | | | | | | ATA_DA2 | ATA_DA1 | ATA_DA0 | SD_A13 | V |
| W | FB_AD_0 | FB_BE/BWE2 | FB_BE/BWE1 | IVDD | FB_CS3 | PST_DDATA4 | IVDD | IVDD | FEC0_RXD1 | FEC0_TXD3 | FEC0_TXEN | IVDD | ATA_RESET | FEC1_RXCLK | U0TXD | IVDD | FEC1_RXER | FEC1_TXD2 | IVDD | FEC1_MDC | ATA_CS1 | ATA_CS0 | W | |
| Y | FB_BE/BWE3 | FB_BE/BWE0 | FB_TS | FB_CS0 | PST_DDATA0 | PST_DDATA3 | FEC0_MDIO | FEC0_RXDV | FEC0_RXD2 | FEC0_TXCLK | FEC0_TXD0 | I2C_SDA | ATA_BUFFER_EN | ATA_IORDY | FEC1_RXD2 | U0CTS | FEC1_RXD0 | RESET | FEC1_TXD3 | FEC1_TXD0 | NC | FEC1_MDIO | Y | |
| AA | FB_OE | USB_VBUS_EN | FB_RW | FB_CS2 | PST_DDATA2 | PST_DDATA7 | FEC0_CRS | FEC0_RXCLK | NC | FEC0_RXER | FEC0_TXD1 | I2C_SCL | IRQ4 | ATA_DMARQ | FEC1_RXD3 | U0RTS | FEC1_RXD1 | FEC1_CRS | FEC1_TXD1 | NC | FEC1_TXEN | FEC1_TXER | AA | |
| AB | GND | FB_TA | FB_CS1 | PST_DDATA1 | PST_DDATA5 | PST_DDATA6 | FEC0_COL | FEC0_MDC | FEC0_RXD3 | FEC0_RXD0 | FEC0_TXD2 | FEC0_TXER | IRQ7 | IRQ3 | FEC1_RXDV | U0RXD | BOOT_MOD1 | FEC1_COL | FEC1_TXCLK | TEST | BOOT_MOD0 | GND | AB | |

Figure 6. MCF54452, MCF54453, MCF54454, and MCF54455 Pinout (360 TEPBGA)

5 Electrical Characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF54455 microprocessor. This section contains detailed information on DC/AC electrical characteristics and AC timing specifications.

The electrical specifications are preliminary and from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. However, for production silicon, these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this MCU document supersede any values found in the module specifications.

5.1 Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings^{1, 2}

| Rating | Symbol | Pin Name | Value | Units |
|--|--------------------------|-----------|--------------|-------|
| External I/O pad supply voltage | EV_{DD} | EVDD | -0.3 to +4.0 | V |
| Internal oscillator supply voltage | $OSCV_{DD}$ | VDD_OSC | -0.3 to +4.0 | V |
| Real-time clock supply voltage | $RTCV_{DD}$ | VDD_RTC | -0.5 to +2.0 | V |
| Internal logic supply voltage | IV_{DD} | IVDD | -0.5 to +2.0 | V |
| SDRAM I/O pad supply voltage | SDV_{DD} | SD_VDD | -0.3 to +4.0 | V |
| PLL supply voltage | PV_{DD} | VDD_A_PLL | -0.5 to +2.0 | V |
| Digital input voltage ³ | V_{IN} | — | -0.3 to +3.6 | V |
| Instantaneous maximum current Single pin limit (applies to all pins) ^{3, 4, 5} | I_{DD} | — | 25 | mA |
| Operating temperature range (packaged) | T_A ($T_L - T_H$) | — | -40 to +85 | °C |
| Storage temperature range | T_{stg} | — | -55 to +150 | °C |

¹ Functional operating conditions are given in Table 8. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

² This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., V_{SS} or EV_{DD}).

³ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, and then use the larger of the two values.

⁴ All functional non-supply pins are internally clamped to V_{SS} and EV_{DD} .

⁵ Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > EV_{DD}$) is greater than I_{DD} , the injection current may flow out of EV_{DD} and could result in external power supply going out of regulation. Ensure the external EV_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MPU is not consuming power (ex; no clock). The power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions.

5.2 Thermal Characteristics

Table 6. Thermal Characteristics

| Characteristic | | Symbol | 256 MAPBGA | 360 TEPBGA | Unit |
|---|-------------------------|----------------|-------------------|-------------------|------|
| Junction to ambient, natural convection | Four layer board (2s2p) | θ_{JA} | 29 ^{1,2} | 24 ^{1,2} | °C/W |
| Junction to ambient (@200 ft/min) | Four layer board (2s2p) | θ_{JMA} | 25 ^{1,2} | 21 ^{1,2} | °C/W |
| Junction to board | | θ_{JB} | 18 ³ | 15 ³ | °C/W |
| Junction to case | | θ_{JC} | 10 ⁴ | 11 ⁴ | °C/W |
| Junction to top of package | | Ψ_{jt} | 2 ^{1,5} | 2 ^{1,5} | °C/W |
| Maximum operating junction temperature | | T_j | 105 | 105 | °C |

¹ θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JMA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

² Per JEDEC JESD51-6 with the board horizontal.

³ Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁴ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

⁵ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_j) in °C can be obtained from:

$$T_j = T_A + (P_D \times \theta_{JMA}) \tag{Eqn. 1}$$

Where:

- T_A = Ambient Temperature, °C
- θ_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
- P_D = $P_{INT} + P_{I/O}$
- P_{INT} = $I_{DD} \times V_{DD}$, Watts - Chip Internal Power
- $P_{I/O}$ = Power Dissipation on Input and Output Pins - User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_j (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_j + 273^\circ C)} \tag{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273^\circ C) + \theta_{JMA} \times P_D^2 \tag{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K , the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A .

5.3 ESD Protection

Table 7. ESD Protection Characteristics^{1, 2}

| Characteristics | Symbol | Value | Units |
|---------------------------------|--------|-------|-------|
| ESD Target for Human Body Model | HBM | 2000 | V |

¹ All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

² A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 8. DC Electrical Specifications

| Characteristic | Symbol | Min | Max | Units |
|---|-------------|------------------------|------------------------|---------|
| Internal logic supply voltage ¹ | V_{DD} | 1.35 | 1.65 | V |
| PLL analog operation voltage range ¹ | PV_{DD} | 1.35 | 1.65 | V |
| External I/O pad supply voltage | EV_{DD} | 3.0 | 3.6 | V |
| Internal oscillator supply voltage | $OSCV_{DD}$ | 3.0 | 3.6 | V |
| Real-time clock supply voltage | $RTCV_{DD}$ | 1.35 | 1.65 | V |
| SDRAM I/O pad supply voltage — DDR mode | SDV_{DD} | 2.25 | 2.75 | V |
| SDRAM I/O pad supply voltage — DDR2 mode | SDV_{DD} | 1.7 | 1.9 | V |
| SDRAM I/O pad supply voltage — Mobile DDR mode | SDV_{DD} | 1.7 | 1.9 | V |
| SDRAM input reference voltage | SDV_{REF} | $0.49 \times SDV_{DD}$ | $0.51 \times SDV_{DD}$ | V |
| Input High Voltage | V_{IH} | $0.7 \times EV_{DD}$ | 3.65 | V |
| Input Low Voltage | V_{IL} | $V_{SS} - 0.3$ | $0.35 \times EV_{DD}$ | V |
| Input Hysteresis | V_{HYS} | $0.06 \times EV_{DD}$ | — | mV |
| Input Leakage Current ² $V_{in} = V_{DD}$ or V_{SS} , Input-only pins | I_{in} | -2.5 | 2.5 | μA |
| Input Leakage Current ³ $V_{in} = V_{DD}$ or V_{SS} , Input-only pins | I_{in} | -5 | 5 | μA |
| High Impedance (Off-State) Leakage Current ⁴ $V_{in} = V_{DD}$ or V_{SS} , All input/output and output pins | I_{OZ} | -10.0 | 10.0 | μA |
| Output High Voltage (All input/output and all output pins) $I_{OH} = -5.0$ mA | V_{OH} | $0.85 \times EV_{DD}$ | — | V |
| Output Low Voltage (All input/output and all output pins) $I_{OL} = 5.0$ mA | V_{OL} | — | $0.15 \times EV_{DD}$ | V |

Table 8. DC Electrical Specifications

| Characteristic | Symbol | Min | Max | Units |
|---|-----------|-------------|-----------|---------|
| Weak Internal Pull Up Device Current, tested at V_{IL} Max. ⁵ | I_{APU} | -10 | -130 | μA |
| Input Capacitance ⁶ All input-only pins All input/output (three-state) pins | C_{in} | — — | 7 7 | pF |
| Load Capacitance Low drive strength High drive strength | C_L | | 25 50 | pF |
| DC Injection Current ^{3, 7, 8, 9} $V_{NEGCLAMP} = V_{SS} - 0.3 V$, $V_{POSCLAMP} = V_{DD} + 0.3$ Single Pin Limit Total MCU Limit, Includes sum of all stressed pins | I_{IC} | -1.0 -10 | 1.0 10 | mA |

¹ $I_{V_{DD}}$ and PV_{DD} should be at the same voltage. PV_{DD} should have a filtered input. Please see the PLL section of this specification for an example circuit. There are three PV_{DD} inputs, one for each PLL. A filter circuit should be used on each PV_{DD} input.

² Valid for all parts, EXCEPT the MCF54452YVR200.

³ Valid just the MCF54452YVR200 part number.

⁴ Worst-case tristate leakage current with only one I/O pin high. Since all I/Os share power when high, the leakage current is distributed among them. With all I/Os high, this spec reduces to $\pm 2 \mu A$ min/max.

⁵ Refer to the *MCF54455 Reference Manual* signals description chapter for pins having weak internal pull-up devices.

⁶ This parameter is characterized before qualification rather than 100% tested.

⁷ All functional non-supply pins are internally clamped to V_{SS} and their respective V_{DD} .

⁸ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁹ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure the external V_{DD} load shunts current greater than the maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, at power-up, the system clock is not present during the power-up sequence until the PLL has attained lock.

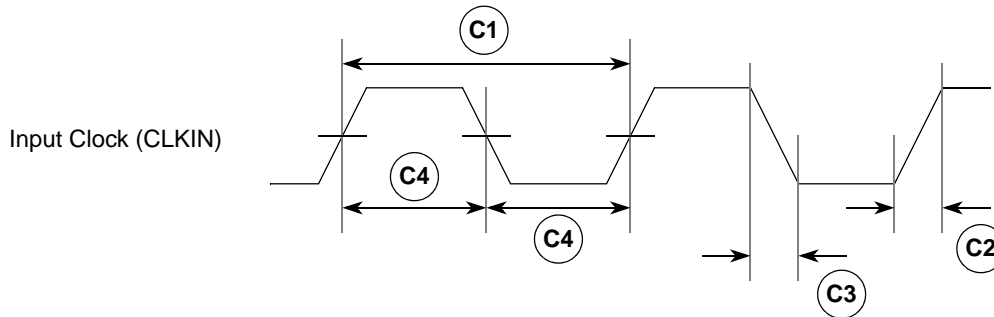
5.5 Clock Timing Specifications

The clock module configures the device for one of several clocking methods. Clocking modes include internal phase-locked loop (PLL) clocking with an external clock reference or an external crystal reference supported by an internal crystal amplifier. The PLL can also be disabled, and an external oscillator can directly clock the device.

The specifications in [Table 9](#) are for the CLKIN input pin (EXTAL input driven by an external clock reference). The duty cycle specification is based on an acceptable tolerance for the PLL, which yields 50% duty-cycle internal clocks to all on-chip peripherals. The MCF5445x devices use the input clock signal as its synchronous bus clock for PCI. A poor duty cycle on the input clock, may affect the overall timing margin to external devices. If negative edge logic is used to interface to PCI, providing a 50% duty-cycle input clock aids in simplifying overall system design.

Table 9. Input Clock Timing Requirements

| Item | Specification | Min | Max | Unit |
|--------|--------------------------------------|-----|-------|------|
| C1 | Cycle time | 15 | 40 | ns |
| 1 / C1 | Frequency | 25 | 66.66 | MHz |
| C2 | Rise time (20% of vdd to 80% of vdd) | - | 2 | ns |
| C3 | Fall time (80% of vdd to 20% of vdd) | - | 2 | ns |
| C4 | Duty cycle (at 50% of vdd) | 40 | 60 | % |


Figure 7. Input Clock Timing Diagram
Table 10. PLL Electrical Characteristics

| Num | Characteristic | Symbol | Min. Value | Max. Value | Unit |
|-----|---|--------------------|---------------------|-------------------|-------|
| 1 | PLL Reference Frequency Range | | | | |
| | Crystal reference | $f_{ref_crystal}$ | 16 | 40 | MHz |
| | External reference | f_{ref_ext} | 16 | 66.66 | MHz |
| 2 | Core/System Frequency | f_{sys} | 512 Hz ¹ | 266.67 MHz | — |
| | Core/System Clock Period | t_{sys} | — | 1/ f_{sys} | ns |
| 19 | VCO Frequency ($f_{vco} = f_{ref} \times PFDR$) | f_{vco} | 300 | 540 | MHz |
| 3 | Crystal Start-up Time ^{2, 3} | t_{cst} | — | 10 | ms |
| 4 | EXTAL Input High Voltage | | | | |
| | Crystal Mode ⁴ | V_{IHEXT} | $V_{XTAL} + 0.4$ | — | V |
| | All other modes (External, Limp) | V_{IHEXT} | $E_{VDD}/2 + 0.4$ | — | V |
| 5 | EXTAL Input Low Voltage | | | | |
| | Crystal Mode ⁴ | V_{ILEXT} | — | $V_{XTAL} - 0.4$ | V |
| | All other modes (External, Limp) | V_{ILEXT} | — | $E_{VDD}/2 - 0.4$ | V |
| 6 | EXTAL Input Rise & Fall Time (20% to 80% E_{VDD}) (External, Limp) | | 1 | 2 | ns |
| 7 | PLL Lock Time ^{3, 5} | t_{pll} | — | 50000 | CLKIN |
| 8 | Duty Cycle of reference ³ (External, Limp) | t_{dc} | 40 | 60 | % |
| 9 | XTAL Current | I_{XTAL} | 1 | 3 | mA |
| 10 | Total on-chip stray capacitance on XTAL | C_{S_XTAL} | — | 1.5 | pF |

Table 10. PLL Electrical Characteristics (continued)

| Num | Characteristic | Symbol | Min. Value | Max. Value | Unit |
|-----|--|---------------------------------|------------------|--|----------------------|
| 11 | Total on-chip stray capacitance on EXTAL | C_{S_EXTAL} | — | 1.5 | pF |
| 12 | Crystal capacitive load | C_L | See crystal spec | | |
| 13 | Discrete load capacitance for XTAL Discrete load capacitance for EXTAL | C_{L_XTAL} C_{L_EXTAL} | — | $2 \times (C_L - C_{S_XTAL} - C_{S_EXTAL} - C_{S_PCB})^6$ | pF |
| 14 | Frequency un-LOCK Range | f_{UL} | -4.0 | 4.0 | % f_{sys} |
| 15 | Frequency LOCK Range | f_{LCK} | -2.0 | 2.0 | % f_{sys} |
| 17 | CLKOUT Period Jitter, ^{3, 4, 7} Measured at f_{SYS} Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter | C_{jitter} | — — | 10 TBD | % FB_CLK % FB_CLK |

¹ The minimum system frequency is the minimum input clock divided by the maximum low-power divider (16 MHz ÷ 32,768). When the PLL is enabled, the minimum system frequency (f_{sys}) is 150 MHz.

² This parameter is guaranteed by characterization before qualification rather than 100% tested. Applies to external clock reference only.

³ Proper PC board layout procedures must be followed to achieve specifications.

⁴ This parameter is guaranteed by design rather than 100% tested.

⁵ This specification is the PLL lock time only and does not include oscillator start-up time.

⁶ C_{S_PCB} is the measured PCB stray capacitance on EXTAL and XTAL.

⁷ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL V_{DD} , EV_{DD} , and V_{SS} and variation in crystal oscillator frequency increase the C_{jitter} percentage for a given interval.

5.6 Reset Timing Specifications

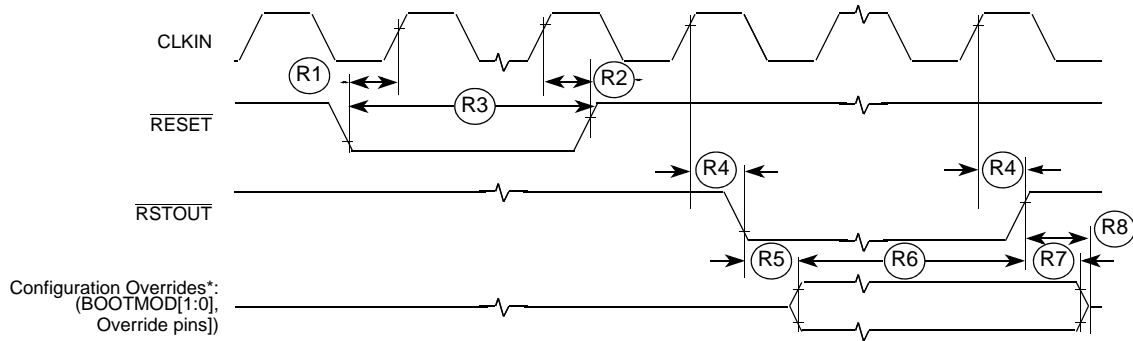
Table 11 lists specifications for the reset timing parameters shown in Figure 8.

Table 11. Reset and Configuration Override Timing

| Num | Characteristic | Min | Max | Unit |
|-----------------|--|-----|-----|--------------|
| R1 ¹ | \overline{RESET} valid to CLKIN (setup) | 9 | — | ns |
| R2 | CLKIN to \overline{RESET} invalid (hold) | 1.5 | — | ns |
| R3 | \overline{RESET} valid time ² | 5 | — | CLKIN cycles |
| R4 | CLKIN to \overline{RSTOUT} valid | — | 10 | ns |
| R5 | \overline{RSTOUT} valid to Configuration Override inputs valid | 0 | — | ns |
| R6 | Configuration Override inputs valid to \overline{RSTOUT} invalid (setup) | 20 | — | CLKIN cycles |
| R7 | Configuration Override inputs invalid after \overline{RSTOUT} invalid (hold) | 0 | — | ns |
| R8 | \overline{RSTOUT} invalid to Configuration Override inputs High Impedance | — | 1 | CLKIN cycles |

¹ \overline{RESET} and Configuration Override data lines are synchronized internally. Setup and hold times must be met only if recognition on a particular clock is required.

² During low power STOP, the synchronizers for the \overline{RESET} input are bypassed and \overline{RESET} is asserted asynchronously to the system. Thus, \overline{RESET} must be held a minimum of 100 ns.


 Figure 8. $\overline{\text{RESET}}$ and Configuration Override Timing

5.7 FlexBus Timing Specifications

A multi-function external bus interface called FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 66MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices, a simple chip-select based interface can be used.

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 12. FlexBus AC Timing Specifications

| Num | Characteristic | Min | Max | Unit | Notes |
|-----|------------------------|-----|-------|------|--------------|
| | Frequency of Operation | 25 | 66.66 | MHz | |
| FB1 | Clock Period | 15 | 40 | ns | |
| FB2 | Output Valid | — | 7.0 | ns | ¹ |
| FB3 | Output Hold | 1.0 | — | ns | 1 |
| FB4 | Input Setup | 3.0 | — | ns | ² |
| FB5 | Input Hold | 0 | — | ns | 2 |

¹ Specification is valid for all FB_AD[31:0], FB_BS[3:0], $\overline{\text{FB_CS}}$ [3:0], FB_OE, FB_R/W, FB_TBST, FB_TSIZ[1:0], and $\overline{\text{FB_TS}}$.

² Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

NOTE

The processor drives the data lines during the first clock cycle of the transfer with the full 32-bit address. This may be ignored by standard connected devices using non-multiplexed address and data buses. However, some applications may find this feature beneficial.

The address and data busses are muxed between the FlexBus and PCI controller. At the end of the read and write bus cycles the address signals are indeterminate.

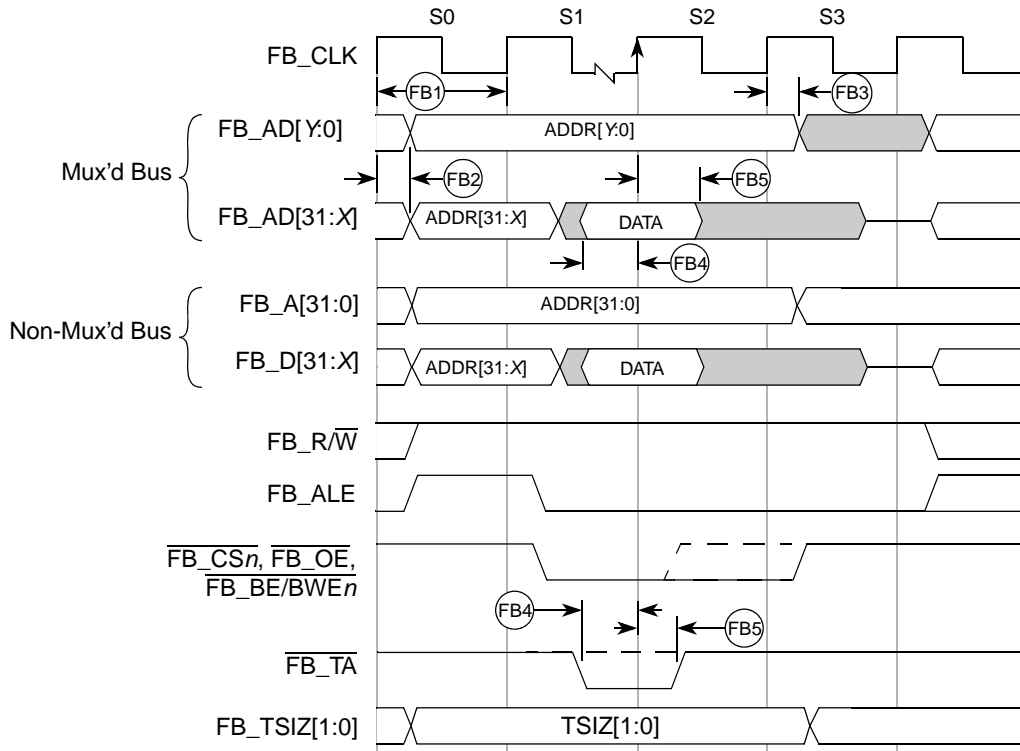


Figure 9. FlexBus Read Timing

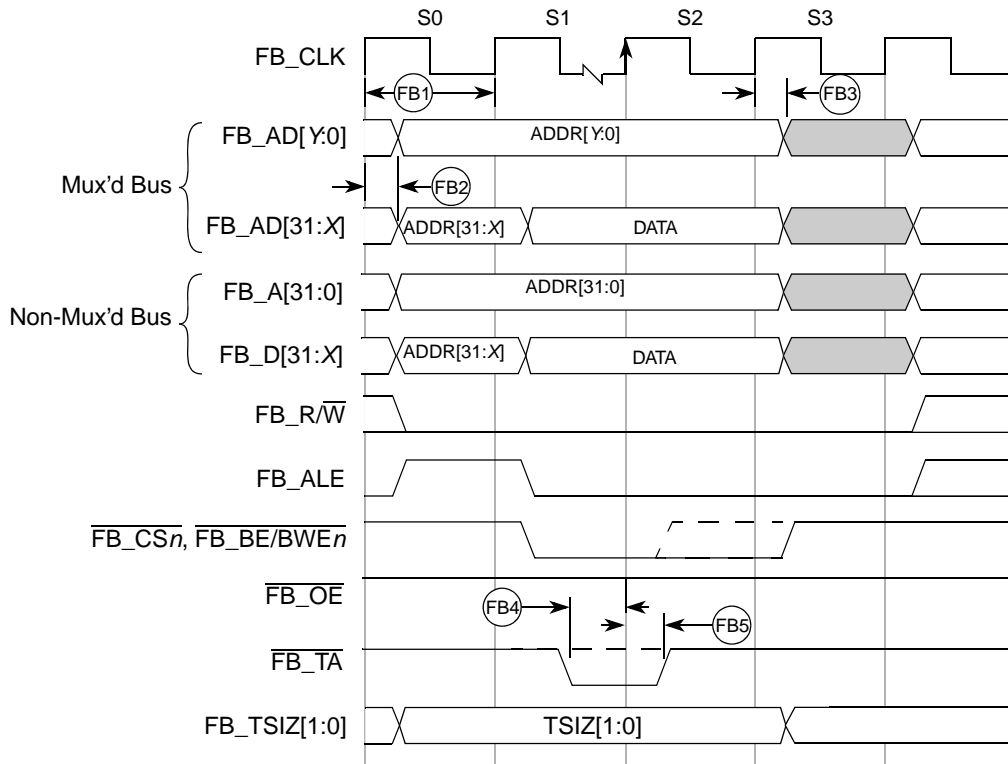


Figure 10. Flexbus Write Timing

5.8 SDRAM AC Timing Characteristics

The following timing numbers must be followed to properly latch or drive data onto the SDRAM memory bus. All timing numbers are relative to the four DQS byte lanes.

Table 13. SDRAM Timing Specifications

| Num | Characteristic | Symbol | Min | Max | Unit | Notes |
|------|---|-------------|---|--|------------|--------|
| | Frequency of Operation | | 60 | 133.33 | MHz | 1 |
| DD1 | Clock Period | t_{SDCK} | 7.5 | 16.67 | ns | |
| DD2 | Pulse Width High | t_{SDCKH} | 0.45 | 0.55 | t_{SDCK} | 2 |
| DD3 | Pulse Width Low | t_{SDCKL} | 0.45 | 0.55 | t_{SDCK} | 3 |
| DD4 | Address, $\overline{SD_CKE}$, $\overline{SD_CAS}$, $\overline{SD_RAS}$, $\overline{SD_WE}$, $\overline{SD_CS}[1:0]$ — Output Valid | t_{CMV} | — | $(0.5 \times t_{SDCK}) + 1.0\text{ns}$ | ns | 3 |
| DD5 | Address, $\overline{SD_CKE}$, $\overline{SD_CAS}$, $\overline{SD_RAS}$, $\overline{SD_WE}$, $\overline{SD_CS}[1:0]$ — Output Hold | t_{CMH} | 2.0 | — | ns | |
| DD6 | Write Command to first DQS Latching Transition | t_{DQSS} | $(1.0 \times t_{SDCK}) - 0.6\text{ns}$ | $(1.0 \times t_{SDCK}) + 0.6\text{ns}$ | ns | |
| DD7 | Data and Data Mask Output Setup (DQ-->DQS) Relative to DQS (DDR Write Mode) | t_{QS} | 1.0 | — | ns | 4 5 |
| DD8 | Data and Data Mask Output Hold (DQS-->DQ) Relative to DQS (DDR Write Mode) | t_{QH} | 1.0 | — | ns | 6 |
| DD9 | Input Data Skew Relative to DQS (Input Setup) | t_{IS} | — | 1.0 | ns | 7 |
| DD10 | Input Data Hold Relative to DQS. | t_{IH} | $(0.25 \times t_{SDCK}) + 0.5\text{ns}$ | — | ns | 8 |

¹ The SDRAM interface operates at the same frequency as the internal system bus.

² Pulse width high plus pulse width low cannot exceed min and max clock period.

³ Command output valid should be 1/2 the memory bus clock (t_{SDCK}) plus some minor adjustments for process, temperature, and voltage variations.

⁴ This specification relates to the required input setup time of DDR memories. The microprocessor's output setup should be larger than the input setup of the DDR memories. If it is not larger, then the input setup on the memory is in violation. $SD_D[31:24]$ is relative to $SD_DQS[3]$; $SD_D[23:16]$ is relative to $SD_DQS[2]$

⁵ The first data beat is valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats are valid for each subsequent DQS edge.

⁶ This specification relates to the required hold time of DDR memories. $SD_D[31:24]$ is relative to $SD_DQS[3]$; $SD_D[23:16]$ is relative to $SD_DQS[2]$

⁷ Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

⁸ Data input hold is derived from each DQS clock edge. It begins with a DQS transition and ends when the first data line becomes invalid.

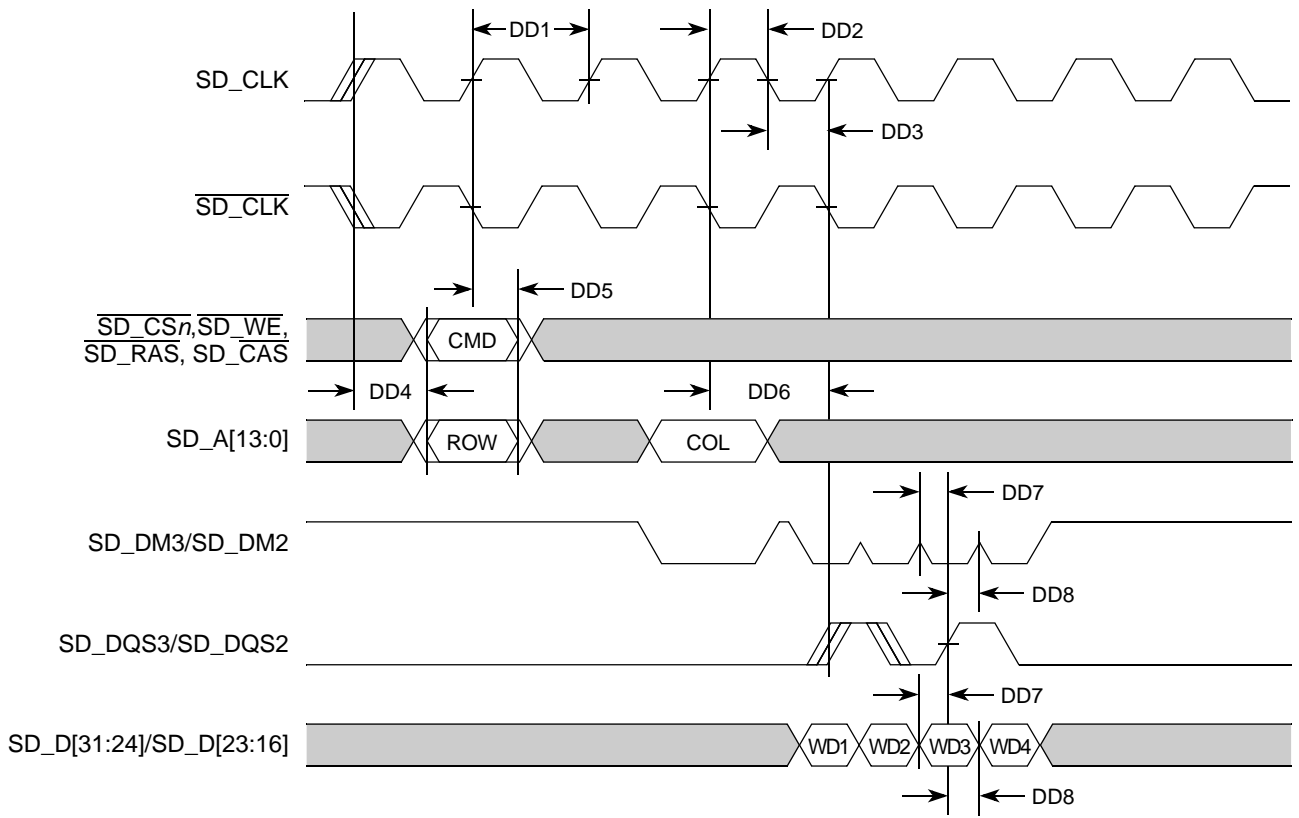


Figure 11. DDR Write Timing

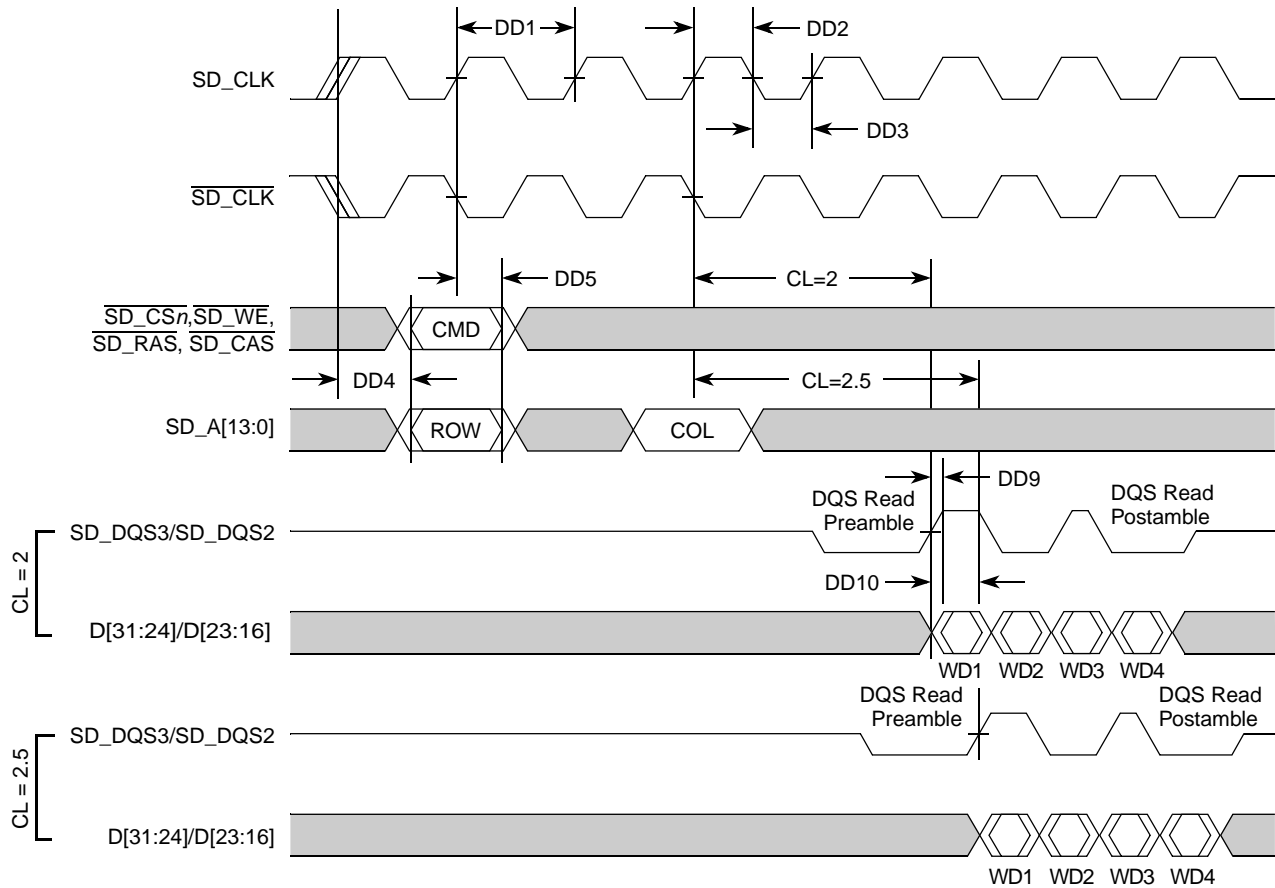


Figure 12. DDR Read Timing

5.9 PCI Bus Timing Specifications

The PCI bus on the device is PCI 2.2 compliant. The following timing numbers are mostly from the PCI 2.2 spec. Refer to the PCI 2.2 spec for a more detailed timing analysis.

Table 14. PCI Timing Specifications^{1,2}

| Num | Characteristic | 33 MHz ³ | | 66 MHz ³ | | Unit |
|-----|---|---------------------|-------|---------------------|-------|------|
| | | Min | Max | Min | Max | |
| | Frequency of Operation | — | 33.33 | 33.33 | 66.66 | MHz |
| P1 | Clock Period | 30 | — | 15 | 30 | ns |
| P2 | Bused PCI signals — input setup | 7.0 | — | 3.0 | — | ns |
| P3 | PCI_GNT[3:0]/PCI_REQ[3:0] — input setup | 10.0 | — | 5.0 | — | ns |
| P4 | All PCI signals — input hold | 0 | — | 0 | — | ns |
| P5 | Bused PCI signals — output valid | — | 11.0 | — | 6.0 | ns |

Table 14. PCI Timing Specifications^{1,2} (continued)

| Num | Characteristic | 33 MHz ³ | | 66 MHz ³ | | Unit |
|-----|--|---------------------|------|---------------------|-----|------|
| | | Min | Max | Min | Max | |
| P6 | PCI_REQ[3:0]/PCI_GNT[3:0] — output valid | — | 12.0 | — | 6.0 | ns |
| P7 | All PCI signals — output hold | 2.0 | — | 1.0 | — | ns |

¹ The PCI bus operates at the CLKIN frequency. All timings are relative to the input clock, CLKIN.

² All PCI signals are bused signals except for PCI_GNT[3:0] and PCI_REQ[3:0]. These signals are defined as point-to-point signals by the PCI Specification.

³ The 66-MHz parameters are only guaranteed when the 66-MHz PCI pad slew rates are selected. Likewise, the 33-MHz parameters are only guaranteed when the 33-MHz PCI pad slew rates are selected.

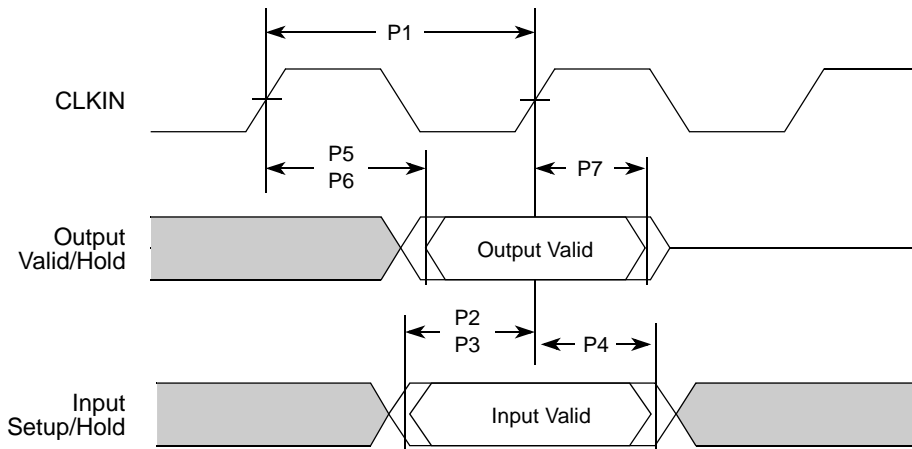


Figure 13. PCI Timing

5.9.1 Overshoot and Undershoot

Figure 14 shows the specification limits for overshoot and undershoot for PCI I/O. To guarantee long term reliability, the specification limits shown must be followed. Good transmission line design practices should be observed to guarantee the specification limits.

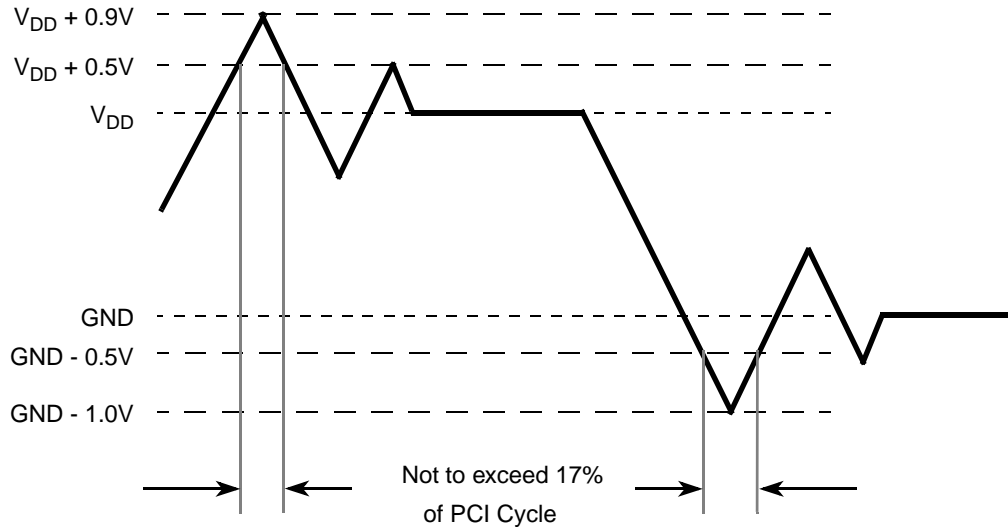


Figure 14. Overshoot and Undershoot Limits

5.10 ULPI Timing Specifications

The ULPI interface is fully compliant with the industry standard UTMI+ Low Pin Interface. Control and data timing requirements for the ULPI pins are given in Table 15. These timings apply to synchronous mode only. All timings are measured with respect to the clock as seen at the USB_CLKIN pin on the MCF5445x. The ULPI PHY is the source of the 60MHz clock.

NOTE

The USB controller requires a 60-MHz clock, even if using the on-chip FS/LS transceiver instead of the ULPI interface. In this case, the 60-MHz clock can be generated by the PLL or input on the USB_CLKIN pin.

Table 15. ULPI Interface Timing

| Num | Characteristic | Min | Nominal | Max | Units |
|-----|---------------------------------|-----|---------|-----|-------|
| | USB_CLKIN operating frequency | — | 60 | — | MHz |
| | USB_CLKIN duty cycle | — | 50 | — | % |
| U1 | USB_CLKIN clock period | — | 16.67 | — | ns |
| U2 | Input Setup (control and data) | 5.0 | — | — | ns |
| U3 | Input Hold (control and data) | 1.0 | — | — | ns |
| U4 | Output Valid (control and data) | — | — | 9.5 | ns |
| U5 | Output Hold (control and data) | 1.0 | — | — | |

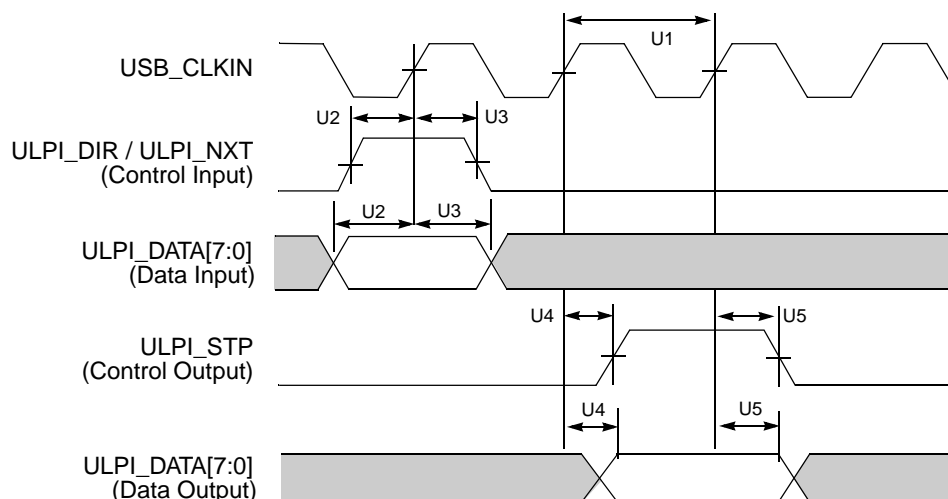


Figure 15. ULPI Timing Diagram

5.11 SSI Timing Specifications

This section provides the AC timings for the SSI in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (SSI_TCR[TSCKP] = 0, SSI_RCR[RSCKP] = 0) and a non-inverted frame sync (SSI_TCR[TFSI] = 0, SSI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SSI_BCLK) and/or the frame sync (SSI_FS) shown in the figures below.

Table 16. SSI Timing — Master Modes¹

| Num | Description | Symbol | Min | Max | Units | Notes |
|-----|--|------------|--------------------|-----|------------|--------------|
| S1 | SSI_MCLK cycle time | t_{MCLK} | $2 \times t_{SYS}$ | — | ns | ² |
| S2 | SSI_MCLK pulse width high / low | | 45% | 55% | t_{MCLK} | |
| S3 | SSI_BCLK cycle time | t_{BCLK} | $8 \times t_{SYS}$ | — | ns | ³ |
| S4 | SSI_BCLK pulse width | | 45% | 55% | t_{BCLK} | |
| S5 | SSI_BCLK to SSI_FS output valid | | — | 15 | ns | |
| S6 | SSI_BCLK to SSI_FS output invalid | | 0 | — | ns | |
| S7 | SSI_BCLK to SSI_TXD valid | | — | 15 | ns | |
| S8 | SSI_BCLK to SSI_TXD invalid / high impedance | | -2 | — | ns | |
| S9 | SSI_RXD / SSI_FS input setup before SSI_BCLK | | 10 | — | ns | |
| S10 | SSI_RXD / SSI_FS input hold after SSI_BCLK | | 0 | — | ns | |

¹ All timings specified with a capacitive load of 25pF.

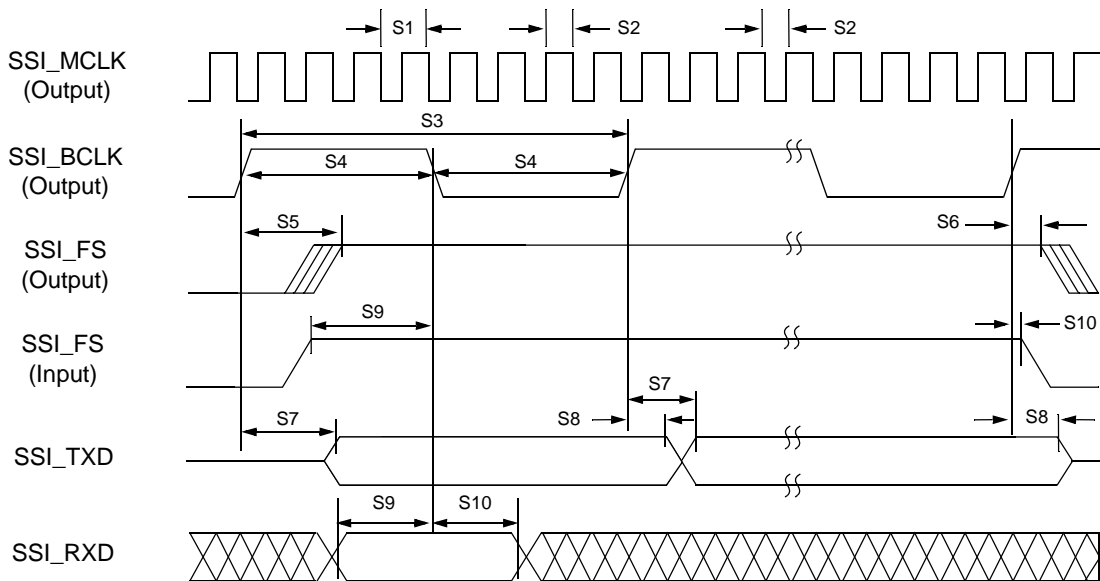
² SSI_MCLK can be generated from SSI_CLKIN or a divided version of the internal system clock (f_{SYS}).

³ SSI_BCLK can be derived from SSI_CLKIN or a divided version of the internal system clock (f_{SYS}).

Table 17. SSI Timing—Slave Modes¹

| Num | Description | Symbol | Min | Max | Units | Notes |
|-----|--|-------------------|---------------------------|-----|-------------------|-------|
| S11 | SSI_BCLK cycle time | t_{BCLK} | $8 \times t_{\text{SYS}}$ | — | ns | |
| S12 | SSI_BCLK pulse width high / low | | 45% | 55% | t_{BCLK} | |
| S13 | SSI_FS input setup before SSI_BCLK | | 10 | — | ns | |
| S14 | SSI_FS input hold after SSI_BCLK | | 2 | — | ns | |
| S15 | SSI_BCLK to SSI_TXD / SSI_FS output valid | | — | 15 | ns | |
| S16 | SSI_BCLK to SSI_TXD / SSI_FS output invalid / high impedance | | 0 | — | ns | |
| S17 | SSI_RXD setup before SSI_BCLK | | 10 | — | ns | |
| S18 | SSI_RXD hold after SSI_BCLK | | 2 | — | ns | |

¹ All timings specified with a capacitive load of 25pF.


Figure 16. SSI Timing—Master Modes

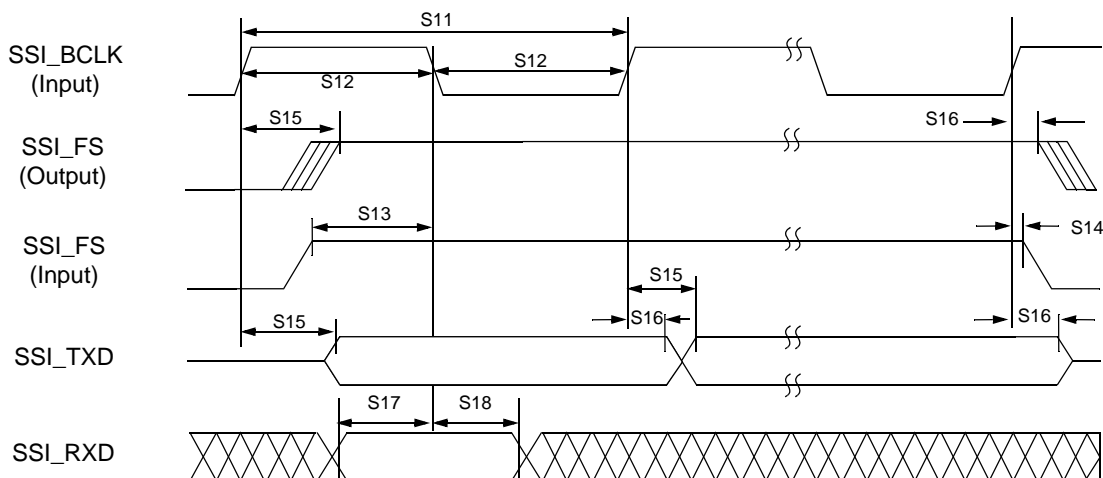


Figure 17. SSI Timing—Slave Modes

5.12 I²C Timing Specifications

Table 18 lists specifications for the I²C input timing parameters shown in Figure 18.

Table 18. I²C Input Timing Specifications between SCL and SDA

| Num | Characteristic | Min | Max | Units |
|-----|--|-----|-----|------------------|
| I1 | Start condition hold time | 2 | — | t _{SYS} |
| I2 | Clock low period | 8 | — | t _{SYS} |
| I3 | I2C_SCL/I2C_SDA rise time (V _{IL} = 0.5 V to V _{IH} = 2.4 V) | — | 1 | ms |
| I4 | Data hold time | 0 | — | ns |
| I5 | I2C_SCL/I2C_SDA fall time (V _{IH} = 2.4 V to V _{IL} = 0.5 V) | — | 1 | ms |
| I6 | Clock high time | 4 | — | t _{SYS} |
| I7 | Data setup time | 0 | — | ns |
| I8 | Start condition setup time (for repeated start condition only) | 2 | — | t _{SYS} |
| I9 | Stop condition setup time | 2 | — | t _{SYS} |

Table 19 lists specifications for the I²C output timing parameters shown in Figure 18.

Table 19. I²C Output Timing Specifications between SCL and SDA

| Num | Characteristic | Min | Max | Units |
|-----------------|--|-----|-----|------------------|
| I1 ¹ | Start condition hold time | 6 | — | t _{SYS} |
| I2 ¹ | Clock low period | 10 | — | t _{SYS} |
| I3 ² | I2C_SCL/I2C_SDA rise time (V _{IL} = 0.5 V to V _{IH} = 2.4 V) | — | — | μs |
| I4 ¹ | Data hold time | 7 | — | t _{SYS} |
| I5 ³ | I2C_SCL/I2C_SDA fall time (V _{IH} = 2.4 V to V _{IL} = 0.5 V) | — | 3 | ns |

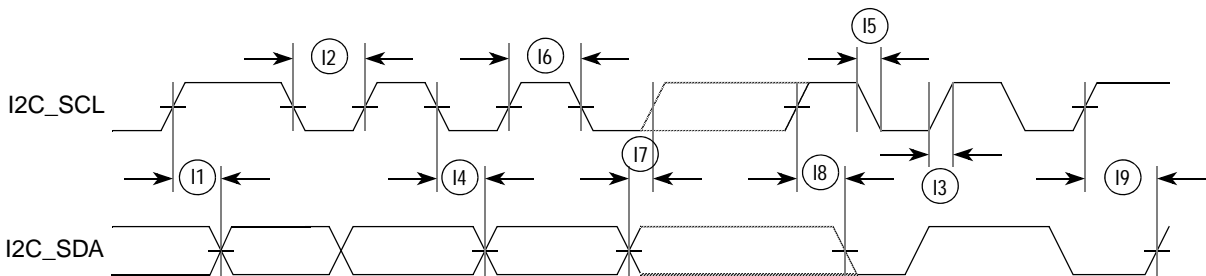
Table 19. I²C Output Timing Specifications between SCL and SDA (continued)

| Num | Characteristic | Min | Max | Units |
|-----------------|--|-----|-----|------------------|
| I6 ¹ | Clock high time | 10 | — | t _{SYS} |
| I7 ¹ | Data setup time | 2 | — | t _{SYS} |
| I8 ¹ | Start condition setup time (for repeated start condition only) | 20 | — | t _{SYS} |
| I9 ¹ | Stop condition setup time | 10 | — | t _{SYS} |

¹ Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 19. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR. However, the numbers given in Table 19 are minimum values.

² Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

³ Specified at a nominal 50-pF load.


Figure 18. I²C Input/Output Timings

5.13 Fast Ethernet Timing Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

5.13.1 Receive Signal Timing Specifications

The following timing specs meet the requirements for MII and 7-Wire style interfaces for a range of transceiver devices.

Table 20. Receive Signal Timing

| Num | Characteristic | MII Mode | | RMII Mode | | Unit |
|-----|--|----------|-----|-----------|-----|--------------|
| | | Min | Max | Min | Max | |
| — | RXCLK frequency | — | 25 | — | 50 | MHz |
| E1 | RXD[n:0], RXDV, RXER to RXCLK setup ¹ | 5 | — | 4 | — | ns |
| E2 | RXCLK to RXD[n:0], RXDV, RXER hold ¹ | 5 | — | 2 | — | ns |
| E3 | RXCLK pulse width high | 35% | 65% | 35% | 65% | RXCLK period |
| E4 | RXCLK pulse width low | 35% | 65% | 35% | 65% | RXCLK period |

¹ In MII mode, n = 3; In RMII mode, n = 1

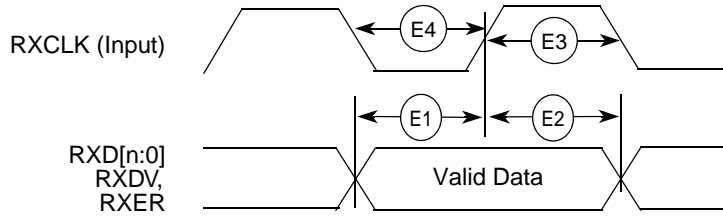


Figure 19. MII Receive Signal Timing Diagram

5.13.2 Transmit Signal Timing Specifications

Table 21. Transmit Signal Timing

| Num | Characteristic | MII Mode | | RMII Mode | | Unit |
|-----|--|----------|-----|-----------|-----|--------------------|
| | | Min | Max | Min | Max | |
| — | TXCLK frequency | — | 25 | — | 50 | MHz |
| E5 | TXCLK to TXD[n:0], TXEN, TXER invalid ¹ | 5 | — | 5 | — | ns |
| E6 | TXCLK to TXD[n:0], TXEN, TXER valid ¹ | — | 25 | — | 14 | ns |
| E7 | TXCLK pulse width high | 35% | 65% | 35% | 65% | t _{TXCLK} |
| E8 | TXCLK pulse width low | 35% | 65% | 35% | 65% | t _{TXCLK} |

¹ In MII mode, n = 3; In RMII mode, n = 1

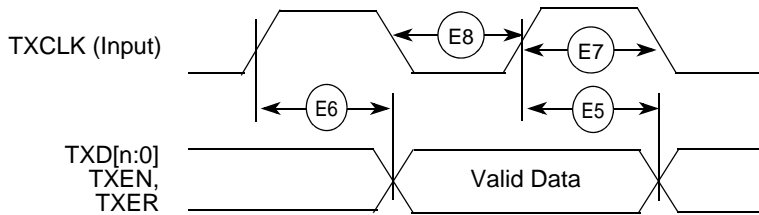


Figure 20. MII Transmit Signal Timing Diagram

5.13.3 Asynchronous Input Signal Timing Specifications

Table 22. MII Transmit Signal Timing

| Num | Characteristic | Min | Max | Unit |
|-----|------------------------------|-----|-----|--------------|
| E9 | CRS, COL minimum pulse width | 1.5 | — | TXCLK period |

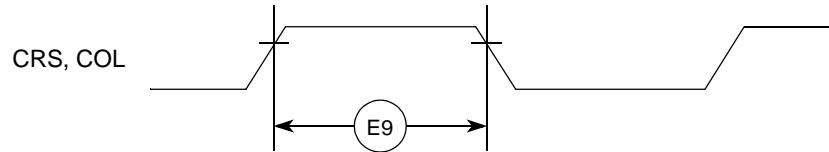


Figure 21. MII Async Inputs Timing Diagram

5.13.4 MII Serial Management Timing Specifications

Table 23. MII Serial Management Channel Signal Timing

| Num | Characteristic | Symbol | Min | Max | Unit |
|-----|----------------------------|-----------|-----|-----|-------------|
| E10 | MDC cycle time | t_{MDC} | 400 | — | ns |
| E11 | MDC pulse width | | 40 | 60 | % t_{MDC} |
| E12 | MDC to MDIO output valid | | — | 375 | ns |
| E13 | MDC to MDIO output invalid | | 25 | — | ns |
| E14 | MDIO input to MDC setup | | 10 | — | ns |
| E15 | MDIO input to MDC hold | | 0 | — | ns |

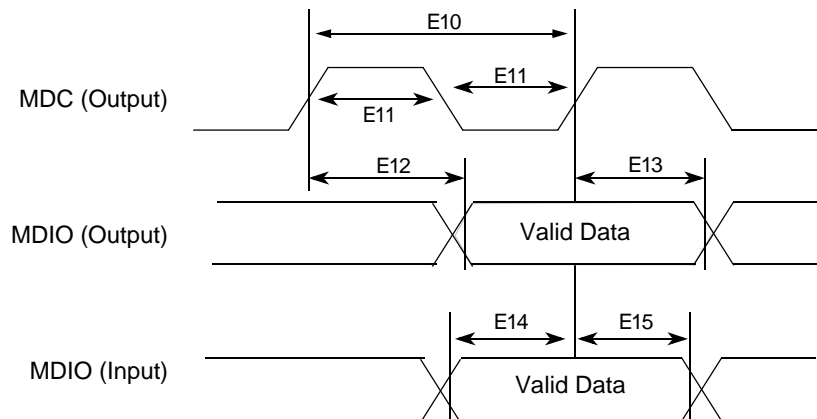


Figure 22. MII Serial Management Channel Timing Diagram

5.14 32-Bit Timer Module Timing Specifications

Table 24 lists timer module AC timings.

Table 24. Timer Module AC Timing Specifications

| Name | Characteristic | Min | Max | Unit |
|------|-----------------------------------|-----|-----|-------------|
| T1 | $DTnIN$ cycle time ($n = 0:3$) | 3 | — | $t_{sys}/2$ |
| T2 | $DTnIN$ pulse width ($n = 0:3$) | 1 | — | $t_{sys}/2$ |

5.15 ATA Interface Timing Specifications

The ATA controller is compatible with the ATA/ATAPI-6 industry standard. Refer to the *ATA/ATAPI-6 Specification* and the ATA controller chapter of the *MCF54455 Reference Manual* for timing diagrams of the various modes of operation.

The timings of the various ATA data transfer modes are determined by a set of timing equations described in the ATA section of the *MCF54455 Reference Manual*. These timing equations must be fulfilled for the ATA host to meet timing. [Table 25](#) provides implementation specific timing parameters necessary to complete the timing equations.

Table 25. ATA Interface Timing Specifications^{1,2}

| Name | Characteristic | Symbol | Min | Max | Unit | Notes |
|------|--|-------------|-----|-----|------|-------|
| A1 | Setup time — ATA_IORDY to SYSCLK falling | t_{SUI} | 4.0 | — | ns | |
| A2 | Hold time — ATA_IORDY from SYSCLK falling | t_{HI} | 3.0 | — | ns | |
| A3 | Setup time — ATA_DATA[15:0] to SYSCLK rising | t_{SU} | 4.0 | — | ns | |
| A4 | Propagation delay — SYSCLK rising to all outputs | t_{CO} | — | 7.0 | ns | 3 |
| A5 | Output skew | t_{SKEW1} | — | 1.5 | ns | 3 |
| A6 | Setup time — ATA_DATA[15:0] valid to ATA_IORDY | t_{I_DS} | 2.0 | — | ns | 4 |
| A7 | Hold time — ATA_IORDY to ATA_DATA[15:0] invalid | t_{I_DH} | 3.5 | — | ns | 4 |

¹ These parameters are guaranteed by design and not testable.

² All timings specified with a capacitive load of 40pF.

³ Applies to $\overline{ATA_CS}[1:0]$, $\overline{ATA_DA}[2:0]$, $\overline{ATA_DIOR}$, $\overline{ATA_DIOW}$, $\overline{ATA_DMACK}$, $\overline{ATA_DATA}[15:0]$

⁴ Applies to Ultra DMA data-in burst only

5.16 DSPI Timing Specifications

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. [Table 26](#) provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the *MCF54455 Reference Manual* for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 26. DSPI Module AC Timing Specifications¹

| Name | Characteristic | Symbol | Min | Max | Unit | Notes |
|--------------------|----------------------------------|-----------|----------------------------|--------------------------|------|-------|
| DS1 | DSPI_SCK Cycle Time | t_{SCK} | $4 \times t_{SYS}$ | — | ns | 2 |
| DS2 | DSPI_SCK Duty Cycle | — | $(t_{sck} \div 2) - 2.0$ | $(t_{sck} \div 2) + 2.0$ | ns | 3 |
| Master Mode | | | | | | |
| DS3 | DSPI_PCS n to DSPI_SCK delay | t_{CSC} | $(2 \times t_{SYS}) - 1.5$ | — | ns | 4 |
| DS4 | DSPI_SCK to DSPI_PCS n delay | t_{ASC} | $(2 \times t_{SYS}) - 3.0$ | — | ns | 5 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | — | — | 5 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | — | -5 | — | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | — | 9 | — | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | — | 0 | — | ns | |
| Slave Mode | | | | | | |
| DS9 | DSPI_SCK to DSPI_SOUT valid | — | — | 10 | ns | |

Table 26. DSPI Module AC Timing Specifications¹ (continued)

| Name | Characteristic | Symbol | Min | Max | Unit | Notes |
|------|---|--------|-----|-----|------|-------|
| DS10 | DSPI_SCK to DSPI_SOUT invalid | — | 0 | — | ns | |
| DS11 | DSPI_SIN to DSPI_SCK input setup | — | 2 | — | ns | |
| DS12 | DSPI_SCK to DSPI_SIN input hold | — | 7 | — | ns | |
| DS13 | $\overline{\text{DSPI_SS}}$ active to DSPI_SOUT driven | — | — | 10 | ns | |
| DS14 | $\overline{\text{DSPI_SS}}$ inactive to DSPI_SOUT not driven | — | — | 10 | ns | |

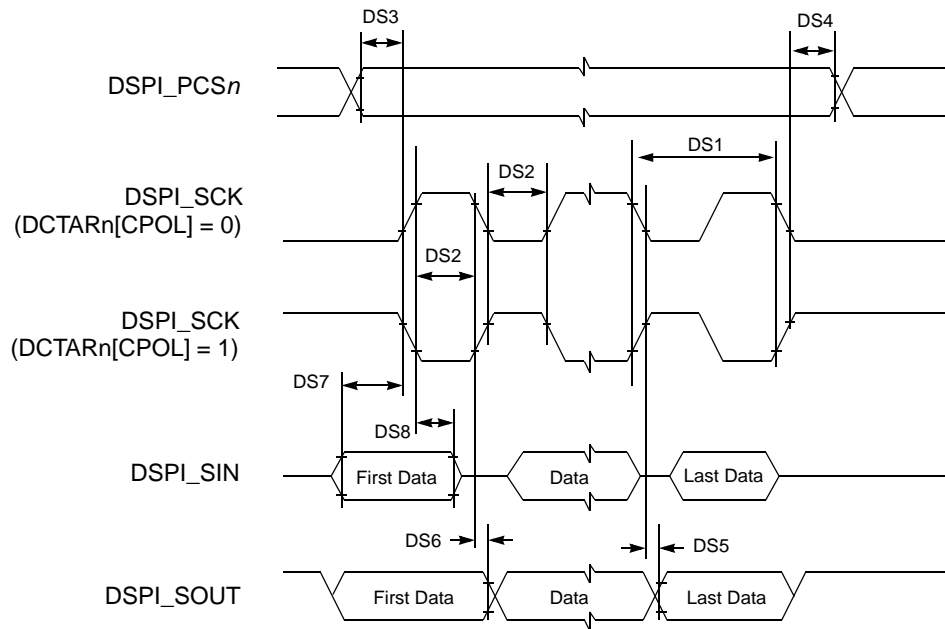
¹ Timings shown are for DMCR[MTFE] = 0 (classic SPI) and DCTARn[CPHA] = 0. Data is sampled on the DSPI_SIN pin on the odd-numbered DSPI_SCK edges and driven on the DSPI_SOUT pin on even-numbered DSPI edges.

² When in master mode, the baud rate is programmable in DCTARn[DBR], DCTARn[PBR], and DCTARn[BR].

³ This specification assumes a 50/50 duty cycle setting. The duty cycle is programmable in DCTARn[DBR], DCTARn[CPHA], and DCTARn[PBR].

⁴ The DSPI_PCSn to DSPI_SCK delay is programmable in DCTARn[PCSSCK] and DCTARn[CSSCK].

⁵ The DSPI_SCK to DSPI_PCSn delay is programmable in DCTARn[PASC] and DCTARn[ASC].


Figure 23. DSPI Classic SPI Timing—Master Mode

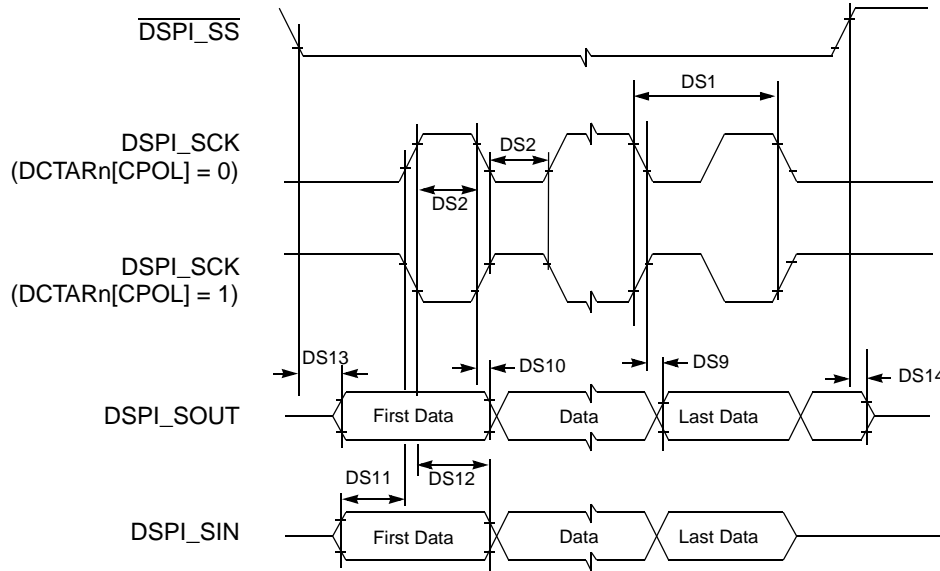


Figure 24. DSPI Classic SPI Timing—Slave Mode

5.17 SBF Timing Specifications

The Serial Boot Facility (SBF) provides a means to read configuration information and system boot code from a broad array of SPI-compatible EEPROMs, flashes, FRAMs, nVSRAMs, etc. Table 27 provides the AC timing specifications for the SBF.

Table 27. SBF AC Timing Specifications

| Name | Characteristic | Symbol | Min | Max | Unit | Notes |
|------|--------------------------------------|-------------|-------------------|-----|-------------|-------|
| SB1 | SBF_CK Cycle Time | t_{SBFCK} | 40 | — | ns | 1 |
| SB2 | SBF_CK High/Low Time | — | 30% | — | t_{SBFCK} | |
| SB3 | $\overline{SBF_CS}$ to SBF_CK delay | — | $t_{SBFCK} - 2.0$ | — | ns | |
| SB4 | SBF_CK to $\overline{SBF_CS}$ delay | — | $t_{SBFCK} - 2.0$ | — | ns | |
| SB5 | SBF_CK to SBF_DO valid | — | -5 | — | ns | |
| SB6 | SBF_CK to SBF_DO invalid | — | 5 | — | ns | |
| SB7 | SBF_DI to SBF_SCK input setup | — | 10 | — | ns | |
| SB8 | SBF_CK to SBF_DI input hold | — | 0 | — | ns | |

¹ At reset, the SBF_CK cycle time is $t_{REF} \times 67$. The first byte of data read from the serial memory contains a divider value that is used to set the SBF_CK cycle time for the duration of the serial boot process.

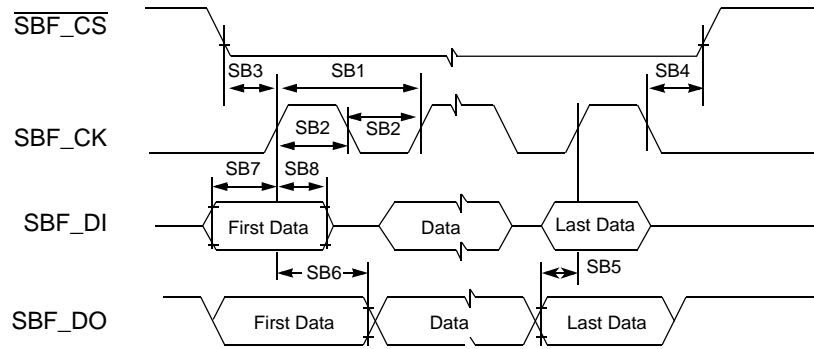


Figure 25. SBF Timing

5.18 General Purpose I/O Timing Specifications

 Table 28. GPIO Timing¹

| Num | Characteristic | Min | Max | Unit |
|-----|------------------------------------|-----|-----|------|
| G1 | FB_CLK High to GPIO Output Valid | — | 9 | ns |
| G2 | FB_CLK High to GPIO Output Invalid | 1.5 | — | ns |
| G3 | GPIO Input Valid to FB_CLK High | 9 | — | ns |
| G4 | FB_CLK High to GPIO Input Invalid | 1.5 | — | ns |

¹ These general purpose specifications apply to the following signals: \overline{IRQn} , all UART signals, all timer signals, \overline{DACKn} and \overline{DREQn} , and all signals configured as GPIO.

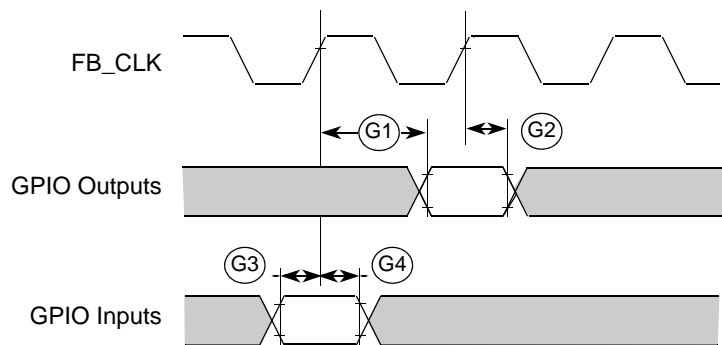


Figure 26. GPIO Timing

5.19 JTAG and Boundary Scan Timing

Table 29. JTAG and Boundary Scan Timing

| Num | Characteristics ¹ | Min | Max | Unit |
|-----|---|-----|-----|------|
| J1 | TCLK Frequency of Operation | DC | 20 | MHz |
| J2 | TCLK Cycle Period | 50 | — | ns |
| J3 | TCLK Clock Pulse Width | 20 | 30 | ns |
| J4 | TCLK Rise and Fall Times | — | 3 | ns |
| J5 | Boundary Scan Input Data Setup Time to TCLK Rise | 5 | — | ns |
| J6 | Boundary Scan Input Data Hold Time after TCLK Rise | 20 | — | ns |
| J7 | TCLK Low to Boundary Scan Output Data Valid | — | 33 | ns |
| J8 | TCLK Low to Boundary Scan Output High Z | — | 33 | ns |
| J9 | TMS, TDI Input Data Setup Time to TCLK Rise | 4 | — | ns |
| J10 | TMS, TDI Input Data Hold Time after TCLK Rise | 10 | — | ns |
| J11 | TCLK Low to TDO Data Valid | — | 11 | ns |
| J12 | TCLK Low to TDO High Z | — | 11 | ns |
| J13 | $\overline{\text{TRST}}$ Assert Time | 50 | — | ns |
| J14 | $\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High | 10 | — | ns |

¹ JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

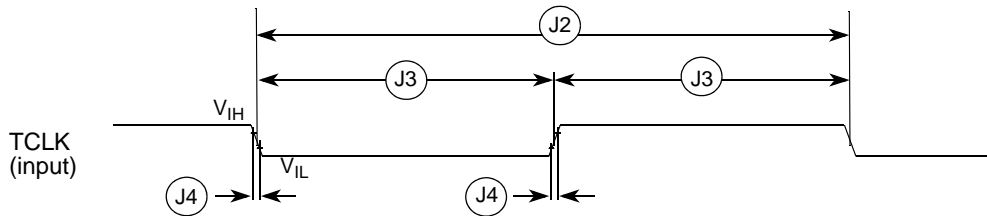


Figure 27. Test Clock Input Timing

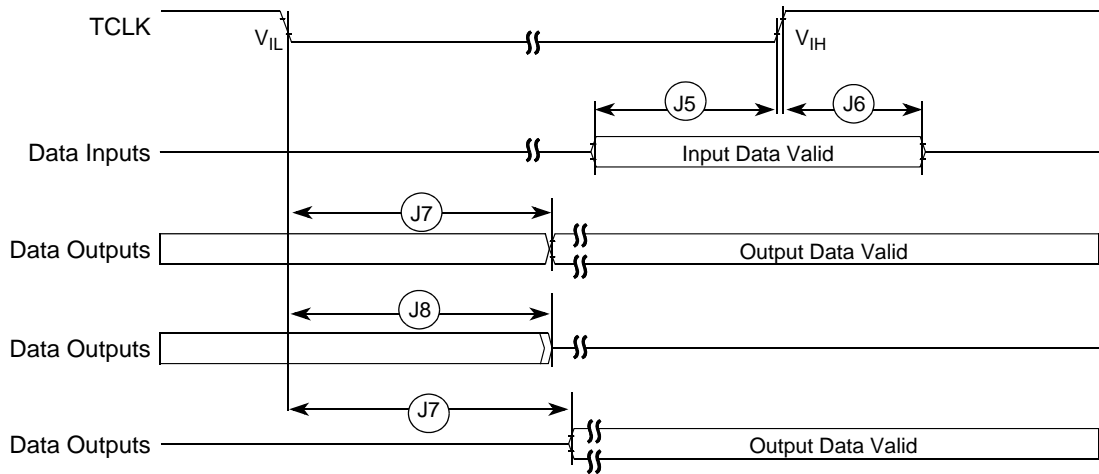


Figure 28. Boundary Scan (JTAG) Timing

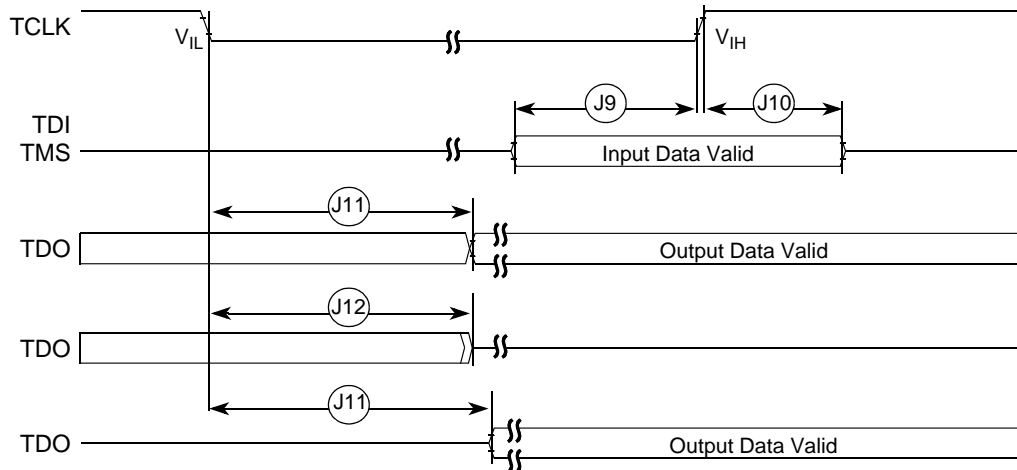


Figure 29. Test Access Port Timing

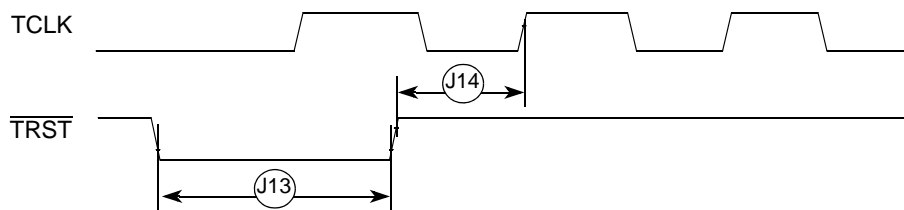


Figure 30. \overline{TRST} Timing

5.20 Debug AC Timing Specifications

Table 30 lists specifications for the debug AC timing parameters shown in Figure 31 and Table 32.

Table 30. Debug AC Timing Specification

| Num | Characteristic | Min | Max | Units |
|-----------------|-----------------------------------|-----|-----|-----------|
| D0 | PSTCLK cycle time | 1 | 1 | t_{sys} |
| D1 | PSTCLK rising to PSTDDATA valid | — | 3.0 | ns |
| D2 | PSTCLK rising to PSTDDATA invalid | 1.5 | — | ns |
| D3 | DSI-to-DSCLK setup | 1 | — | PSTCLK |
| D4 ¹ | DSCLK-to-DSO hold | 4 | — | PSTCLK |
| D5 | DSCLK cycle time | 5 | — | PSTCLK |
| D6 | BKPT assertion time | 1 | — | PSTCLK |

¹ DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

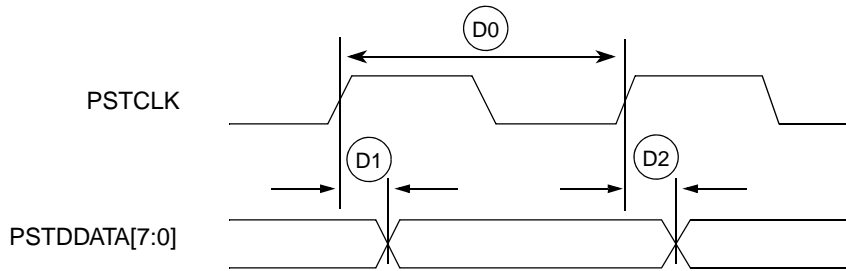


Figure 31. Real-Time Trace AC Timing

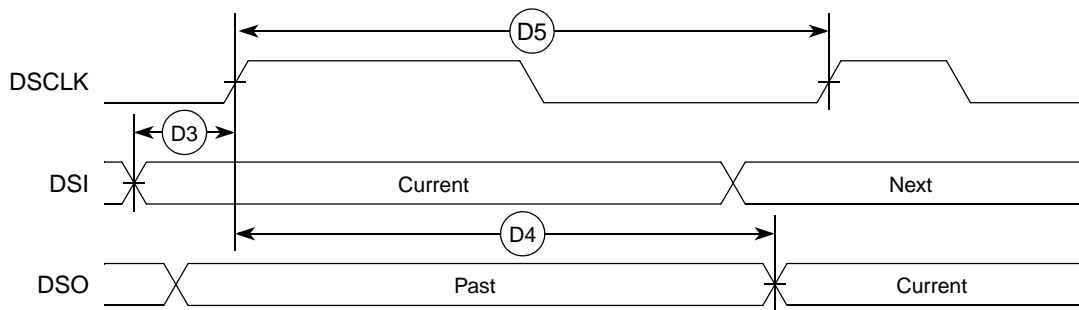


Figure 32. BDM Serial Port AC Timing

6 Power Consumption

All power consumption data is lab data measured on an M54455EVB running the Freescale Linux BSP.

Table 31. MCF4455 Application Power Consumption¹

| Core Freq. | | Idle | MP3 Playback | TFTP Download | USB HS File Copy | Units |
|------------|--------------------|------------|--------------|---------------|------------------|-----------|
| 266 MHz | IV_{DD} | 215.6 | 288.8 | 274.4 | 263.7 | mA |
| | EV_{DD} | 27.6 | 33.6 | 32.6 | 32.4 | |
| | SDV_{DD} | 142.9 | 158.2 | 161.1 | 158.0 | |
| | Total Power | 672 | 829 | 809 | 787 | mW |
| 200 MHz | IV_{DD} | 163.8 | 228.0 | 213.8 | 207.9 | mA |
| | EV_{DD} | 29.9 | 34.7 | 34.3 | 33.8 | |
| | SDV_{DD} | 142.2 | 158.5 | 160.0 | 153.4 | |
| | Total Power | 601 | 742 | 722 | 699 | mW |

¹ All voltage rails at nominal values: IV_{DD} = 1.5 V, EV_{DD} = 3.3 V, and SDV_{DD} = 1.8 V.

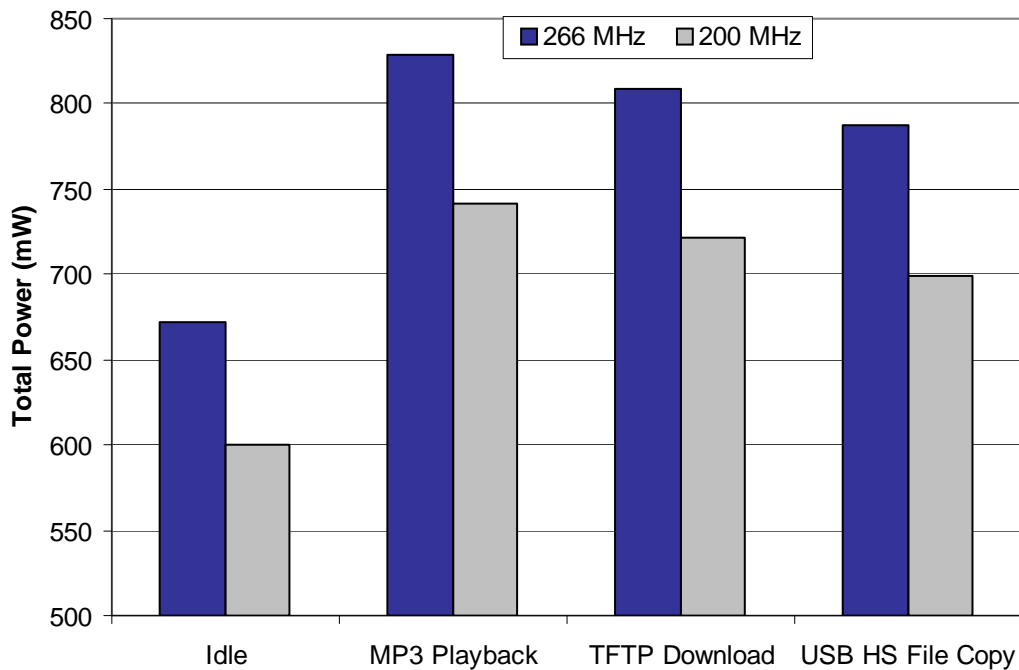


Figure 33. Power Consumption in Various Applications

Power Consumption

All current consumption data is lab data measured on a single device using an evaluation board. [Table 32](#) shows the typical power consumption in low-power modes. These current measurements are taken after executing a STOP instruction.

Table 32. Current Consumption in Low-Power Modes^{1,2}

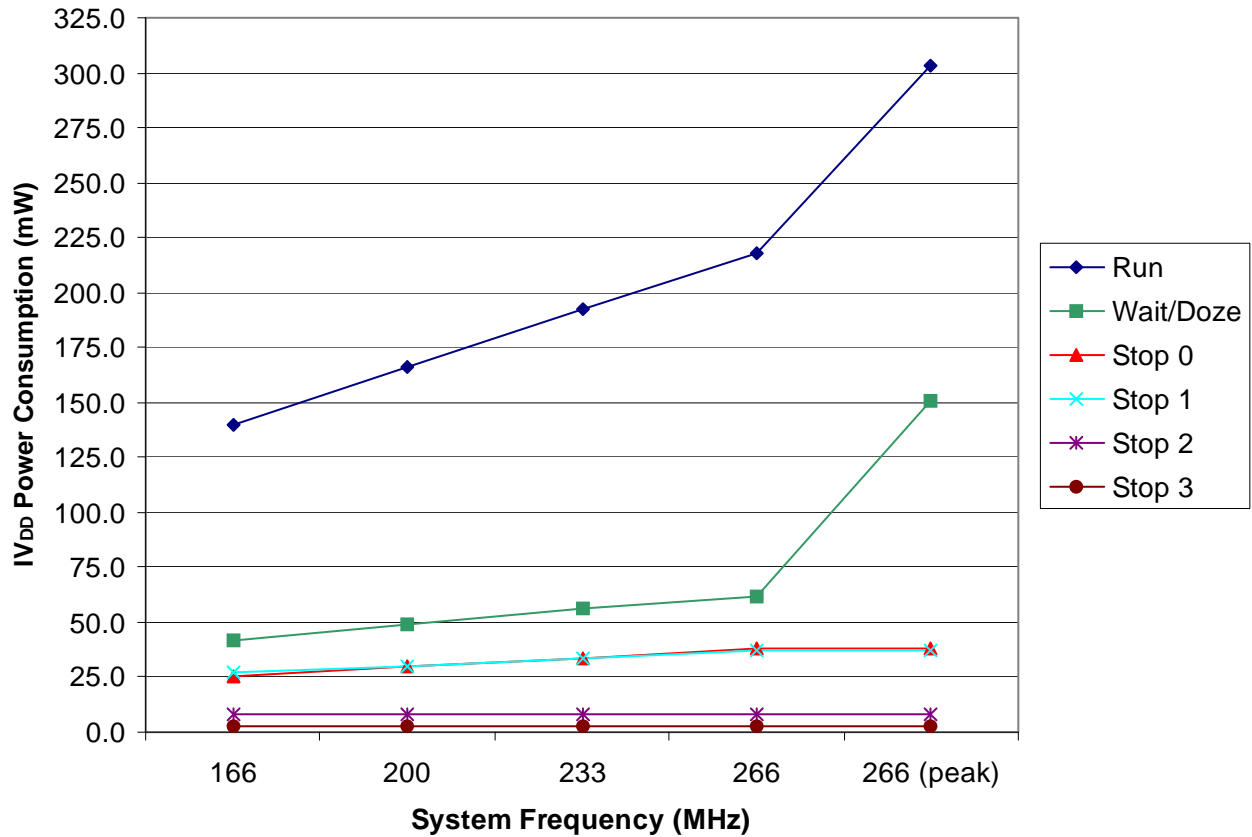
| Mode | Voltage Supply | System Frequency | | | | |
|-----------|-------------------|------------------------|------------------------|------------------------|------------------------|-------------------------|
| | | 166 (Typ) ³ | 200 (Typ) ³ | 233 (Typ) ³ | 266 (Typ) ³ | 266 (Peak) ⁴ |
| RUN | $I_{V_{DD}}$ (mA) | 93.4 | 110.9 | 128.2 | 145.4 | 202.1 |
| | Power (mW) | 140.1 | 166.3 | 192.4 | 218.1 | 303.2 |
| WAIT/DOZE | $I_{V_{DD}}$ (mA) | 28.0 | 32.7 | 37.5 | 41.1 | 100.2 |
| | Power (mW) | 42.0 | 49.1 | 56.2 | 61.7 | 150.3 |
| STOP 0 | $I_{V_{DD}}$ (mA) | 17.1 | 19.8 | 22.5 | 25.2 | 25.2 |
| | Power (mW) | 25.7 | 29.7 | 33.7 | 37.8 | 37.8 |
| STOP 1 | $I_{V_{DD}}$ (mA) | 17.9 | 19.8 | 22.4 | 25.1 | 25.1 |
| | Power (mW) | 26.8 | 29.6 | 33.6 | 37.6 | 37.6 |
| STOP 2 | $I_{V_{DD}}$ (mA) | 5.7 | 5.7 | 5.7 | 5.7 | 5.7 |
| | Power (mW) | 8.6 | 8.6 | 8.6 | 8.6 | 8.6 |
| STOP 3 | $I_{V_{DD}}$ (mA) | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 |
| | Power (mW) | 2.6 | 2.6 | 2.6 | 2.6 | 2.6 |

¹ All values are measured on an M54455EVB with 1.5V $I_{V_{DD}}$ power supply. Tests performed at room temperature.

² Refer to the Power Management chapter in the *MCF54455 Reference Manual* for more information on low-power modes.

³ All peripheral clocks are off except UART0, INTC0, IACK, edge port, reset controller, CCM, PLL, and FlexBus prior to entering low-power mode.

⁴ All peripheral clocks on prior to entering low-power mode.


 Figure 34. IV_{DD} Power Consumption in Low-Power Modes

7 Package Information

The latest package outline drawings are available on the product summary pages on <http://www.freescale.com/coldfire>. Table 33 lists the case outline numbers per device. Use these numbers in the web page's keyword search engine to find the latest package outline drawings.

Table 33. Package Information

| Device | Package Type | Case Outline Numbers |
|----------|--------------|----------------------|
| MCF54450 | 256 MAPBGA | 98ARH98219A |
| MCF54451 | | |
| MCF54452 | 360 TEPBGA | 98ARE10605D |
| MCF54453 | | |
| MCF54454 | | |
| MCF54455 | | |

8 Product Documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at <http://www.freescale.com/coldfire>.

9 Revision History

Table 34 summarizes revisions to this document.

Table 34. Revision History

| Rev. No. | Date | Summary of Changes |
|----------|---------------|---|
| 0 | Sept 17, 2007 | Initial public release. |
| 1 | Feb 15, 2008 | Corrected VSS pin locations in MCF5445x signal information and muxing table for the 360 TEPBGA package: changed "...M9, M16, M17..." to "...M9–M14, M16..." Updated FlexBus read and write timing diagrams and added two notes before them. Change FB_A[23:0] to FB_A[31:0] in FlexBus read and write timing diagrams. Added power consumption section. |
| 2 | May 1, 2008 | In Family Configurations table, added PCI as feature on 256-pin devices. On these devices the PCI_AD bus is limited to 24-bits. In Absolute Maximum Ratings table, changed RTCV _{DD} specification from "-0.3 to +4.0" to "-0.5 to +2.0". In DC Electrical Specifications table: <ul style="list-style-type: none"> • Changed RTCV_{DD} specification from 3.0–3.6 to 1.35–1.65. • Changed High Impedance (Off-State) Leakage Current (I_{OZ}) specification from ±1 to ±10μA, and added footnote to this spec: "Worst-case tristate leakage current with only one I/O pin high. Since all I/Os share power when high, the leakage current is distributed among them. With all I/Os high, this spec reduces to ±2 μA min/max." |
| 3 | Dec 1, 2008 | Changed "360PBGA" heading to "360 TEPBGA" in Table 6. Changed the following specs in Table 13: <ul style="list-style-type: none"> • Minimum frequency of operation from — to 60MHz. • Maximum clock period from — to 16.67 ns. |
| 4 | Apr 12, 2009 | Rescinded previous errata, the 256-pin devices do not contain the PCI bus controller: <ul style="list-style-type: none"> • In Table 4, in PCI_AD_n signal section, added a separate row for each package, with PCI_AD_n signals shown as — for 256-pin devices. • In Figure 5, changed the PCI_AD_n pins to their alternative function, FB_A_n. |
| 5 | Apr 27, 2009 | In Table 2 changed MCF54450VM180 to MCF54450CVM180 and changed its temperature entry from "0° to +70° C" to "-40° to +85° C". |
| 6 | Oct 15, 2009 | In Table 8 changed Input Leakage Current (I _{in}) from ±1.0 to ±2.5μA. |
| 7 | Oct 18, 2011 | In Table 2, added MCF54452YVR200 part number, with temperature range from -40° to +105° C. In Table 8, added Input Leakage Current (I _{in}) values for MCF54452YVR200 part number. |
| 8 | Jan 18, 2012 | In Table 4, added pin N7 in the VSS pin list for the 360 TEPBGA. |

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