FIELD PROGRAMMABLE SS VERSACLOCK SYNTHESIZER ICS341

Description

The ICS341 is a low cost, single-output, field programmable clock synthesizer. The ICS341 can generate an output frequency from 250 kHz to 200 MHz and may employ Spread Spectrum techniques to reduce system electro-magnetic interference (EMI).

Using IDT's VersaClock™ software to configure the PLL and output, the ICS341 contains a One-Time Programmable (OTP) ROM to allow field programmability. Programming features include 4 selectable configuration registers.

The device employs Phase-Locked Loop (PLL) techniques to run from a standard fundamental mode, inexpensive crystal, or clock. It can replace multiple crystals and oscillators, saving board space and cost.

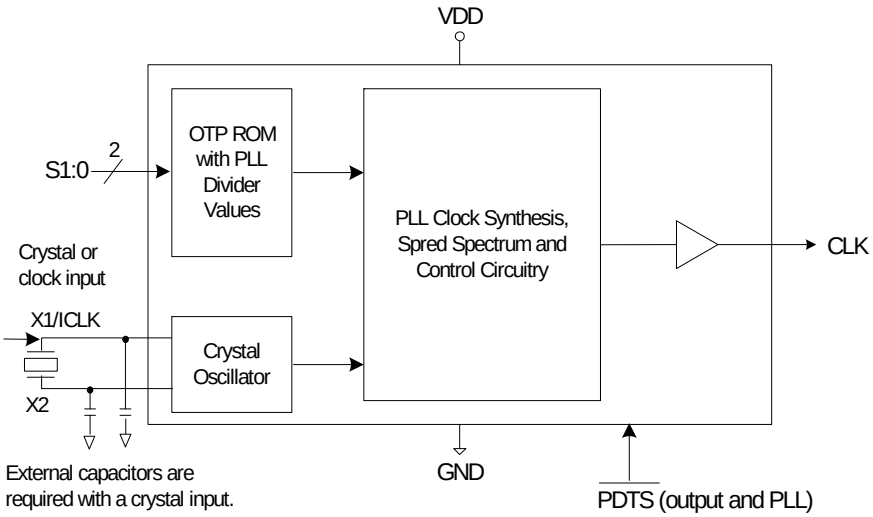
The device also has a power-down feature that tri-states the clock outputs and turns off the PLLs when the $\overline{\text{PDTS}}$ pin is taken low.

The ICS341 is also available in factory programmed custom versions for high-volume applications.

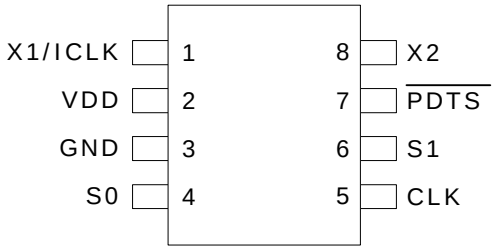
Features

- 8-pin SOIC package (Pb-free)
- Highly accurate frequency generation
  - M/N Multiplier PLL: M = 1...2048, N = 1...1024
- Output clock frequencies up to 200 MHz
- Four ROM locations for frequency and spread selection
- Spread spectrum capability for lower system EMI
  - Center or Down Spread up to 4% total
  - Selectable 32 kHz or 120 kHz modulation
- Input crystal frequency from 5 to 27 MHz
- Input clock frequency from 2 to 50 MHz
- Operating voltage of 3.3 V
- Advanced, low-power CMOS process
- For two output clocks, use the ICS342. For three output clocks, see the ICS343. For more than three outputs, see the ICS345 or ICS348.

Block Diagram



Pin Assignment



8-pin (150 mil) SOIC

Output Clock Selection Table

S1	S0	CLK (MHz)	Spread Percentage
0	0	User Configurable	User Configurable
0	1	User Configurable	User Configurable
1	0	User Configurable	User Configurable
1	1	User Configurable	User Configurable

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/ICLK	XI	Connect this pin to a crystal or external clock input.
2	VDD	Power	Connect to +3.3 V.
3	GND	Power	Connect to ground.
4	S0	Input	Select pin 0 for frequency selection on CLK. Internal pull-up resistor.
5	CLK	Output	Clock output. Weak internal pull-down when tri-state.
6	S1	Input	Select pin 1 for frequency selection on CLK. Internal pull-up resistor.
7	$\overline{PDTS}$	Input	Powers down entire chip. Tri-states CLK outputs when low. Internal pull-up resistor.
8	X2	XO	Connect this pin to a crystal, or float for clock input.

External Components

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS341 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between VDD and the PCB ground plane.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal (C_L -6 pF)*2. In this equation, C_L= crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF [(16-6) x 2] = 20.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS341. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

ICS341 Configuration Capabilities

The architecture of the ICS341 allows the user to easily configure the device to a wide range of output frequencies, for a given input reference frequency.

The frequency multiplier PLL provides a high degree of precision. The M/N values (the multiplier/divide values available to generate the target VCO frequency) can be set within the range of M = 1 to 2048 and N = 1 to 1024.

The ICS341 also provides separate output divide values, from 2 through 20, to allow the two output clock banks to support widely differing frequency values from the same PLL.

Each output frequency can be represented as:

$$OutputFreq = \frac{REFFreq}{OutputDivide} \cdot \frac{M}{N}$$

IDT VersaClock Software

IDT applies years of PLL optimization experience into a user friendly software that accepts the user's target reference clock and output frequencies and generates the lowest jitter, lowest power configuration, with only a press of a button. The user does not need to have prior PLL experience or determine the optimal VCO frequency to support multiple output frequencies.

VersaClock software quickly evaluates accessible VCO frequencies with available output divide values and provides an easy to understand, bar code rating for the target output frequencies. The user may evaluate output accuracy, performance trade-off scenarios in seconds.

Spread Spectrum Modulation

The ICS341 utilizes frequency modulation (FM) to distribute energy over a range of frequencies. By modulating the output clock frequencies, the device effectively lowers energy across a broader range of frequencies; thus, lowering a system's electro-magnetic interference (EMI).

The modulation rate is the time from transitioning from a minimum frequency to a maximum frequency and then back to the minimum.

Spread Spectrum Modulation can be applied as either "center spread" or "down spread". During center spread modulation, the deviation from the target frequency is equal in the positive and negative directions. The effective average frequency is equal to the target frequency. In applications where the clock is driving a component with a maximum frequency rating, down spread should be applied. In this case, the maximum frequency, including modulation, is the target frequency. The effective average frequency is less than the target frequency.

The ICS341 operates in both center spread and down spread modes. For center spread, the frequency can be modulated between +/- 0.125% to +/-2.0%. For down spread, the frequency can be modulated between -0.25% to -4.0%.

Both output frequency banks will utilize identical spread spectrum percentage deviations and modulation rates, if a common VCO frequency can be identified.

Spread Spectrum Modulation Rate

The spread spectrum modulation frequency applied to the output clock frequency may occur at a variety of rates. For applications requiring the driving of "down-circuit" PLLs, Zero Delay Buffers, or those adhering to PCI standards, the spread spectrum modulation rate should be set to 30-33 kHz. For other applications, a 120 kHz modulation option is available.

Using VersaClock Products with an Input Clock Source

In order to ensure proper startup with an input clock rather than a crystal, the supply voltage must be within the operating range (3.3V ±10%) and the input signal must be stable and free from glitching. The input clock must provide pulses of at least 20ns, and no more than 500ns, for at least 160 clock cycles without any interruptions to the clock or power during this period. It may take up to 4ms for output frequencies to reach their target frequency values.

An alternative method is to have the $\overline{PDTS}$ pin asserted low while power supplies and clock sources stabilize.Once the power supply and input clock source are constant and within the acceptable frequency range, bring $\overline{PDTS}$ high. This approach is preferred if the clock source is derived from another PLL, or the source oscillator produces unpredictable output pulses prior to stabilization. No considerations need to be taken when using a crystal input source with VersaClock products.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS341. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Parameter	Condition	Min.	Typ.	Max.	Units
Supply Voltage, VDD	Referenced to GND	-0.5		7	V
Inputs	Referenced to GND	-0.5		VDD+ 0.5	V
Clock Outputs	Referenced to GND	-0.5		VDD+ 0.5	V
Storage Temperature		-65		150	°C
Soldering Temperature	Max 10 seconds			260	°C
Junction Temperature				125	°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (ICS341M)	0		+70	°C
Ambient Operating Temperature (ICS341MI)	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.15	+3.3	+3.45	V
Power Supply Ramp Time			4	ms

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3V ±5%**, Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15	3.3	3.45	V
Operating Supply Current Input High Voltage	IDD	Configuration Dependent - See VersaClock™				mA
		33.3333 MHz output, $\overline{PDTS}$ = 1, no load Note 1		11		mA
		$\overline{PDTS}$ = 0		20		µA
Input High Voltage	V_{IH}	S1:S0	2			V
Input Low Voltage	V_{IL}	S1:S0			0.4	V
Input High Voltage, $\overline{PDTS}$	V_{IH}		VDD-0.5			V
Input Low Voltage, $\overline{PDTS}$	V_{IL}				0.4	V
Input High Voltage	V_{IH}	ICLK	VDD/2+1			V
Input Low Voltage	V_{IL}	ICLK			VDD/2-1	V
Output High Voltage (CMOS High)	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Short Circuit Current	I_{OS}			±70		mA
Nominal Output Impedance	Z_O			20		Ω
Internal pull-up resistor	R_{PUP}	S1:S0		250		kΩ
Internal pull-up resistor	R_{PUP}	$\overline{PDTS}$		250		kΩ
Internal pull-down resistor	R_{PD}	CLK output		525		kΩ
Input Capacitance	C_{IN}	inputs		4		pF

Note 1: Example with 25 MHz crystal input with output of 33.$\overline{3}$ MHz, no load, and VDD = 3.3 V.

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3V ±5%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}	Fundamental Crystal	5		27	MHz
		Input Clock	2		50	MHz
Output Frequency			0.25		200	MHz
Output Rise Time	t_{OR}	20% to 80%, Note 1		1		ns
Output Fall Time	t_{OF}	80% to 20%, Note 1		1		ns
Duty Cycle		Note 2	40	49-51	60	%
Output Frequency Synthesis Error		Configuration Dependent		TBD		ppm
Power-up Time		PLL lock time from power-up		4	10	ms
		$\overline{PDTS}$ goes high until stable CLK output, Spread Spectrum Off		.2	2	ms
		$\overline{PDTS}$ goes high until stable CLK output, Spread Spectrum On		4	7	ms
One Sigma Clock Period Jitter		Configuration Dependent		50		ps
Maximum Absolute Jitter	t_{ja}	Deviation from Mean. Configuration Dependent		±200		ps

Note 1: Measured with 15 pF load.

Note 2: Duty Cycle is configuration dependent. Most configurations are minimum 45% and maximum 55%.

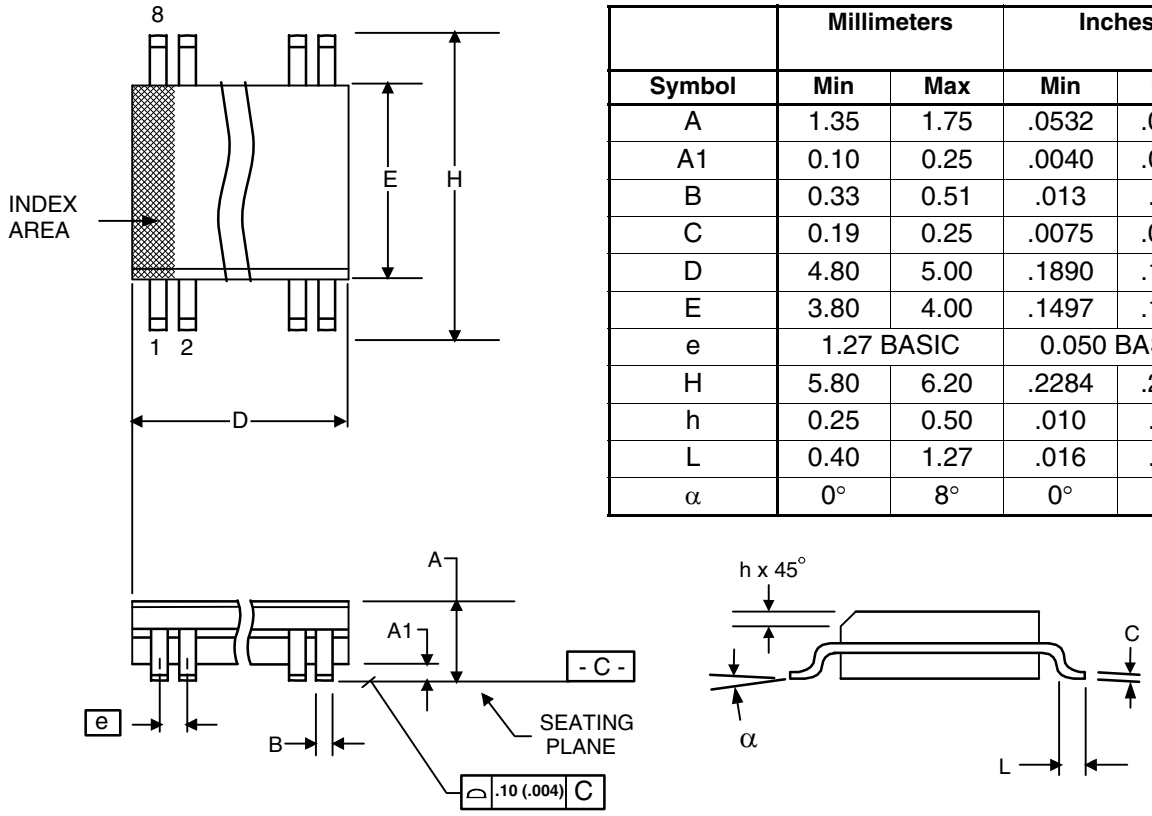
Note 3: ICS test mode output occurs for first 170 clock cycles on CLK for each PLL powered up. $\overline{PDTS}$ transition high on select address change.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
341MPLF	341MPLF	Tubes	8-pin SOIC	0 to +70° C
341MPLFT	341MPLF	Tape and Reel	8-pin SOIC	0 to +70° C
341MIPLF	341MIPLF	Tubes	8-pin SOIC	-40 to +85° C
341MIPLFT	341MIPLF	Tape and Reel	8-pin SOIC	-40 to +85° C
341MP-XXLF	341-XXMPLF	Tubes	8-pin SOIC	0 to +70° C
341MP-XXLFT	341-XXMPLF	Tape and Reel	8-pin SOIC	0 to +70° C
341MIP-XXLF	341-XXMIPLF	Tubes	8-pin SOIC	-40 to +85° C
341MIP-XXLFT	341-XXMIPLF	Tape and Reel	8-pin SOIC	-40 to +85° C

"LF" suffix to the part number denotes Pb-Free configuration, RoHS compliant.

The 341M-XXLF and 341MI-XXLF are factory programmed versions of the 341MPLF and 341MIPLF. A unique "-XX" suffix is assigned by the factory for each custom configuration, and a separate data sheet is kept on file. For more information on custom part numbers programmed at the factory, please contact your local IDT sales and marketing representative.

Revision History

Rev.	Date	Originator	Description of Change
M	09/06/13	S. Zheng	Added brief applications section/verbiage “Using VersaClock Products with an Input Clock Source” on page 3.
N	07/28/16	V.A.	Updated ordering information for factory programmables.

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