

# NCP1612

## Enhanced, High-Efficiency Power Factor Controller

The NCP1612 is designed to drive PFC boost stages based on an innovative *Current Controlled Frequency Fold-back (CCFF)* method. In this mode, the circuit classically operates in *Critical conduction Mode (CrM)* when the inductor current exceeds a programmable value. When the current is below this preset level, the NCP1612 linearly decays the frequency down to about 20 kHz when the current is null. *CCFF* maximizes the efficiency at both nominal and light load. In particular, the stand-by losses are reduced to a minimum.

Like in *FCCrM* controllers, an internal circuitry allows near-unity power factor even when the switching frequency is reduced. Housed in a SO-10 package, the circuit also incorporates the features necessary for robust and compact PFC stages, with few external components.

### General Features

- Near-Unity Power Factor
- Critical Conduction Mode (CrM)
- Current Controlled Frequency Fold-back (CCFF): Low Frequency Operation is Forced at Low Current Levels
- On-time Modulation to Maintain a Proper Current Shaping in CCFF Mode
- Skip Mode Near the Line Zero Crossing
- Fast Line / Load Transient Compensation (Dynamic Response Enhancer)
- Valley Turn On
- High Drive Capability: -500 mA/+800 mA
- $V_{CC}$  Range: from 9.5 V to 35 V
- Low Start-up Consumption
- A Version: Low  $V_{CC}$  Start-up Level (10.5 V), B Version: High  $V_{CC}$  Start-up Level (17.0 V)
- Line Range Detection
- pfcOK Signal
- This is a Pb-Free Device

### Safety Features

- Separate Pin for Fast Over-Voltage Protection (FOVP) and Bulk Under-Voltage Detection (BUV)
- Soft Over-Voltage Protection
- Brown-Out Detection
- Soft-Start for Smooth Start-up Operation (A version)
- Over Current Limitation
- Disable Protection if the Feedback and FOVP/BUV pins are not connected
- Thermal Shutdown

- Latched Off Capability
- Low Duty-Cycle Operation if the Bypass Diode is shorted
- Open Ground Pin Fault Monitoring

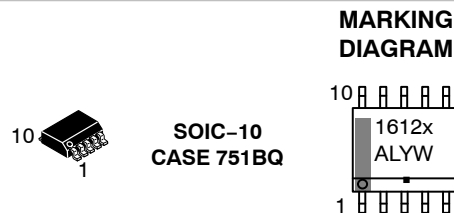
### Typical Applications

- PC Power Supplies
- All Off Line Appliances Requiring Power Factor Correction



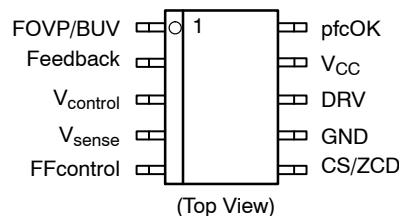
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1612x = Specific Device Code  
x = A or B  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 29 of this data sheet.

# NCP1612

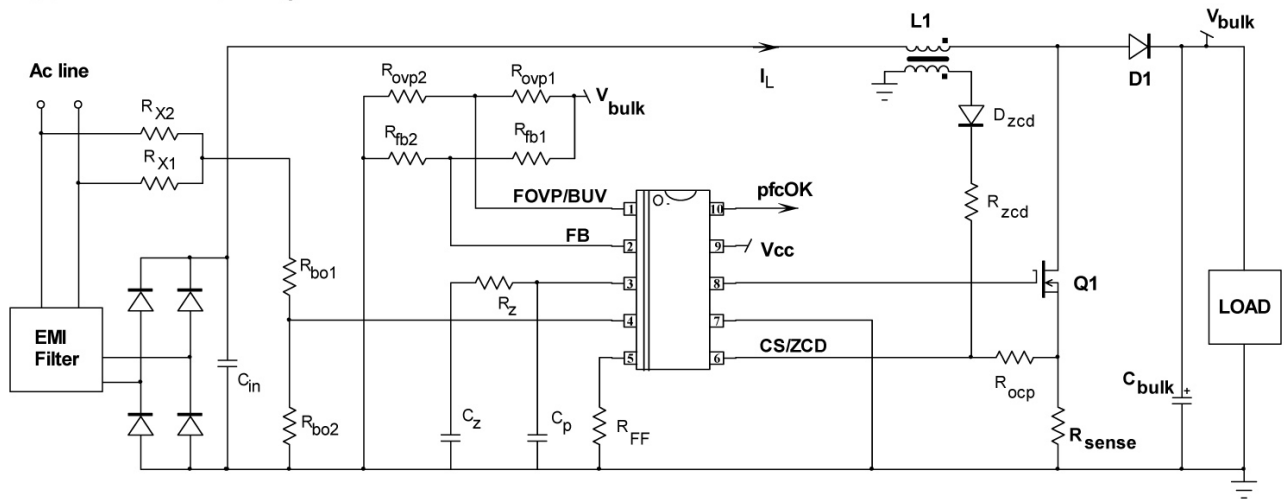


Figure 1. Typical Application Schematic

## MAXIMUM RATINGS TABLE

Symbol	Pin	Rating	Value	Unit
V <sub>CC</sub>	9	Power Supply Input	-0.3, +35	V
V <sub>i</sub>	1, 2, 4, 5, 10	Input Voltage (Note 1)	-0.3, +9	V
V <sub>i</sub> (CS/ZCD)	6	Input Voltage	-0.3, V <sub>CL(pos)*</sub>	V
V <sub>CONTROL</sub>	3	V <sub>CONTROL</sub> pin	-0.3, V <sub>CONTROLMAX*</sub>	V
DRV	8	Driver Voltage Driver Current	-0.3, V <sub>DRV*</sub> -500, +800	V mA
P <sub>D</sub> R <sub>θJA</sub>		Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T <sub>A</sub> = 70°C Thermal Resistance Junction-to-Air	550 145	mW °C/W
T <sub>J</sub>		Operating Junction Temperature Range	-40 to +125	°C
T <sub>Jmax</sub>		Maximum Junction Temperature	150	°C
T <sub>Smax</sub>		Storage Temperature Range	-65 to 150	°C
T <sub>Lmax</sub>		Lead Temperature (Soldering, 10s)	300	°C
MSL		Moisture Sensitivity Level	1	-
		ESD Capability, Human Body Model (Note 2)	> 2000	V
		ESD Capability, Machine Model (Note 2)	> 200	V
		ESD Capability, Charged Device Model (Note 2)	2000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

\*V<sub>CL(pos)</sub> is the CS/ZCD pin positive clamp voltage. "V<sub>CONTROLMAX</sub>" is the V<sub>CONTROL</sub> pin clamp voltage. "V<sub>DRV</sub>" is the DRV clamp voltage (V<sub>DRVhigh</sub>) if this clamp voltage is below V<sub>CC</sub>. "V<sub>DRV</sub>" is V<sub>CC</sub> otherwise.

- When the applied voltage exceeds 5 V, these pins sink about  $\frac{V_1 - 5 \text{ V}}{4 \text{ k}\Omega}$  that is about 1.25 mA if V<sub>i</sub> = 9 V
- This device(s) contains ESD protection and exceeds the following tests:  
Human Body Model 2000 V per JEDEC Standard JESD22-A114E  
Machine Model Method 200 V per JEDEC Standard JESD22-A115-A  
Charged Device Model Method 200 V per JEDEC Standard JESD22-C101E
- This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78.

# NCP1612

## TYPICAL ELECTRICAL CHARACTERISTICS (Conditions: $V_{CC} = 15\text{ V}$ , $T_J$ from $-40^\circ\text{C}$ to $+125^\circ\text{C}$ , unless otherwise specified)

Symbol	Rating	Min	Typ	Max	Unit
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### START-UP AND SUPPLY CIRCUIT

$V_{CC(on)}$	Start-Up Threshold, $V_{CC}$ increasing: A version B version	9.75 15.80	10.50 17.00	11.25 18.20	V
$V_{CC(off)}$	Minimum Operating Voltage, $V_{CC}$ falling	8.5	9.0	9.5	V
$V_{CC(HYST)}$	Hysteresis ( $V_{CC(on)} - V_{CC(off)}$ ) A version B version	0.75 6.00	1.50 8.00	- -	V
$V_{CC(reset)}$	$V_{CC}$ level below which the circuit resets	2.5	4.0	6.0	V
$I_{CC(start)}$	Start-Up Current, $V_{CC} = 9.4\text{ V}$	-	20	50	$\mu\text{A}$
$I_{CC(op)1}$	Operating Consumption, no switching ( $V_{SENSE}$ pin being grounded)	-	0.5	1.0	mA
$I_{CC(op)2}$	Operating Consumption, 50 kHz switching, no load on DRV pin	-	2.0	3.0	mA

### CURRENT CONTROLLED FREQUENCY FOLD-BACK

$T_{DT1}$	Dead-Time, $V_{FFcontrol} = 2.60\text{ V}$ (Note 4)	-	-	0	$\mu\text{s}$
$T_{DT2}$	Dead-Time, $V_{FFcontrol} = 1.75\text{ V}$	14	18	22	$\mu\text{s}$
$T_{DT3}$	Dead-Time, $V_{FFcontrol} = 1.00\text{ V}$	32	38	44	$\mu\text{s}$
$I_{DT1}$	FFcontrol Pin current, $V_{sense} = 1.4\text{ V}$ and $V_{control}$ maximum	180	200	220	$\mu\text{A}$
$I_{DT2}$	FFcontrol Pin current, $V_{sense} = 2.8\text{ V}$ and $V_{control}$ maximum	110	135	160	$\mu\text{A}$
$V_{SKIP-H}$	FFcontrol pin Skip Level, $V_{FFcontrol}$ rising	-	0.75	0.85	V
$V_{SKIP-L}$	FFcontrol pin Skip Level, $V_{FFcontrol}$ falling	0.55	0.65	-	V
$V_{SKIP-L}$	FFcontrol pin Skip Hysteresis	50	-	-	mV

### GATE DRIVE

$T_R$	Output voltage rise-time @ $C_L = 1\text{ nF}$ , 10-90% of output signal	-	30	-	ns
$T_F$	Output voltage fall-time @ $C_L = 1\text{ nF}$ , 10-90% of output signal	-	20	-	ns
$R_{OH}$	Source resistance	-	10	-	$\Omega$
$R_{OL}$	Sink resistance	-	7.0	-	$\Omega$
$I_{SOURCE}$	Peak source current, $V_{DRV} = 0\text{ V}$ (guaranteed by design)	-	500	-	mA
$I_{SINK}$	Peak sink current, $V_{DRV} = 12\text{ V}$ (guaranteed by design)	-	800	-	mA
$V_{DRVlow}$	DRV pin level at $V_{CC}$ close to $V_{CC(off)}$ with a 10 k $\Omega$ resistor to GND	8.0	-	-	V
$V_{DRVhigh}$	DRV pin level at $V_{CC} = 35\text{ V}$ ( $R_L = 33\text{ k}\Omega$ , $C_L = 220\text{ pF}$ )	10	12	14	V

### REGULATION BLOCK

$V_{REF}$	Feedback Voltage Reference: @ $25^\circ\text{C}$ Over the temperature range	2.44 2.42	2.50 2.50	2.54 2.54	V
$I_{EA}$	Error Amplifier Current Capability	-	$\pm 20$	-	$\mu\text{A}$
$G_{EA}$	Error Amplifier Gain	110	220	290	$\mu\text{S}$
$V_{CONTROL}$ $-V_{CONTROLMAX}$ $-V_{CONTROLMIN}$	$V_{CONTROL}$ Pin Voltage: - @ $V_{FB} = 2\text{ V}$ - @ $V_{FB} = 3\text{ V}$	- -	4.5 0.5	- -	V
$V_{OUTL} / V_{REF}$	Ratio ( $V_{OUT}$ Low Detect Threshold / $V_{REF}$ ) (guaranteed by design)	95.0	95.5	96.0	%
$H_{OUTL} / V_{REF}$	Ratio ( $V_{OUT}$ Low Detect Hysteresis / $V_{REF}$ ) (guaranteed by design)	-	-	0.5	%
$I_{BOOST}$	$V_{CONTROL}$ Pin Source Current when ( $V_{OUT}$ Low Detect) is activated	180	220	250	$\mu\text{A}$

4. There is actually a minimum dead-time that is the delay between the core reset detection and the DRV turning on ( $T_{ZCD}$  parameter of the "Current Sense and Zero Current Detection Blocks" section).

# NCP1612

## TYPICAL ELECTRICAL CHARACTERISTICS (Conditions: $V_{CC} = 15\text{ V}$ , $T_J$ from $-40^\circ\text{C}$ to $+125^\circ\text{C}$ , unless otherwise specified)

Symbol	Rating	Min	Typ	Max	Unit
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### CURRENT SENSE AND ZERO CURRENT DETECTION BLOCKS

$V_{CS(th)}$	Current Sense Voltage Reference	450	500	550	mV
$T_{LEB, OCP}$	Over-Current Protection Leading Edge Blanking Time (guaranteed by design)	100	200	350	ns
$T_{LEB, OVS}$	“OverStress” Leading Edge Blanking Time (guaranteed by design)	50	100	170	ns
$T_{OCP}$	Over-Current Protection Delay from $V_{CS/ZCD} > V_{CS(th)}$ to DRV low ( $dV_{CS/ZCD} / dt = 10\text{ V}/\mu\text{s}$ )	–	40	200	ns
$V_{ZCD(th)H}$	Zero Current Detection, $V_{CS/ZCD}$ rising	675	750	825	mV
$V_{ZCD(th)L}$	Zero Current Detection, $V_{CS/ZCD}$ falling	200	250	300	mV
$V_{ZCD(hyst)}$	Hysteresis of the Zero Current Detection Comparator	375	500	–	mV
$R_{ZCD/CS}$	$V_{ZCD(th)H}$ over $V_{CS(th)}$ Ratio	1.4	1.5	1.6	–
$V_{CL(pos)}$	CS/ZCD Positive Clamp @ $I_{CS/ZCD} = 5\text{ mA}$	–	15.6	–	V
$I_{ZCD(bias)}$	Current Sourced by the CS/ZCD Pin, $V_{CS/ZCD} = V_{ZCD(th)H}$	0.5	–	2.0	$\mu\text{A}$
$I_{ZCD(bias)}$	Current Sourced by the CS/ZCD Pin, $V_{CS/ZCD} = V_{ZCD(th)L}$	0.5	–	2.0	$\mu\text{A}$
$T_{ZCD}$	( $V_{CS/ZCD} < V_{ZCD(th)L}$ ) to (DRV high)	–	60	200	ns
$T_{SYNC}$	Minimum ZCD Pulse Width	–	110	200	ns
$T_{WDG}$	Watch Dog Timer	80	200	320	$\mu\text{s}$
$T_{WDG(OS)}$	Watch Dog Timer in “Overstress” Situation	400	800	1200	$\mu\text{s}$
$T_{TMO}$	Time-Out Timer	20	30	50	$\mu\text{s}$
$I_{ZCD(gnd)}$	Source Current for CS/ZCD pin impedance Testing	–	250	–	$\mu\text{A}$

### STATIC OVP

$D_{MIN}$	Duty Cycle, $V_{FB} = 3\text{ V}$ , $V_{control}$ pin open	–	–	0	%
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### ON-TIME CONTROL

$T_{ON(LL)}$	Maximum On Time, $V_{sense} = 1.4\text{ V}$ and $V_{control}$ maximum (CrM)	22.0	25.0	29.0	$\mu\text{s}$
$T_{ON(LL)2}$	On Time, $V_{sense} = 1.4\text{ V}$ and $V_{control} = 2.5\text{ V}$ (CrM)	10.5	12.5	14.0	$\mu\text{s}$
$T_{ON(HL)}$	Maximum On Time, $V_{sense} = 2.8\text{ V}$ and $V_{control}$ maximum (CrM)	7.3	8.5	9.6	$\mu\text{s}$
$T_{ON(LL)(MIN)}$	Minimum On Time, $V_{sense} = 1.4\text{ V}$ (not tested, guaranteed by characterization)	–	–	200	ns
$T_{ON(HL)(MIN)}$	Minimum On Time, $V_{sense} = 2.8\text{ V}$ (not tested, guaranteed by characterization)	–	–	100	ns

### FEED-BACK OVER AND UNDER-VOLTAGE PROTECTION (SOFT OVP AND UVP)

$R_{softOVP}$	Ratio (soft OVP Threshold, $V_{FB}$ rising) over $V_{REF}$ ( $V_{softOVP}/V_{REF}$ ) (guaranteed by design)	104	105	106	%
$R_{softOVP(HYST)}$	Ratio (Soft OVP Hysteresis) over $V_{REF}$ (guaranteed by design)	1.5	2.0	2.5	%
$R_{UVP}$	Ratio (UVP Threshold, $V_{FB}$ rising) over $V_{REF}$ ( $V_{UVP}/V_{REF}$ ) (guaranteed by design)	8	12	16	%
$R_{UVP(HYST)}$	Ratio (UVP Hysteresis) over $V_{REF}$ (guaranteed by design)	–	–	1	%
$(I_B)_{FB}$	FB Pin Bias Current @ $V_{FB} = V_{softOVP}$ and $V_{FB} = V_{UVP}$	50	200	450	nA

### FAST OVER VOLTAGE PROTECTION AND BULK UNDER-VOLTAGE PROTECTION (FAST OVP AND BUVP)

$V_{fastOVP}$	Latching Fast OVP Threshold, $V_{FOVP/BUVP}$ rising	–	2.7	–	V
$R_{fastOVP1}$	Ratio (Fast OVP Threshold, $V_{FOVP/BUVP}$ rising) over (soft OVP Threshold, $V_{FB}$ rising) ( $V_{fastOVP}/V_{softOVP}$ ) (guaranteed by design)	101.5	102.0	102.5	%
$R_{fastOVP2}$	Ratio (Fast OVP Threshold, $V_{FOVP/BUVP}$ rising) over $V_{REF}$ ( $V_{fastOVP}/V_{REF}$ ) (guaranteed by design)	106	107	108	%
$V_{BUVP}$	BUVP Threshold, $V_{FOVP/BUVP}$ falling	–	1.9	–	V

4. There is actually a minimum dead-time that is the delay between the core reset detection and the DRV turning on ( $T_{ZCD}$  parameter of the “Current Sense and Zero Current Detection Blocks” section).

# NCP1612

**TYPICAL ELECTRICAL CHARACTERISTICS** (Conditions:  $V_{CC} = 15\text{ V}$ ,  $T_J$  from  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise specified)

Symbol	Rating	Min	Typ	Max	Unit
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## FAST OVER VOLTAGE PROTECTION AND BULK UNDER-VOLTAGE PROTECTION (FAST OVP AND BUV)

$R_{BUV}$	Ratio (BUV Threshold, $V_{FOVP/BUV}$ falling) over $V_{REF}$ ( $V_{BUV}/V_{REF}$ ) (guaranteed by design)	74	76	78	%
$(I_B)_{FOVP/BUV}$	FOVP/BUV Pin Bias Current @ $V_{FOVP/BUV} = V_{fastOVP}$ and $V_{FOVP/BUV} = V_{BUV}$	50	200	450	nA
$V_{UVP2}$	Threshold for Floating Pin Detection	0.2	0.3	0.4	V

## BROWN-OUT PROTECTION AND FEED-FORWARD

$V_{BOH}$	Brown-Out Threshold, $V_{sense}$ rising	0.96	1.00	1.04	V
$V_{BOL}$	Brown-Out Threshold, $V_{sense}$ falling	0.86	0.90	0.94	V
$V_{BO(HYST)}$	Brown-Out Comparator Hysteresis	60	100	–	mV
$T_{BO(blank)}$	Brown-Out Blanking Time	35	50	65	ms
$I_{CONTROL(BO)}$	$V_{CONTROL}$ Pin Sink Current, $V_{sense} < V_{BOL}$	40	50	60	$\mu\text{A}$
$V_{HL}$	High-Line Detection Comparator Threshold, $V_{sense}$ rising	2.1	2.2	2.3	V
$V_{LL}$	High-Line Detection Comparator Threshold, $V_{sense}$ falling	1.6	1.7	1.8	V
$V_{HL(hyst)}$	High-Line Detection Comparator Hysteresis	400	500	600	mV
$T_{HL(blank)}$	Blanking Time for Line Range Detection	15	25	35	ms
$I_{BO(bias)}$	Brown-Out Pin Bias Current, $V_{sense} = V_{BO}$	–250	–	250	nA

## pfcOK SIGNAL

$(V_{pfcOK})_L$	pfcOK low state voltage @ $I_{pfcOK} = 5\text{ mA}$	–	–	250	mV
$V_{STDWN}$	Shutdown Threshold Voltage	7.0	7.5	8.0	V
$R_{pfcOK}$	Impedance of the pfcOK pin	150	300	–	k $\Omega$

## THERMAL SHUTDOWN

$T_{LIMIT}$	Thermal Shutdown Threshold	–	150	–	$^\circ\text{C}$
$H_{TEMP}$	Thermal Shutdown Hysteresis	–	50	–	$^\circ\text{C}$

4. There is actually a minimum dead-time that is the delay between the core reset detection and the DRV turning on ( $T_{ZCD}$  parameter of the “Current Sense and Zero Current Detection Blocks” section).

## DETAILED PIN DESCRIPTION

Pin Number	Name	Function
1	FOVP / BUV	$V_{pin1}$ is the input signal for the Fast Over-Voltage (FOVP) and Bulk Under-Voltage (BUV) comparators. The circuit disables the driver if $V_{pin1}$ exceeds the FOVP threshold which is set 2% higher than the reference for the soft OVP comparator (that monitors the feedback pin) so that pins 1 and 2 can receive the same portion of the output voltage. The BUV comparator trips when $V_{pin1}$ drops below 76% of the 2.5 V reference voltage to disable the driver and ground the pfcOK pin. The BUV function has no action whenever the pfcOK pin is in low state. As a matter of fact, pin1 monitors the output voltage and checks if it is high enough for proper operation of the downstream converter. A 250 nA sink current is built-in to ground the pin and disable the driver if the pin is accidentally open.
2	Feedback	This pin receives a portion of the PFC output voltage for the regulation and the Dynamic Response Enhancer (DRE) that drastically speeds-up the loop response when the output voltage drops below 95.5% of the desired output level. $V_{pin2}$ is also the input signal for the Over-Voltage (OVP) and Under-Voltage (UVP) comparators. The UVP comparator prevents operation as long as $V_{pin2}$ is lower than 12% of the reference voltage ( $V_{REF}$ ). A soft OVP comparator gradually reduces the duty-ratio to zero when $V_{pin2}$ exceeds 105% of $V_{REF}$ (soft OVP). A 250 A sink current is built-in to trigger the UVP protection and disable the part if the feedback pin is accidentally open.

# NCP1612

## DETAILED PIN DESCRIPTION

Pin Number	Name	Function
3	V <sub>CONTROL</sub>	The error amplifier output is available on this pin. The network connected between this pin and ground adjusts the regulation loop bandwidth that is typically set below 20 Hz to achieve high Power Factor ratios. Pin 3 is grounded when the circuit is off so that when it starts operation, the power increases slowly to provide a soft-start function.
4	V <sub>SENSE</sub>	A portion of the instantaneous input voltage is to be applied to pin4 in order to detect brown-out conditions. If $V_{pin4}$ is lower than 1 V for more than 50 ms, the circuit stops pulsing until the pin voltage rises again and exceeds 1 V. This pin also detects the line range. By default, the circuit operates the "low-line gain" mode. If $V_{pin4}$ exceeds 1.8 V, the circuit detects a high-line condition and reduces the loop gain by 3. Conversely, if the pin voltage remains lower than 1.8 V for more than 25 ms, the low-line gain is set. Connecting the pin 4 to ground disables the part.
5	FF <sub>CONTROL</sub>	This pin sources a current representative to the line current. Connect a resistor between pin5 and ground to generate a voltage representative of the line current. When this voltage exceeds the internal 2.5 V reference ( $V_{REF}$ ), the circuit operates in critical conduction mode. If the pin voltage is below 2.5 V, a dead-time is generated that approximately equates $[83 \mu s \cdot (1 - (V_{pin5}/V_{REF}))]$ . By this means, the circuit forces a longer dead-time when the current is small and a shorter one as the current increases. The circuit skips cycles whenever $V_{pin5}$ is below 0.65 V to prevent the PFC stage from operating near the line zero crossing where the power transfer is particularly inefficient. This does result in a slightly increased distortion of the current. If superior power factor is required, offset pin 5 by more than 0.75 V offset to inhibit the skip function.
6	CS / ZCD	This pin monitors the MOSFET current to limit its maximum current. This pin is also connected to an internal comparator for Zero Current Detection (ZCD). This comparator is designed to monitor a signal from an auxiliary winding and to detect the core reset when this voltage drops to zero. The auxiliary winding voltage is to be applied through a diode to avoid altering the current sense information for the on-time (see application schematic).
7	Ground	Connect this pin to the PFC stage ground.
8	Drive	The high-current capability of the totem pole gate drive (-0.5/+0.8 A) makes it suitable to effectively drive high gate charge power MOSFETs.
9	V <sub>CC</sub>	This pin is the positive supply of the IC. The circuit starts to operate when $V_{CC}$ exceeds 10.5 V (A version, 17.0 V for the B version) and turns off when $V_{CC}$ goes below 9.0 V (typical values). After start-up, the operating range is 9.5 V up to 35 V.
10	pfcOK	This pin is grounded until the PFC output has reached its nominal level. It is also grounded if the NCP1612 detects a fault. For the rest of the time, i.e., when the PFC stage outputs the nominal bulk voltage, pin10 is in high-impedance state. This circuit latches off if pin10 exceeds 7.5 V.

# NCP1612

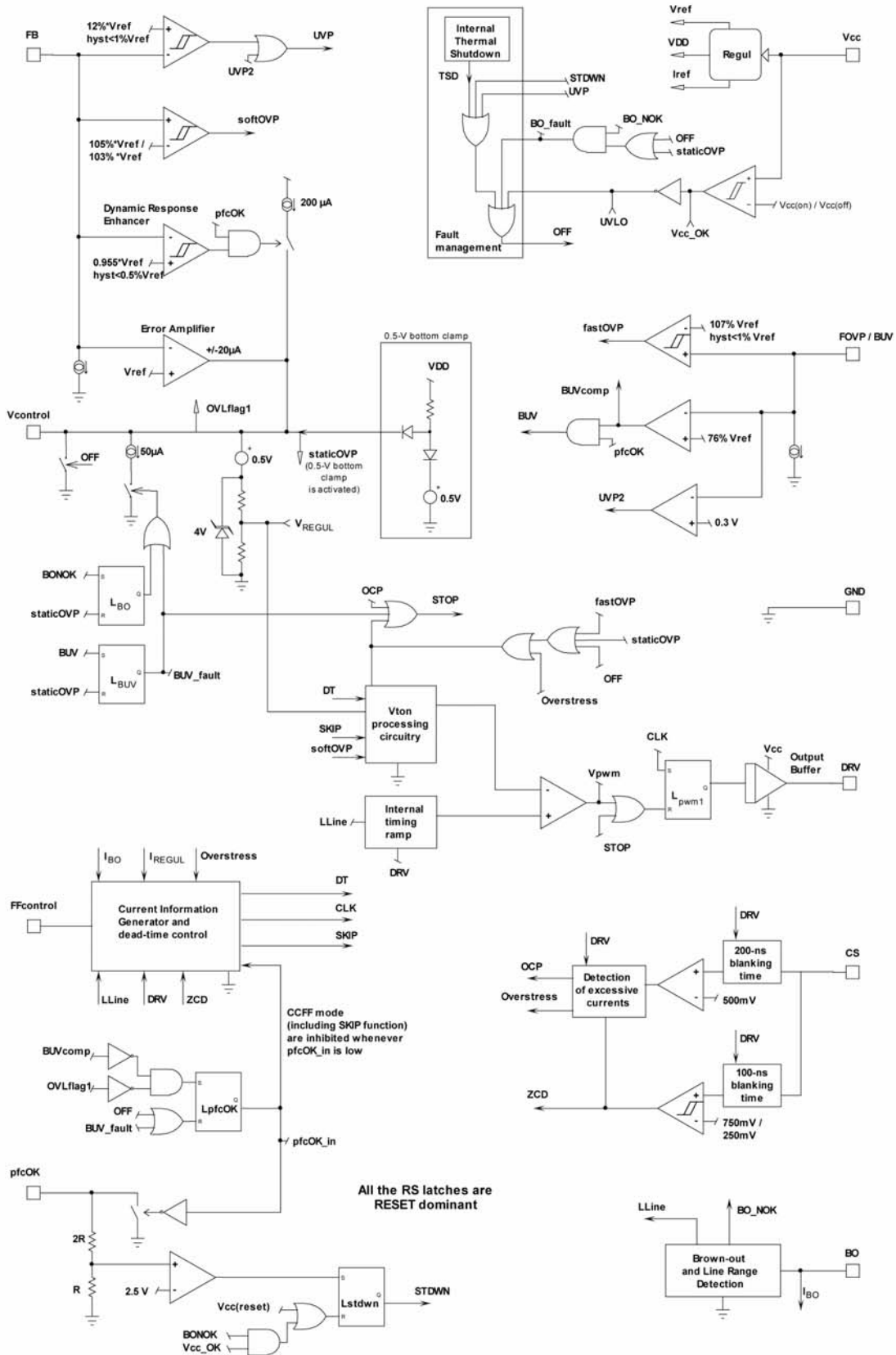


Figure 2. Block Diagram

TYPICAL CHARACTERISTICS

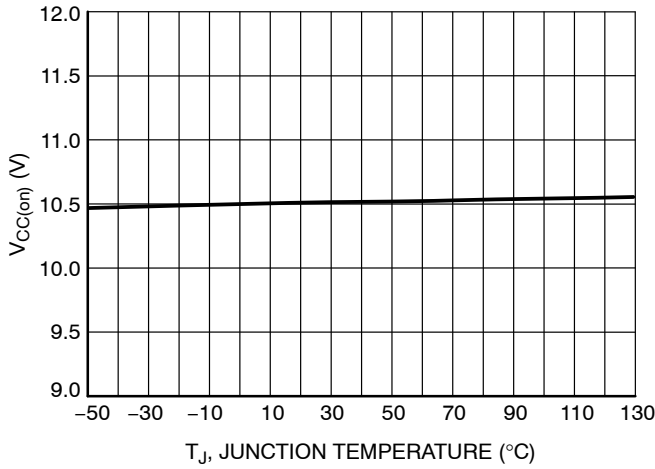


Figure 3. Start-Up Threshold,  $V_{CC}$  Increasing ( $V_{CC(on)}$ ) vs. Temperature (A Version)

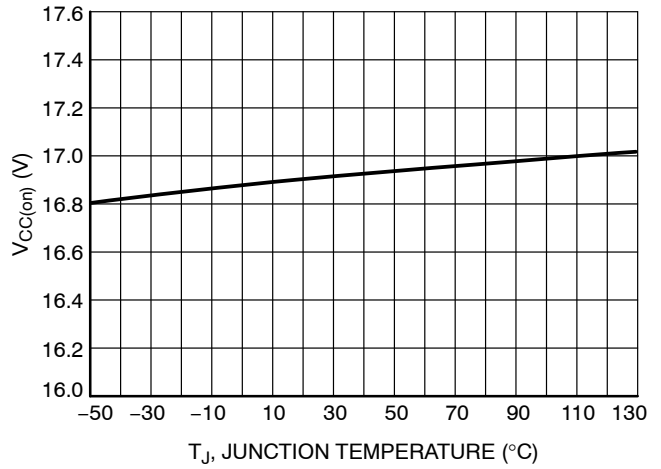


Figure 4. Start-Up Threshold,  $V_{CC}$  Increasing ( $V_{CC(on)}$ ) vs. Temperature (B Version)

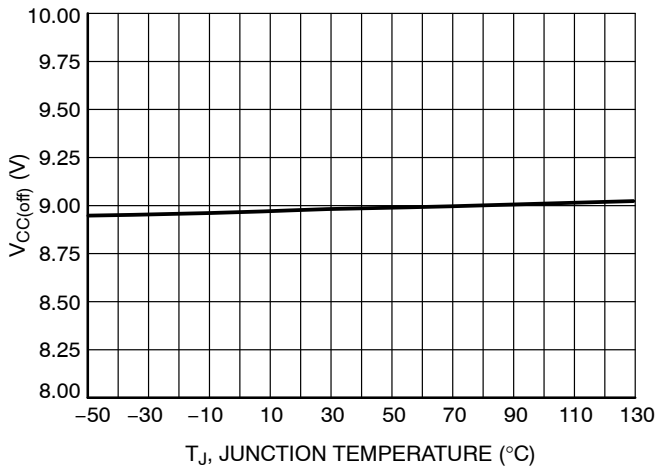


Figure 5.  $V_{CC}$  Minimum Operating Voltage,  $V_{CC}$  Falling ( $V_{CC(off)}$ ) vs. Temperature

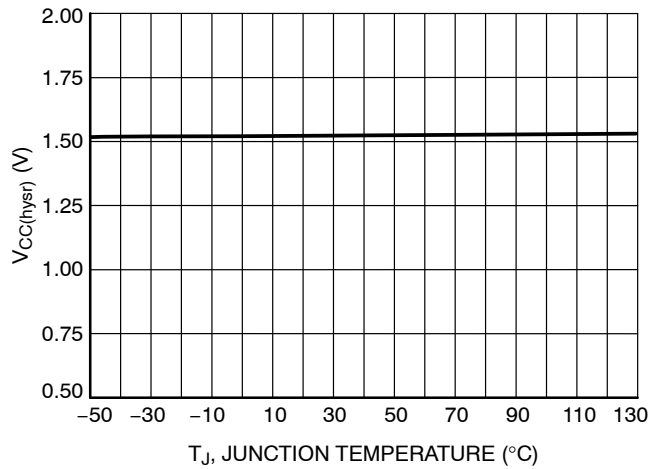


Figure 6. Hysteresis ( $V_{CC(on)} - V_{CC(off)}$ ) vs. Temperature (A Version)

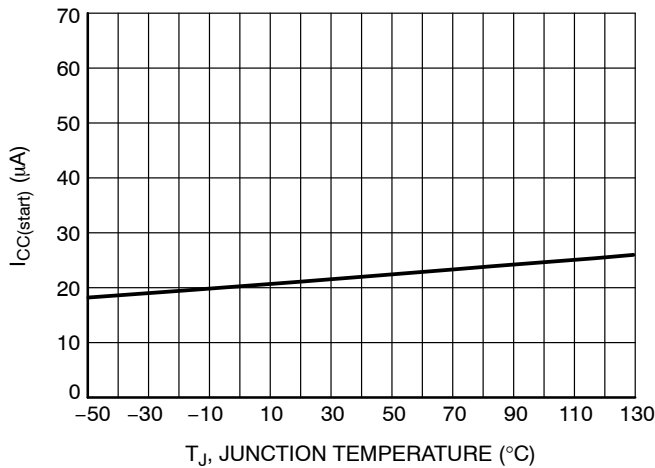


Figure 7. Start-Up Current @  $V_{CC} = 9.4$  V vs. Temperature

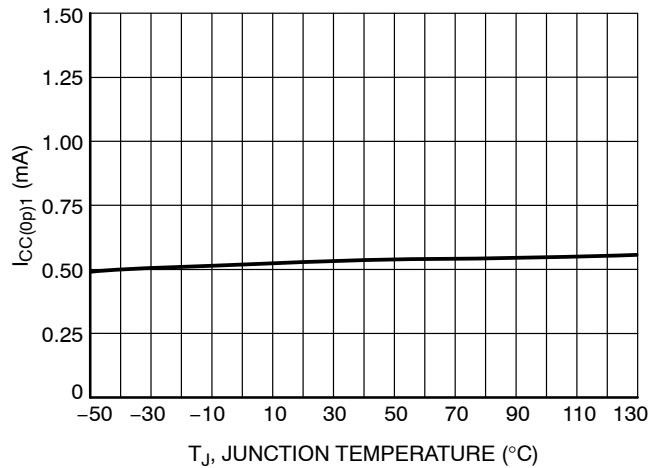


Figure 8. Operating Current, No Switching ( $V_{SENSE}$  Grounded) vs. Temperature



TYPICAL CHARACTERISTICS

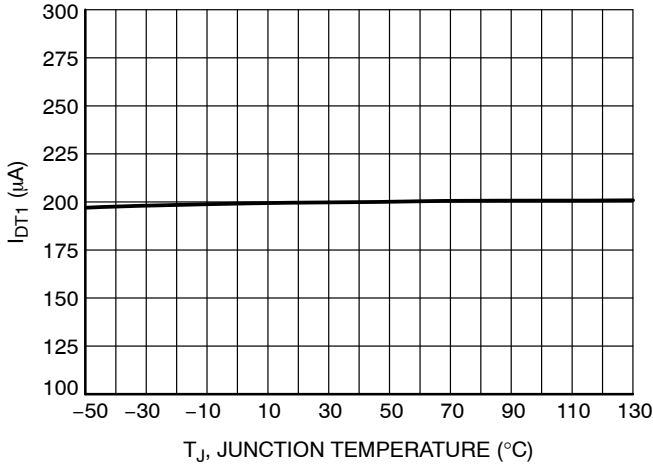


Figure 9. FFcontrol Pin Current,  $V_{SENSE} = 1.4\text{ V}$  and  $V_{CONTROL}$  Maximum vs. Temperature

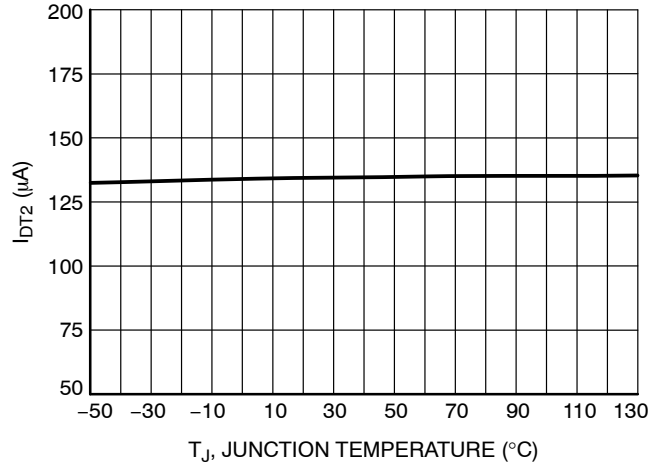


Figure 10. FFcontrol Pin Current,  $V_{SENSE} = 2.8\text{ V}$  and  $V_{CONTROL}$  Maximum vs. Temperature

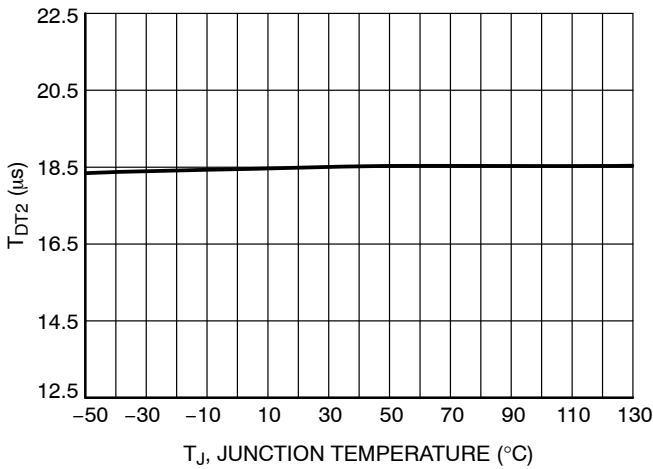


Figure 11. Dead-Time,  $V_{FFcontrol} = 1.75\text{ V}$  vs. Temperature

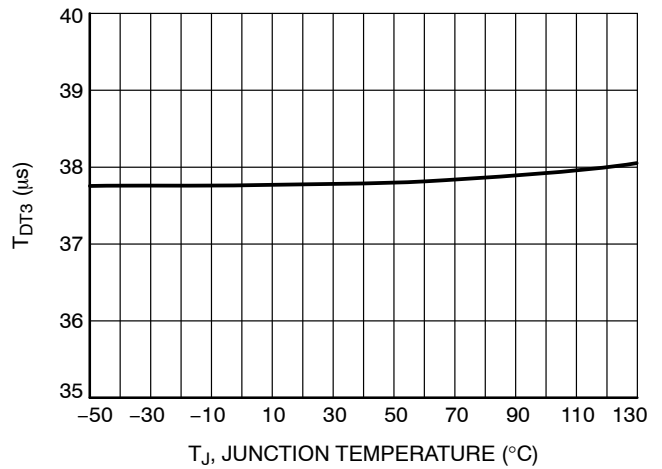


Figure 12. Dead-Time,  $V_{FFcontrol} = 1.00\text{ V}$  vs. Temperature

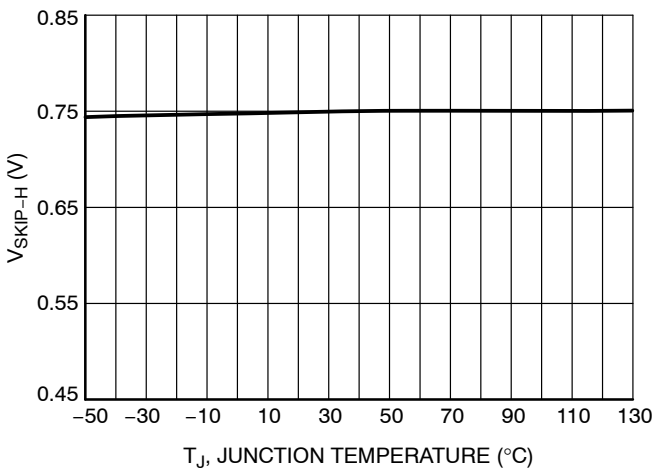


Figure 13. FFcontrol Pin Skip Level ( $V_{FFcontrol}$  Rising) vs. Temperature

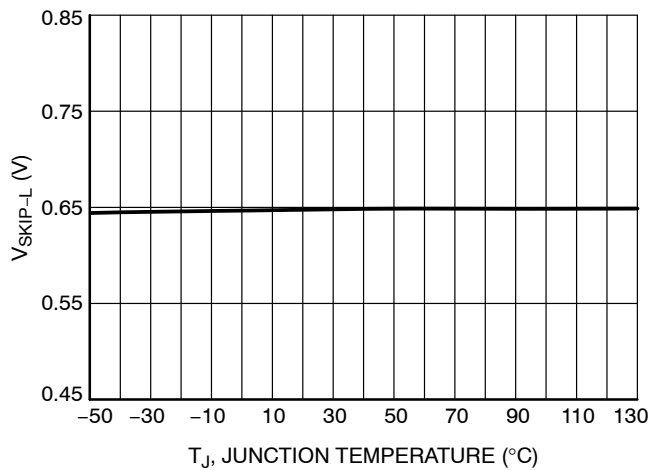


Figure 14. FFcontrol Pin Skip Level ( $V_{FFcontrol}$  Falling) vs. Temperature

TYPICAL CHARACTERISTICS

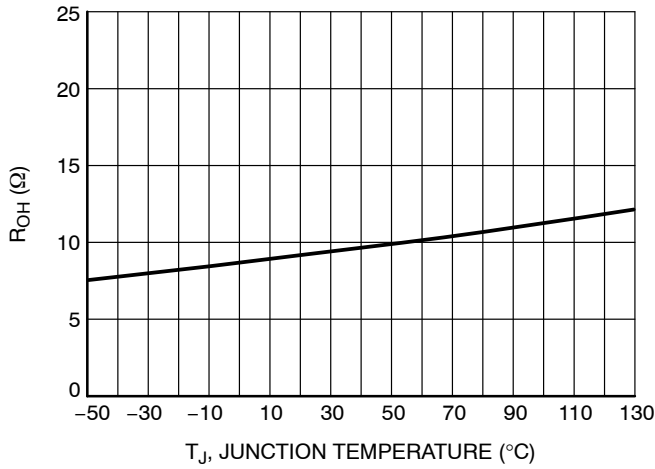


Figure 15. DRV Source Resistance vs. Temperature

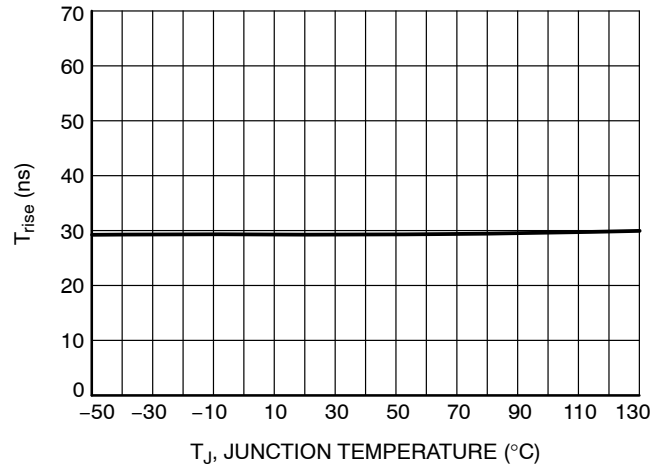


Figure 16. DRV Voltage Rise-Time (C<sub>L</sub> = 1 nF, 10–90% of Output Signal) vs. Temperature

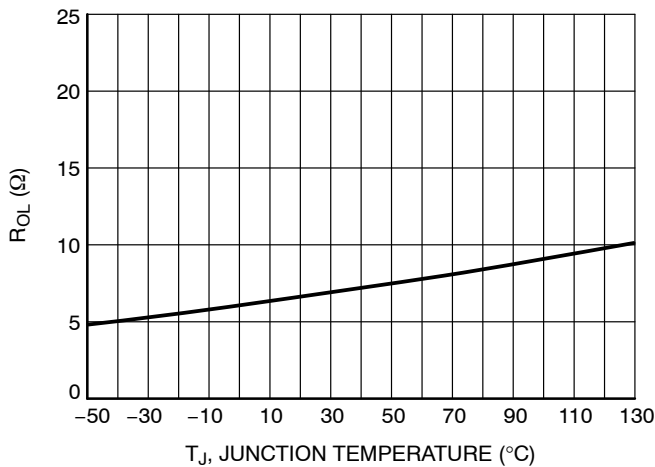


Figure 17. DRV Sink Resistance vs. Temperature

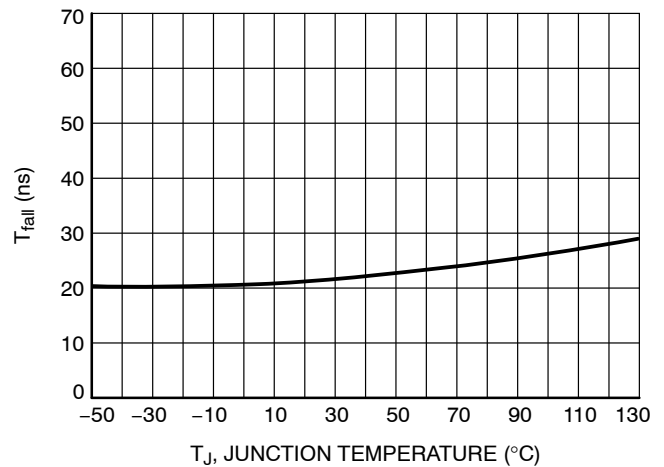


Figure 18. DRV Voltage Fall-Time (C<sub>L</sub> = 1 nF, 10–90% of Output Signal) vs. Temperature

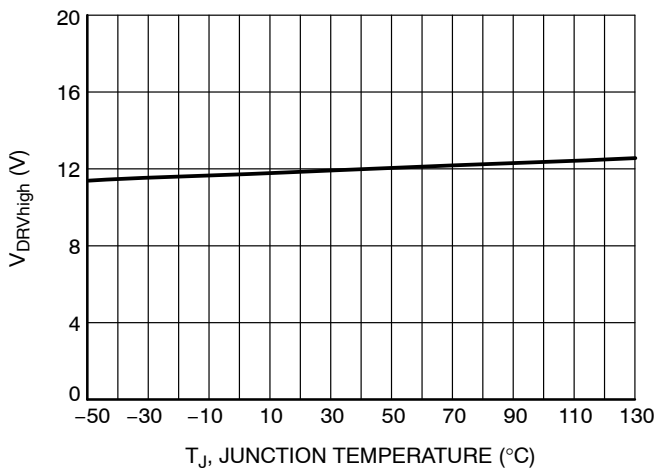


Figure 19. DRV Pin Level @ V<sub>CC</sub> = 35 V (R<sub>L</sub> = 33 kΩ, C<sub>L</sub> = 1 nF) vs. Temperature

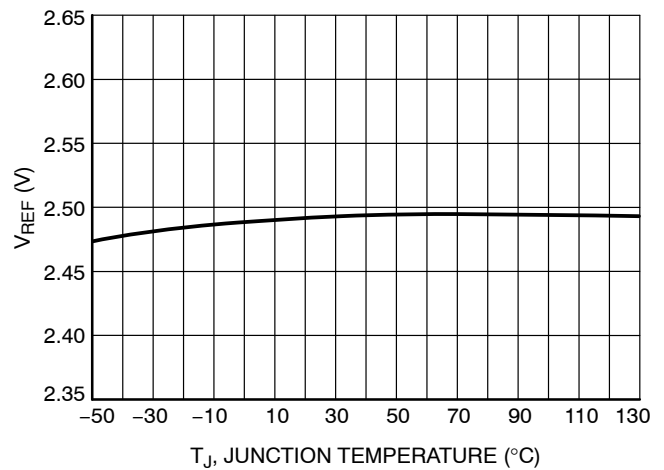


Figure 20. Feedback Reference Voltage vs. Temperature

TYPICAL CHARACTERISTICS

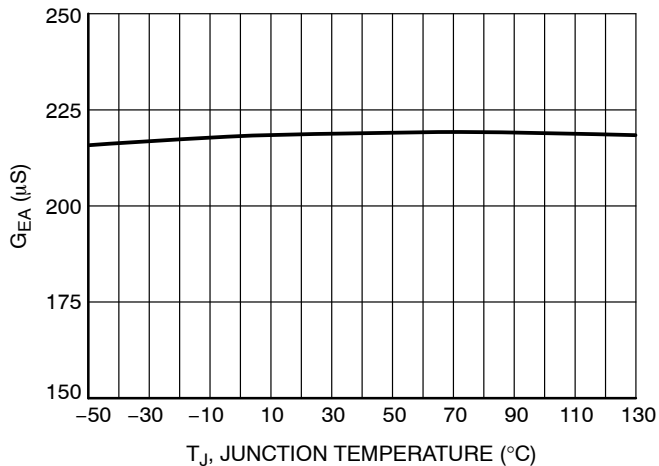


Figure 21. Error Amplifier Transconductance Gain vs. Temperature

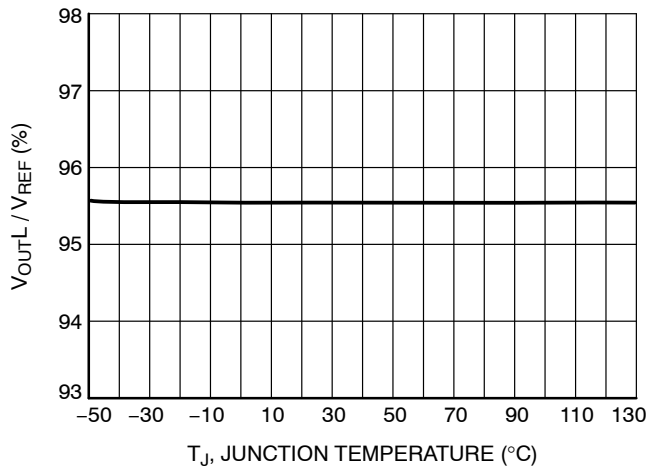


Figure 22. Ratio (V<sub>OUT</sub> Low Detect Threshold / V<sub>REF</sub>) vs. Temperature

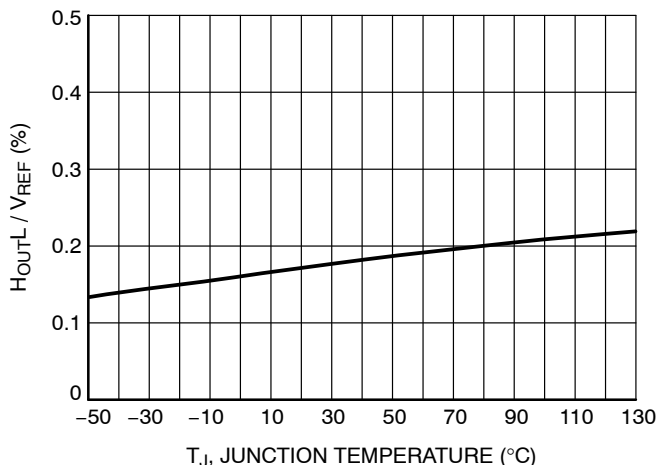


Figure 23. Ratio (V<sub>OUT</sub> Low Detect Hysteresis / V<sub>REF</sub>) vs. Temperature

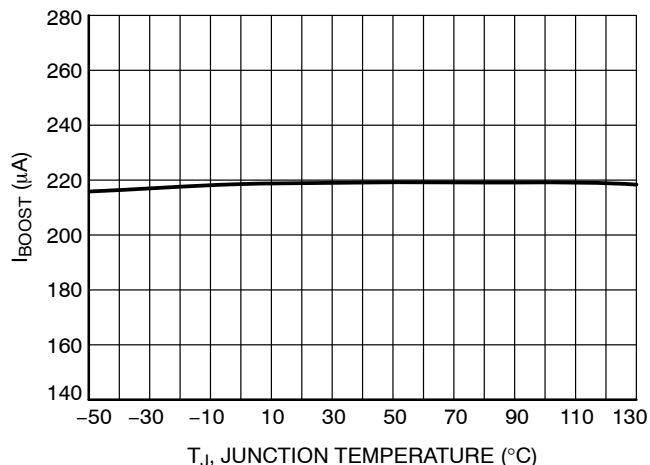


Figure 24. V<sub>CONTROL</sub> Source Current when (V<sub>OUT</sub> Low Detect) is Activated for Dynamic Response Enhancer (DRE) vs. Temperature

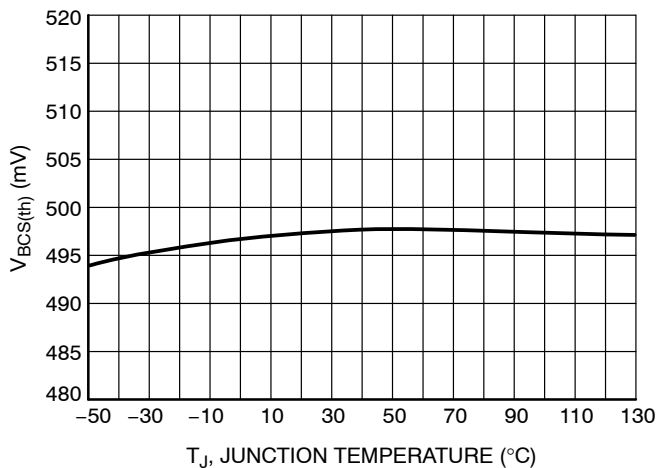


Figure 25. Current Sense Voltage Threshold vs. Temperature

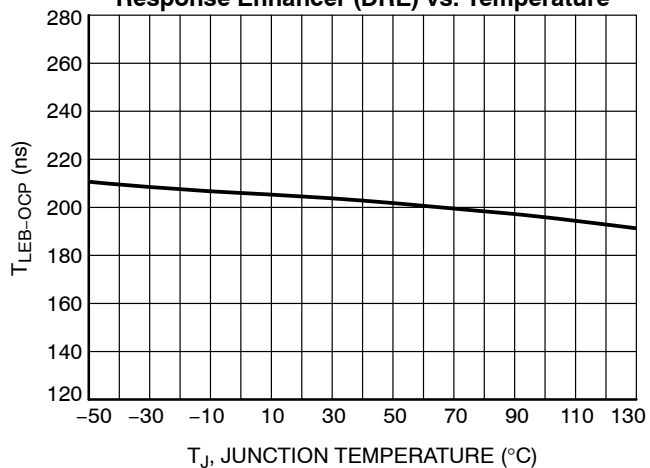


Figure 26. Over-Current Protection Leading Edge Blanking vs. Temperature

TYPICAL CHARACTERISTICS

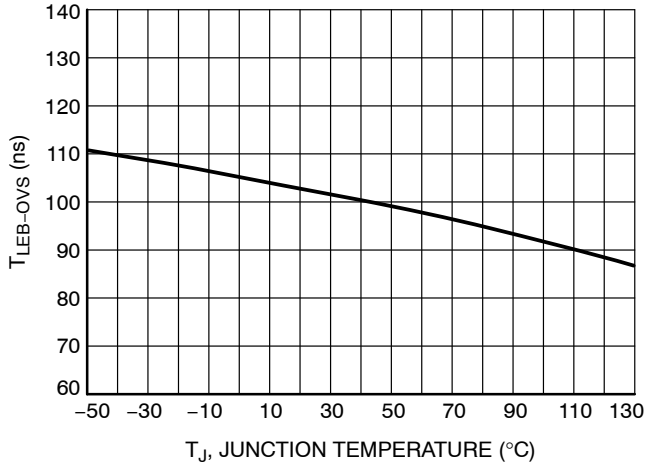


Figure 27. “Overstress” Protection Leading Edge Blanking vs. Temperature

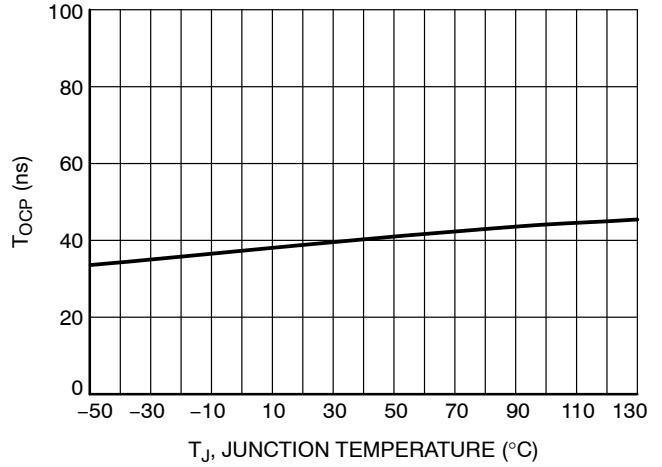


Figure 28. Over-Current Protection Delay from V<sub>CS/ZCD</sub> > V<sub>CS(th)</sub> to DRV Low (dV<sub>CS/ZCD</sub> / dt = 10 V/μs) vs. Temperature

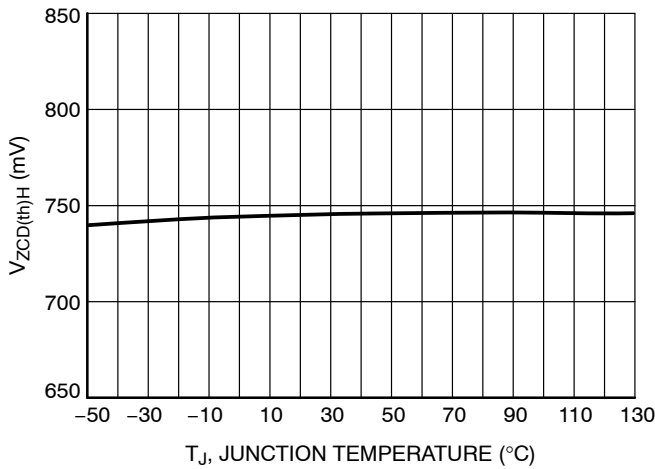


Figure 29. Zero Current Detection, V<sub>CS/ZCD</sub> Rising vs. Temperature

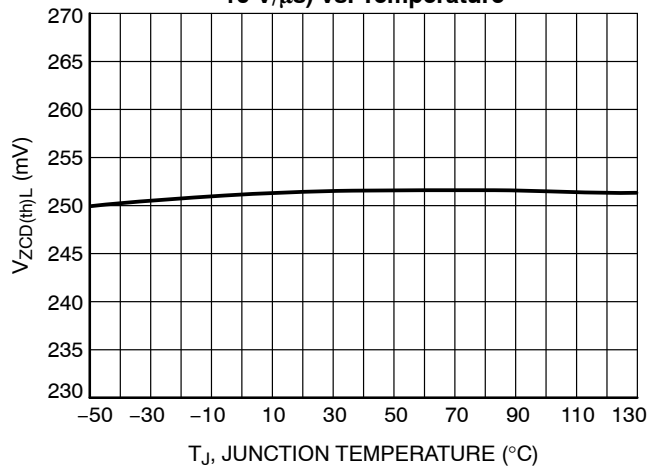


Figure 30. Zero Current Detection, V<sub>CS/ZCD</sub> Falling vs. Temperature

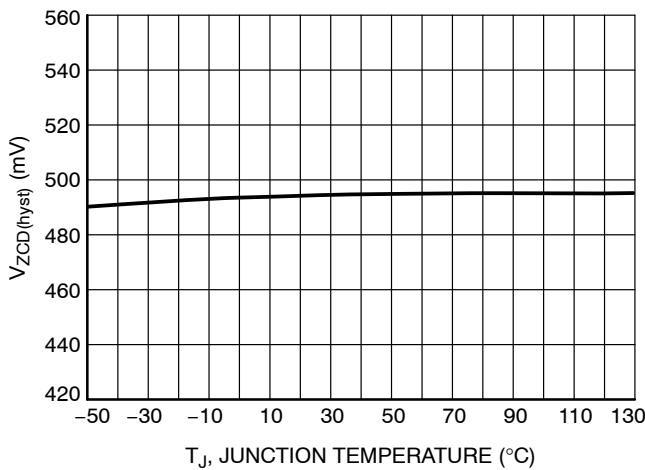


Figure 31. Hysteresis of the Zero Current Detection Comparator vs. Temperature

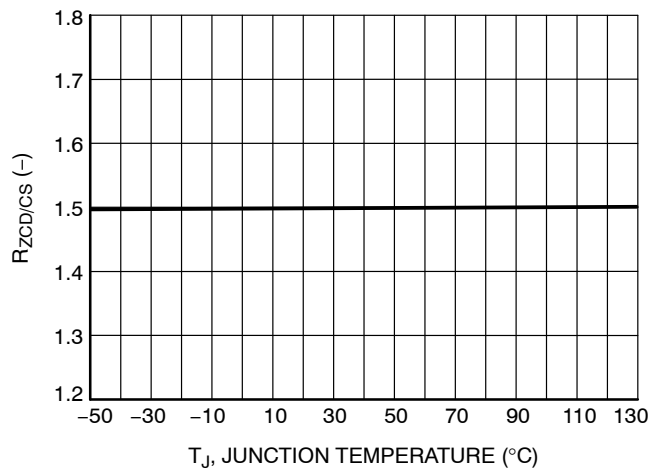


Figure 32. V<sub>ZCD(th)</sub> over V<sub>CS(th)</sub> Ratio vs. Temperature

TYPICAL CHARACTERISTICS

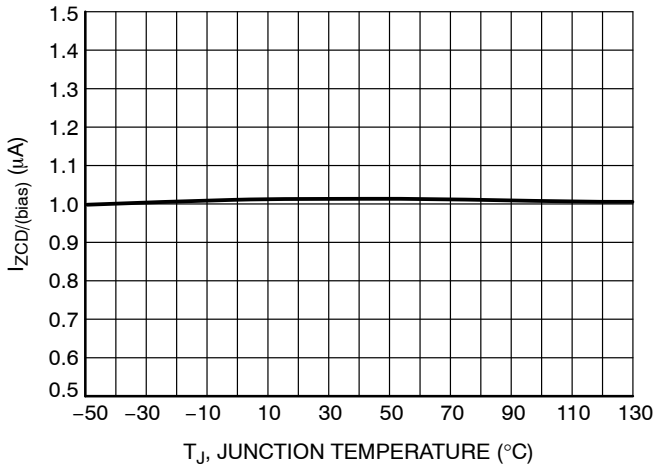


Figure 33. CS/ZCD Pin Bias Current @ V<sub>CS/ZCD</sub> = 0.75 V vs. Temperature

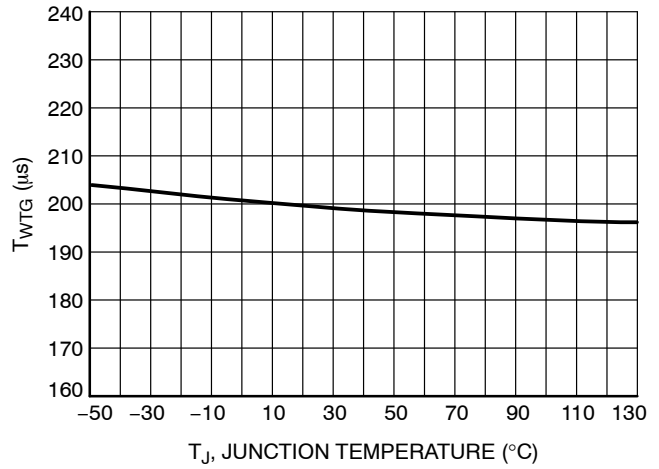


Figure 34. Watchdog Timer vs. Temperature

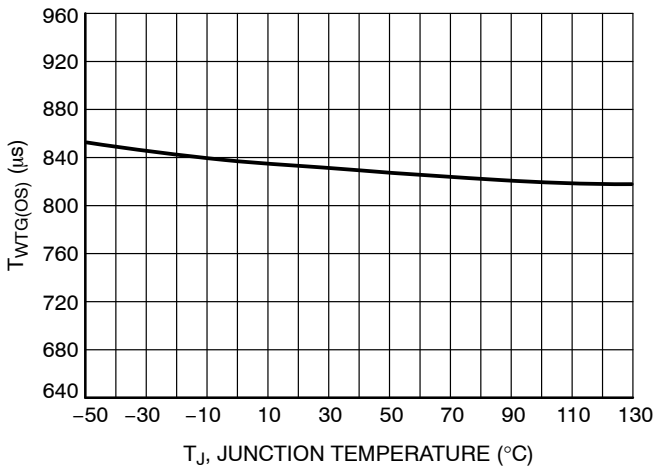


Figure 35. Watchdog Timer in "Overstress" Situation vs. Temperature

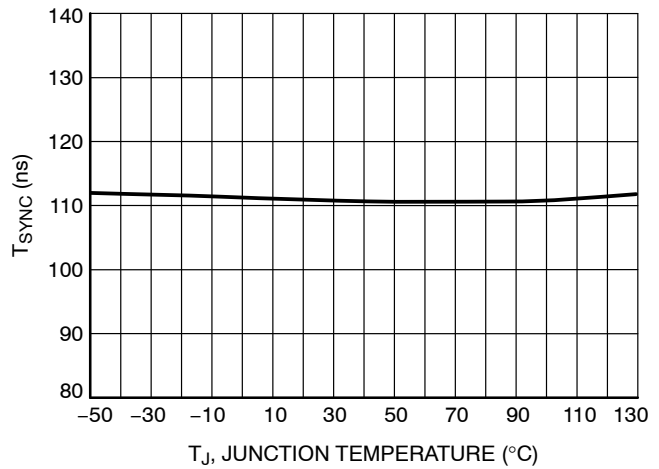


Figure 36. Minimum ZCD Pulse Width for ZCD Detection vs. Temperature

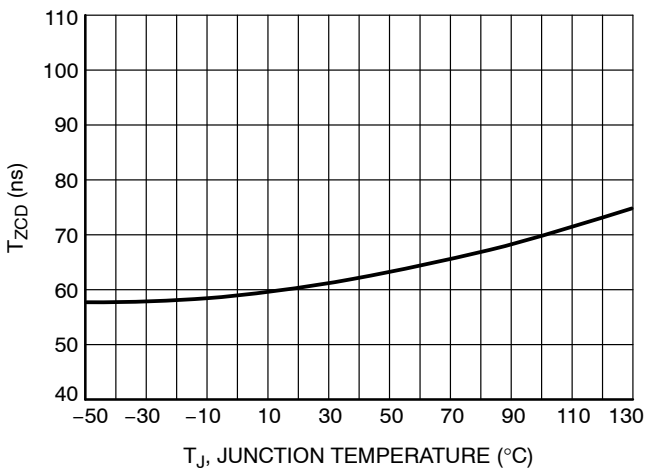


Figure 37. ((V<sub>CS/ZCD</sub> < V<sub>ZCD(th)</sub>) to DRV High) Delay vs. Temperature

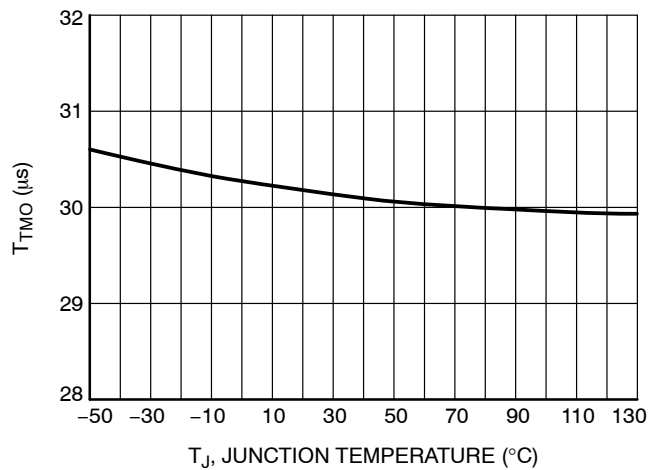


Figure 38. Timeout Timer vs. Temperature

TYPICAL CHARACTERISTICS

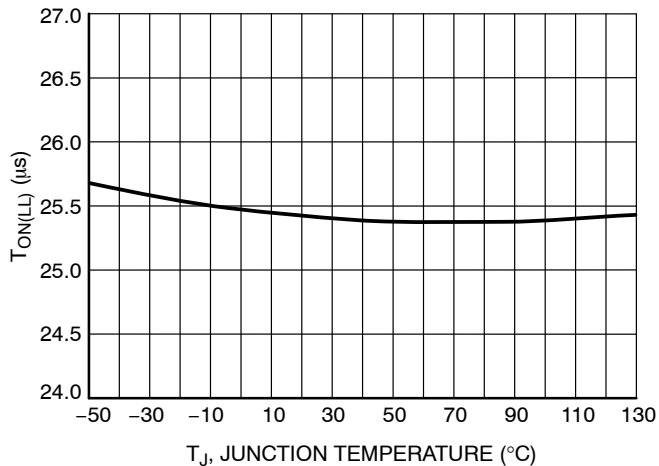


Figure 39. Maximum On Time @  $V_{SENSE} = 1.4\text{ V}$  vs. Temperature

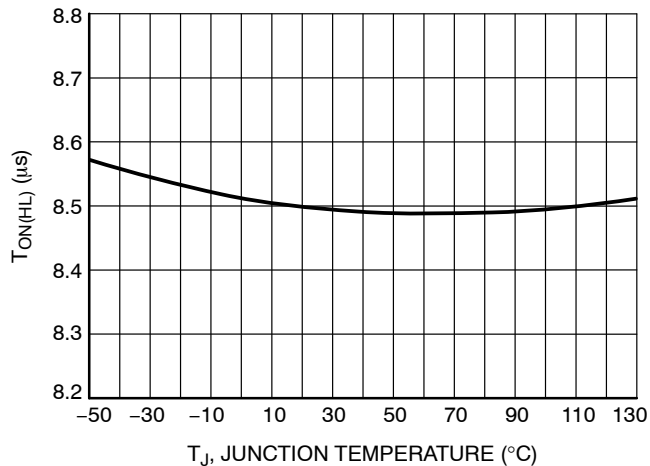


Figure 40. Maximum On Time @  $V_{SENSE} = 2.8\text{ V}$  vs. Temperature

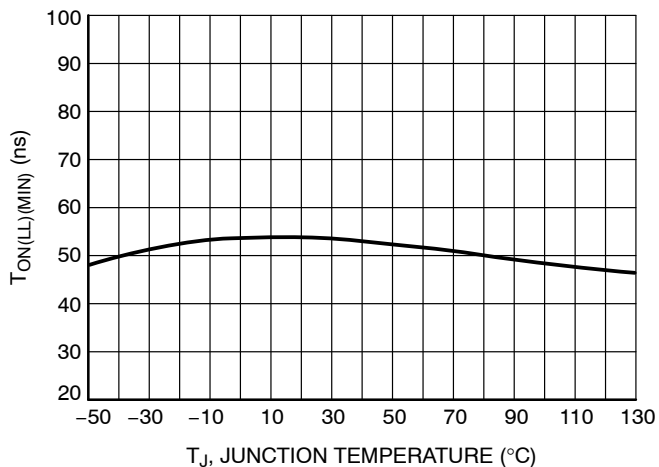


Figure 41. Minimum On Time @  $V_{SENSE} = 1.4\text{ V}$  vs. Temperature

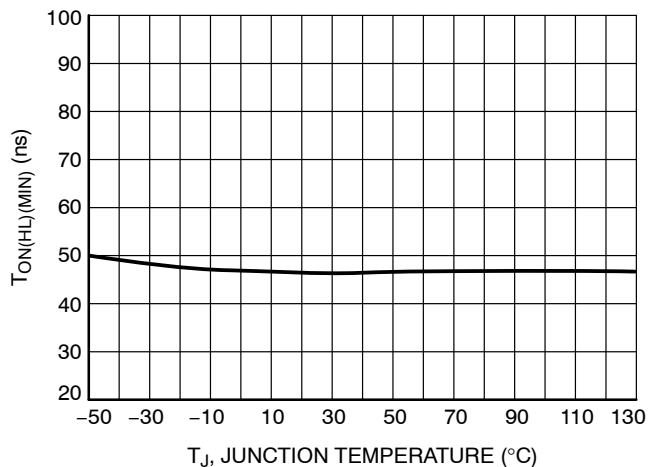


Figure 42. Minimum On Time @  $V_{SENSE} = 2.8\text{ V}$  vs. Temperature

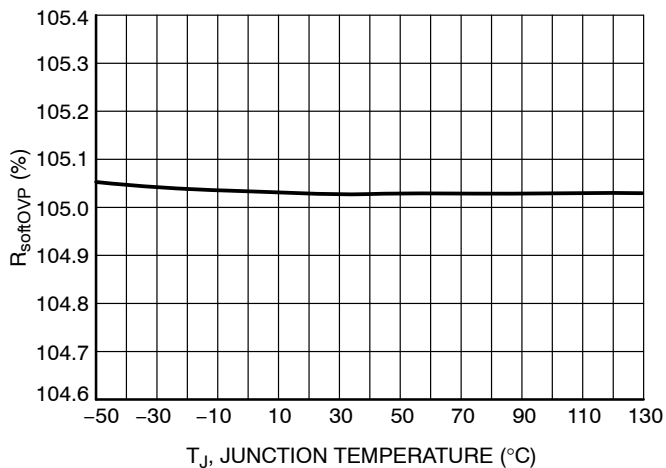


Figure 43. Ratio (Soft OVP Threshold,  $V_{FB}$  Rising) over  $V_{REF}$  vs. Temperature

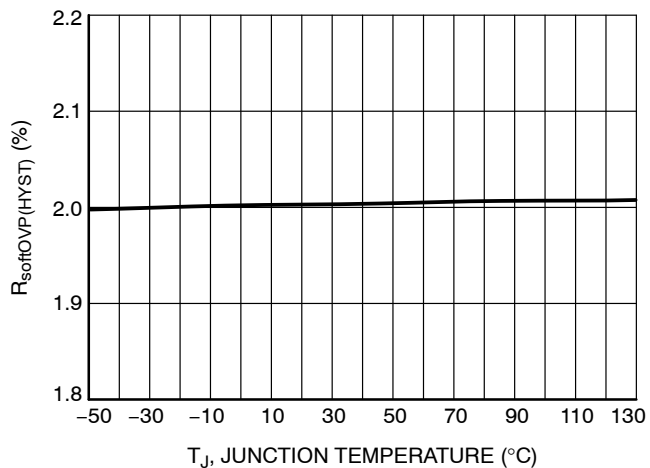


Figure 44. Ratio (Soft OVP Hysteresis) over  $V_{REF}$  vs. Temperature

TYPICAL CHARACTERISTICS

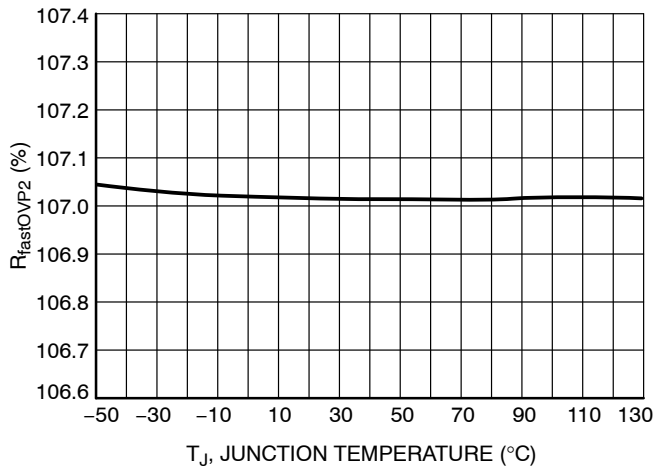


Figure 45. Ratio (fastOVP Threshold, VFOVP/BUV Rising) over VREF vs. Temperature

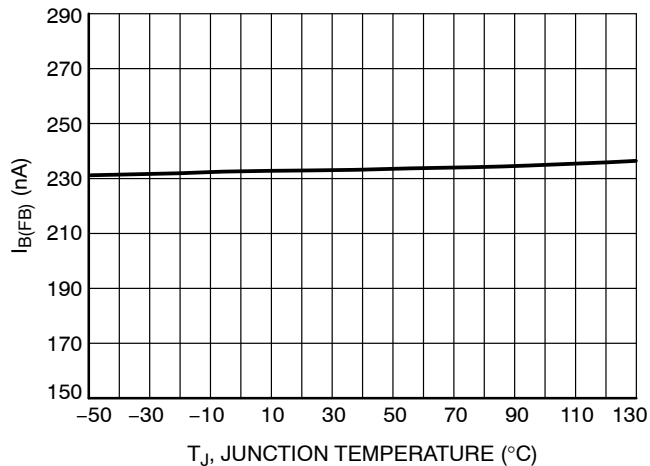


Figure 46. Feedback Pin Bias Current @ V<sub>FB</sub> = V<sub>OVP</sub> vs. Temperature

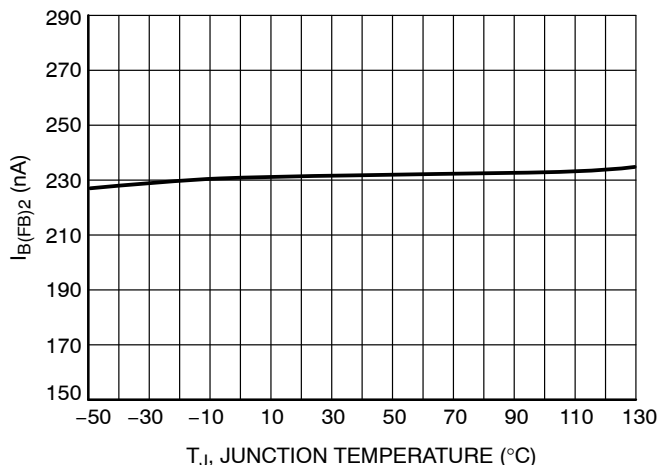


Figure 47. Feedback Pin Bias Current @ V<sub>FB</sub> = V<sub>UVP</sub> vs. Temperature

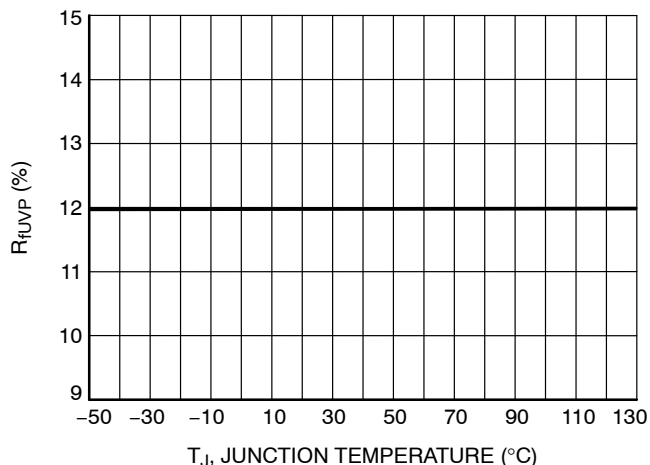


Figure 48. Ratio (UVP Threshold, V<sub>FB</sub> Rising) over VREF vs. Temperature

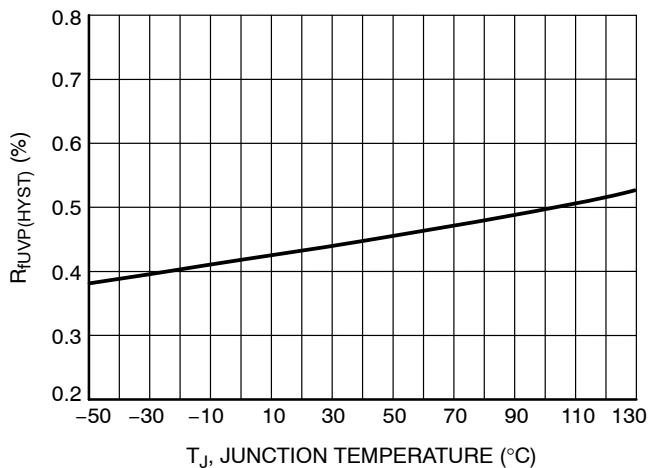


Figure 49. Ratio (UVP Hysteresis) over VREF vs. Temperature

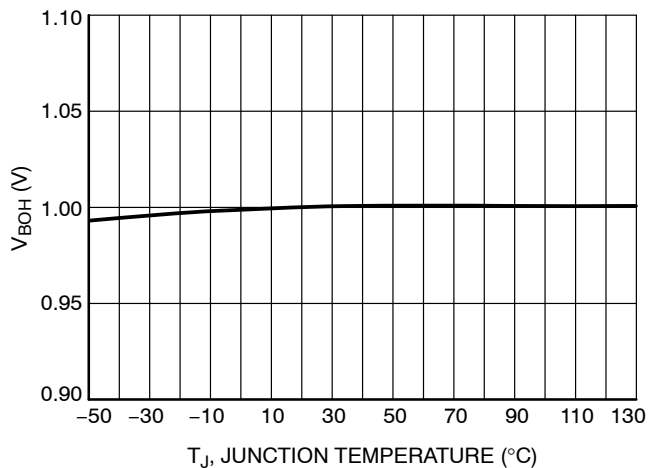


Figure 50. Brown-Out Threshold, V<sub>SENSE</sub> Rising vs. Temperature

TYPICAL CHARACTERISTICS

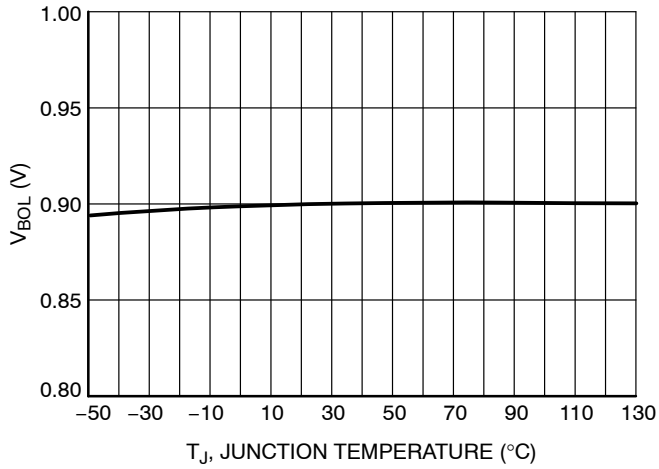


Figure 51. Brown-Out Threshold, V<sub>SENSE</sub> Falling vs. Temperature

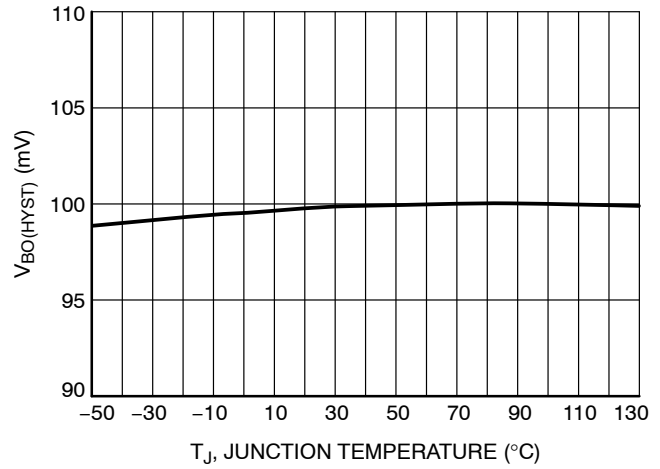


Figure 52. Brown-Out Comparator Hysteresis vs. Temperature

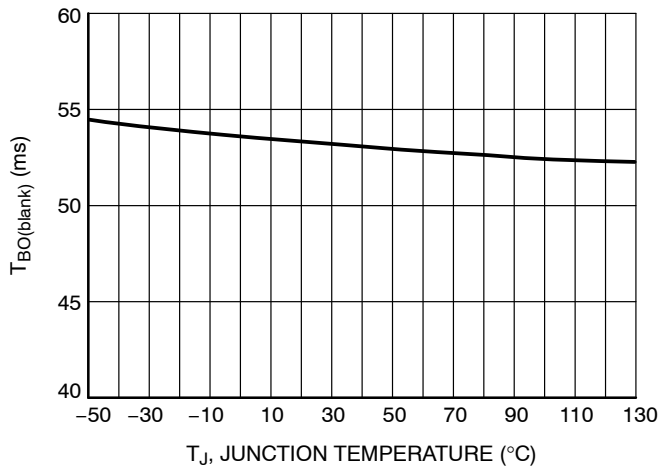


Figure 53. Brown-Out Blanking Time vs. Temperature

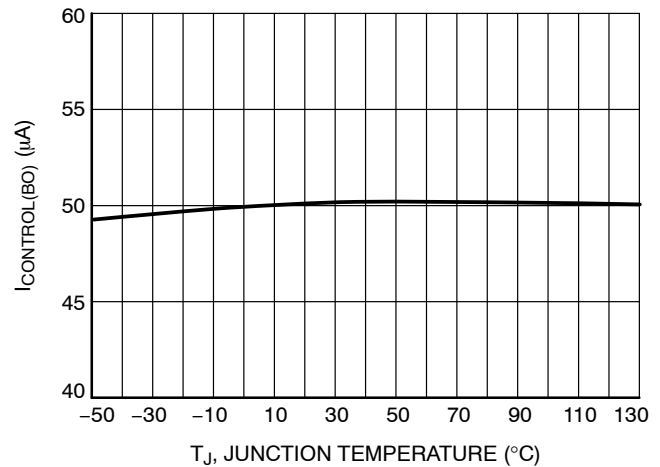


Figure 54. V<sub>CONTROL</sub> Pin Sink Current when a Brown-Out Situation is Detected vs. Temperature

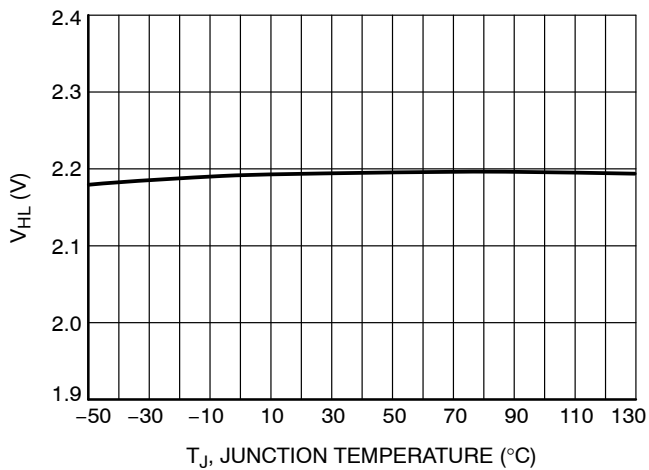


Figure 55. Comparator Threshold for Line Range Detection, V<sub>SENSE</sub> Rising vs. Temperature

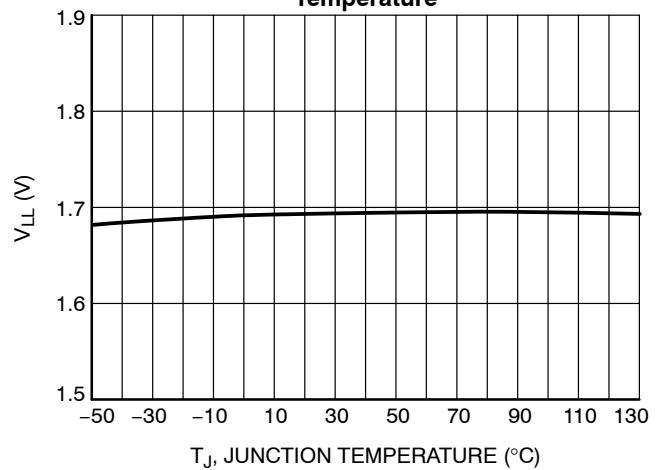


Figure 56. Comparator Threshold for Line Range Detection, V<sub>SENSE</sub> Falling vs. Temperature



## TYPICAL CHARACTERISTICS

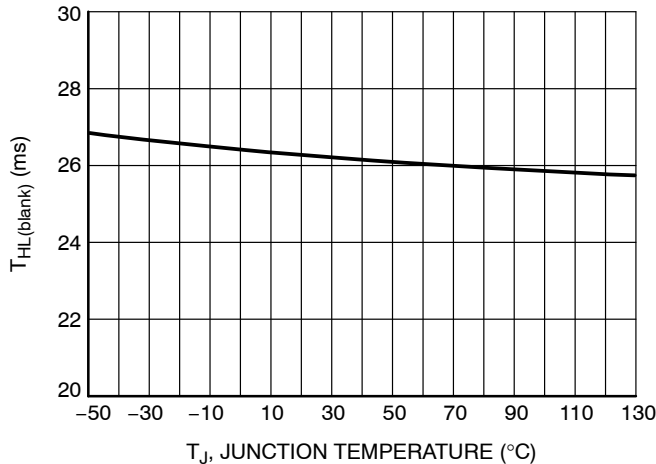


Figure 57. Blanking Time for Line Range Detection vs. Temperature

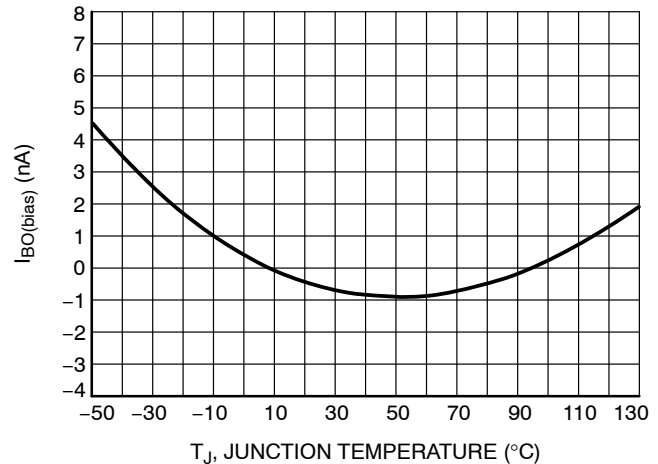


Figure 58. Brown-Out Pin Bias Current, (V<sub>SENSE</sub> = V<sub>BOH</sub>) vs. Temperature

## DETAILED OPERATING DESCRIPTION

## Introduction

The NCP1612 is designed to optimize the efficiency of your PFC stage throughout the load range. In addition, it incorporates protection features for rugged operation. More generally, the NCP1612 is ideal in systems where cost-effectiveness, reliability, low stand-by power and high efficiency are the key requirements:

- **Current Controlled Frequency Fold-back:** the NCP1612 is designed to drive PFC boost stages in so-called Current Controlled Frequency Fold-back (CCFF). In this mode, the circuit classically operates in Critical conduction Mode (CrM) when the inductor current exceeds a programmable value. When the current is below this preset level, the NCP1612 linearly reduces the frequency down to about 20 kHz when the current is zero. CCFF maximizes the efficiency at both nominal and light load. In particular, stand-by losses are reduced to a minimum. Similarly to FCCrM controllers, an internal circuitry allows near-unity power factor even when the switching frequency is reduced.
- **Skip Mode:** to further optimize the efficiency, the circuit skips cycles near the line zero crossing when the current is very low. This is to avoid circuit operation when the power transfer is particularly inefficient at the cost of current distortion. When superior power factor is required, this function can be inhibited by offsetting the “FFcontrol” pin by 0.75 V.
- **Low Start-up Current and large V<sub>CC</sub> range (B version):** The consumption of the circuit is minimized to allow the use of high-impedance start-up resistors to pre-charge the V<sub>CC</sub> capacitor. Also, the minimum value of the UVLO hysteresis is 6 V to avoid the need for large V<sub>CC</sub> capacitors and help shorten the start-up time without the need for too dissipative start-up elements. The A version is preferred in applications where the circuit is fed by an external power source (from an auxiliary power supply or from a downstream converter). Its maximum start-up level (11.25 V) is set low enough so that the circuit can be powered from a 12 V rail. After start-up, the high V<sub>CC</sub> maximum rating allows a large operating range from 9.5 V up to 35 V.
- **pfcOK signal:** the pfcOK pin is to disable/enable the downstream converter. Grounded until the PFC output has reached its nominal level and whenever the NCP1612 detects a fault, it is in high-impedance when the PFC stage outputs the nominal bulk voltage. In addition, the circuit latches off if a voltage exceeding 7.5 V is applied to pin 10.
- **Fast Line / Load Transient Compensation (Dynamic Response Enhancer):** since PFC stages exhibit low loop bandwidth, abrupt changes in the load or input voltage (e.g. at start-up) may cause excessive over or under-shoot. This circuit limits possible deviations from the regulation level as follows:
  - The soft and fast Over Voltage Protections firmly contains the output voltage when it tends to become excessive.
  - The NCP1612 dramatically speeds-up the regulation loop when the output voltage goes below 95.5 % of its regulation level. This function is enabled only after the PFC stage has started-up not to eliminate the soft-start effect.
- **Safety Protections:** the NCP1612 permanently monitors the input and output voltages, the MOSFET current and the die temperature to protect the system from possible over-stress making the PFC stage extremely robust and

reliable. In addition to the OVP protection, these methods of protection are provided:

- Maximum Current Limit: the circuit senses the MOSFET current and turns off the power switch if the set current limit is exceeded. In addition, the circuit enters a low duty-cycle operation mode when the current reaches 150% of the current limit as a result of the inductor saturation or a short of the bypass diode.
- Under-Voltage Protection: this circuit turns off when it detects that the output voltage is below 12% of the voltage reference (typically). This feature protects the PFC stage if the ac line is too low or if there is a failure in the feedback network (e.g., bad connection).
- Detection of the output voltage improper level: the “FOVP/BUV” monitors the output voltage. Typically, the same portion of the output voltage is applied as to the feedback pin. The circuit disables the driver if the pin 1 voltage exceeds 102% of the soft OVP threshold. The circuit also monitors the output voltage to detect when the PFC stage cannot maintain the bulk voltage at a high enough level (BUV situation). When the BUV function trips, the

“pfcOK” pin is grounded, to disable the downstream converter.

- Brown-Out Detection: the circuit detects low ac line conditions and stops operation thus protecting the PFC stage from excessive stress.
- Thermal Shutdown: an internal thermal circuitry disables the gate drive when the junction temperature exceeds 150°C (typically). The circuit resumes operation once the temperature drops below approximately 100°C (50°C hysteresis).
- Output Stage Totem Pole: the NCP1612 incorporates a -0.5 A / +0.8 A gate driver to efficiently drive most TO220 or TO247 power MOSFETs.

**NCP1612 Operation Modes**

As mentioned, the NCP1612 PFC controller implements a Current Controlled Frequency Fold-back (CCFF) where:

- The circuit operates in classical Critical conduction Mode (CrM) when the inductor current exceeds a programmable value.
- When the current is below this preset level, the NCP1612 linearly reduces the operating frequency down to about 20 kHz when the current is zero.

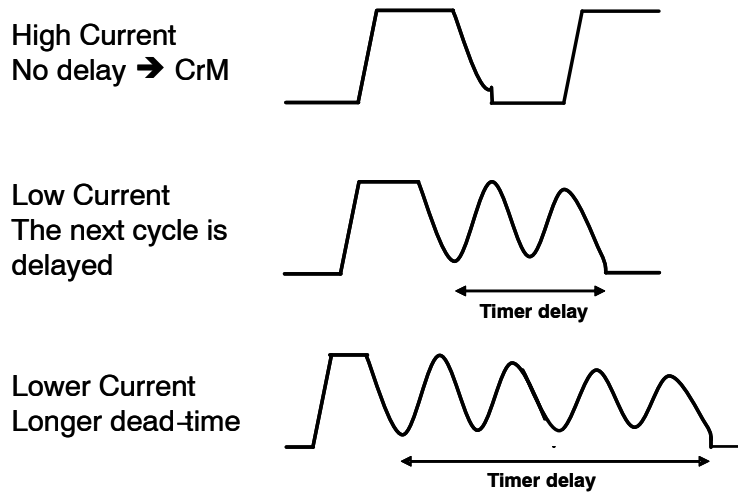


Figure 59. CCFF Operation

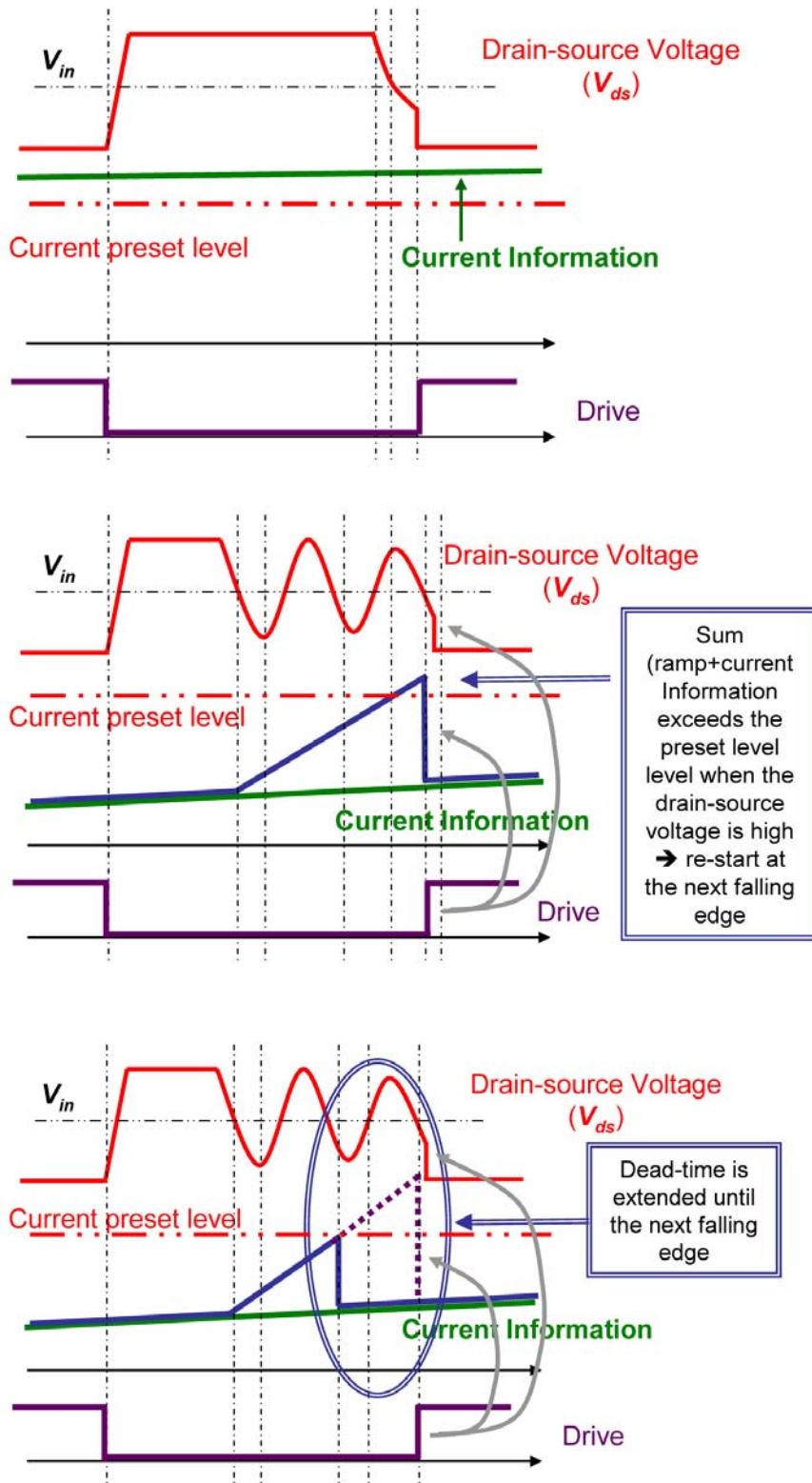
As illustrated in Figure 59, under high load conditions, the boost stage is operating in CrM but as the load is reduced, the controller enters controlled frequency discontinuous operation.

Figure 60 details the operation. A voltage representative of the input current (“current information”) is generated. If this signal is higher than a 2.5 V internal reference (named “Dead-Time Ramp Threshold” in Figure 60), there is no dead-time and the circuit operates in CrM. If the current information is lower than the 2.5 V threshold, a dead-time is inserted that lasts for the time necessary for the internal

ramp to reach 2.5 V from the current information floor. Hence, the lower the current information is, the longer the dead-time. When the current information is 0.75 V, the dead-time is 50 μs.

To further reduce the losses, the MOSFET turns on is stretched until its drain-source voltage is at its valley. As illustrated in Figure 60, the ramp is synchronized to the drain-source ringing. If the ramp exceeds the 2.5 V threshold while the drain-source voltage is below  $V_{in}$ , the ramp is extended until it oscillates above  $V_{in}$  so that the drive will turn on at the next valley.

# NCP1612



Top: CrM operation when the current information exceeds the preset level during the demagnetization phase

Middle: the circuit re-starts at the next valley if the sum (ramp + current information) exceeds the preset level during the dead-time, while the drain-source voltage is high

Bottom: the sum (ramp + current information) exceeds the preset level while during the dead-time, the drain-source voltage is low. The circuit skips the current valley and re-starts at the following one.

**Figure 60. Dead-Time generation**

**Current Information Generation**

The “FFcontrol” pin sources a current that is representative of the input current. In practice,  $I_{pin5}$  is built by multiplying the internal control signal ( $V_{REGUL}$ , i.e., the internal signal that controls the on-time) by the sense voltage (pin 4) that is proportional to the input voltage. The

multiplier gain ( $K_m$  of Figure 61) is three times less in high-line conditions (that is when the “LLine” signal from the brown-out block is in low state) so that  $I_{pin5}$  provides a voltage representative of the input current across resistor  $R_{FF}$  placed between pin 5 and ground. Pin 5 voltage is the current information.

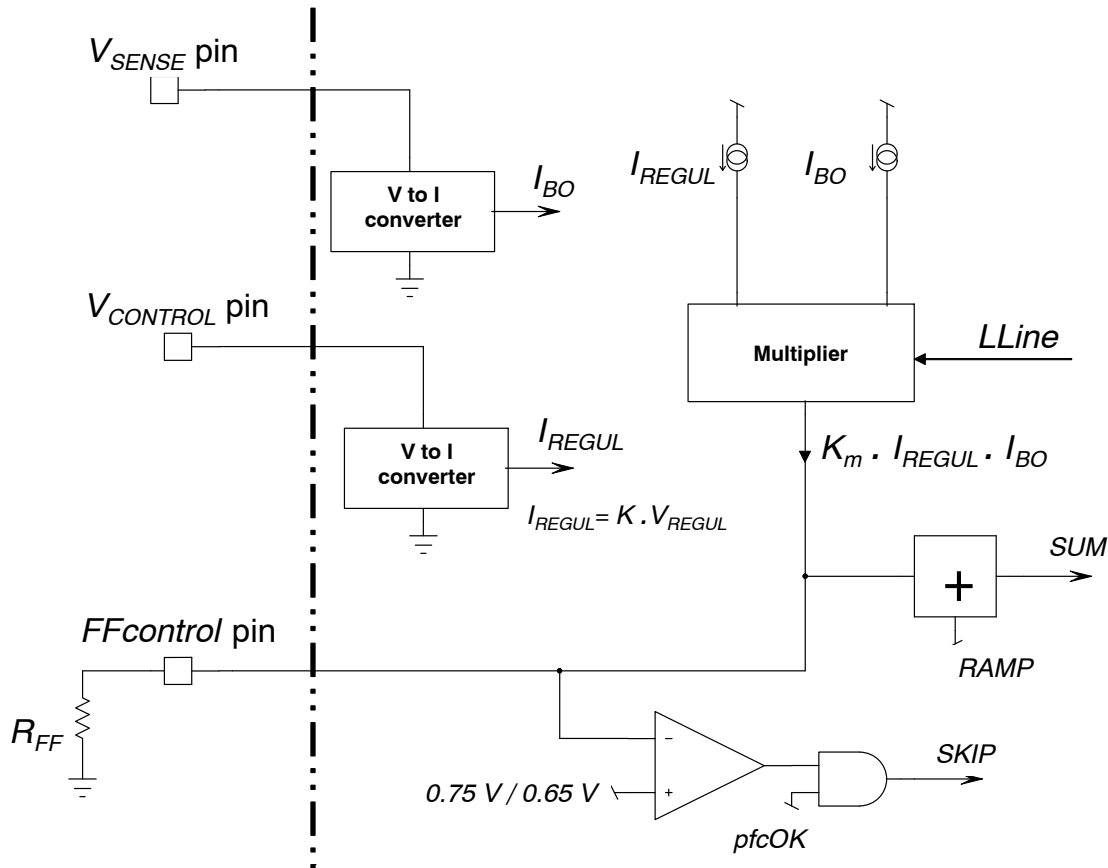


Figure 61. Generation of the current information

**Skip Mode**

As illustrated in Figure 61, the circuit also skips cycles near the line zero crossing where the current is very low. A comparator monitors the pin 5 voltage (“FFcontrol” voltage) and inhibits the switching operation when  $V_{pin5}$  is lower than a 0.65 V internal reference. Switching resumes when  $V_{pin5}$  exceeds 0.75 V (0.1 V hysteresis). This function prevents circuit operation when the power transfer is particularly inefficient at the expense of slightly increased current distortion. When superior power factor is needed, this function can be inhibited offsetting the “FFcontrol” pin

by 0.75 V. The skip mode capability is disabled whenever the PFC stage is not in nominal operation (as dictated by the “pfcOK” signal – see block diagram and “pfcOK Internal Signal” Section).

The circuit does not abruptly interrupt the switching when  $V_{pin5}$  goes below 0.65 V. Instead, the signal  $V_{TON}$  that controls the on-time is gradually decreased by grounding the  $V_{REGUL}$  signal applied to the  $V_{TON}$  processing block (see Figure 66). Doing so, the on-time smoothly decays to zero in 3 to 4 switching periods typically. Figure 62 shows the practical implementation.

# NCP1612

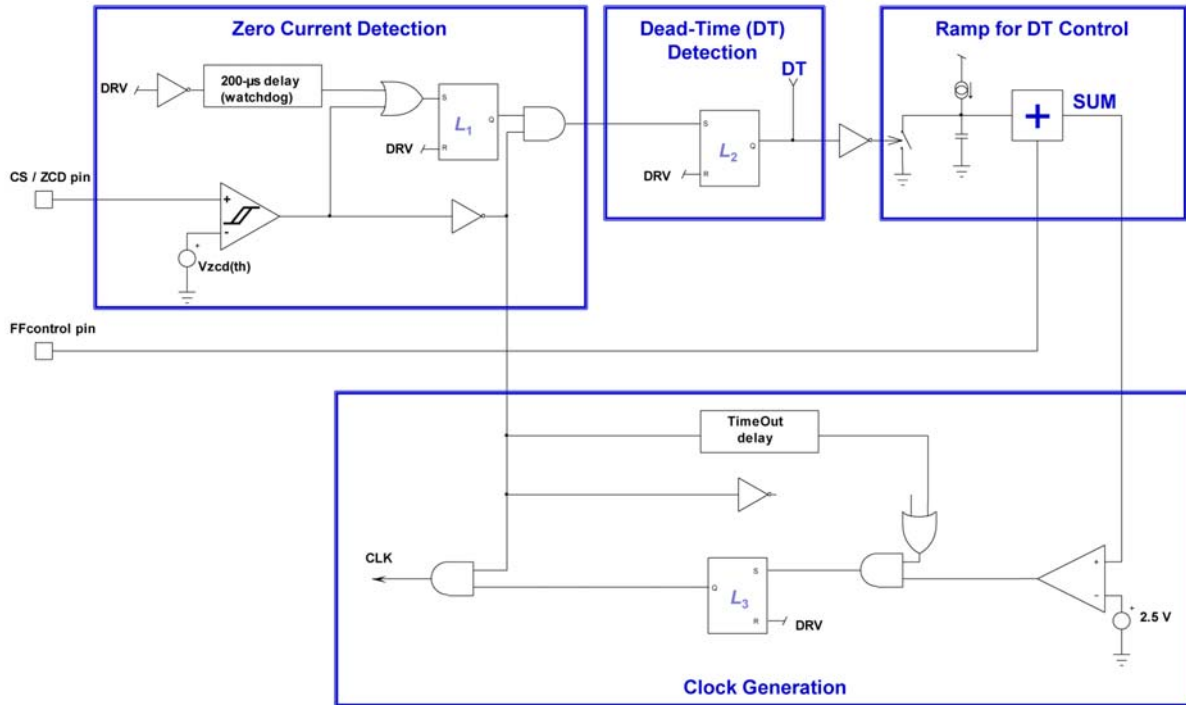


Figure 62. CCFF Practical Implementation

CCFF maximizes the efficiency at both nominal and light load. In particular, the stand-by losses are reduced to a minimum. Also, this method avoids that the system stalls between valleys. Instead, the circuit acts so that the PFC

stage transitions from the  $n$  valley to  $(n + 1)$  valley or vice versa from the  $n$  valley to  $(n - 1)$  cleanly as illustrated by Figure 63.

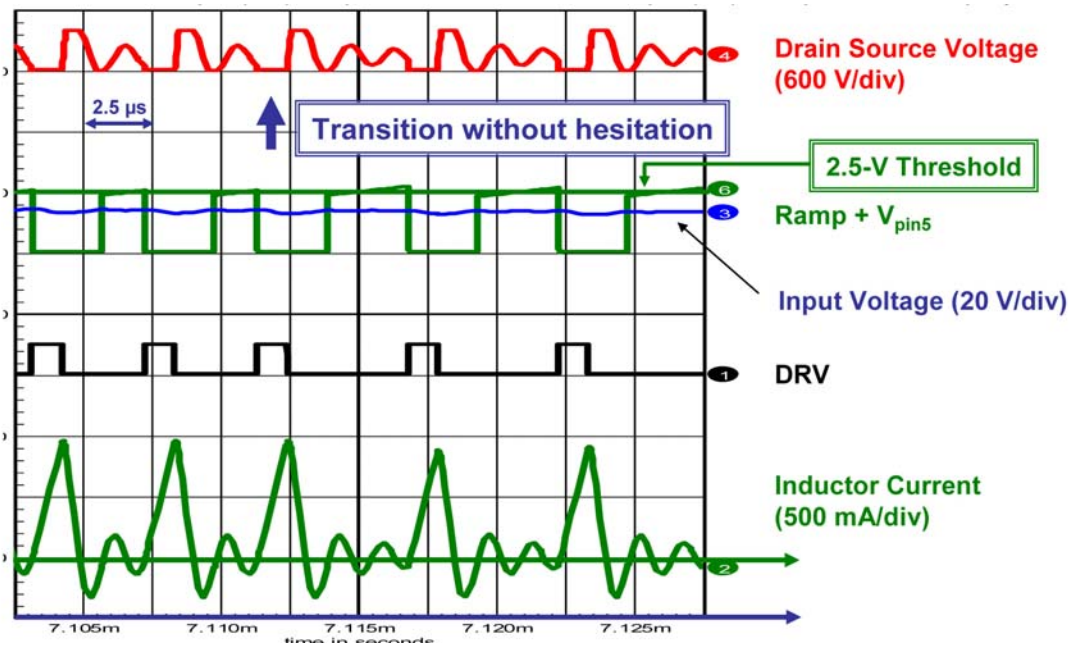
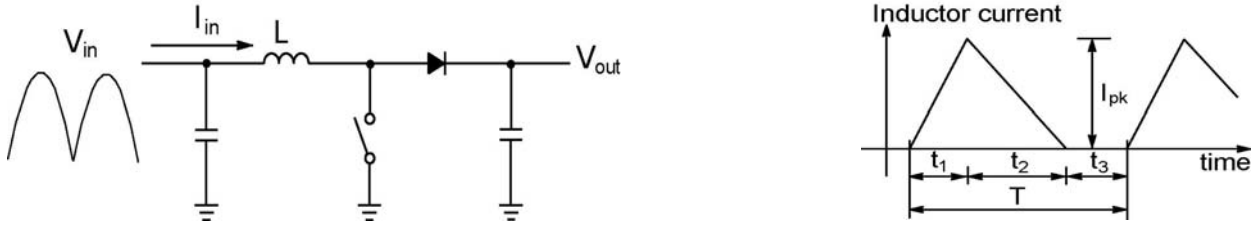


Figure 63. Clean Transition Without Hesitation Between Valleys

**NCP1612 On-time Modulation**

Let's analyze the ac line current absorbed by the PFC boost stage. The initial inductor current at the beginning of each switching cycle is always zero. The coil current ramps up when the MOSFET is *on*. The slope is  $(V_{IN}/L)$  where  $L$  is the coil inductance. At the end of the on-time ( $t_1$ ), the inductor starts to demagnetize. The inductor current ramps down until it reaches zero. The duration of this phase is ( $t_2$ ). In some cases, the system enters then the dead-time ( $t_3$ ) that lasts until the next clock is generated.



**Figure 64. PFC Boost Converter (left) and Inductor Current in DCM (right)**

The NCP1612 operates in voltage mode. As portrayed by Figure 65, the MOSFET on-time  $t_1$  is controlled by the signal  $V_{ton}$  generated by the regulation block and an internal ramp as follows:

$$t_1 = \frac{C_{ramp} \cdot V_{ton}}{I_{ch}} \quad (\text{eq. 2})$$

The charge current is constant at a given input voltage (as mentioned, it is three times higher at high line compared to its value at low line).  $C_{ramp}$  is an internal capacitor.

The output of the regulation block ( $V_{CONTROL}$ ) is linearly transformed into a signal ( $V_{REGUL}$ ) varying between 0 and 1 V. ( $V_{REGUL}$ ) is the voltage that is injected into the PWM section to modulate the MOSFET duty-cycle. The NCP1612 includes some circuitry that processes ( $V_{REGUL}$ ) to form the signal ( $V_{ton}$ ) that is used in the PWM section (see Figure 66). ( $V_{ton}$ ) is modulated in response to the dead-time sensed during the precedent current cycles, that is, for a proper shaping of the ac line current. This modulation leads to:

$$V_{ton} = \frac{T \cdot V_{REGUL}}{t_1 + t_2} \quad (\text{eq. 3})$$

or

$$V_{ton} \cdot \frac{t_1 + t_2}{T} = V_{REGUL}$$

Given the low regulation bandwidth of the PFC systems, ( $V_{CONTROL}$ ) and then ( $V_{REGUL}$ ) are slow varying signals. Hence, the  $(V_{ton} \cdot (t_1 + t_2)/T)$  term is substantially constant. Provided that in addition, ( $t_1$ ) is proportional to ( $V_{ton}$ ), Equation 1 leads to: , where  $k$  is a constant. More exactly:

One can show that the ac line current is given by:

$$I_{in} = V_{in} \left[ \frac{t_1(t_1 + t_2)}{2TL} \right] \quad (\text{eq. 1})$$

Where  $T = (t_1 + t_2 + t_3)$  is the switching period and  $V_{in}$  is the ac line rectified voltage.

In light of this equation, we immediately note that  $I_{in}$  is proportional to  $V_{in}$  if  $[t_1(t_1 + t_2) / T]$  is a constant.

$$I_{in} = k \cdot V_{in}$$

$$\text{where : } k = \text{constant} = \left[ \frac{1}{2L} \cdot \frac{V_{REGUL}}{(V_{REGUL})_{max}} \cdot t_{on,max} \right]$$

Where  $t_{on,max}$  is the maximum on-time obtained when  $V_{REGUL}$  is at its  $(V_{REGUL})_{max}$  maximum level. The parametric table shows that  $t_{on,max}$  is equal to 25  $\mu s$  ( $T_{ON(LL)}$ ) at low line and to 8.5  $\mu s$  ( $T_{ON(HL)}$ ) at high line (when pin4 happens to exceeds 1.8 V with a pace higher than 40 Hz – see BO 25 ms blanking time).

Hence, we can re-write the above equation as follows:

$$I_{in} = \frac{V_{in} \cdot T_{ON(LL)}}{2 \cdot L} \cdot \frac{V_{REGUL}}{(V_{REGUL})_{max}}$$

at low line.

$$I_{in} = \frac{V_{in} \cdot T_{ON(HL)}}{2 \cdot L} \cdot \frac{V_{REGUL}}{(V_{REGUL})_{max}}$$

at high line.

From these equations, we can deduce the expression of the average input power:

$$P_{in,avg} = \frac{(V_{in,rms})^2 \cdot V_{REGUL} \cdot T_{ON(LL)}}{2 \cdot L \cdot (V_{REGUL})_{max}}$$

at low line

$$P_{in,avg} = \frac{(V_{in,rms})^2 \cdot V_{REGUL} \cdot T_{ON(HL)}}{2 \cdot L \cdot (V_{REGUL})_{max}}$$

at high line

Where  $(V_{REGUL})_{max}$  is the  $V_{REGUL}$  maximum value.

Hence, the maximum power that can be delivered by the PFC stage is:

$$(P_{in,avg})_{max} = \frac{(V_{in,rms})^2 \cdot T_{ON(LL)}}{2 \cdot L}$$

at low line

$$(P_{in,avg})_{max} = \frac{(V_{in,rms})^2 \cdot T_{ON(HL)}}{2 \cdot L}$$

at high line

The input current is then proportional to the input voltage. Hence, the ac line current is properly shaped.

One can note that this analysis is also valid in the CrM case. This condition is just a particular case of this

functioning where  $(t_3 = 0)$ , which leads to  $(t_1 + t_2 = T)$  and  $(V_{TON} = V_{REGUL})$ . That is why the NCP1612 automatically adapts to the conditions and transitions from DCM and CrM (and vice versa) without power factor degradation and without discontinuity in the power delivery.

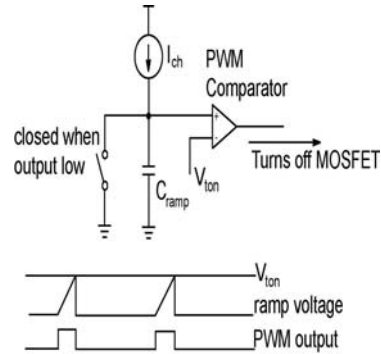


Figure 65. PWM circuit and timing diagram.

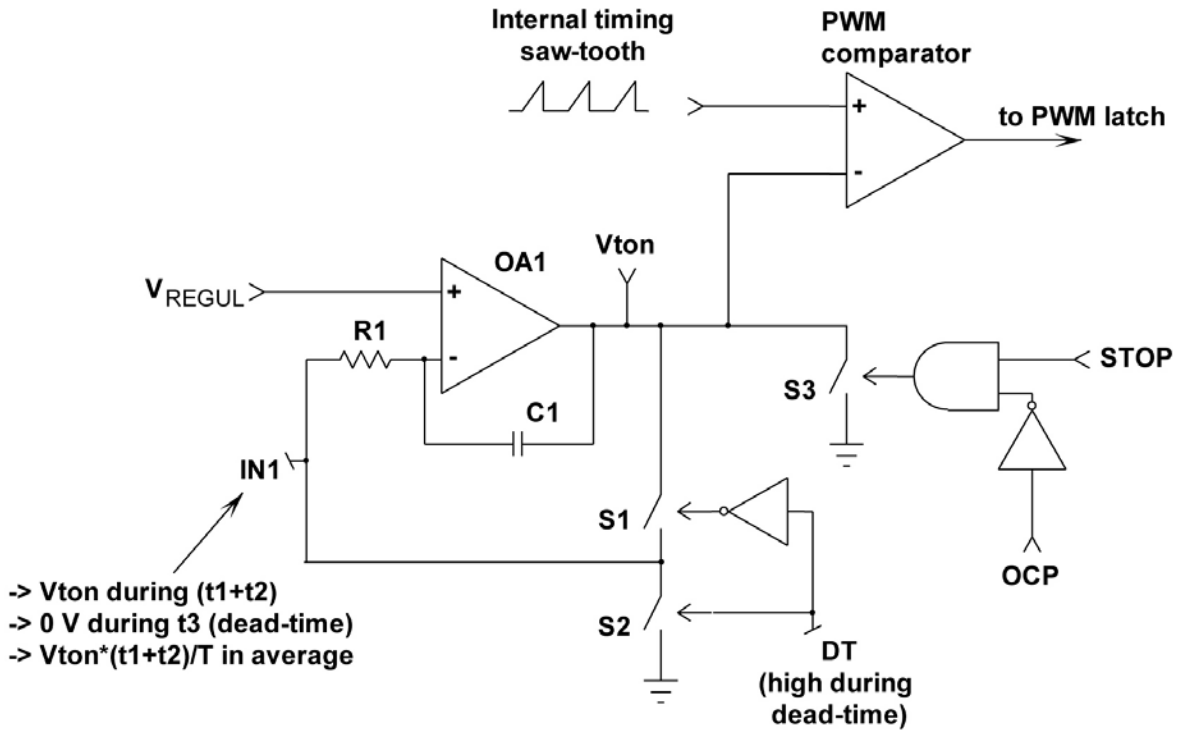


Figure 66.  $V_{TON}$  Processing Circuit. The integrator OA1 amplifies the error between  $V_{REGUL}$  and IN1 so that on average,  $(V_{TON} \cdot (t_1+t_2)/T)$  equates  $V_{REGUL}$ .

**Remark:**

The “ $V_{ton}$  processing circuit” is “informed” when a condition possibly leading to a long interruption of the drive activity (functions generating the STOP signal that disables the drive – see block diagram – except OCP, i.e.,  $BUV\_fault$ , OVP, OverStress, SKIP, staticOVP and OFF). Otherwise, such situations would be viewed as a normal dead-time

phase and  $V_{ton}$  would inappropriately over-dimension  $V_{ton}$  to compensate it. Instead, as illustrated in Figure 66, the  $V_{ton}$  signal is grounded leading to a short soft-start when the circuit recovers.

**Regulation Block and Low Output Voltage Detection**

A trans-conductance error amplifier (OTA) with access to the inverting input and output is provided. It features a typical trans-conductance gain of 200  $\mu$ S and a maximum capability of  $\pm 20 \mu$ A. The output voltage of the PFC stage is typically scaled down by a resistors divider and monitored by the inverting input (pin 2). Bias current is minimized (less than 500 nA) to allow the use of a high impedance feed-back network. However, it is high enough so that the pin remains in low state if the pin is not connected.

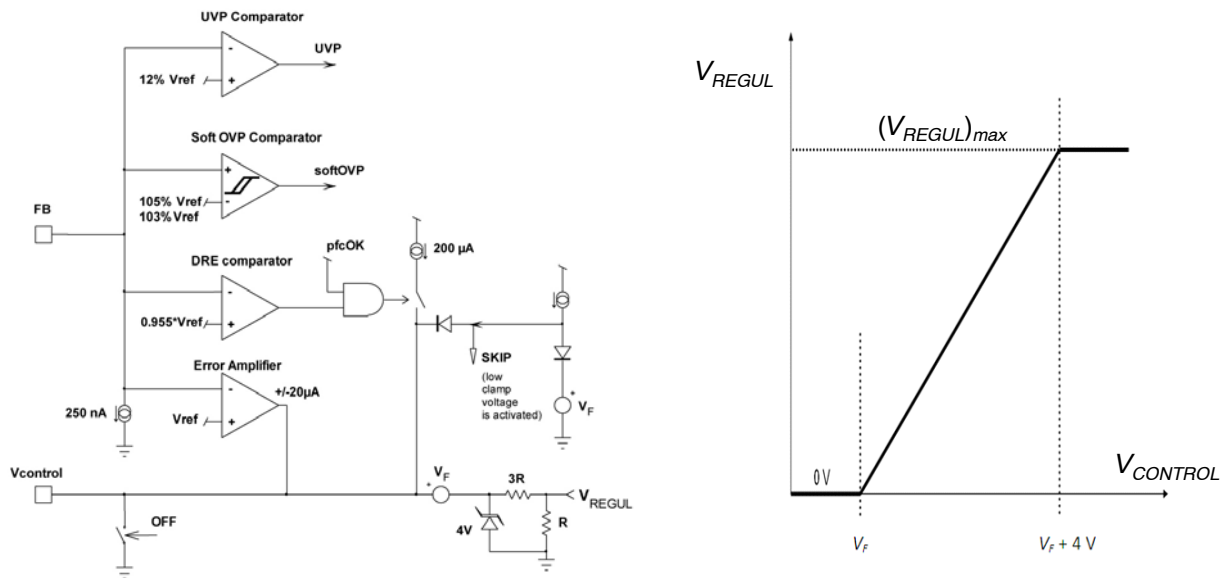
The output of the error amplifier is brought to pin 3 for external loop compensation. Typically a type-2 network is applied between pin 3 and ground, to set the regulation bandwidth below about 20 Hz and to provide a decent phase boost.

The swing of the error amplifier output is limited within an accurate range:

- It is forced above a voltage drop ( $V_F$ ) by some circuitry.
- It is clamped not to exceed  $4.0 \text{ V} +$  the same  $V_F$  voltage drop.

Hence,  $V_{pin3}$  features a 4 V voltage swing.  $V_{pin3}$  is then offset down by ( $V_F$ ) and scaled down by a resistors divider before it connects to the “ $V_{TON}$  processing block” and the PWM section. Finally, the output of the regulation block is a signal (“ $V_{REGUL}$ ” of the block diagram) that varies between 0 and a top value corresponding to the maximum on-time.

The  $V_F$  value is 0.5 V typically.



**Figure 67. a) Regulation Block Figure (left), b) Correspondence between  $V_{CONTROL}$  and  $V_{REGUL}$  (right)**

Given the low bandwidth of the regulation loop, abrupt variations of the load, may result in excessive over or under-shoots. Over-shoot is limited by the soft Over-Voltage Protection (OVP) connected to the feedback pin or the fast OVP of pin1.

The NCP1612 embeds a “dynamic response enhancer” circuitry (DRE) that contains under-shoots. An internal comparator monitors the feed-back ( $V_{pin1}$ ) and when  $V_{pin2}$  is lower than 95.5% of its nominal value, it connects a 200  $\mu$ A current source to speed-up the charge of the compensation network. Effectively this appears as a 10x increase in the loop gain.

In A version, DRE is disabled during the start-up sequence until the PFC stage has stabilized (that is when the “pfcOK” signal of the block diagram, is high). The resulting slow and gradual charge of the pin 3 voltage ( $V_{CONTROL}$ ) softens the soft start-up sequence. In B version, DRE is enabled during start-up to speed-up this phase and allow for the use of smaller  $V_{CC}$  capacitors.

The circuit also detects overshoot and immediately reduces the power delivery when the output voltage exceeds 105% of its desired level. The NCP1612 does not abruptly interrupt the switching. Instead, the signal  $V_{TON}$  that controls the on-time is gradually decreased by grounding the  $V_{REGUL}$  signal applied to the  $V_{TON}$  processing block (see Figure 66). Doing so, the on-time smoothly decays to zero in 4 to 5 switching periods typically. If the output voltage still increases, the fast OVP comparator immediately disables the driver if the output voltage exceeds 108.5% of its desired level.

The error amplifier OTA and the soft OVP, UVP and DRE comparators share the same input information. Based on the typical value of their parameters and if ( $V_{out,nom}$ ) is the output voltage nominal value (e.g., 390 V), we can deduce:

- **Output Regulation Level:**  $V_{out,nom}$
- **Output soft OVP Level:**  $V_{out,sovp} = 105\% \times V_{out,nom}$
- **Output UVP Level:**  $V_{out,uvp} = 12\% \times V_{out,nom}$



- **Output DRE Level:**  $V_{out,dre} = 95.5\% \times V_{out,nom}$

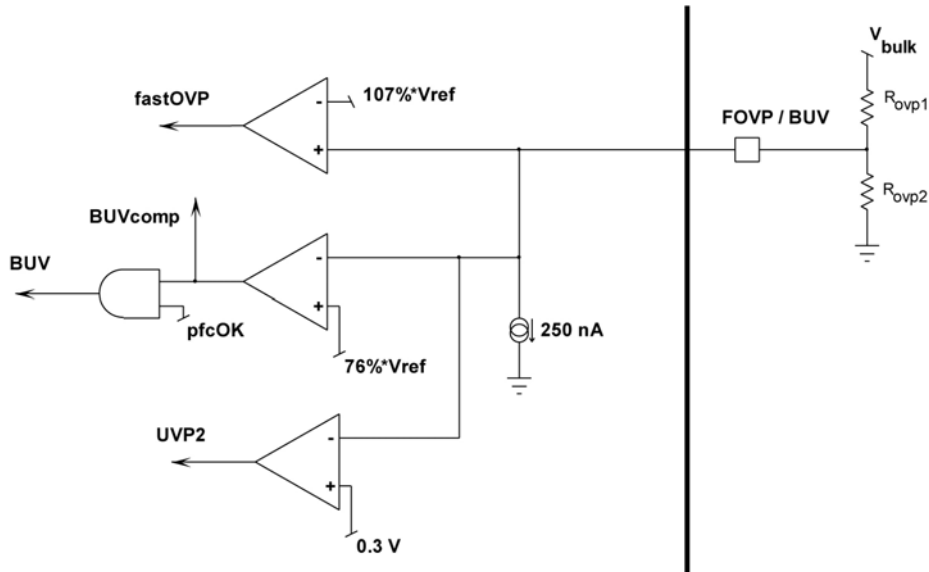
**Fast OVP and Bulk Under-Voltage (BUV)**

These functions check that the output voltage is within the proper window:

- The fast Over-Voltage Protection trips if the bulk voltage reaches abnormal levels. When the feedback network is properly designed and correctly connected, the bulk voltage cannot exceed the level set by the soft OVP function ( $V_{out,sovp} = 105\% \times V_{out,nom}$ , see precedent section). This second protection offers some redundancy for a higher safety level. The FOVP threshold is set 2% higher than the soft OVP comparator reference so that the same portion of the output voltage can be applied to both the FOVP/BUV and feedback input pins (pins 1 and 2).

- The BUV comparator trips when  $V_{pin1}$  drops below 76% of the 2.5 V reference voltage ( $V_{BUV} = 76\% \times V_{REF}$ ). In the case, the circuit grounds the pfcOK pin (to disable the downstream converter) and gradually discharges the  $V_{CONTROL}$  signal until the SKIP level is obtained (see block diagram) so that the next start-up sequence will be performed with a soft-start. The drive output is disabled for the  $V_{CONTROL}$  discharge time. When the  $V_{CONTROL}$  discharge is complete, the circuit can attempt to recover operation.

However, the BUV function has no action whenever the pfcOK pin is in low state, not to inappropriately interrupt start-up phases.



**Figure 68. Bulk Under-Voltage Detection**

As a matter of fact, pin1 monitors the output voltage and checks if it is within the window for proper operation.

Assuming that the same portion of the output voltage is applied to FOVP/BUV and feedback pins:

- Output fast OVP Level:  $V_{out,fovp} = 107\% \times V_{out,nom}$
- Output BUV Level:  $V_{out,BUV} = 76\% \times V_{out,nom}$

Hence, if the output regulation voltage is 390 V, the FOVP and BUV output voltage levels are 417 and 296 V respectively.

A 250 nA sink current is built-in to ground the pin if the FOVP / BUV pin is accidentally open. The circuit disables the drive as long as the pin voltage is below 300 mV (typically).

**Current Sense and Zero Current Detection**

The NCP1612 is designed to monitor the current flowing through the power switch. A current sense resistor ( $R_{sense}$ ) is inserted between the MOSFET source and ground to

generate a positive voltage proportional to the MOSFET current ( $V_{CS}$ ). The  $V_{CS}$  voltage is compared to a 500 mV internally reference. When  $V_{CS}$  exceeds this threshold, the OCP signal turns high to reset the PWM latch and forces the driver low. A 200 ns blanking time prevents the OCP comparator from tripping because of the switching spikes that occur when the MOSFET turns on.

The CS pin is also designed to receive a signal from an auxiliary winding for Zero Current Detection. As illustrated in Figure 69, an internal ZCD comparator monitors the pin6 voltage and if this voltage exceeds 750 mV, a demagnetization phase is detected (signal ZCD is high). The auxiliary winding voltage is applied through a diode to prevent this signal from distorting the current sense information during the on-time. Thus, the OCP protection is not impacted by the ZCD sensing circuitry. This

comparator incorporates a 500 mV hysteresis and is able to detect ZCD pulses longer than 200 ns. When pin 6 voltage drops below the lower ZCD threshold, the driver can turn high within 200 ns.

It may happen that the MOSFET turns on while a huge current flows through the inductor. As an example such a situation can occur at start-up when large in-rush currents charge the bulk capacitor to the line peak voltage. Traditionally, a bypass diode is generally placed between the input and output high-voltage rails to divert this inrush

current. If this diode is accidentally shorted, the MOSFET will also see a high current when it turns on. In both cases, the current can be large enough to trigger the ZCD comparator. An AND gate detects that this event occurs while the drive signal is high. In this case, a latch is set and the “OverStress” signal goes high and disables the driver for a 800 μs delay. This long delay leads to a very low duty-cycle operation in case of “OverStress” fault in order to limit the risk of overheating.

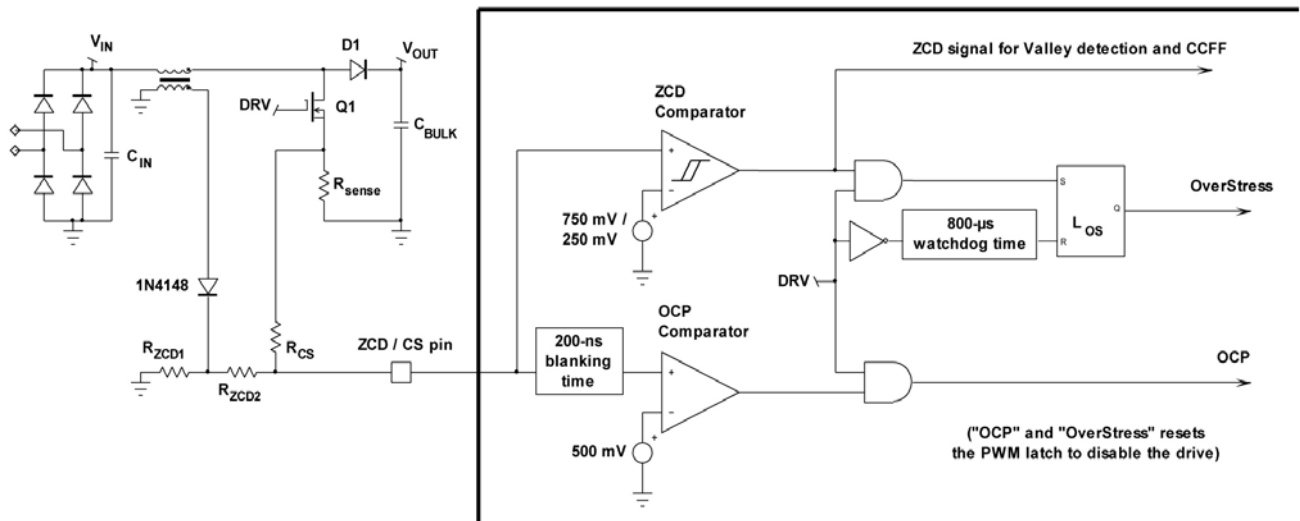


Figure 69. Current Sense and Zero Current Detection Blocks

When no signal is received that triggers the ZCD comparator during the off-time, an internal 200 μs watchdog timer initiates the next drive pulse. At the end of this delay, the circuit senses the CS/ZCD pin impedance to detect a possible grounding of this pin and prevent operation. The CS/ZCD external components must be selected to avoid false fault detection. 3.9 kΩ is the recommended minimum impedance to be applied to the CS/ZCD pin when considering the NCP1612 parameters tolerance over the -40°C to 125°C temperature range. Practically, R<sub>CS</sub> must be higher than 3.9 kΩ in the application of Figure 69.

**pfcOK Signal**

The pfcOK pin is in high-impedance state when the PFC stage operates nominally and is grounded in the following cases:

- During the PFC stage start-up, that is, until the output voltage has stabilized at the right level.
- If the output voltage is too low for proper operation of the downstream converter, more specifically, when the “BUV\_fault” signal (see Figure 2) is in high state.
- In the case of a condition preventing the circuit from operating properly like in a Brown-out situation or when one of the following faults turns off the circuit:

- Incorrect feeding of the circuit (“UVLO” high when  $V_{CC} < V_{CC(off)}$ ,  $V_{CC(off)}$  equating 9 V typically).
- Excessive die temperature detected by the thermal shutdown.
- Under-Voltage Protection
- Latched-off of the part
- Regulation loop failure (UVP)
- Brown-out Situation (BO\_fault high – see Figure 2)

The pfcOK signal is controlled as illustrated by Figure 70. The circuit monitors the current sourced by the OTA. If there is no current, we can deduce that the output voltage has reached its nominal level. The start-up phase is then complete and pfcOK remains high-impedance until a fault is detected. *Upon startup, the internal signals and the internal supply rails need some time to stabilize. The pfcOK latch cannot be set during this time and until a sufficient blanking time has elapsed.* For the sake of simplicity, this blanking delay is not represented in Figure 70.

Another mandatory condition to set pfcOK high is the low state of the “BUVcomp” signal. This second necessary condition ensures that the voltage applied to pin 1 is high enough not to immediately trigger the BUV protection.

The pfcOK pin is to be used to enable the downstream converter.

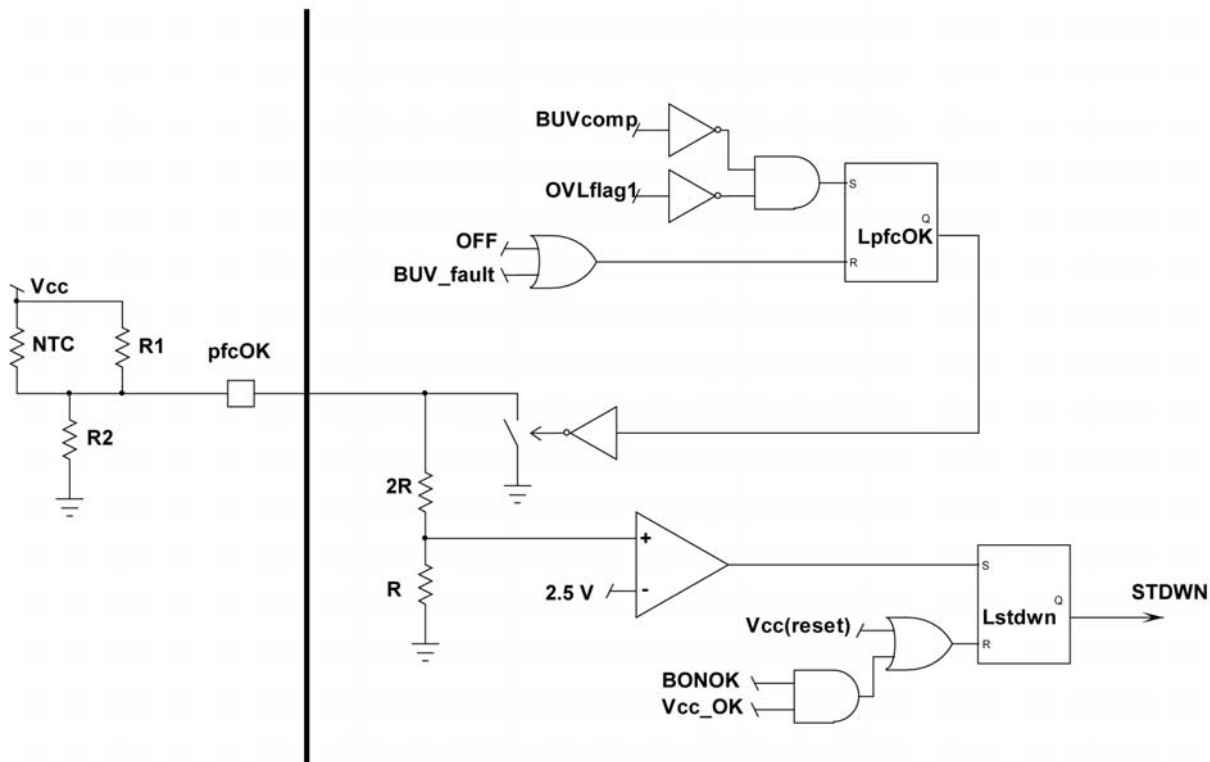


Figure 70. pfcOK Detection

The circuit also incorporates a comparator to a 7.5 V threshold so that the part latches off if the pfcOK pin voltage exceeds 7.5 V. This pin is to protect the part in presence of a major fault like a die over-heating. To recover operation, a brown-out condition must be detected (if circuit  $V_{CC}$  is properly fed) or  $V_{CC}$  must drop below  $V_{CC(reset)}$ .

**Brown-Out Detection**

The  $V_{SENSE}$  pin (pin4) receives a portion of the instantaneous input voltage ( $V_{in}$ ). As  $V_{in}$  is a rectified sinusoid, the monitored signal varies between zero or a small voltage and a peak value.

For the brown-out block, we need to ensure that the line magnitude is high enough for operation. This is done as follows:

- The  $V_{SENSE}$  pin voltage is compared to a 1 V reference.
- If  $V_{pin4}$  exceeds 1 V, the input voltage is considered sufficient
- If  $V_{pin4}$  remains below 0.9 V for 50 ms, the circuit detects a brown-out situation (100 mV hysteresis).

By default, when the circuit starts operation, the circuit is in a fault state (“BO\_NOK” high) until  $V_{pin4}$  exceeds 1 V.

When “BO\_NOK” is high, the drive is not disabled. Instead, a 50  $\mu$ A current source is applied to pin3 to gradually reduce  $V_{CONTROL}$ . As a result, the circuit only stops pulsing when the SKIP function is activated ( $V_{CONTROL}$  reaches the skip detection threshold). At that

moment, the circuit turns off (see Figure 2). This method limits any risk of false triggering. The input of the PFC stage has some impedance that leads to some sag of the input voltage when the drawn current is large. If the PFC stage stops while a high current is absorbed from the mains, the abrupt decay of the current may make the input voltage rise and the circuit detect a correct line level. Instead, the gradual decrease of  $V_{CONTROL}$  avoids a line current discontinuity and limits risk of false triggering.

Pin4 is also used to sense the line for feed-forward. A similar method is used:

- The  $V_{SENSE}$  pin voltage is compared to a 2.2 V reference.
- If  $V_{pin4}$  exceeds 2.2 V, the circuit detects a high-line condition and the loop gain is divided by three (the internal PWM ramp slope is three times steeper)
- Once this occurs, if  $V_{pin4}$  remains below 1.7 V for 25 ms, the circuit detects a low-line situation (500 mV hysteresis).

At startup, the circuit is in low-line state (“LLine” high”) until  $V_{pin4}$  exceeds 2.2 V.

The line range detection circuit allows more optimal loop gain control for universal (wide input mains) applications.

As portrayed in Figure 71, the pin 4 voltage is also utilized to generate the current information required for the frequency fold-back function.

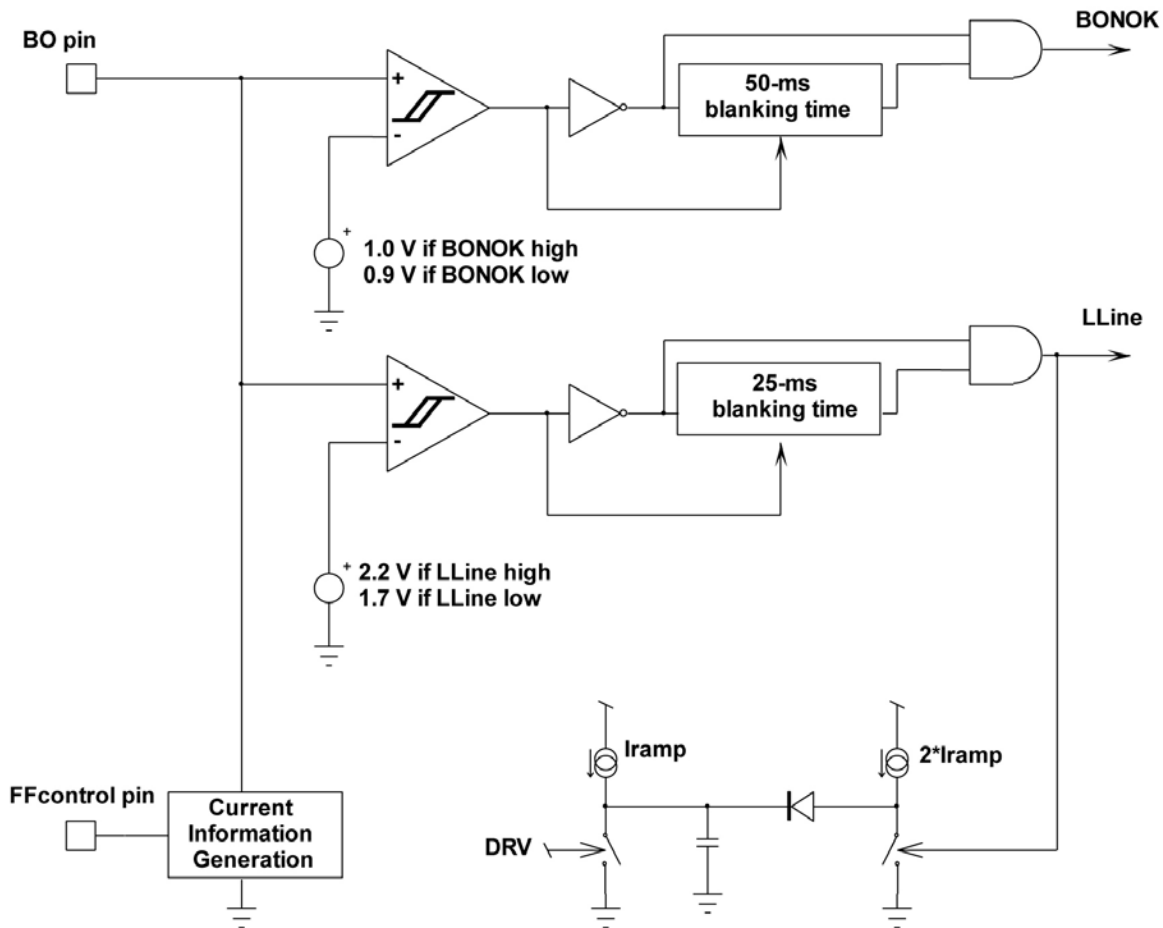


Figure 71. Input Line Sense Monitoring

**Thermal Shutdown (TSD)**

An internal thermal circuitry disables the circuit gate drive and keeps the power switch off when the junction temperature exceeds 150°C. The output stage is then enabled once the temperature drops below about 100°C (50°C hysteresis).

The temperature shutdown remains active as long as the circuit is not reset, that is, as long as  $V_{CC}$  is higher than  $V_{CC(RESET)}$ . The reset action forces the TSD threshold to be the upper one (150°C), thus ensuring that any cold start-up will be done with the proper TSD level.

**Output Drive Section**

The output stage contains a totem pole optimized to minimize the cross conduction current during high frequency operation. The gate drive is kept in a sinking mode whenever the Under-Voltage Lockout is active or more generally whenever the circuit is off. Its high current capability (-500 mA/+800 mA) allows it to effectively drive high gate charge power MOSFET. As the circuit exhibits a large  $V_{CC}$  range (up to 35 V), the drive pin voltage is clamped not to provide the MOSFET gate with more than 14 V.

**Reference Section**

The circuit features an accurate internal 2.5 V reference voltage ( $V_{REF}$ ) optimized to be  $\pm 2.4\%$  accurate over the temperature range.

**OFF Mode**

As previously mentioned, the circuit turns off when one of the following faults is detected:

- Incorrect feeding of the circuit (“UVLO” high when  $V_{CC} < V_{CC(off)}$ ,  $V_{CC(off)}$  equating 9 V typically).
- Excessive die temperature detected by the thermal shutdown.
- Brown-Out Fault and SKIP (see block diagram)
- Output Under-Voltage situation ( $V_{pin1}$  and/or  $V_{pin2}$  lower than 12% of  $V_{REF}$ )
- Latched off produced by pulling the pfcOK pin above 7.5 V.

Generally speaking, the circuit turns off when the conditions are not proper for desired operation. In this mode, the controller stops operating. The major part of the circuit sleeps and its consumption is minimized.

## NCP1612

### Failure Detection

When manufacturing a power supply, elements can be accidentally shorted or improperly soldered. Such failures can also happen to occur later on because of the components fatigue or excessive stress, soldering defaults or external interactions. In particular, adjacent pins of controllers can be shorted, a pin can be grounded or badly connected. Such open/short situations are generally required not to cause fire, smoke nor big noise. The NCP1612 integrates functions that ease meeting this requirement. Among them, we can list:

- Floating feedback pins  
A 250 nA sink current source pulls down the voltage on the feedback and FOVP/BUV pin so that the UVP protection trips and prevents the circuit from operating if one of this pin is floating. This current source is small (450 nA maximum) so that its impact on the output regulation and OVP levels remain negligible with the resistor dividers typically used to sense the bulk voltage.
- Fault of the GND connection  
If the GND pin is properly connected, the supply current drawn from the positive terminal of the  $V_{CC}$  capacitor, flows out of the GND pin to return to the negative terminal of the  $V_{CC}$  capacitor. If the GND pin is not connected, the circuit ESD diodes offer another return path. The accidental non connection of the GND pin can hence be detected by detecting that one of this

ESD diode is conducting. Practically, the CS/ZCD ESD diode is monitored. If such a fault is detected for 200  $\mu$ s, the circuit stops operating.

- Detection the CS/ZCD pin improper connection  
The CS/ZCD pin sources a 1  $\mu$ A current to pull up the pin voltage and hence disable the part if the pin is floating. If the CS/ZCD pin is grounded, the circuit cannot monitor the ZCD signal and the 200  $\mu$ s watchdog timer is activated. When the watchdog time has elapsed, the circuit sources a 250  $\mu$ A current source to pull-up the CS/ZCD pin voltage. No drive pulse is initiated until the CS/ZCD pin voltage exceeds the ZCD 0.75 V threshold. Hence, if the pin is grounded, the circuit stops operating. Circuit operation requires the pin impedance to be 3.9 k $\Omega$  or more, the tolerance of the NCP1612 impedance testing function being considered over the  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  temperature range.
- Boost or bypass diode short  
The NCP1612 addresses the short situations of the boost and bypass diodes (a bypass diode is generally placed between the input and output high-voltage rails to divert this inrush current). Practically, the overstress protection is implemented to detect such conditions and forces a low duty-cycle operation until the fault is gone.

Refer to application note AND9079/D for more details.

### ORDERING INFORMATION

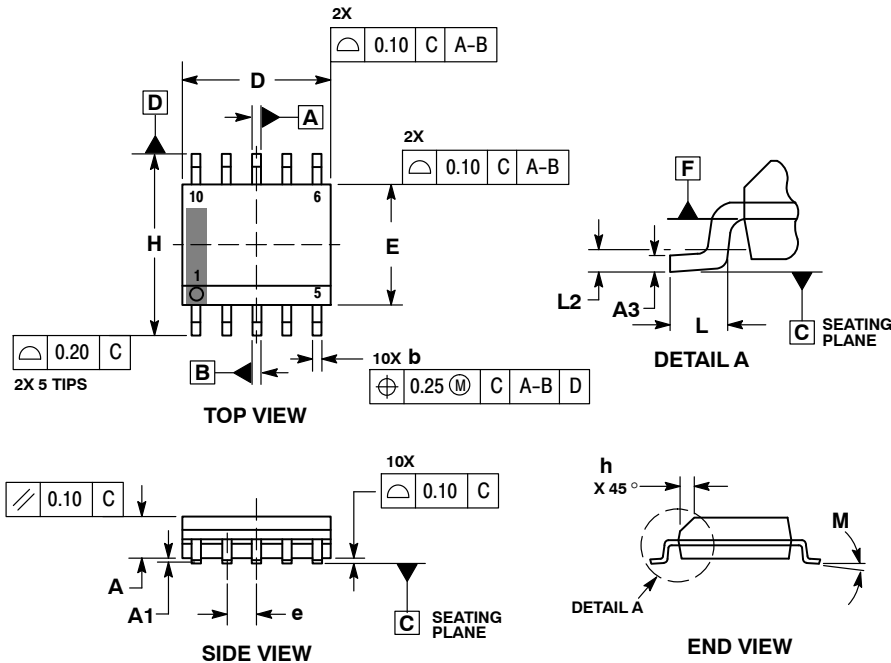
Device	Circuit Version	Marking	Package	Shipping <sup>†</sup>
NCP1612ADR2G	NCP1612A	1612A	SOIC-10 (Pb-Free)	3000 / Tape & Reel
NCP1612BDR2G	NCP1612B	1612B		

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NCP1612

## PACKAGE DIMENSIONS

SOIC-10 NB  
CASE 751BQ  
ISSUE A

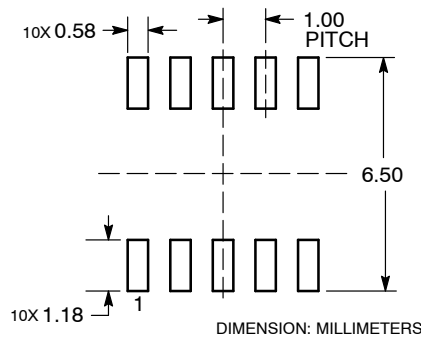


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF 'b' AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS	
	MIN	MAX
A	1.25	1.75
A1	0.10	0.25
A3	0.17	0.25
b	0.31	0.51
D	4.80	5.00
E	3.80	4.00
e	1.00 BSC	
H	5.80	6.20
h	0.37 REF	
L	0.40	1.27
L2	0.25 BSC	
M	0°	8°

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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