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MAX20334

Overvoltage and Surge-Protected Dual SPDT Data Line Switch

General Description

The MAX20334 is a 2 x SPDT switch with overvoltage protection intended for use with portable devices. In high-voltage charging solutions, a data line short event to the high-voltage V_{BUS} can result in either charger misdetection or permanent damage to the portable device. The MAX20334 is designed to protect the downstream data line from a high-voltage short or surge event.

The device combines low on-capacitance (C_{ON}) and low on-resistance (R_{ON}) necessary for high-performance switching applications in portable electronics. The MAX20334 features internal positive overvoltage, negative overvoltage, and surge protection. The device handles USB low/full/high-speed signaling and operates from a 2.7V to 5.5V supply.

The MAX20334 is available in a 12-bump (1.23mm x 1.63mm) wafer-level package (WLP) and operates over the -40°C to +85°C extended temperature range.

Applications

- Smart Phones
- Phablets
- Tablets

Benefits and Features

- Distortion-Free, High-Speed Signaling
 - Dual SPDT
 - Signal Range: 0V to 5V
 - R_{ON} : 4 Ω (typ)
 - Bandwidth 600MHz
- Flexible System Design
 - Separate Control for Each Switch Path
 - $\overline{EN}$ to Save Supply Current
 - FLAG Signals Fault Event
 - 12-Bump WLP (1.23mm x 1.63mm) Package
 - -40°C to +85°C Operating Temperature Range
- Robust and Safety
 - Positive Overvoltage Protection up to +20.5V
 - Hot Plug-In Robustness

Ordering Information appears at end of data sheet.

Absolute Maximum Ratings

(All voltages referenced to GND.)

V _{CC} , CSA, CSB, EN, FLAG	-0.5V to +6V
COMA, COMB (Note 1)	-0.5V to +20.5V
PA1, PA2, PB1, PB2	-0.5V to +6V
Current into all pins	±100mA

Continuous Power Dissipation (T_A = +70°C)

WLP (derate 13.73mW/°C above +70°)	1098mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Surge capable from -30V to +45V by the surge tester with 2Ω source impedance IEC61000-4-5 modified waveform.

Package Information

PACKAGE TYPE: 12 WLP	
Package Code	W121C1+1
Outline Number	21-100286
Land Pattern Number	Refer to Application Note 1891
THERMAL RESISTANCE (FOUR-LAYER BOARD)	
Junction to Ambient (θ _{JA})	72.8°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 4.3V, T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY OPERATION						
Operating Voltage	V _{CC}		2.7		5.5	V
Supply Current	I _{CC}	V _{IN} below OVLO		26	51	μA
Supply OVLO Shutdown Current	I _{CC_O}	V _{COM_} = 6V, V _{PA_} /V _{PB_} = 0V		29	58	μA
Power On Reset	V _{POR}			2.3		V
COMA, COMB, PA1, PA2, PB1, PB2						
Positive Overvoltage Trip Level	V _{POVLO}	(Note 3) V _{IN} rising	4.6	4.8	5	V
		V _{IN} falling	4.5			
COM_ On Leakage Equivalent Resistance	R _{COM_ON}	V _{COM_} = 2.5V	3	6.3	15	MΩ
PA_, PB_ Off Leakage Current	I _{P_OFF}	Switch open, V _{CC} = 3V, V _{PA_} = 0V, 2.5V, V _{COM_} = 0V, 2.5V	-0.1		0.1	μA
COM_ Current Sink		V _{COM_} = 20V		0.3		mA
COM_ Positive Overvoltage Fault Protection Response Time	t _{FP}	V _{COM_} = 1V to 10V step, V _{CC} = 2.7V to 5.5V, R _{PA_} = R _{PB_} = 1kΩ, (Figure 2)		100		ns
COM_ Positive Overvoltage Fault Protection Recovery Time	t _{FPR}	V _{COM_} = 10V to 1V step, V _{CC} = 2.7V to 5.5V, R _{PA_} = R _{PB_} = 1kΩ, (Figure 2)		80		μs

Electrical Characteristics (continued)

(V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 4.3V, T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
COMA to PA1/PA2, COMB to PB1/PB2						
Analog Signal Range	V _{COM_}		0		5	V
Internal SWPOS Regulator	V _{SWPOS}	V _{CC} = 2.7V		5		V
On-Resistance	R _{ON}	V _{CC} = 3V, I _{COM_} = 10mA, T _A = +25°C		4	8	Ω
On-Resistance Match Between Channels	ΔR _{ON}	V _{CC} = 3V, V _{P_} = 0V, I _{COM_} = 10mA (Note 4, 5)			0.2	Ω
On-Resistance Flatness	R _{FLAT}	V _{CC} = 3V, I _{COM_} = 10mA, V _{COM_} = 0V to 1V (Note 6)			0.3	Ω
Turn-On Time (Figure 3)	t _{ON}	V _{PA_} /V _{PB_} = 1.5V, R _L = 50Ω, From an CSA/CSB control		45	90	μs
		V _{PA_} /V _{PB_} = 1.5V, R _L = 50Ω, From an $\overline{\text{EN}}$ control		90	120	
Turn-Off Time (Figure 3)	t _{OFF}	V _{PA_} /V _{PB_} = 1.5V, R _L = 50Ω, $\overline{\text{EN}}$ control or CSA/CSB control		0.5	10	μs
Output Skew Same Switch	t _{SK(P)}	Figure 4		40		ps
Output Skew Between Switch	t _{SK(O)}	Figure 4		40		ps
Break-Before-Make Time Delay	t _D	R _L = 50Ω, time delay between one side of the switch opening and the other side closing		20		μs
Power On Reset Time	t _{POR}			0.4	0.7	ms
COM_ On Capacitance	C _{COM_ON}	V _{COM_} = 0.5V _{PP} , DC bias = 0V, f = 1MHz		10		pF
DIGITAL SIGNAL ($\overline{\text{FLAG}}$, $\overline{\text{EN}}$, CSA, CSB)						
$\overline{\text{FLAG}}$ Output Voltage Low	V _{OL}	I _{$\overline{\text{FLAG}}$} = 1mA			0.4	V
$\overline{\text{FLAG}}$ Output Leakage	I _{LEAK}	V _{$\overline{\text{FLAG}}$} = 5.5V	-1		1	μA
Input Voltage High	V _{IH}	$\overline{\text{EN}}$, CSA, CSB	1.4			V
Input Voltage Low	V _{IL}	$\overline{\text{EN}}$, CSA, CSB			0.4	V
Input Leakage	I _{LEAK}	$\overline{\text{EN}}$, CSA, CSB = 5.5V or GND	-1		1	μA
AC CHARACTERISTICS (NOTE 4)						
-3dB Bandwidth	BW	V _{COM_} = 0dBm, R _S = R _L = 50Ω, Figure 5		600		MHz
Off Isolation		f = 100kHz, V _{COM_} = 1V _{RMS} , R _L = 50Ω, Figure 5		-95		dB
Crosstalk (Note 7)		f = 100kHz, V _{COM_} = 1V _{RMS} , R _L = 50Ω, Figure 5		-80		dB

Electrical Characteristics (continued)

(V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 4.3V, T_A = +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL PROTECTION						
Thermal Shutdown	T _{SHDN}			150		°C
Thermal Hysteresis	T _{HYST}			20		°C
ESD PROTECTION						
Human Body Model	COMA, COMB			±15		kV
IEC61000-4-2 Contact Discharge	COMA, COMB	(Note 8)		±8		kV
IEC61000-4-2 Air Gap	COMA, COMB			±15		kV
Human Body Model	All Other Pins			±2		kV

- Note 2:** All devices are 100% production tested at T_A = +25°C. Specifications over the operating temperature range are guaranteed by design.
- Note 3:** The switch turns off for voltages above V_{POVLO} protecting downstream circuits in case of a fault condition.
- Note 4:** Guaranteed by design.
- Note 5:** $\Delta R_{ON(MAX)} = |R_{ON(CH1)} - R_{ON(CH2)}|$
- Note 6:** Flatness is defined as the difference between the maximum and minimum value of on-resistance, as measured over specified analog signal ranges.
- Note 7:** Between two switches.
- Note 8:** Strike applied through 1m cable, 12nH peaking inductors installed in series with COMx pins.

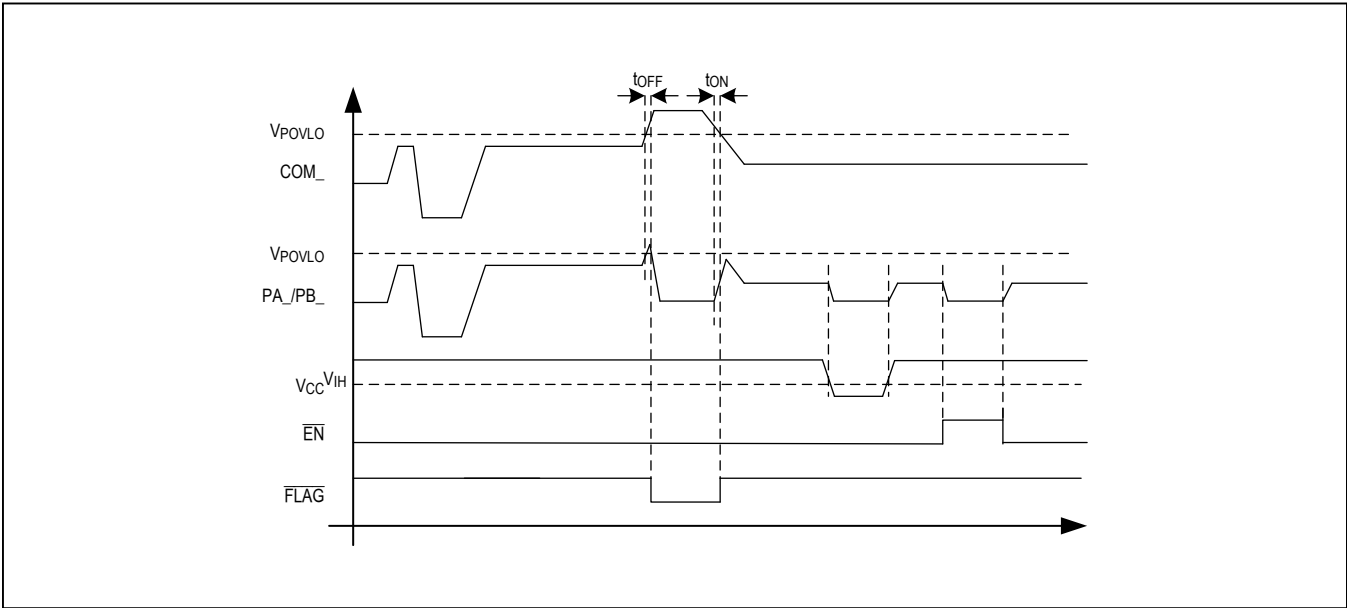


Figure 1. Timing Diagram

MAX20334

Overvoltage and Surge-Protected

Dual SPDT Data Line Switch

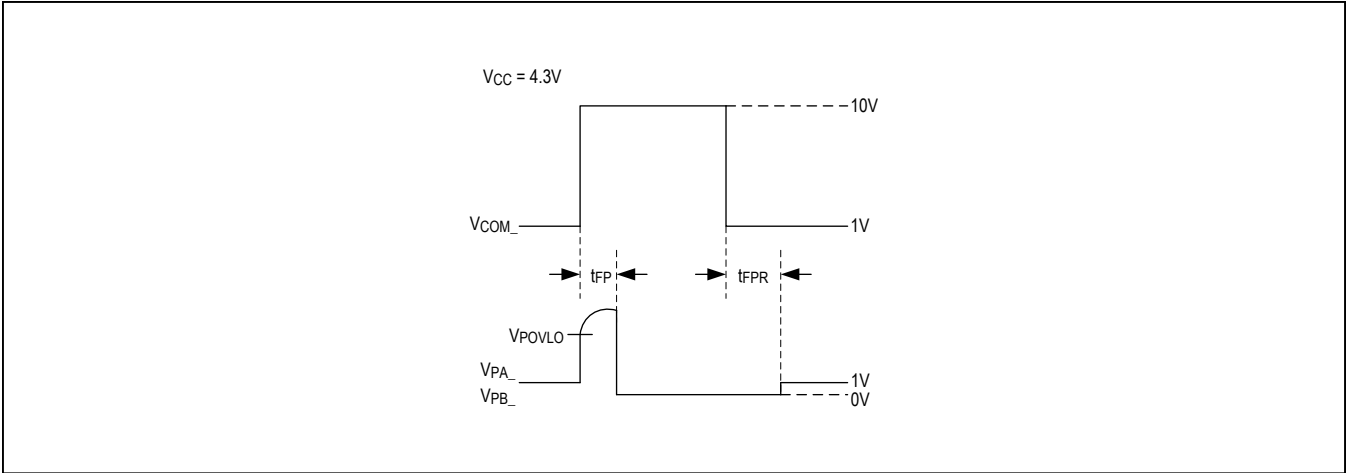


Figure 2. Fault Protection Timing Diagram

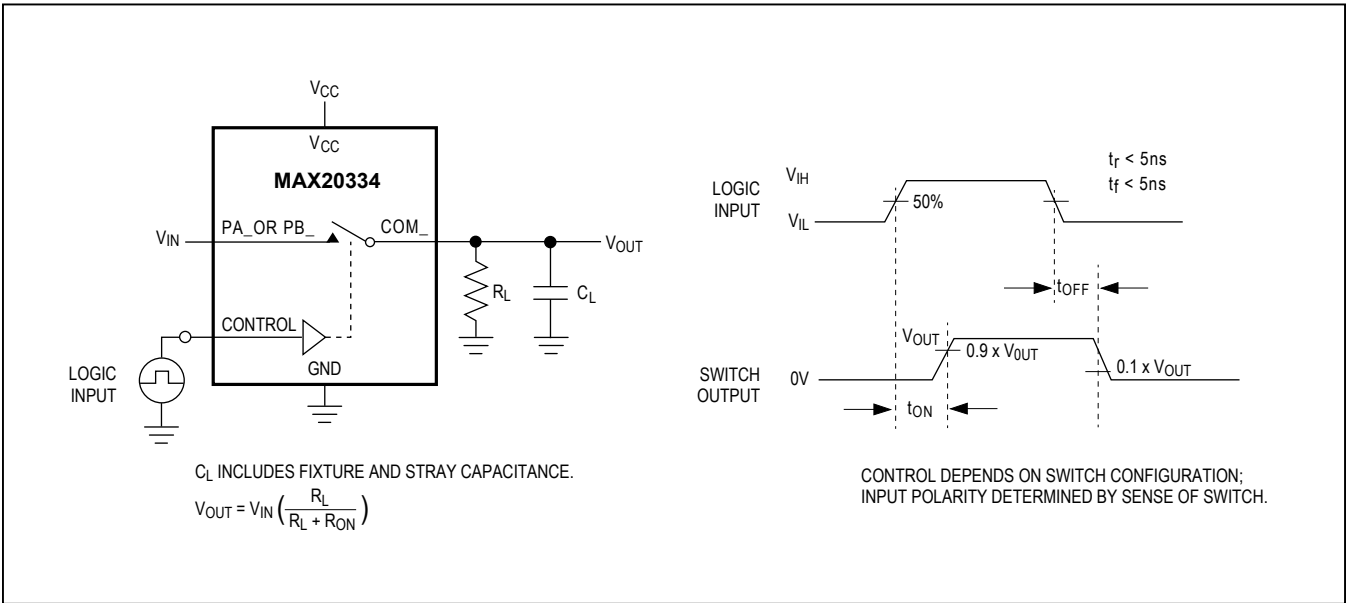


Figure 3. Switching Timing Diagram

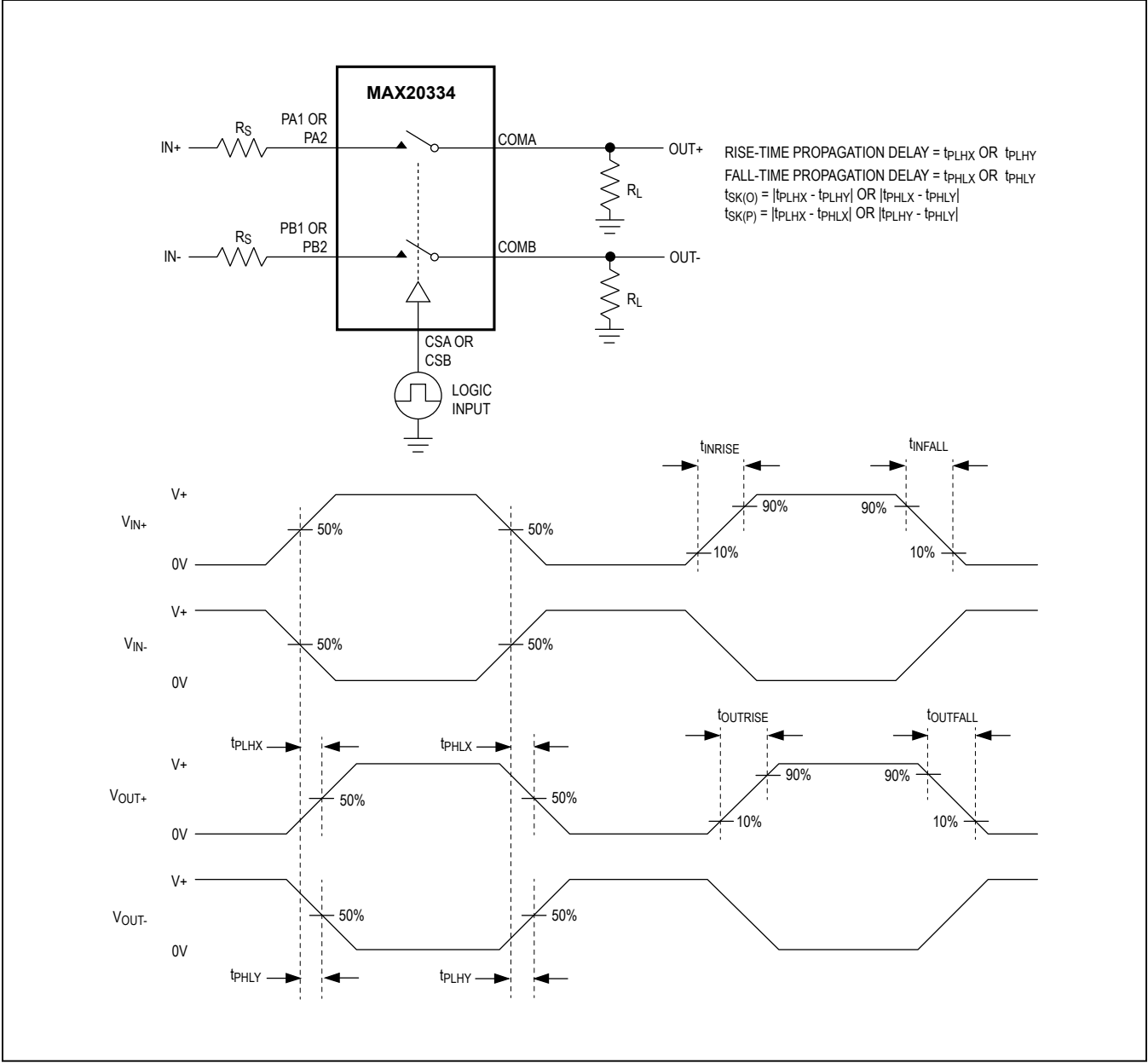


Figure 4. Output Skew Timing Diagram

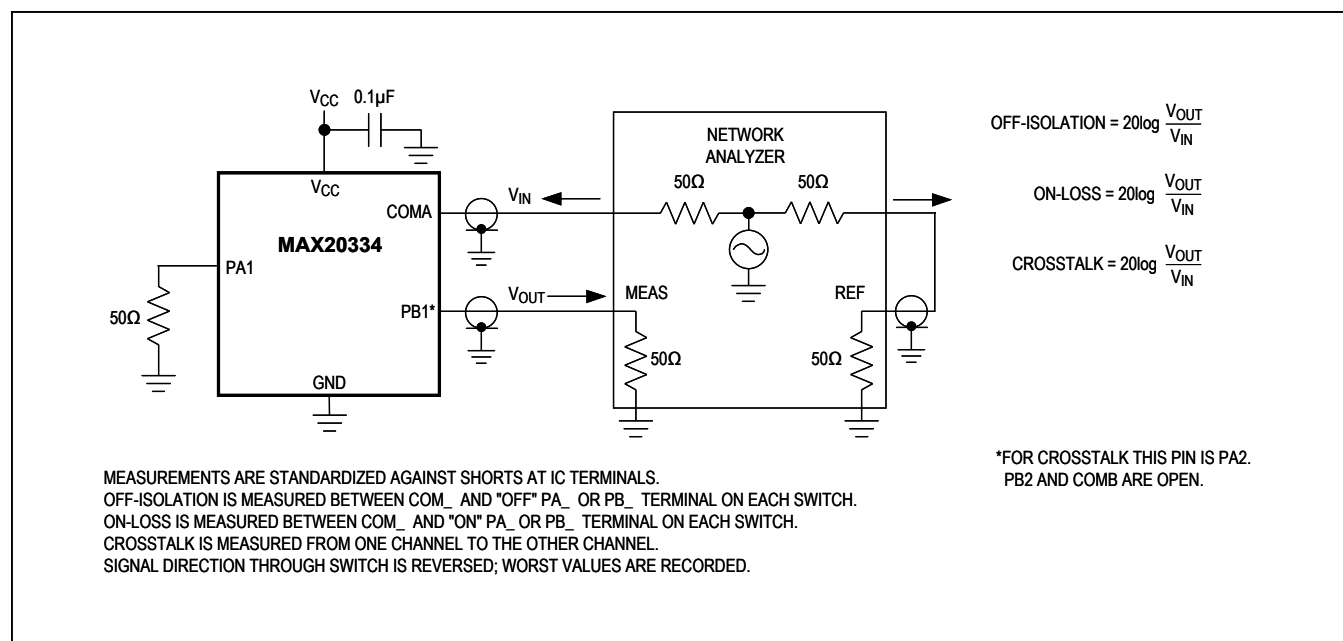
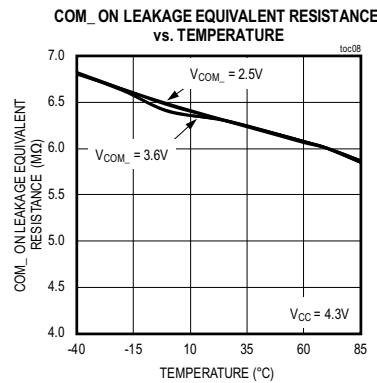
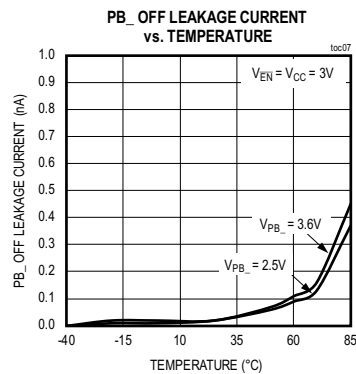
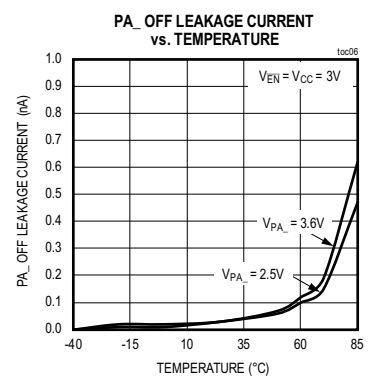
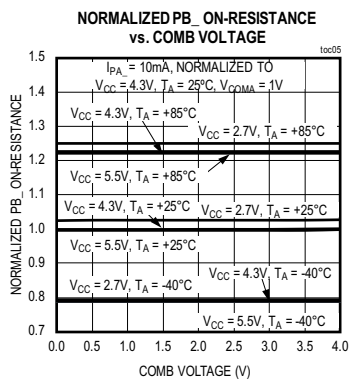
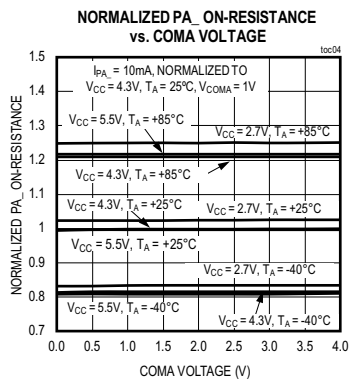
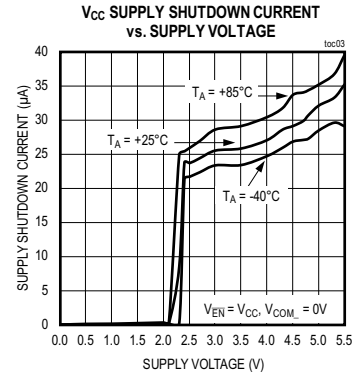
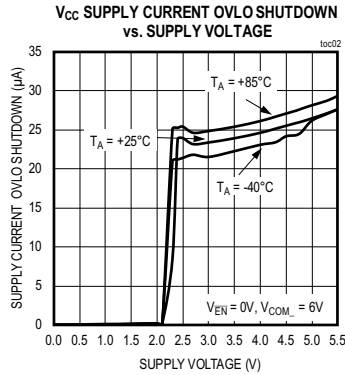
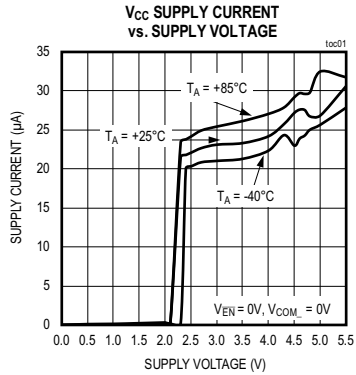
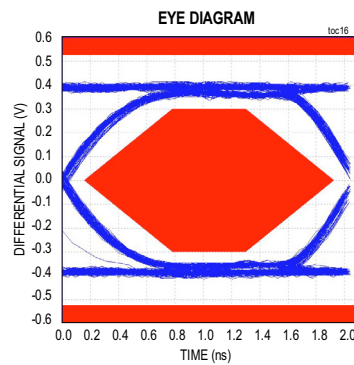
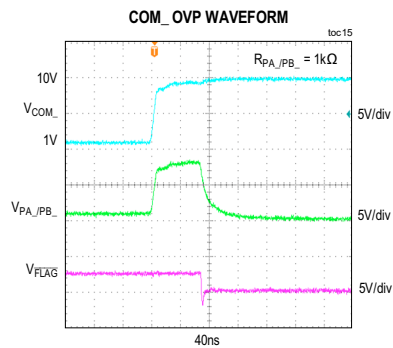
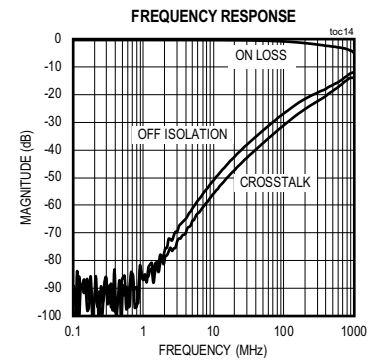
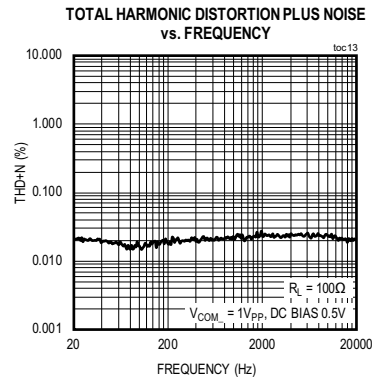
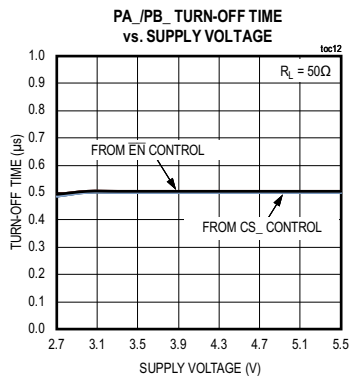
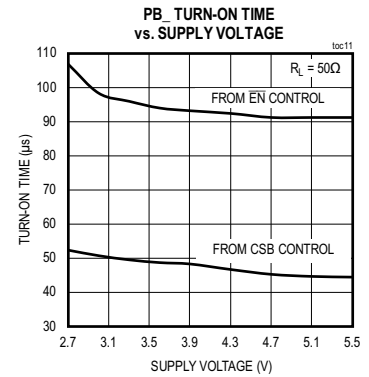
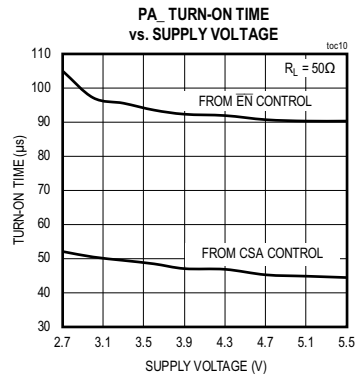
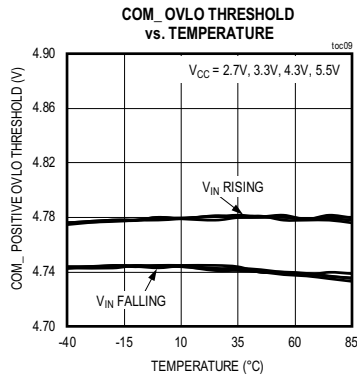


Figure 5. On-Loss, Off-Isolation, and Crosstalk

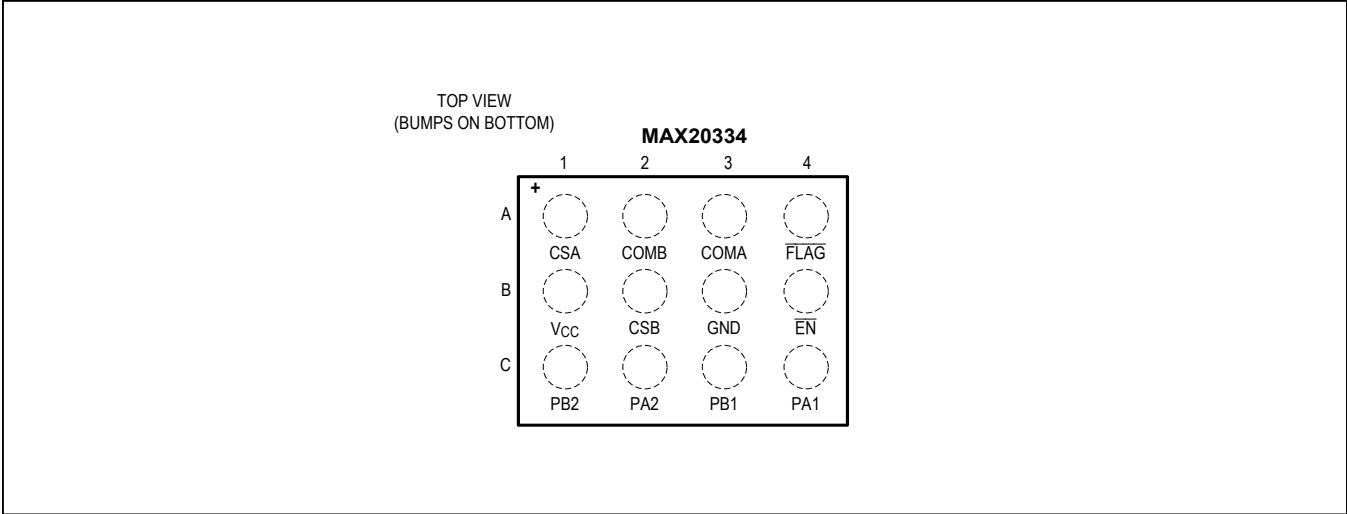
Typical Operating Characteristics

(V_{CC} = 4.3V, T_A = +25°C, unless otherwise noted.)

Typical Operating Characteristics (continued)

(V_{CC} = 4.3V, T_A = +25°C, unless otherwise noted.)

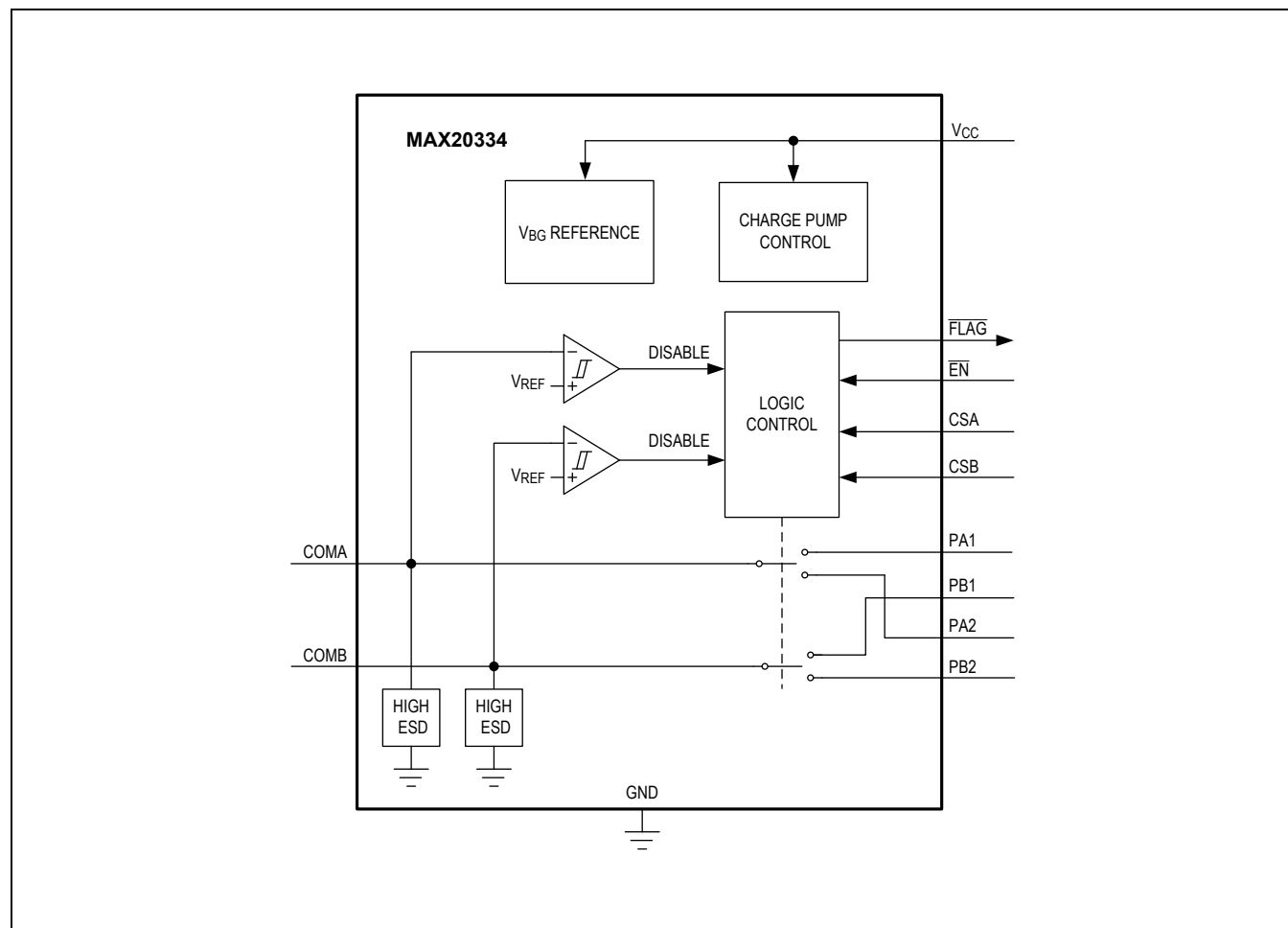
Bump Configuration



Bump Description

BUMP	NAME	FUNCTION
A1	CSA	Channel Select Input for COMA. When CSA is low, COMA is connected to PA1. When CSA is high, COMA is connected to PA2.
A2	COMB	Data Line B Input from External USB Port
A3	COMA	Data Line A Input from External USB Port
A4	FLAG	Open-Drain Flag Output. $\overline{\text{FLAG}}$ is driven low when OVP or thermal shutdown occurs.
B1	V _{CC}	Supply Voltage Input. Bypass V _{CC} with a 0.1 μ F ceramic capacitor as close to the device as possible.
B2	CSB	Channel Select Input for COMB. When CSB is low, COMB is connected to PB1. When CSB is high, COMB is connected to PB2.
B3	GND	Ground
B4	$\overline{\text{EN}}$	Active-Low Enable Input
C1	PB2	Data Line 2 to COMB
C2	PA2	Data Line 2 to COMA
C3	PB1	Data Line 1 to COMB
C4	PA1	Data Line 1 to COMA

Functional Diagram



Detailed Description

The MAX20334 is a high ESD and surge-protected, dual-SPDT switch that operates from a 2.7V to 5.5V supply and are designed to multiplex USB 2.0 high-speed signals and various analog signals. The switch combines low on-capacitance (C_{ON}) and low on-resistance (R_{ON}) necessary for high-performance switching applications, while withstanding the overvoltage event. The device meets the requirements for USB 2.0 signaling.

Analog Signal

The MAX20334 is bidirectional, allowing PA₊, PB₊, and COM₊ to be configured as either inputs or outputs.

The device can handle analog signals 0V to 5V.

Switch Control

The MAX20334 switches are individually controlled by CSA and CSB. When $\overline{EN}$ is high, the switches are open and the device is in a low supply current mode. (Table 1)

FLAG Output

The $\overline{FLAG}$ is an open-drain output. It asserts low when there is an overvoltage, or a thermal shutdown occurs.

Thermal Shutdown Protection

The MAX20334 features thermal shutdown protection to protect the device from overheating. The device turns off when the junction temperature exceeds +150°C (typ). The device exits thermal shutdown and resumes normal operation after the junction temperature cools by 20°C (typ). During thermal shutdown, the switches are open.

Application Information

Extended ESD

ESD protection structures are incorporated on all pins to protect against electrostatic discharges up to $\pm 2\text{kV}$ (Human Body Model) encountered during handling and

assembly. COMA and COMB are further protected against ESD up to $\pm 15\text{kV}$ (Human Body Model), $\pm 15\text{kV}$ (Air Gap Discharge method described in IEC 61000-4-2), and $\pm 8\text{kV}$ (Contact Discharge method described in IEC61000-4-2) without damage. Note that, if PA₊ and PB₊ are used as inputs and require higher than $\pm 2\text{kV}$, additional ESD protection is needed.

The ESD structures withstand high ESD, both in normal operation and when the device is powered down. After an ESD event, the MAX20334 continues to function without latchup.

ESD Test Condition

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 6 shows the Human Body Model, while Figure 7 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5k Ω resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The major difference between tests performed using the Human Body Model and those using IEC 61000-4-2 is the higher peak current in IEC 61000-4-2. This is due the series resistance being lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 8 shows the IEC 61000-4-2 model, while Figure 9 shows the current waveform for the IEC 61000-4-2 ESD Contact Discharge test.

Table 1. Functional Truth Table

	$\overline{EN}$				
	0				1
	[CSA:CSB]				[CSA:CSB]
	00	01	10	11	D.C.
COMA =	PA1	PA1	PA2	PA2	OPEN
COMB =	PB1	PB2	PB1	PB2	OPEN

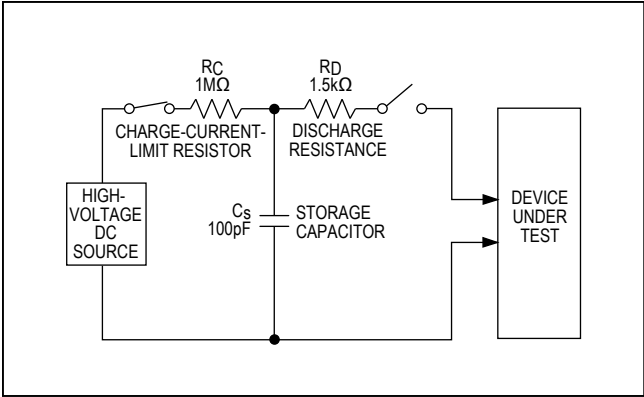


Figure 6. Human Body ESD Test Model

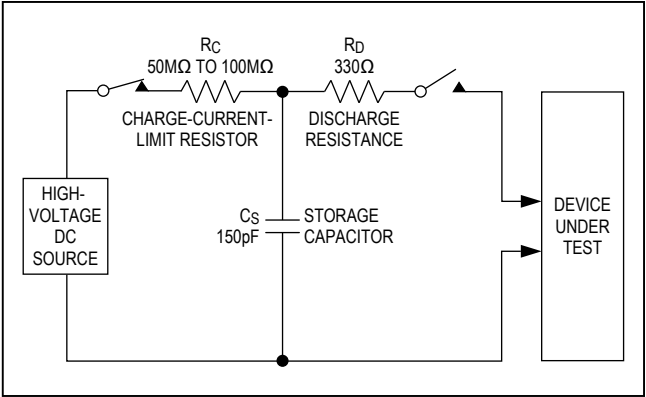


Figure 8. IEC 61000-4-2 ESD Test Model

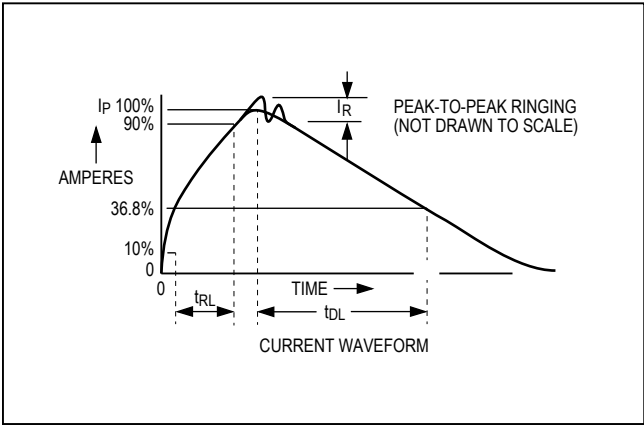


Figure 7. Human Body Current Waveform

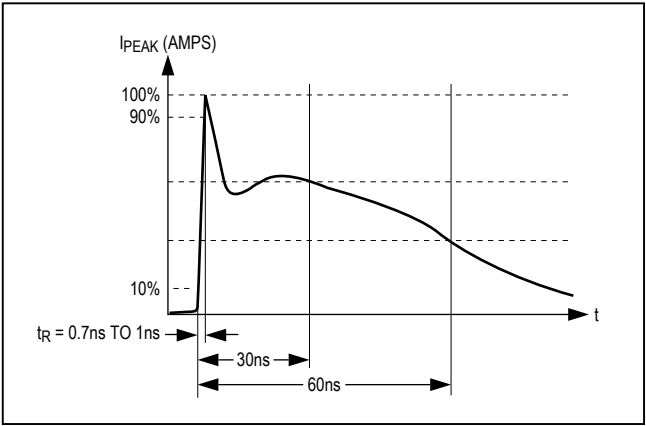
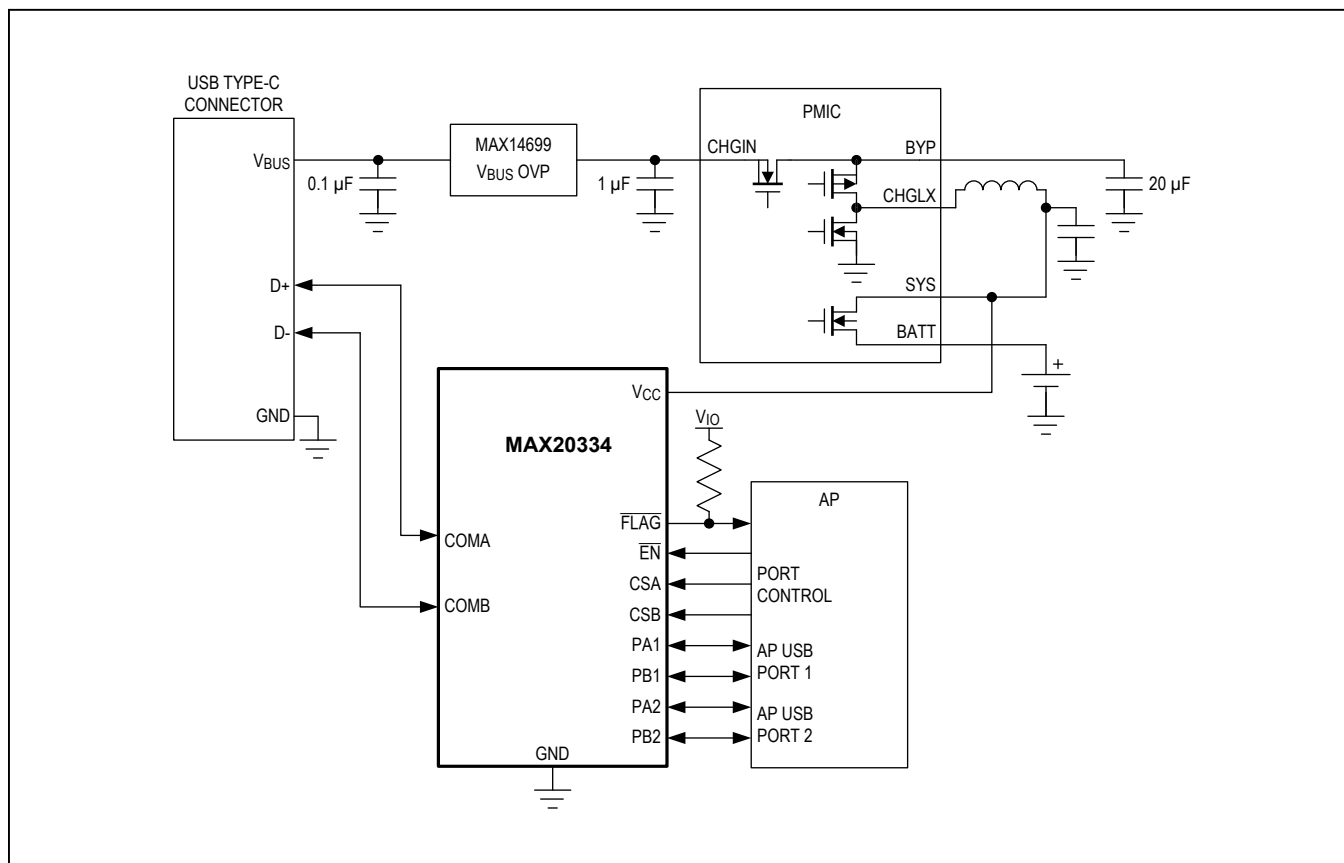


Figure 9. IEC 61000-4-2 ESD Generator Current Waveform

Typical Application Circuit



Chip Information

PROCESS: BiCMOS

Ordering Information

PART	TOP MARK	TEMP RANGE	PIN-PACKAGE
MAX20334EWC+T	AEI	-40°C TO +85°C	12 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/19	Initial release	—
1	9/19	Updated <i>Electrical Characteristics</i> table, <i>Extended ESD</i> section	4, 12

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at <https://www.maximintegrated.com/en/storefront/storefront.html>.

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