

Nonvolatile, 32-Position Digital Potentiometer

DS4301

General Description

The DS4301 is a single 32-position linear digital potentiometer with 200kΩ end-to-end resistance. The wiper setting is stored in EEPROM, so the DS4301 powers up with the last stored setting. The position of the wiper is controlled through a simple three-terminal increment/decrement interface. The DS4301 is ideal for white LED backlight brightness control. Its 8-pin μSOP package, 2.4V to 5.5V supply range, and 200kΩ end-to-end resistance are especially suited for portable, battery-powered applications such as cellular telephones and PDAs.

Applications

- White LED Backlight Brightness Control
- Portable Battery-Powered Devices such as PDAs and Cellular Phones
- Any Application that Requires a Small, Low-Cost NV Potentiometer

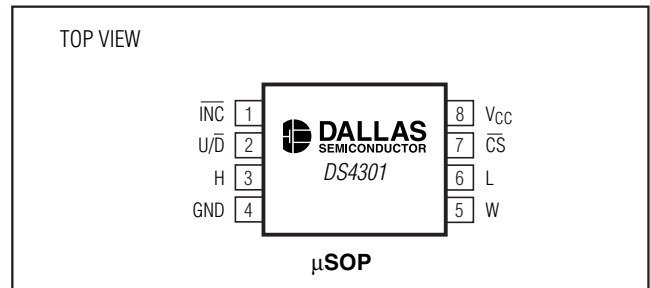
Features

- ◆ Single, 32-Position, 200kΩ Linear Nonvolatile (NV) Potentiometer Ideal for Battery-Powered Applications
- ◆ Three-Terminal Increment/Decrement Interface to Adjust Wiper Position
- ◆ Wide Voltage Supply Range (2.4V to 5.5V)
- ◆ Command-Initiated NV Wiper Storage
- ◆ Operates Over the Industrial Temperature Range (-40°C to +85°C)
- ◆ Available in 8-Pin μSOP

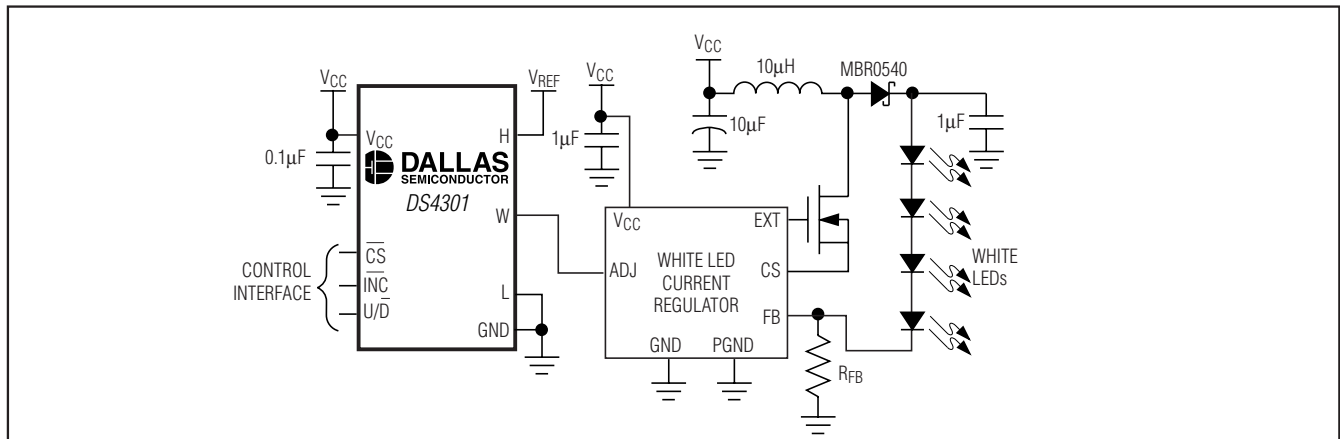
Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|-------------|----------------|------------------|
| DS4301U-200 | -40°C to +85°C | 8 μSOP (118 mil) |

Pin Configuration



Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC} Pin Relative to Ground-0.5V to +6.0V
 Voltage Range on \overline{CS} , \overline{INC} , U/\overline{D} , L, W, H Pins
 Relative to Ground*-0.5V to $V_{CC} + 0.5V$
 Wiper Current $\pm 3mA$
 Operating Temperature Range-40°C to +85°C

Programming Temperature0°C to +70°C
 Storage Temperature Range-55°C to +125°C
 Soldering TemperatureSee IPC/JEDEC
 J-STD-020A Specification

*Not to exceed 6.0V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATION CONDITIONS

($V_{CC} = V_{CC\ MIN}$ to $V_{CC\ MAX}$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise specified.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|----------|------------|---------------------|----------------------|------|-------|
| Supply Voltage | V_{CC} | (Note 1) | +2.4 | | +5.5 | V |
| Input Logic 1 (\overline{CS} , \overline{INC} , U/\overline{D}) | V_{IH} | | $0.7 \times V_{CC}$ | $V_{CC} + 0.3$ | | V |
| Input Logic 0 (\overline{CS} , \overline{INC} , U/\overline{D}) | V_{IL} | | -0.3 | $+0.3 \times V_{CC}$ | | V |
| Resistor Inputs | L, H, W | | -0.3 | $V_{CC} + 0.3$ | | V |
| Wiper Current | I_W | | -1 | | +1 | mA |

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = V_{CC\ MIN}$ to $V_{CC\ MAX}$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise specified.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------|------------|------------|-----|-----|-----|---------|
| Input Leakage | I_L | | -1 | | +1 | μA |
| Standby Current (Note 2) | I_{STBY} | 3V | | 30 | 60 | μA |
| | | 5V | | 15 | 60 | |
| Digital Input Capacitance | $C_{I/O}$ | | | | 10 | pF |

ANALOG RESISTOR CHARACTERISTICS

($V_{CC} = V_{CC\ MIN}$ to $V_{CC\ MAX}$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise specified.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------|--------|---------------------|-------|-----|-------|-----------------|
| End-to-End Resistor Tolerance | | $T_A = +25^\circ C$ | -20 | | +20 | % |
| Wiper Resistance | R_W | | | 500 | 2000 | Ω |
| Absolute Linearity | | (Note 3) | -0.5 | | +0.5 | LSB |
| Relative Linearity | | (Note 4) | -0.25 | | +0.25 | LSB |
| End-to-End Temp Coefficient | | | -250 | | +250 | ppm/ $^\circ C$ |
| Ratiometric Temp Coefficient | | | | 7 | | ppm/ $^\circ C$ |

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AC ELECTRICAL CHARACTERISTICS

($V_{CC} = V_{CC\ MIN}$ to $V_{CC\ MAX}$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$. See Figure 2 for timing diagram.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------|------------|-----|-----|-----|---------|
| \overline{CS} to \overline{INC} Setup | t_{CI} | | 50 | | | ns |
| U/\overline{D} to \overline{INC} Setup | t_{DI} | | 100 | | | ns |
| \overline{INC} Low Period | t_{iL} | | 50 | | | ns |
| \overline{INC} High Period | t_{iH} | | 100 | | | ns |
| \overline{INC} Inactive to \overline{CS} Inactive | t_{iC} | | 500 | | | ns |
| \overline{CS} Deselect Time | t_{CPH} | | 100 | | | ns |
| Wiper Change to \overline{INC} Low | t_{iW} | | | | 200 | ns |
| \overline{INC} Rise and Fall Times | t_R, t_F | | | | 5 | μs |
| \overline{INC} Low to \overline{CS} Inactive | t_{iK} | (Note 5) | 50 | | | ns |
| Wiper Storage Time | t_{WST} | (Note 6) | | | 10 | ms |
| \overline{CS} Low Pulse | t_{CLP} | | 100 | | | ns |
| Wiper Load Time | t_{WLT} | (Note 7) | | 500 | | μs |
| Power-Up Time | t_{PU} | (Note 8) | | 2 | | ms |

NONVOLATILE MEMORY CHARACTERISTICS

($V_{CC} = V_{CC\ MIN}$ to $V_{CC\ MAX}$)

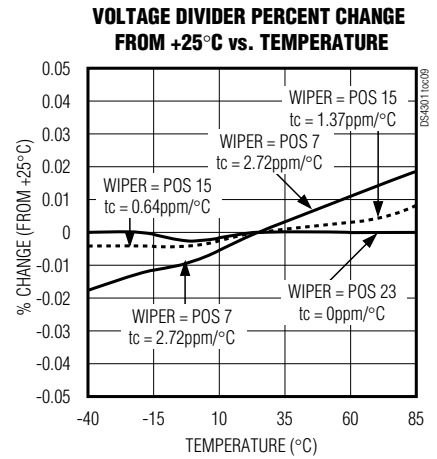
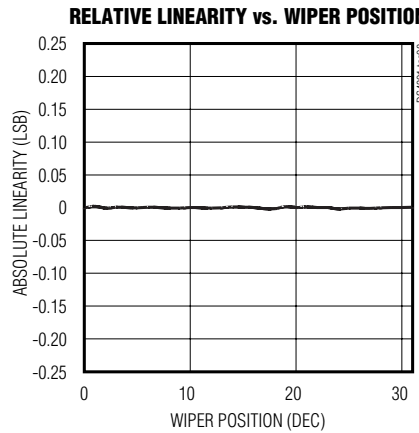
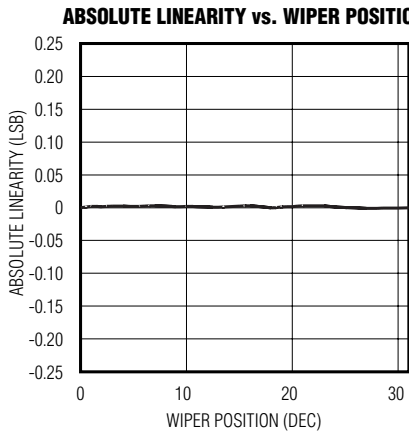
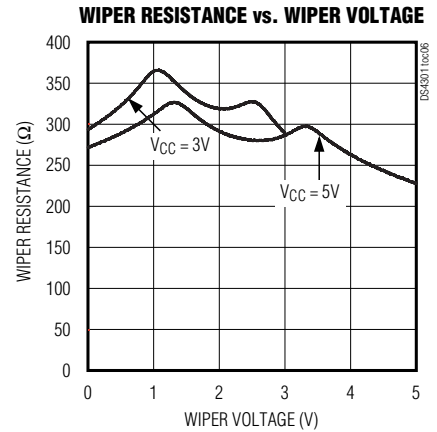
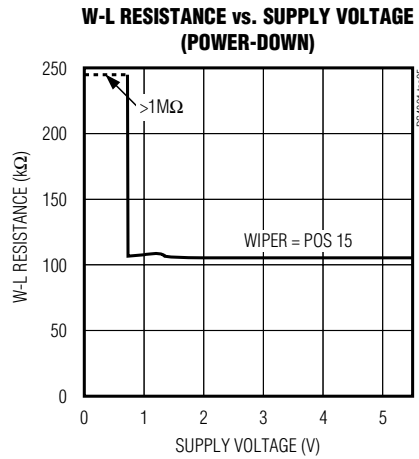
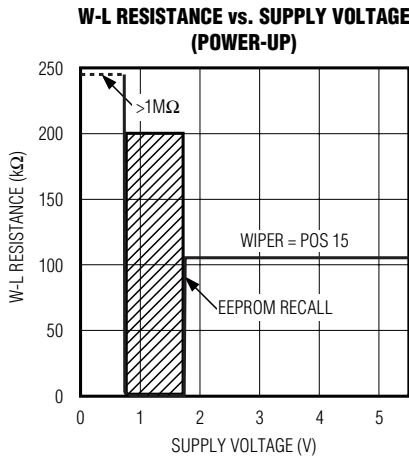
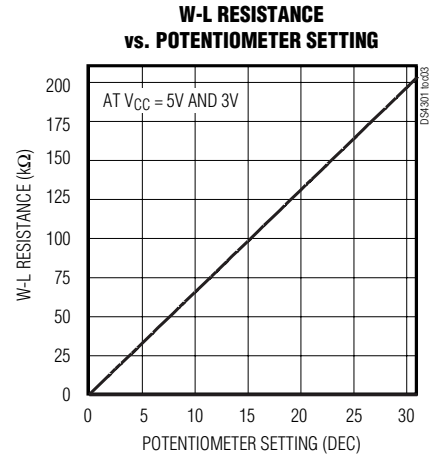
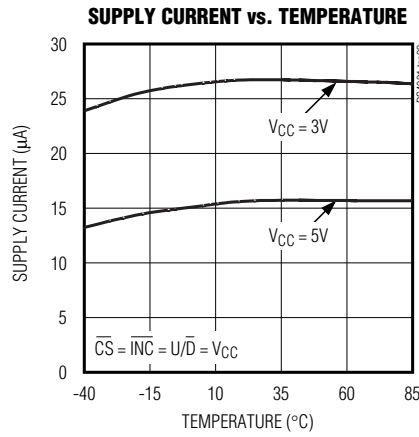
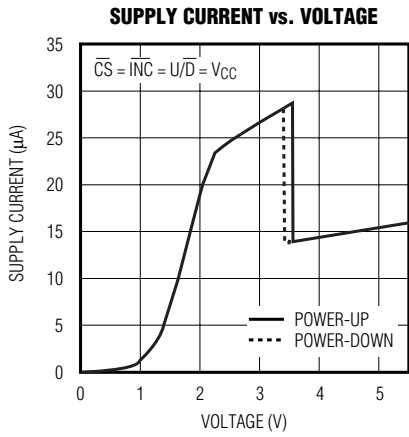
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------|--------|----------------|--------|-----|-----|-------|
| EEPROM Write Cycles | | +70°C (Note 9) | 50,000 | | | |

- Note 1:** All voltages are referenced to ground.
- Note 2:** STBY specified for V_{CC} equal to 3.0V and 5.0V while control port logic pins are driven to V_{CC} or GND.
- Note 3:** Absolute linearity is used to determine wiper voltage versus expected voltage as determined by wiper position.
- Note 4:** Relative linearity is used to determine the change of wiper voltage between two adjacent wiper positions.
- Note 5:** The \overline{INC} low to \overline{CS} inactive time is the transition time that allows the three control pins to become inactive without writing the wiper position to the EEPROM.
- Note 6:** Wiper storage time is the time required for the wiper position to be written to the EEPROM. During this time, the three-terminal interface is inactive.
- Note 7:** Wiper load time is specified as the time required to load the wiper position stored in EEPROM once V_{CC} has reached a stable operating voltage greater than or equal to $V_{CC\ MIN}$.
- Note 8:** Power-up time is specified as the time required before the three control pins become active once a stable power supply level of at least $V_{CC\ MIN}$ has been reached.
- Note 9:** The maximum number of EEPROM write cycles is guaranteed by design and is not tested in production.

Nonvolatile, 32-Position Digital Potentiometer

Typical Operating Characteristics

($V_{CC} = 5.0V$; $T_A = +25^\circ C$, unless otherwise noted.)

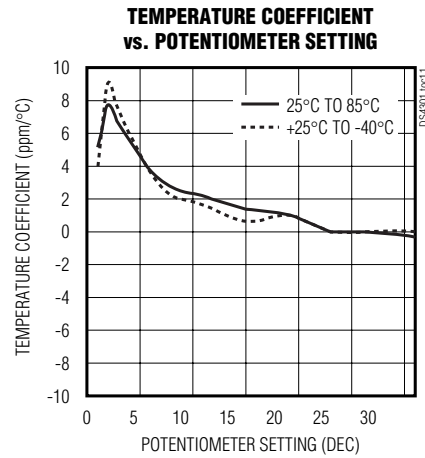
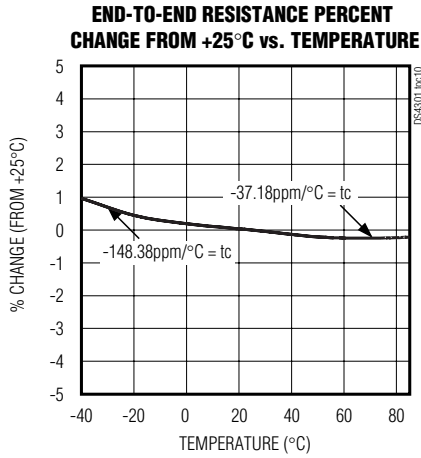


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Typical Operating Characteristics (continued)

($V_{CC} = 5.0V$; $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

| PIN | NAME | FUNCTION |
|-----|------------------|--|
| 1 | \overline{INC} | Increment/Decrement Wiper Control. When \overline{INC} transitions from high-to-low, the wiper moves in the direction established by the state of the U/\overline{D} pin. |
| 2 | U/\overline{D} | Up/Down Control. Sets the directions of wiper movement. When set to a high state, a high-to-low transition on the \overline{INC} pin increments the wiper. When set to a low state, a high-to-low transition on the \overline{INC} pin decrements the wiper. |
| 3 | H | High-End Terminal of the Potentiometer |
| 4 | GND | Ground Terminal |
| 5 | W | Wiper Terminal of the Potentiometer |
| 6 | L | Low-End Terminal of the Potentiometer |
| 7 | \overline{CS} | Chip Select. When set to a low state, the wiper position can be adjusted using U/\overline{D} and \overline{INC} . When in a high-state, activity on \overline{INC} and U/\overline{D} does not affect or change the wiper position. |
| 8 | V_{CC} | Power Supply Terminal |

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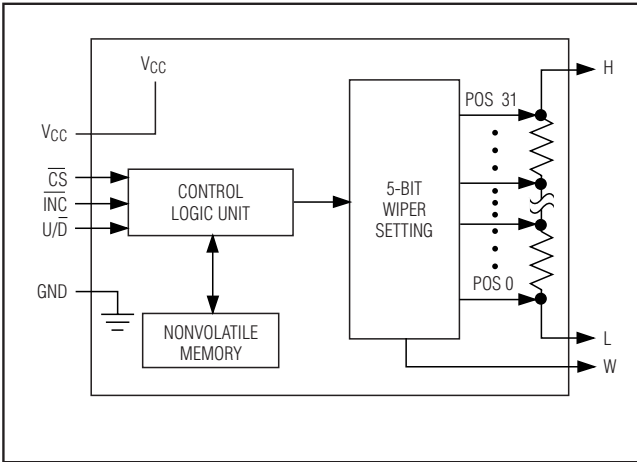


Figure 1. Block Diagram

Detailed Description

The DS4301 is a single nonvolatile digital potentiometer. This 32-position linear potentiometer has an end-to-end resistance of 200kΩ, and operates over a wide 2.4V to 5.5V supply voltage range. The wiper position is controlled by the three interface pins (U/D, CS, and INC), and the wiper setting can be stored in EEPROM on command.

Power-Up

On power-up, once a stable supply voltage of $V_{CC\ MIN}$ has been reached, the stored wiper setting is loaded from the EEPROM within t_{WLT} . Also on power-up, the DS4301 wiper control pins become active approximately t_{PU} after a stable supply voltage of $V_{CC\ MIN}$ has been reached.

Wiper Control

Adjusting the wiper of the DS4301 involves using the three control pins (U/D, CS, and INC). See the *Timing Diagram* in Figure 2. To enable wiper adjustment, a high-to-low transition on the CS pin is required. Hold CS low for the duration of the communication. Doing this enables the INC pin to change the wiper position. Set the U/D pin high to increment or low to decrement the wiper position. The state of the U/D pin should be set more than t_{D1} before the INC signal is transitioned from high to low. After the CS pin is active low, a high-to-low transition on the INC pin moves the wiper in the direction dictated by the U/D pin. Continue to pulse INC (high to low) until the desired wiper position is reached. On the last edge, hold the INC line low. With the desired wiper position set, there are two ways to proceed. One method terminates communication without allowing the value of the current wiper position to be written to the EEPROM. This is done by transitioning the CS signal to the high state before bringing the INC signal high. As long as the state of the CS pin is high before the state of the INC pin goes high, the current wiper setting is not written to EEPROM. Because the current wiper setting was not stored to the NV memory, the previously stored wiper setting, not the current wiper setting, is loaded from memory if power is cycled to the device

The other method is used to store a new wiper setting in the EEPROM. This is done by bringing the state of the INC pin high for a time of t_{IC} before bringing the state of the CS pin high. Once the states of both CS and INC pins are high, the current wiper setting is stored in EEPROM after a time of t_{WST} . If power is

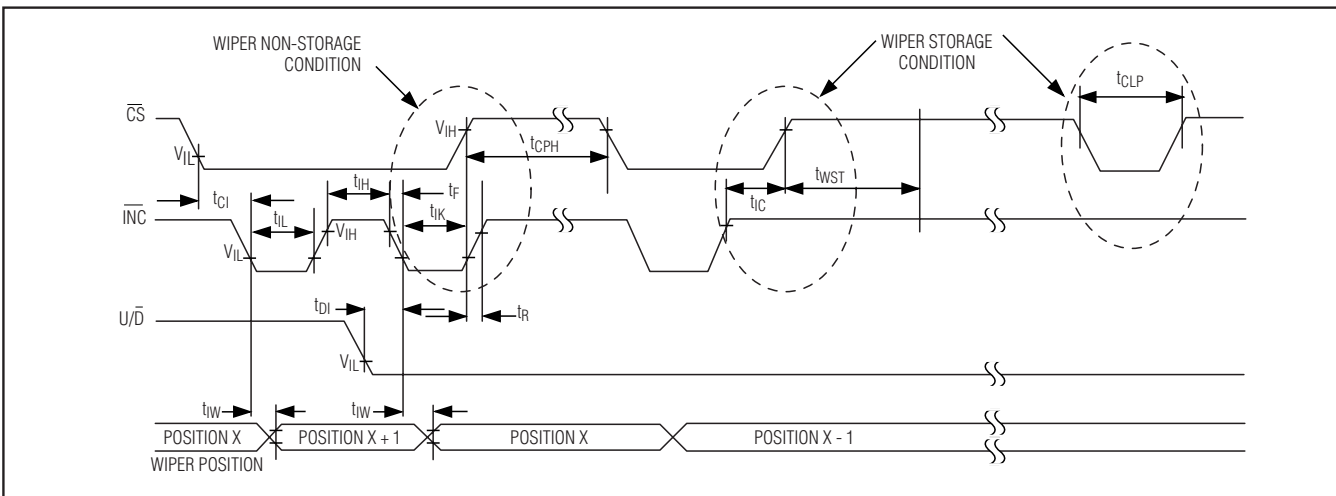


Figure 2. Timing Diagram

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cycled to the device, the wiper setting that was just stored is the setting loaded on power-up.

Wiper storage does not have to occur immediately after a change in wiper position. At anytime the current wiper position can be stored to the EEPROM by simply issuing a low pulse to the \overline{CS} pin for t_{CLP} while the \overline{INC} pin remains in a high state. The wiper does not move during this action and the current wiper setting is stored in EEPROM after t_{WST} .

For applications that require a specific wiper setting to be loaded on power-up and never changed, write the desired wiper setting to the EEPROM, then tie \overline{CS} to V_{CC} . Every time power is cycled to the DS4301, the desired wiper setting is loaded from EEPROM, and since \overline{CS} is tied to V_{CC} , no changes can be made to the wiper setting.

EEPROM Characteristics

There is a limit to the number of times the EEPROM can be written to before a wear-out occurs (see the *Nonvolatile Memory Characteristics* table). After EEPROM wear-out occurs, the wiper can still be adjusted, however accurately storing the wiper position is no longer possible. When power is removed from the part, the current wiper position is lost. Upon power-up, the wiper setting stored in EEPROM is loaded within t_{WLT} of V_{CC} reaching a stable voltage level greater than or equal to $V_{CC\ MIN}$. If EEPROM wear-out has occurred, the wiper setting that is loaded is unknown.

Application Information

To achieve the best results when using the DS4301, decouple the power supply with a $0.01\mu F$ or $0.1\mu F$ capacitor. Use a high-quality ceramic surface-mount capacitor when possible. Surface-mount components minimize lead inductance, improving performance. Ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

Chip Information

TRANSISTOR COUNT: 3512

SUBSTRATE INFO: P-substrate

Package Information

For the latest package outline information, go to www.maxim-ic.com/DallasPackInfo.

DS4301

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