

# Multiple Channel DC-DC Power Management IC

The 34704 is a multi-channel Power Management IC (PMIC) used to address power management needs for various multimedia application microprocessors. Its ability to provide either 5 or 8 independent output voltages with a single input power supply (2.7 and 5.5 V) together with its high efficiency, make it ideal for portable devices powered up by Li-Ion/polymer batteries or for USB powered devices as well. This device is powered by SMARTMOS technology.

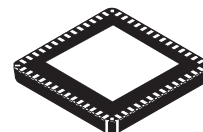
The 34704 is housed in a 7x7 mm, Pb-free, QFN56 and is capable of operating at a switching frequency of up to 2.0 MHz. This makes it possible to reduce external component size and to implement full space efficient power management solutions.

## Features

- 8 DC/DC (34704A) or 5 DC/DC (34704B) switching regulators with up to  $\pm 2\%$  output voltage accuracy
- Dynamic voltage scaling on all regulators.
- Selectable output voltage or current regulation on REG8
- I<sup>2</sup>C programmability
- Output undervoltage and overvoltage detection for each regulator
- Overcurrent limit detection and short-circuit protection for each regulator
- Thermal limit detection for each regulator, except REG7
- Integrated compensation for REG1, REG3, REG6, and REG8
- 5.0  $\mu$ A maximum shutdown current (All regulators are off, 5.5 V VIN)
- True cutoff on all of the boost and buck-boost regulators

**34704**

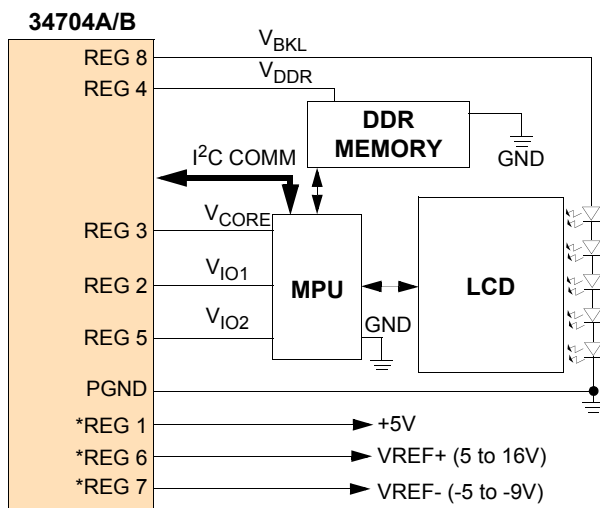
**MULTI-CHANNEL IC**



**EP SUFFIX (PB-FREE)**  
**98ASA00712D**  
**56-PIN QFN**

## ORDERING INFORMATION

| Device        | Temperature Range (T <sub>A</sub> ) | Package   |
|---------------|-------------------------------------|-----------|
| MC34704AEP/R2 | -20 °C to 85 °C                     | 56 QFN EP |
| MC34704BEP/R2 |                                     |           |



\* Available only in 34704A device

**Figure 1. 34704 Simplified Application Diagram**



DEVICE VARIATIONS

Table 1. Device Variations

| Orderable Part Number | No. of Regulators | Regulator Number  |
|-----------------------|-------------------|-------------------|
| MC34704AEP/R2         | 8                 | Reg 1 - 8         |
| MC34704BEP/R2         | 5                 | Reg 2, 3, 4, 5, 8 |

# INTERNAL BLOCK DIAGRAM

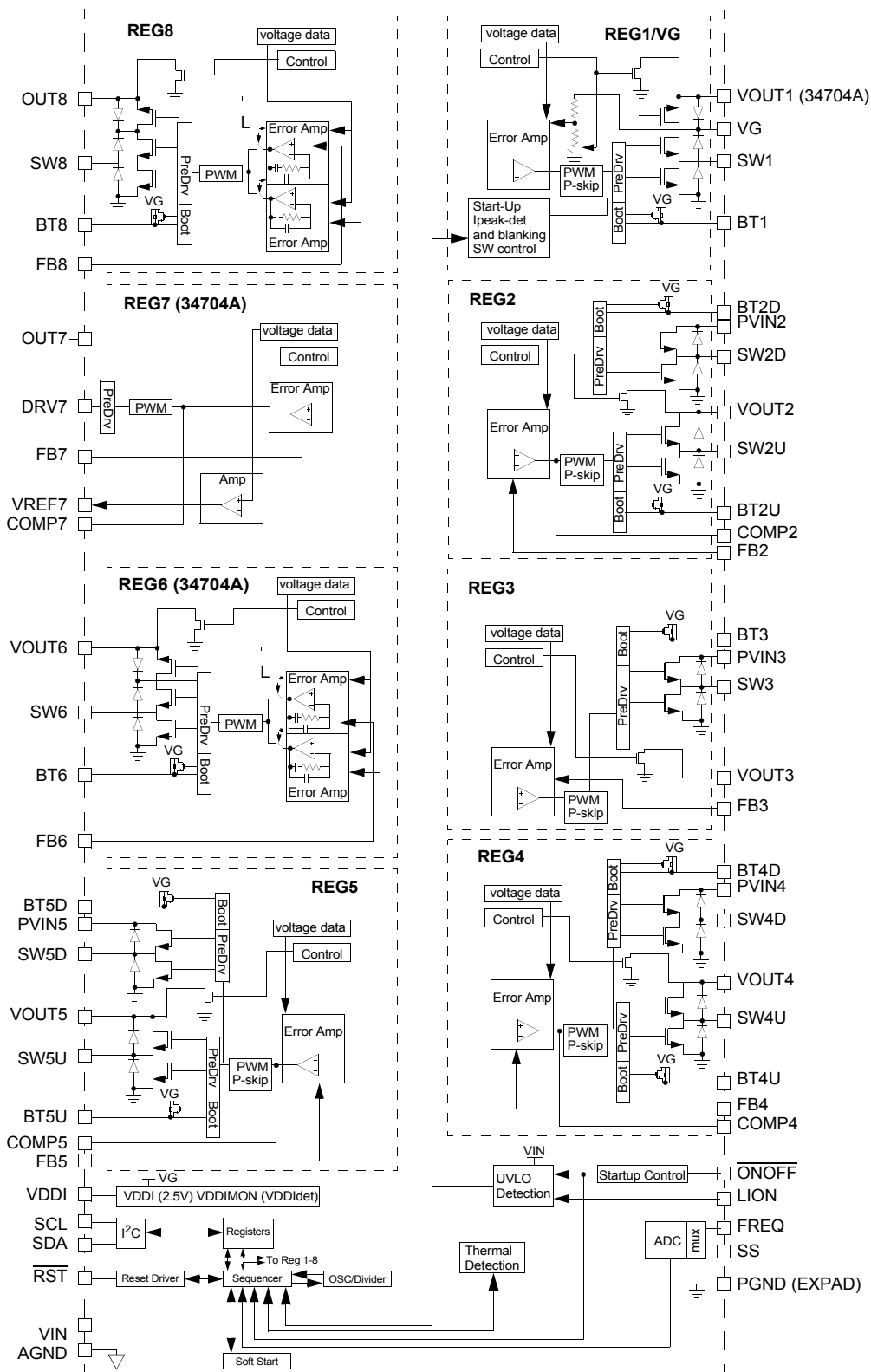
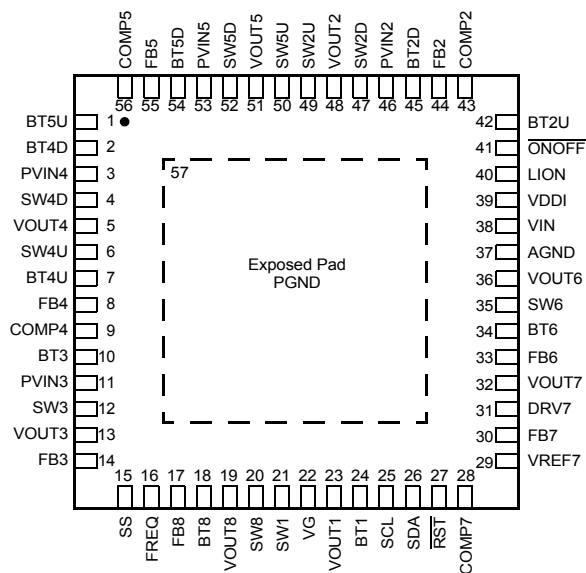
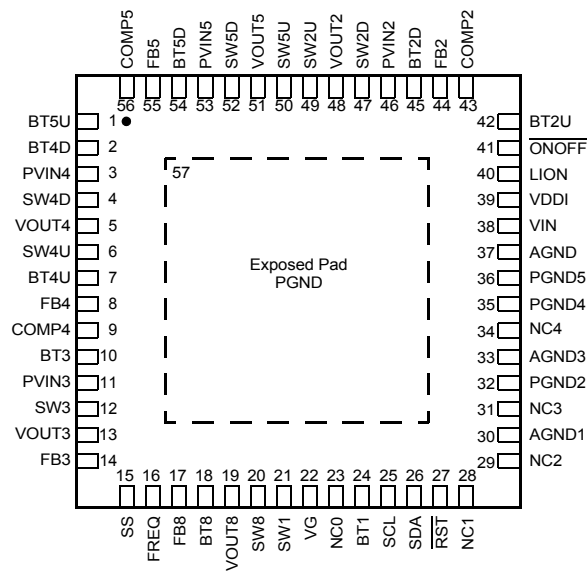


Figure 2. 34704 Internal Block Diagram

## PIN CONNECTIONS


**34704A**

**34704B**
**Figure 3. 34704 Pin Connections**
**Table 2. 34704 Pin Definitions**

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 17](#).

| Pin Number | Device | Pin Name | Pin Function | Formal Name                                                    | Definition                                                                                                                                                                                  |
|------------|--------|----------|--------------|----------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1          | A/B    | BT5U     | Passive      | REG5 Boost Stage bootstrap capacitor input pin                 | Connect a 1.0 $\mu$ F capacitor between this pin and SW5U pin to enhance the gate of the Switch Power MOSFET.                                                                               |
| 2          | A/B    | BT4D     | Passive      | REG4 Buck Stage bootstrap capacitor input pin                  | Connect a 0.01 $\mu$ F capacitor between this pin and SW4D pin to enhance the gate of the Switch Power MOSFET.                                                                              |
| 3          | A/B    | PVIN4    | Power        | REG4 power supply input voltage                                | This is the connection to the drain of the high-side switch FET. Input decoupling /filtering is required for proper REG4 operation. Use a 10uF decoupling capacitor for better performance. |
| 4          | A/B    | SW4D     | Input/Output | REG4 Buck Stage switching node                                 | The inductor is connected between this pin and the SW4U pin.                                                                                                                                |
| 5          | A/B    | VOUT4    | Output       | REG4 regulated output voltage pin                              | Connect this pin to the load and to the output filter as close to the pin as possible.                                                                                                      |
| 6          | A/B    | SW4U     | Input/Output | REG4 Boost Stage switching node                                | The inductor is connected between this pin and the SW4D pin.                                                                                                                                |
| 7          | A/B    | BT4U     | Passive      | REG4 Boost Stage bootstrap capacitor input pin                 | Connect a 0.01 $\mu$ F capacitor between this pin and SW4U pin to enhance the gate of the Switch Power MOSFET.                                                                              |
| 8          | A/B    | FB4      | Input        | REG4 voltage feedback input for voltage regulation/programming | Connect the feedback resistor divider to this pin.                                                                                                                                          |
| 9          | A/B    | COMP4    | Passive      | REG4 compensation network connection                           | REG4 compensation network connection.                                                                                                                                                       |
| 10         | A/B    | BT3      | Passive      | REG3 bootstrap capacitor input pin                             | Connect a 0.01 $\mu$ F capacitor between this pin and SW3 pin to enhance the gate of the Switch Power MOSFET.                                                                               |

**Table 2. 34704 Pin Definitions (continued)**

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 17](#).

| Pin Number        | Device | Pin Name                | Pin Function | Formal Name                                                    | Definition                                                                                                                                                                                  |
|-------------------|--------|-------------------------|--------------|----------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11                | A/B    | PVIN3                   | Power        | REG3 power supply input voltage                                | This is the connection to the drain of the high-side switch FET. Input decoupling /filtering is required for proper REG3 operation. Use a 10uf decoupling capacitor for better performance. |
| 12                | A/B    | SW3                     | Output       | REG3 switching node                                            | The inductor is connected between this pin and the regulated REG3 output.                                                                                                                   |
| 13                | A/B    | VOUT3                   | Output       | REG3 output voltage return pin                                 | This is the discharge path of REG3 output voltage.                                                                                                                                          |
| 14                | A/B    | FB3                     | Input        | REG3 voltage feedback input for voltage regulation/programming | Connect the feedback resistor divider to this pin.                                                                                                                                          |
| 15                | A/B    | SS                      | Input        | Soft start time                                                | The soft start time for all regulators can be adjusted by connecting this pin to an external resistor divider between VDDI and AGND pins.                                                   |
| 16                | A/B    | FREQ                    | Input        | Oscillator frequency                                           | The oscillator frequency can be adjusted by connecting this pin to an external resistor divider between VDDI and AGND pins. This pin sets $F_{SW1}$ value.                                  |
| 17                | A/B    | FB8                     | Input        | REG8 voltage feedback input for voltage regulation/programming | Connect the feedback resistor divider to this pin.                                                                                                                                          |
| 18                | A/B    | BT8                     | Passive      | REG8 bootstrap capacitor input pin                             | Connect a 0.01 $\mu$ F capacitor between this pin and SW8 pin to enhance the gate of the Synchronous Power MOSFET.                                                                          |
| 19                | A/B    | VOUT8                   | Output       | REG8 regulated output voltage pin                              | Connect this pin directly to the load directly and to the output filter as close to the pin as possible.                                                                                    |
| 20                | A/B    | SW8                     | Output       | REG8 switching node                                            | The inductor is connected between this pin and the VIN pin.                                                                                                                                 |
| 21                | A/B    | SW1                     | Output       | REG1 switching node                                            | The inductor is connected between this pin and the VIN Pin.                                                                                                                                 |
| 22                | A/B    | VG                      | Passive      | REG1 regulated output voltage before the cutoff switch         | REG1 regulated output voltage before the cut-off switch. This supplies the internal circuits and the gate drive                                                                             |
| 23 <sup>(1)</sup> | A      | VOUT1                   | Output       | REG1 regulated output voltage pin.                             | Connect this pin directly to the load directly and to the output filter as close to the pin as possible.                                                                                    |
|                   | B      | NC0                     | No Connect   | -                                                              | Pin 23 is not connected.                                                                                                                                                                    |
| 24                | A/B    | BT1                     | Passive      | REG1 bootstrap capacitor input pin                             | Connect a 1.0 $\mu$ F capacitor between this pin and SW1 pin to enhance the gate of the Switch Power MOSFET.                                                                                |
| 25                | A/B    | SCL                     | Input/Output | I <sup>2</sup> C serial interface clock input                  | I <sup>2</sup> C serial interface clock input.                                                                                                                                              |
| 26                | A/B    | SDA                     | Input/Output | I <sup>2</sup> C serial interface data input                   | I <sup>2</sup> C serial interface data input.                                                                                                                                               |
| 27                | A/B    | $\overline{\text{RST}}$ | Open Drain   | Power reset output signal (Microprocessor Reset)               | This is an open drain output and must be pulled up by an external resistor to a supply voltage like $V_{IN}$ .                                                                              |
| 28                | A      | COMP7                   | Passive      | REG7 compensation network connection                           | REG7 compensation network connection.                                                                                                                                                       |
|                   | B      | NC1                     | No Connect   | -                                                              | Pin 28 is not connected                                                                                                                                                                     |
| 29                | A      | VREF7                   | Output       | REG7 resistor feedback network reference voltage               | Connect this pin to the bottom of the feedback resistor divider.                                                                                                                            |
|                   | B      | NC2                     | No Connect   | -                                                              | Pin 29 is not connected                                                                                                                                                                     |

**Table 2. 34704 Pin Definitions (continued)**

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 17](#).

| Pin Number | Device | Pin Name | Pin Function | Formal Name                                                    | Definition                                                                                                                                                                                 |
|------------|--------|----------|--------------|----------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 30         | A      | FB7      | Input        | REG7 voltage feedback input for voltage regulation/programming | Connect the feedback resistor divider to this pin.                                                                                                                                         |
|            | B      | AGND1    | -            | -                                                              | Pin 30 is connected to AGND                                                                                                                                                                |
| 31         | A      | DRV7     | Output       | REG7 external Power MOSFET gate drive                          | REG7 external Power MOSFET gate drive.                                                                                                                                                     |
|            | B      | NC3      | No Connect   | -                                                              | Pin 31 is not connected                                                                                                                                                                    |
| 32         | A      | VOUT7    | Output       | REG7 output voltage return pin.                                | This is the discharge path of REG7 output voltage.                                                                                                                                         |
|            | B      | PGND1    | -            | -                                                              | Pin 32 is connected to PGND                                                                                                                                                                |
| 33         | A      | FB6      | Input        | REG6 voltage feedback input for voltage regulation/programming | Connect the feedback resistor divider to this pin.                                                                                                                                         |
|            | B      | AGND2    | -            | -                                                              | Pin 33 is connected to AGND                                                                                                                                                                |
| 34         | A      | BT6      | Passive      | REG6 bootstrap capacitor input pin.                            | Connect a 0.01 $\mu$ F capacitor between this pin and SW6 pin to enhance the gate of the Synchronous Power MOSFET.                                                                         |
|            | B      | NC4      | No Connect   | -                                                              | Pin 34 is not connected                                                                                                                                                                    |
| 35         | A      | SW6      | Output       | REG6 switching node                                            | The inductor is connected between this pin and the VIN pin.                                                                                                                                |
|            | B      | PGND2    | -            | -                                                              | Pin 35 is connected to PGND                                                                                                                                                                |
| 36         | A      | VOUT6    | Output       | REG6 regulated output voltage pin                              | Connect this pin directly to the load directly and to the output filter as close to the pin as possible.                                                                                   |
|            | B      | PGND3    | -            | -                                                              | Pin 36 is connected to PGND                                                                                                                                                                |
| 37         | A/B    | AGND     | Ground       | Analog ground of the IC                                        | Analog ground of the IC.                                                                                                                                                                   |
| 38         | A/B    | VIN      | Power        | Battery voltage connection                                     | Input decoupling /filtering is required for the device to operate properly.                                                                                                                |
| 39         | A/B    | VDDI     | Output       | Internal supply voltage                                        | Connect a 1.0 $\mu$ F low ESR decoupling filter capacitor between this pin and GND.                                                                                                        |
| 40         | A/B    | LION     | Input        | Battery Detection                                              | Always pull this pin High with a 470kohm Resistor to indicate Input power is present.                                                                                                      |
| 41         | A/B    | ONOFF    | Input        | Dual function IC turn On/ Off                                  | This is a hardware enable/disable for the 34704A/B. It can be connected to a mechanical switch to turn the power On or Off.                                                                |
| 42         | A/B    | BT2U     | Passive      | REG2 Boost Stage bootstrap capacitor input pin                 | Connect a 1.0 $\mu$ F capacitor between this pin and SW2U pin to enhance the gate of the Switch Power MOSFET.                                                                              |
| 43         | A/B    | COMP2    | Passive      | REG2 compensation network connection                           | REG2 compensation network connection.                                                                                                                                                      |
| 44         | A/B    | FB2      | Input        | REG2 voltage feedback input for voltage regulation/programming | Connect the feedback resistor divider to this pin.                                                                                                                                         |
| 45         | A/B    | BT2D     | Passive      | REG2 Buck Stage bootstrap capacitor input pin                  | Connect a 1.0 $\mu$ F capacitor between this pin and SW2D pin to enhance the gate of the Switch Power MOSFET.                                                                              |
| 46         | A/B    | PVIN2    | Power        | REG2 power supply input voltage                                | This is the connection to the drain of the high-side switch FET. Input decoupling /filtering is required for proper REG2 operation. Use a 10uf decoupling capacitor for better performance |

**Table 2. 34704 Pin Definitions (continued)**

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 17](#).

| Pin Number  | Device | Pin Name | Pin Function | Formal Name                                                    | Definition                                                                                                                                                                                 |
|-------------|--------|----------|--------------|----------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 47          | A/B    | SW2D     | Input/Output | REG2 Buck Stage switching node                                 | The inductor is connected between this pin and the SW2U pin.                                                                                                                               |
| 48          | A/B    | VOUT2    | Output       | REG2 regulated output voltage pin                              | Connect this pin to the load and to the output filter as close to the pin as possible.                                                                                                     |
| 49          | A/B    | SW2U     | Input/Output | REG2 Boost Stage switching node                                | The inductor is connected between this pin and the SW2D pin.                                                                                                                               |
| 50          | A/B    | SW5U     | Input/Output | REG5 Boost Stage switching node                                | The inductor is connected between this pin and the SW5D pin.                                                                                                                               |
| 51          | A/B    | VOUT5    | Output       | REG5 regulated output voltage pin                              | Connect this pin to the load and to the output filter as close to the pin as possible.                                                                                                     |
| 52          | A/B    | SW5D     | Input/Output | REG5 Buck Stage switching node                                 | The inductor is connected between this pin and the SW5U pin.                                                                                                                               |
| 53          | A/B    | PVIN5    | Power        | REG5 power supply input voltage                                | This is the connection to the drain of the high-side switch FET. Input decoupling /filtering is required for proper REG5 operation. Use a 10uf decoupling capacitor for better performance |
| 54          | A/B    | BT5D     | Passive      | REG5 Buck Stage bootstrap capacitor input pin                  | Connect a 1.0 $\mu$ F capacitor between this pin and SW5D pin to enhance the gate of the Switch Power MOSFET.                                                                              |
| 55          | A/B    | FB5      | Input        | REG5 voltage feedback input for voltage regulation/programming | Connect the feedback resistor divider to this pin.                                                                                                                                         |
| 56          | A/B    | COMP5    | Passive      | REG5 compensation network connection                           | REG5 compensation network connection.                                                                                                                                                      |
| Exposed Pad | A/B    | PGND     | Ground       | Power Ground Connection for all of the regulators except REG7  | Power Ground Connection for all of the regulators except REG7. This pad is provided to enhance thermal performance.                                                                        |

**Notes**

1. If regulator 1 is not used, leave pin 23 Unconnected, All other components should be used to provide VG to the system
2. If regulators 5, 6, 7 and 8 are not used, connect the corresponding pins as follows: FB, SW and VOUT nodes: tied to GND; BT, COMP and PVIN pins: Not connected; DRV and VREF nodes (REG7 only): Not connected
3. REG 2,3 and 4 should always be populated.

## ELECTRICAL CHARACTERISTICS

### MAXIMUM RATINGS

**Table 3. Maximum Ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Ratings                                                                                                                                                                                                          | Symbol                                 | Value                                     | Unit |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|-------------------------------------------|------|
| <b>ELECTRICAL RATINGS</b>                                                                                                                                                                                        |                                        |                                           |      |
| Battery Input Supply Voltage (VIN) Pin<br>PVINx, $\overline{RST}$ , $\overline{ONOFF}$ , LION, DRV7 <sup>(8)</sup> , VG, SCL, SDA and VOUT1-5 Pins<br>VDDI, COMPx, FBx, VREF7 <sup>(8)</sup> , FREQ, and SS Pins | V <sub>IN</sub>                        | -0.3 to 6.0<br>-0.3 to 6.0<br>-0.3 to 3.0 | V    |
| SW1-5 Pins                                                                                                                                                                                                       | V <sub>SW-LOW</sub>                    | -1.0 to 6.0                               | V    |
| SW8, SW6 <sup>(8)</sup> Pins                                                                                                                                                                                     | V <sub>SW-HIGH</sub>                   | -1.0 to 27                                | V    |
| BTx Pins (Referenced to switch node)                                                                                                                                                                             | V <sub>BT</sub> -V <sub>SW</sub>       | -0.3 to 6.0                               | V    |
| BTx Pins to GND                                                                                                                                                                                                  | V <sub>BT</sub>                        | -0.3 to 27                                | V    |
| VOUT8, VOUT6 <sup>(8)</sup> Pins                                                                                                                                                                                 | V <sub>OUT-HIGH</sub>                  | -0.3 to 27                                | V    |
| VOUT7 Pin <sup>(8)</sup>                                                                                                                                                                                         | V <sub>OUT-NEG</sub>                   | -10.0 to 0.3                              | V    |
| Continuous Output Current<br>REG1 <sup>(8)</sup><br>REG2,5<br>REG3<br>REG4<br>REG6,7 <sup>(8)</sup><br>REG8                                                                                                      |                                        | 500<br>500<br>550<br>300<br>60<br>30      | mA   |
| ESD Voltage<br>Human Body Model<br>Charge Device Model                                                                                                                                                           | V <sub>ESD1</sub><br>V <sub>ESD2</sub> | ±1000<br>±500                             | V    |

### THERMAL RATINGS

|                                                   |                     |             |    |
|---------------------------------------------------|---------------------|-------------|----|
| Maximum Junction Temperature                      | T <sub>J(MAX)</sub> | +150        | °C |
| Storage Temperature                               | T <sub>STG</sub>    | -65 to +150 | °C |
| Maximum Power Dissipation (T <sub>A</sub> = 85°C) | PD                  | 2.5         | W  |

### THERMAL RESISTANCE<sup>(7)</sup>

|                                                                  |                                      |          |      |
|------------------------------------------------------------------|--------------------------------------|----------|------|
| Thermal Resistance<br>Junction to Ambient<br>Junction to Board   | R <sub>ΘJA</sub><br>R <sub>ΘJB</sub> | 26<br>10 | °C/W |
| Peak Package Reflow Temperature During Reflow <sup>(5),(6)</sup> | T <sub>PPRT</sub>                    | Note 6   | °C   |

#### Notes

- ESD testing is performed in accordance with the Human Body Model (HBM) (C<sub>ZAP</sub> = 100 pF, R<sub>ZAP</sub> = 1500 Ω), and the Charge Device Model (CDM), Robotic (C<sub>ZAP</sub> = 4.0 pF).
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescall's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to [www.freescale.com](http://www.freescale.com), search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxx enter 33xxx), and review parametrics.
- Thermal Resistance is based on a four-layer board (2s2p)
- Available only on the 34704A

## STATIC ELECTRICAL CHARACTERISTICS

**Table 4. Static Electrical Characteristics**

Characteristics noted under conditions  $2.7\text{ V} \leq V_{\text{IN}} \leq 5.5\text{ V}$ ,  $-20^\circ\text{C} \leq T_{\text{A}} \leq 85^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_{\text{A}} = 25^\circ\text{C}$  under nominal conditions, unless otherwise noted.

| Characteristic                                                                                                                                                                                                                      | Symbol                         | Min         | Typ           | Max         | Unit             |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|-------------|---------------|-------------|------------------|
| <b>POWER INPUT</b>                                                                                                                                                                                                                  |                                |             |               |             |                  |
| Input Supply Voltage Typical Range                                                                                                                                                                                                  | $V_{\text{IN}}$                | 2.7         | -             | 5.5         | V                |
| Input DC Supply Current <sup>(9)</sup><br>VIN Pin Only<br>All regulators are ON, no load; $V_{\text{IN}} = 3.6\text{ V}$ , FSW = 1.0 MHz<br>Regulators 1 - 5 On, Reg 6, 7 and 8 Off; $V_{\text{IN}} = 3.6\text{ V}$ , FSW = 1.0 MHz | $I_{\text{IN}}$                | -<br>-<br>- | -<br>86<br>32 | -<br>-<br>- | mA               |
| Input DC Shutdown Supply Current <sup>(9)</sup><br>(Shutdown, All regulators are OFF and $V_{\text{IN}} = 5.5\text{V}$ )<br>This includes any pin connected to the battery                                                          | $I_{\text{OFF}}$               | -           | -             | 5.0         | $\mu\text{A}$    |
| Rising UVLO Threshold                                                                                                                                                                                                               | $\text{UVLO}_{\text{R}}$       | -           | -             | 3.0         | V                |
| Falling UVLO Threshold                                                                                                                                                                                                              | $\text{UVLO}_{\text{F}}$       | -           | -             | 2.7         | V                |
| <b>RST</b>                                                                                                                                                                                                                          |                                |             |               |             |                  |
| RST Low Level Output Voltage<br>$I_{\text{OL}} = 1.0\text{ mA}$                                                                                                                                                                     | $V_{\text{RST-OL}}$            | -           | -             | 0.4         | V                |
| RST Leakage Current, Off-state @ $25^\circ\text{C}$                                                                                                                                                                                 | $I_{\text{RST-LKG}}$           | -           | -             | 1.0         | $\mu\text{A}$    |
| <b>Current Limit Monitoring</b>                                                                                                                                                                                                     |                                |             |               |             |                  |
| Over and Short-circuit Current Limit Accuracy                                                                                                                                                                                       | -                              | -20         | -             | 20          | %                |
| <b>REGULATOR 1 &amp; VG</b>                                                                                                                                                                                                         |                                |             |               |             |                  |
| VG Output Voltage                                                                                                                                                                                                                   | $V_{\text{VG}}$                | -           | 5.0           | -           | V                |
| REG1 Output Voltage <sup>(10)</sup>                                                                                                                                                                                                 | $V_{\text{OUT}}$               | -           | 5.0           | -           | V                |
| Output Accuracy                                                                                                                                                                                                                     | -                              | -4.0        | -             | 4.0         | %                |
| Line/Load Regulation <sup>(9)</sup>                                                                                                                                                                                                 | $\text{REG}_{\text{LN/LD}}$    | -1.0        | -             | 1.0         | %                |
| Dynamic Voltage Scaling Range                                                                                                                                                                                                       | $V_{\text{DYN}}$               | -10         | -             | 10          | %                |
| Dynamic Voltage Scaling Step Size                                                                                                                                                                                                   | $V_{\text{DYN\_STEP}}$         | -           | 2.5           | -           | %                |
| Continuous Output Current <sup>(9)</sup>                                                                                                                                                                                            | $I_{\text{OUT}}$               | -           | 100           | 500         | mA               |
| Overcurrent Limit (Detected in Low-side FET)                                                                                                                                                                                        | $I_{\text{LIM\_ION}}$          | -           | 2.7           | -           | A                |
| Short-circuit Current Limit (Detected in the Blocking FET)                                                                                                                                                                          | $I_{\text{SHORT\_ION}}$        | -           | 4.0           | -           | A                |
| Overcurrent Limit Accuracy                                                                                                                                                                                                          | -                              | -20         | -             | 20          | %                |
| N-CH Switch Power MOSFET $R_{\text{DS(on)}}$                                                                                                                                                                                        | $R_{\text{DS(on)}\text{-SW}}$  | -           | 100           | -           | $\text{m}\Omega$ |
| N-CH Synch. Power MOSFET $R_{\text{DS(on)}}$                                                                                                                                                                                        | $R_{\text{DS(on)}\text{-SY}}$  | -           | 150           | -           | $\text{m}\Omega$ |
| N-CH Shutdown Power MOSFET $R_{\text{DS(on)}}$                                                                                                                                                                                      | $R_{\text{DS(on)}\text{-SH}}$  | -           | 100           | -           | $\text{m}\Omega$ |
| Discharge MOSFET $R_{\text{DS(on)}}$                                                                                                                                                                                                | $R_{\text{DS(on)}\text{-DIS}}$ | -           | 70            | -           | $\Omega$         |
| Thermal Shutdown Threshold <sup>(9)</sup>                                                                                                                                                                                           | $T_{\text{SD}}$                | -           | 170           | -           | $^\circ\text{C}$ |
| Thermal Shutdown Hysteresis <sup>(9)</sup>                                                                                                                                                                                          | $T_{\text{SD-HYS}}$            | -           | 25            | -           | $^\circ\text{C}$ |
| SW1 Leakage Current (Off State) @ $25^\circ\text{C}$                                                                                                                                                                                | $I_{\text{SW1\_LKG}}$          | -           | -             | 1.0         | $\mu\text{A}$    |
| Peak Current Detection Threshold at Power Up <sup>(9)</sup>                                                                                                                                                                         | $I_{\text{PEAK}}$              | -           | 300           | -           | mA               |

Notes:

9. Guaranteed by Design
10. Available only on the 34704A

**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $2.7\text{ V} \leq V_{\text{IN}} \leq 5.5\text{ V}$ ,  $-20^\circ\text{C} \leq T_{\text{A}} \leq 85^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_{\text{A}} = 25^\circ\text{C}$  under nominal conditions, unless otherwise noted.

| Characteristic                                               | Symbol                           | Min   | Typ                   | Max  | Unit             |
|--------------------------------------------------------------|----------------------------------|-------|-----------------------|------|------------------|
| <b>REGULATOR 2</b>                                           |                                  |       |                       |      |                  |
| Output Voltage Range                                         | $V_{\text{OUT}}$                 | 0.6   | 3.3                   | 3.6  | V                |
| Output Accuracy                                              | -                                | -2.0  | -                     | 2.0  | %                |
| Line/Load Regulation <sup>(11)</sup>                         | $\text{REG}_{\text{LN/LD}}$      | -1.0  | -                     | 1.0  | %                |
| Feedback Reference Voltage                                   | $V_{\text{FB}}$                  | -     | 0.600 <sup>(12)</sup> | -    | V                |
| Dynamic Voltage Scaling Range                                | $V_{\text{DYN}}$                 | -17.5 | -                     | 17.5 | %                |
| Dynamic Voltage Scaling Step Size                            | $V_{\text{DYN\_STEP}}$           | -     | 2.5                   | -    | %                |
| Continuous Output Current <sup>(11)</sup>                    | $I_{\text{OUT}}$                 | -     | 200                   | 500  | mA               |
| Overcurrent Limit (Detected in buck high-side FET)           | $I_{\text{LIM\_ION}}$            | -     | 1.4                   | -    | A                |
| Short-circuit Current Limit (Detected in buck high-side FET) | $I_{\text{SHORT\_ION}}$          | -     | 2.1                   | -    | A                |
| Battery Overcurrent Limit Accuracy                           | -                                | -20   | -                     | 20   | %                |
| N-CH Buck Switch Power MOSFET $R_{\text{DS(on)}}$            | $R_{\text{DS(on)}}^{\text{SW}}$  | -     | 120                   | -    | m $\Omega$       |
| N-CH Buck Synch. Power MOSFET $R_{\text{DS(on)}}$            | $R_{\text{DS(on)}}^{\text{SY}}$  | -     | 1000                  | -    | m $\Omega$       |
| N-CH Boost Switch Power MOSFET $R_{\text{DS(on)}}$           | $R_{\text{DS(on)}}^{\text{SW}}$  | -     | 120                   | -    | m $\Omega$       |
| N-CH Boost Synch. Power MOSFET $R_{\text{DS(on)}}$           | $R_{\text{DS(on)}}^{\text{SY}}$  | -     | 120                   | -    | m $\Omega$       |
| Discharge MOSFET $R_{\text{DS(on)}}$                         | $R_{\text{DS(on)}}^{\text{DIS}}$ | -     | 70                    | -    | $\Omega$         |
| Thermal Shutdown Threshold <sup>(11)</sup>                   | $T_{\text{SD}}$                  | -     | 170                   | -    | $^\circ\text{C}$ |
| Thermal Shutdown Hysteresis <sup>(11)</sup>                  | $T_{\text{SD-HYS}}$              | -     | 25                    | -    | $^\circ\text{C}$ |
| PVIN2 Leakage Current (Off State) @25 $^\circ\text{C}$       | $I_{\text{PVIN2G\_LKG}}$         | -     | -                     | 1.0  | $\mu\text{A}$    |
| SW2D Leakage Current (Off State) @25 $^\circ\text{C}$        | $I_{\text{SW2D\_LKG}}$           | -     | -                     | 1.0  | $\mu\text{A}$    |
| SW2U Leakage Current (Off State) @25 $^\circ\text{C}$        | $I_{\text{SW2U\_LKG}}$           | -     | -                     | 1.0  | $\mu\text{A}$    |

**REGULATOR 3**

|                                                              |                                  |       |                       |      |                  |
|--------------------------------------------------------------|----------------------------------|-------|-----------------------|------|------------------|
| Output Voltage Range                                         | $V_{\text{OUT}}$                 | 0.6   | 1.2                   | 1.8  | V                |
| Output Accuracy                                              | -                                | -4.0  | -                     | 4.0  | %                |
| Line/Load Regulation <sup>(11)</sup>                         | $\text{REG}_{\text{LN/LD}}$      | -1.0  | -                     | 1.0  | %                |
| Feedback Reference Voltage                                   | $V_{\text{FB}}$                  | -     | 0.600 <sup>(12)</sup> | -    | V                |
| Dynamic Voltage Scaling Range                                | $V_{\text{DYN}}$                 | -17.5 | -                     | 17.5 | %                |
| Dynamic Voltage Scaling Step Size                            | $V_{\text{DYN\_STEP}}$           | -     | 2.5                   | -    | %                |
| Continuous Output Current <sup>(11)</sup>                    | $I_{\text{OUT}}$                 | -     | 150                   | 550  | mA               |
| Overcurrent Limit (Detected in buck high-side FET)           | $I_{\text{LIM\_ION}}$            | -     | 1.0                   | -    | A                |
| Short-circuit Current Limit (Detected in buck high-side FET) | $I_{\text{SHORT\_ION}}$          | -     | 1.5                   | -    | A                |
| Overcurrent Limit Accuracy                                   | -                                | -20   | -                     | 20   | %                |
| N-CH Switch Power MOSFET $R_{\text{DS(on)}}$                 | $R_{\text{DS(on)}}^{\text{SW}}$  | -     | 500                   | -    | m $\Omega$       |
| N-CH Synch. Power MOSFET $R_{\text{DS(on)}}$                 | $R_{\text{DS(on)}}^{\text{SY}}$  | -     | 500                   | -    | m $\Omega$       |
| Discharge MOSFET $R_{\text{DS(on)}}$                         | $R_{\text{DS(on)}}^{\text{DIS}}$ | -     | 70                    | -    | $\Omega$         |
| Thermal Shutdown Threshold <sup>(11)</sup>                   | $T_{\text{SD}}$                  | -     | 170                   | -    | $^\circ\text{C}$ |
| Thermal Shutdown Hysteresis <sup>(11)</sup>                  | $T_{\text{SD-HYS}}$              | -     | 25                    | -    | $^\circ\text{C}$ |
| PVIN3 Leakage Current (Off State) @25 $^\circ\text{C}$       | $I_{\text{PVIN3\_LKG}}$          | -     | -                     | 1.0  | $\mu\text{A}$    |
| SW3 Leakage Current (Off State) @25 $^\circ\text{C}$         | $I_{\text{SW3\_LKG}}$            | -     | -                     | 1.0  | $\mu\text{A}$    |

Notes:

11. Guaranteed by Design
12.  $V_{\text{FB}}$  is 0.6V when the part is powered up and no DVS is changed. DVS is achieved by modifying  $V_{\text{FB}}$  reference.

**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $2.7\text{ V} \leq V_{\text{IN}} \leq 5.5\text{ V}$ ,  $-20^\circ\text{C} \leq T_{\text{A}} \leq 85^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_{\text{A}} = 25^\circ\text{C}$  under nominal conditions, unless otherwise noted.

| Characteristic                                               | Symbol                           | Min  | Typ                   | Max | Unit |
|--------------------------------------------------------------|----------------------------------|------|-----------------------|-----|------|
| <b>REGULATOR 4</b>                                           |                                  |      |                       |     |      |
| Output Voltage Range                                         | $V_{\text{OUT}}$                 | 0.6  | 1.8                   | 3.6 | V    |
| Output Accuracy                                              | -                                | -2.0 | -                     | 2.0 | %    |
| Line/Load Regulation <sup>(13)</sup>                         | $\text{REG}_{\text{LN/LD}}$      | -1.0 | -                     | 1.0 | %    |
| Feedback Reference Voltage                                   | $V_{\text{FB}}$                  | -    | 0.600 <sup>(14)</sup> | -   | V    |
| Dynamic Voltage Scaling Range                                | $V_{\text{DYN}}$                 | -10  | -                     | 10  | %    |
| Dynamic Voltage Scaling Step Size                            | $V_{\text{DYN\_STEP}}$           | -    | 1.0                   | -   | %    |
| Continuous Output Current <sup>(13)</sup>                    | $I_{\text{OUT}}$                 | -    | 100                   | 300 | mA   |
| Overcurrent Limit (Detected in buck high-side FET)           | $I_{\text{LIM\_ION}}$            | -    | 1.5                   | -   | A    |
| Short-circuit Current Limit (Detected in buck high-side FET) | $I_{\text{SHORT\_ION}}$          | -    | 2.25                  | -   | A    |
| Overcurrent Limit Accuracy                                   | -                                | -20  | -                     | 20  | %    |
| N-CH Buck Switch Power MOSFET $R_{\text{DS(on)}}$            | $R_{\text{DS(on)}}^{\text{SW}}$  | -    | 200                   | -   | mΩ   |
| N-CH Buck Synch. Power MOSFET $R_{\text{DS(on)}}$            | $R_{\text{DS(on)}}^{\text{SY}}$  | -    | 600                   | -   | mΩ   |
| N-CH Boost Switch Power MOSFET $R_{\text{DS(on)}}$           | $R_{\text{DS(on)}}^{\text{SW}}$  | -    | 200                   | -   | mΩ   |
| N-CH Boost Synch. Power MOSFET $R_{\text{DS(on)}}$           | $R_{\text{DS(on)}}^{\text{SY}}$  | -    | 600                   | -   | mΩ   |
| Discharge MOSFET $R_{\text{DS(on)}}$                         | $R_{\text{DS(on)}}^{\text{DIS}}$ | -    | 70                    | -   | Ω    |
| Thermal Shutdown Threshold <sup>(13)</sup>                   | $T_{\text{SD}}$                  | -    | 170                   | -   | °C   |
| Thermal Shutdown Hysteresis <sup>(13)</sup>                  | $T_{\text{SD-HYS}}$              | -    | 25                    | -   | °C   |
| PVIN4 Leakage Current (Off State) @25°C                      | $I_{\text{PVIN4\_LKG}}$          | -    | -                     | 1.0 | μA   |
| SW4D Leakage Current (Off State) @25°C                       | $I_{\text{SW4D\_LKG}}$           | -    | -                     | 1.0 | μA   |
| SW4U Leakage Current (Off State) @25°C                       | $I_{\text{SW4U\_LKG}}$           | -    | -                     | 1.0 | μA   |

**REGULATOR 5**

|                                                              |                                  |       |                       |      |    |
|--------------------------------------------------------------|----------------------------------|-------|-----------------------|------|----|
| Output Voltage Range                                         | $V_{\text{OUT}}$                 | 0.6   | 3.3                   | 3.6  | V  |
| Output Accuracy                                              | -                                | -2.0  | -                     | 2.0  | %  |
| Line/Load Regulation <sup>(13)</sup>                         | $\text{REG}_{\text{LN/LD}}$      | -1.0  | -                     | 1.0  | %  |
| Feedback Reference Voltage                                   | $V_{\text{FB}}$                  | -     | 0.600 <sup>(14)</sup> | -    | V  |
| Dynamic Voltage Scaling Range                                | $V_{\text{DYN}}$                 | -17.5 | -                     | 17.5 | %  |
| Dynamic Voltage Scaling Step Size                            | $V_{\text{DYN\_STEP}}$           | -     | 2.5                   | -    | %  |
| Continuous Output Current <sup>(13)</sup>                    | $I_{\text{OUT}}$                 | -     | 150                   | 500  | mA |
| Overcurrent Limit (Detected in buck high-side FET)           | $I_{\text{LIM\_ION}}$            | -     | 1.4                   | -    | A  |
| Short-circuit Current Limit (Detected in buck high-side FET) | $I_{\text{SHORT\_ION}}$          | -     | 2.1                   | -    | A  |
| Overcurrent Limit Accuracy                                   | -                                | -20   | -                     | 20   | %  |
| N-CH Buck Switch Power MOSFET $R_{\text{DS(on)}}$            | $R_{\text{DS(on)}}^{\text{SW}}$  | -     | 120                   | -    | mΩ |
| N-CH Buck Synch. Power MOSFET $R_{\text{DS(on)}}$            | $R_{\text{DS(on)}}^{\text{SY}}$  | -     | 1000                  | -    | mΩ |
| N-CH Boost Switch Power MOSFET $R_{\text{DS(on)}}$           | $R_{\text{DS(on)}}^{\text{SW}}$  | -     | 120                   | -    | mΩ |
| N-CH Boost Synch. Power MOSFET $R_{\text{DS(on)}}$           | $R_{\text{DS(on)}}^{\text{SY}}$  | -     | 120                   | -    | mΩ |
| Discharge MOSFET $R_{\text{DS(on)}}$                         | $R_{\text{DS(on)}}^{\text{DIS}}$ | -     | 70                    | -    | Ω  |
| Thermal Shutdown Threshold <sup>(13)</sup>                   | $T_{\text{SD}}$                  | -     | 170                   | -    | °C |
| Thermal Shutdown Hysteresis <sup>(13)</sup>                  | $T_{\text{SD-HYS}}$              | -     | 25                    | -    | °C |

Notes:

13. Guaranteed by Design

14.  $V_{\text{FB}}$  is 0.6V when the part is powered up and no DVS is changed. DVS is achieved by modifying  $V_{\text{FB}}$  reference.

**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ ,  $-20^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25^\circ\text{C}$  under nominal conditions, unless otherwise noted.

| Characteristic                          | Symbol                  | Min | Typ | Max | Unit          |
|-----------------------------------------|-------------------------|-----|-----|-----|---------------|
| PVIN5 Leakage Current (Off State) @25°C | $I_{\text{PVIN5\_LKG}}$ | -   | -   | 1.0 | $\mu\text{A}$ |
| SW5D Leakage Current (Off State) @25°C  | $I_{\text{SW5D\_LKG}}$  | -   | -   | 1.0 | $\mu\text{A}$ |
| SW5U Leakage Current (Off State) @25°C  | $I_{\text{SW5U\_LKG}}$  | -   | -   | 1.0 | $\mu\text{A}$ |

**REGULATOR 6<sup>(16)</sup>**

|                                                            |                             |      |                       |     |                  |
|------------------------------------------------------------|-----------------------------|------|-----------------------|-----|------------------|
| Output Voltage Range                                       | $V_{\text{OUT}}$            | 5.0  | 15                    | 15  | V                |
| Output Accuracy                                            | -                           | -4.0 | -                     | 4.0 | %                |
| Line/Load Regulation <sup>(15)</sup>                       | $\text{REG}_{\text{LN/LD}}$ | -1.0 | -                     | 1.0 | %                |
| Feedback Reference Voltage                                 | $V_{\text{FB}}$             | -    | 0.600 <sup>(17)</sup> | -   | V                |
| Dynamic Voltage Scaling Range                              | $V_{\text{DYN}}$            | -10  | -                     | 10  | %                |
| Dynamic Voltage Scaling Step Size                          | $V_{\text{DYN\_STEP}}$      | -    | 2.5                   | -   | %                |
| Continuous Output Current <sup>(15)</sup>                  | $I_{\text{OUT}}$            | -    | 50                    | 60  | mA               |
| Overcurrent Limit (Detected in low-side FET)               | $I_{\text{LIM\_ION}}$       | -    | 3.0                   | -   | A                |
| Short-circuit Current Limit (Detected in the Blocking FET) | $I_{\text{SHORT\_ION}}$     | -    | 4.5                   | -   | A                |
| Overcurrent Limit Accuracy                                 | -                           | -20  | -                     | 20  | %                |
| N-CH Switch Power MOSFET $R_{\text{DS(on)}}$               | $R_{\text{DS(on)}\_SW}$     | -    | 200                   | -   | $\text{m}\Omega$ |
| N-CH Synch. Power MOSFET $R_{\text{DS(on)}}$               | $R_{\text{DS(on)}\_SY}$     | -    | 600                   | -   | $\text{m}\Omega$ |
| N-CH Shutdown Power MOSFET $R_{\text{DS(on)}}$             | $R_{\text{DS(on)}\_SH}$     | -    | 200                   | -   | $\text{m}\Omega$ |
| Discharge MOSFET $R_{\text{DS(on)}}$                       | $R_{\text{DS(on)}\_DIS}$    | -    | 70                    | -   | $\Omega$         |
| Thermal Shutdown Threshold <sup>(15)</sup>                 | $T_{\text{SD}}$             | -    | 170                   | -   | $^\circ\text{C}$ |
| Thermal Shutdown Hysteresis <sup>(15)</sup>                | $T_{\text{SD-HYS}}$         | -    | 25                    | -   | $^\circ\text{C}$ |
| SW6 Leakage Current (Off State) @25°C                      | $I_{\text{SW6\_LKG}}$       | -    | -                     | 1.0 | $\mu\text{A}$    |

**REGULATOR 7<sup>(16)</sup>**

|                                                                        |                               |      |                       |      |          |
|------------------------------------------------------------------------|-------------------------------|------|-----------------------|------|----------|
| Output Voltage Range                                                   | $V_{\text{OUT}}$              | -5.0 | -7.0                  | -9.0 | V        |
| Output Accuracy                                                        | -                             | -2.0 | -                     | 2.0  | %        |
| Line/Load Regulation <sup>(15)</sup>                                   | $\text{REG}_{\text{LN/LD}}$   | -1.0 | -                     | 1.0  | %        |
| Feedback Reference Voltage                                             | $V_{\text{FB}}$               | -    | 0.600 <sup>(17)</sup> | -    | V        |
| Continuous Output Current <sup>(15)</sup>                              | $I_{\text{OUT}}$              | -    | 50                    | 60   | mA       |
| Discharge MOSFET $R_{\text{DS(on)}}$                                   | $R_{\text{DS(on)}\_DIS}$      | -    | 55                    | -    | $\Omega$ |
| Gate Drive Voltage High Level (@ -50 mA, $V_{\text{IN}}=3.6\text{V}$ ) | $V_{\text{IN}}-V_{\text{OH}}$ | -    | 0.8                   | 1.4  | V        |
| Gate Drive Voltage Low Level (@ 50 mA, $V_{\text{IN}}=3.6\text{V}$ )   | $V_{\text{OL}}$               | -    | 1.1                   | 1.8  | V        |
| VREF7 Output Voltage                                                   | $V_{\text{REF7}}$             | -    | 1.5                   | -    | V        |
| VREF7 Voltage Accuracy                                                 | -                             | 1.43 | -                     | 1.57 | V        |
| VREF7 Output Load Regulation (10 $\mu\text{A}$ to 1.0 mA)              | $\text{REG}_{\text{LD}}$      | 1.43 | -                     | 1.57 | V        |

**Notes**

15. Guaranteed by Design
16. Available only on the 34704A
17.  $V_{\text{FB}}$  is 0.6V when the part is powered up and no DVS is changed. DVS is achieved by modifying  $V_{\text{FB}}$  reference.

**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ ,  $-20^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25^{\circ}\text{C}$  under nominal conditions, unless otherwise noted.

| Characteristic                                             | Symbol               | Min                 | Typ                   | Max | Unit               |
|------------------------------------------------------------|----------------------|---------------------|-----------------------|-----|--------------------|
| <b>REGULATOR 8</b>                                         |                      |                     |                       |     |                    |
| Output Voltage Range                                       | $V_{OUT}$            | 5.0 <sup>(19)</sup> | 15                    | 15  | V                  |
| Output Accuracy                                            | -                    | -4.0                | -                     | 4.0 | %                  |
| Feedback Reference Voltage                                 | $V_{FB}$             | -                   | 0.600 <sup>(20)</sup> | -   | V                  |
| Feedback Reference Voltage on current regulation mode      | $V_{FB}$             | -                   | 0.230 <sup>(21)</sup> | -   | V                  |
| Dynamic Voltage Scaling Range                              | $V_{DYN}$            | -10                 | -                     | 10  | %                  |
| Dynamic Voltage Scaling Step Size                          | $V_{DYN\_STEP}$      | -                   | 2.5                   | -   | %                  |
| Line/Load Regulation <sup>(18)</sup>                       | $REG_{LN/LD}$        | -1.0                | -                     | 1.0 | %                  |
| Continuous Output Current <sup>(18)</sup>                  | $I_{OUT}$            | -                   | 15                    | 30  | mA                 |
| Overcurrent Limit (Detected in low-side FET)               | $I_{LIM\_ION}$       | -                   | 1.0                   | -   | A                  |
| Short-circuit Current Limit (Detected in the Blocking FET) | $I_{SHORT\_ION}$     | -                   | 1.5                   | -   | A                  |
| Overcurrent Limit Accuracy                                 | -                    | -20                 | -                     | 20  | %                  |
| N-CH Switch Power MOSFET $R_{DS(on)}$                      | $R_{DS(on)\sim SW}$  | -                   | 450                   | -   | m $\Omega$         |
| N-CH Synch. Power MOSFET $R_{DS(on)}$                      | $R_{DS(on)\sim SY}$  | -                   | 1000                  | -   | m $\Omega$         |
| N-CH Shutdown Power MOSFET $R_{DS(on)}$                    | $R_{DS(on)\sim SH}$  | -                   | 450                   | -   | m $\Omega$         |
| Discharge MOSFET $R_{DS(ON)}$                              | $R_{DS(on)\sim DIS}$ | -                   | 70                    | -   | $\Omega$           |
| Thermal Shutdown Threshold <sup>(18)</sup>                 | $T_{SD}$             | -                   | 170                   | -   | $^{\circ}\text{C}$ |
| Thermal Shutdown Hysteresis <sup>(18)</sup>                | $T_{SD-HYS}$         | -                   | 25                    | -   | $^{\circ}\text{C}$ |
| SW8 Leakage Current (Off State) @25 $^{\circ}\text{C}$     | $I_{SW8\_LKG}$       | -                   | -                     | 1.0 | $\mu\text{A}$      |

**Notes**

18. Guaranteed by Design
19. When Battery voltage is higher than 5.0V and  $V_{OUT8}$  is 5.0V, a polarization diode is necessary to achieve accurate output voltage. [See Component Calculation on page 39](#) for further details.
20.  $V_{FB}$  is 0.6V when the part is powered up and no DVS is changed. DVS is achieved by modifying  $V_{FB}$  reference.
21. When in Current regulation mode, the Voltage reference is set to 0.230mV to set the maximum current, and it is internally decreased to achieve a factor of the maximum current passing through the LED string

## DYNAMIC ELECTRICAL CHARACTERISTICS

**Table 5. Dynamic Electrical Characteristics**

Characteristics noted under conditions  $2.7\text{ V} \leq V_{\text{IN}} \leq 5.5\text{ V}$ ,  $-20^\circ\text{C} \leq T_{\text{A}} \leq 85^\circ\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_{\text{A}} = 25^\circ\text{C}$  under nominal conditions, unless otherwise noted.

| Characteristic                                    | Symbol                 | Min | Typ  | Max  | Unit          |
|---------------------------------------------------|------------------------|-----|------|------|---------------|
| <b>I<sup>2</sup>C COMMUNICATION</b>               |                        |     |      |      |               |
| Device Physical Address (7 bit Address)           |                        | -   | \$54 | -    |               |
| Maximum I <sup>2</sup> C Speed                    |                        | -   | -    | 400  | kHz           |
| <b>FREQ</b>                                       |                        |     |      |      |               |
| Selectable Switching Frequency 1                  | $f_{\text{SW1}}$       | 750 | -    | 2000 | kHz           |
| Selectable Switching Frequency 2                  | $f_{\text{SW2}}$       | 250 | -    | 1000 | kHz           |
| Selectable Switching Frequency Step Size          | $f_{\text{STEP}}$      | -   | 250  | -    | kHz           |
| Switching Frequency Accuracy                      |                        | -10 | -    | 10   | %             |
| Retry Timeout Period <sup>(23)</sup>              | $t_{\text{TIMEOUT}}$   | -   | 10   | -    | ms            |
| <b>CURRENT LIMIT MONITORING</b>                   |                        |     |      |      |               |
| Overcurrent Limit Timer <sup>(23)</sup>           | $t_{\text{LIMIT}}$     | -   | 10   | -    | ms            |
| Retry Timeout Period <sup>(23)</sup>              | $t_{\text{RETRY}}$     | -   | 10   | -    | ms            |
| <b>OUTPUT OVERVOLTAGE/UNDERVOLTAGE MONITORING</b> |                        |     |      |      |               |
| Undervoltage Threshold (Response A)               | $V_{\text{UV-R}}$      | -   | -20  | -    | %             |
| Overvoltage Threshold (Response A)                | $V_{\text{OV-R}}$      | -   | 20   | -    | %             |
| Undervoltage Threshold (Response B)               | $V_{\text{UV-R}}$      | -   | -20  | -    | %             |
| Overvoltage Threshold (Response B)                | $V_{\text{OV-R}}$      | -   | 20   | -    | %             |
| Filter Delay Timer <sup>(23)</sup>                | $t_{\text{FILTER}}$    | -   | 20   | -    | $\mu\text{s}$ |
| <b>RST</b>                                        |                        |     |      |      |               |
| RST Reset Delay <sup>(23)</sup>                   | $t_{\text{RST-DELAY}}$ | -   | 10   |      | ms            |
| <b>REGULATOR 1 &amp; VG</b>                       |                        |     |      |      |               |
| Operating Frequency <sup>(22), (23)</sup>         | $f_{\text{SW1}}$       | 750 | -    | 1500 | kHz           |
| Operating Frequency Selection Step Size           | $f_{\text{STEP}}$      | -   | 250  | -    | kHz           |
| Constant Time Off Value <sup>(23)</sup>           | $t_{\text{OFF}}$       | -   | 1.0  | -    | $\mu\text{s}$ |
| Low-side Timeout <sup>(23)</sup>                  | $t_{\text{TIMEOUT}}$   | -   | 15   | -    | $\mu\text{s}$ |
| <b>REGULATOR 2</b>                                |                        |     |      |      |               |
| Operating Frequency <sup>(23)</sup>               | $f_{\text{SW1}}$       | 750 | -    | 2000 | kHz           |
| Operating Frequency Selection Step Size           | $f_{\text{STEP}}$      | -   | 250  | -    | kHz           |

**Notes**

22. When REG1 is used, the maximum  $f_{\text{SW1}}$  Frequency programed with external components should be 1500 kHz
23. Guaranteed by design.

**Table 5. Dynamic Electrical Characteristics**

Characteristics noted under conditions  $2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ ,  $-20^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ,  $\text{GND} = 0\text{ V}$ , unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_A = 25^{\circ}\text{C}$  under nominal conditions, unless otherwise noted.

| Characteristic                          | Symbol            | Min | Typ | Max  | Unit |
|-----------------------------------------|-------------------|-----|-----|------|------|
| <b>REGULATOR 3</b>                      |                   |     |     |      |      |
| Operating Frequency                     | $f_{\text{SW1}}$  | 750 | -   | 2000 | kHz  |
| Operating Frequency Selection Step Size | $f_{\text{STEP}}$ | -   | 250 | -    | kHz  |
| <b>REGULATOR 4</b>                      |                   |     |     |      |      |
| Operating Frequency                     | $f_{\text{SW1}}$  | 750 | -   | 2000 | kHz  |
| Operating Frequency Selection Step Size | $f_{\text{STEP}}$ | -   | 250 | -    | kHz  |
| <b>REGULATOR 5</b>                      |                   |     |     |      |      |
| Operating Frequency                     | $f_{\text{SW1}}$  | 750 | -   | 2000 | kHz  |
| Operating Frequency Selection Step Size | $f_{\text{STEP}}$ | -   | 250 | -    | kHz  |
| <b>REGULATOR 6</b>                      |                   |     |     |      |      |
| Operating Frequency                     | $f_{\text{SW2}}$  | 250 | -   | 1000 | kHz  |
| Operating Frequency Selection Step Size | $f_{\text{STEP}}$ | -   | 250 | -    | kHz  |
| <b>REGULATOR 7</b>                      |                   |     |     |      |      |
| Operating Frequency Selections          | $f_{\text{SW2}}$  | 250 | -   | 1000 | kHz  |
| Operating Frequency Selection Step Size | $f_{\text{STEP}}$ | -   | 250 | -    | kHz  |
| <b>REGULATOR 8</b>                      |                   |     |     |      |      |
| Operating Frequency                     | $f_{\text{SW2}}$  | 250 | -   | 1000 | kHz  |
| Operating Frequency Selection Step Size | $f_{\text{STEP}}$ | -   | 250 | -    | kHz  |

## FUNCTIONAL DESCRIPTION

### INTRODUCTION

The 34704 is an multi-channel power management IC (PMIC) meant to address power management needs for various multimedia applications microprocessors in various configurations with a target overall efficiency of > 80% at typical loads.

The 34704 accepts an input voltage from various sources:

- 1 cell Li-Ion/Polymer (2.7 to 4.2 V)
- 5.0 V USB supply or AC wall adapter

The different channels are:

| REGULATOR            | REGULATOR TYPE         | V <sub>OUT</sub> TYP (V) | I <sub>OUT</sub> TYP (mA) | I <sub>OUT</sub> MAX (mA) | TARGET APPLICATION |
|----------------------|------------------------|--------------------------|---------------------------|---------------------------|--------------------|
| REG1 <sup>(25)</sup> | Synchronous Boost      | 5.0                      | 100                       | 500                       | +5.0 V REF         |
| REG2                 | Synchronous Buck-Boost | 2.8 / 3.3                | 200                       | 500                       | μP I/O             |
| REG3                 | Synchronous Buck       | 1.2 / 1.5 / 1.8          | 150                       | 550                       | μP Core            |
| REG4                 | Synchronous Buck-Boost | 1.8 / 2.5                | 100                       | 300                       | DDR                |
| REG5                 | Synchronous Buck-Boost | 3.3                      | 150                       | 500                       | μP I/O             |
| REG6 <sup>(25)</sup> | Synchronous Boost      | 15.0                     | 20                        | 60                        | REF+               |
| REG7 <sup>(25)</sup> | Inverter Boost         | -7.0                     | 20                        | 60                        | REF -              |
| REG8                 | Synchronous Boost      | 15.0                     | 15                        | 30                        | Backlight Display  |

#### Notes

24. Synchronous Buck-Boost: These regulators can work as pure BUCK regulator when the output voltage is lower than the input voltage; and work as pure BOOST regulator when the input voltage is lower than the output voltage. Compensation should be done for the worst case scenario, which is in most of the cases when the device is working as a boost converter, after compensating for this scenario it is recommended to verify the buck operation to assure stability in the whole operating range.
25. Available only on the 34704A

REG1, REG3, REG6, and REG8 use internal compensation, while REG2, REG4, REG5, and REG7 use external compensation.

The switching frequency of all regulators except REG6, 7, & 8 can be selected through the FREQ pin between 750 kHz and 2.0 MHz in 250 kHz steps. The high frequency operation is meant to minimize the size of external components while lower operating frequencies will allow for higher efficiency. REG7 is limited to operate at a lower frequency to minimize switching noise induced by driving the external switching MOSFET, but also can operate at the 1.0 MHz value with proper board layout. REG 6, 7, and 8 switching frequency can be selected between 250 kHz and 1.0 MHz in 250 kHz steps through I<sup>2</sup>C.

For all regulators and at lower loads, a pulse skipping mode is implemented to maintain high efficiency.

Note that pulse skipping occurs when the regulator enters into discontinuous conduction mode (DCM) at very light loads, however transitions between DCM and CCM may result in noisy switching nodes, therefore it is recommended to design the regulators to work in CCM all the time. Pulse skipping function is not guaranteed by circuit implementation. The 34704 uses 4 different phases of switching for all

regulators except REG6, 7, and 8, to spread out the current draw by the individual converters from the input supply over time, to reduce the peak input current demand. This allows for better EMI performance and reduction in the input filter requirements.

Each regulator except REG1 uses an external feedback resistor divider to set the output voltage. All output voltages can be adjusted dynamically (Dynamic Voltage Scaling) on the fly through an I<sup>2</sup>C serial interface. All converters, except REG1, utilize automatic soft-start by ramping the reference voltage to the error amplifier to prevent sudden change in duty cycle and output current/voltage at power up. REG1 (VG) will limit the inrush current by implementing a peak current detect and a constant off time.

The 34704 is equipped with a dual function Power On/Off pin (ONOFF). This pin can be controlled by a mechanical switch to turn the device on or off. Pressing and releasing the mechanical switch turns the 34704 on while pressing and holding the switch for a time period (programmable through I<sup>2</sup>C) turns the 34704 off. Enable/disable control is also granted through I<sup>2</sup>C for groups of regulators and the whole IC.

## FUNCTIONAL PIN DESCRIPTION

### REG5 BOOST STAGE BOOTSTRAP CAPACITOR INPUT PIN (BT5U)

Connect a 1.0  $\mu\text{F}$  capacitor between this pin and SW5U pin to enhance the gate of the Switch Power MOSFET.

### REG4 BUCK STAGE BOOTSTRAP CAPACITOR INPUT PIN (BT4D)

Connect a 0.01  $\mu\text{F}$  capacitor between this pin and SW4D pin to enhance the gate of the Switch Power MOSFET.

### REG4 POWER SUPPLY INPUT VOLTAGE (PVIN4)

This is the connection to the drain of the high-side switch FET. Input decoupling /filtering is required for proper REG4 operation.

### REG4 BUCK STAGE SWITCHING NODE (SW4D)

The inductor is connected between this pin and the SW4U pin.

### REG4 REGULATED OUTPUT VOLTAGE PIN (VOUT4)

Connect this pin to the load and to the output filter as close to the pin as possible.

### REG4 BOOST STAGE SWITCHING NODE (SW4U)

The inductor is connected between this pin and the SW4D pin.

### REG4 BOOST STAGE BOOTSTRAP CAPACITOR INPUT PIN (BT4U)

Connect a 0.01  $\mu\text{F}$  capacitor between this pin and SW4U pin to enhance the gate of the Switch Power MOSFET.

### REG4 VOLTAGE FEEDBACK INPUT FOR VOLTAGE REGULATION/PROGRAMMING (FB4)

Connect the feedback resistor divider to this pin.

### REG4 COMPENSATION NETWORK CONNECTION (COMP4)

REG4 compensation network connection.

### REG3 BOOTSTRAP CAPACITOR INPUT PIN (BT3)

Connect a 0.01  $\mu\text{F}$  capacitor between this pin and SW3 pin to enhance the gate of the Switch Power MOSFET.

### REG3 POWER SUPPLY INPUT VOLTAGE (PVIN3)

This is the connection to the drain of the high-side switch FET. Input decoupling /filtering is required for proper REG3 operation.

### REG3 SWITCHING NODE (SW3)

The inductor is connected between this pin and the regulated REG3 output.

### REG3 OUTPUT VOLTAGE RETURN PIN (VOUT3)

This is the discharge path of REG3 output voltage.

### REG3 VOLTAGE FEEDBACK INPUT FOR VOLTAGE REGULATION/PROGRAMMING (FB3)

Connect the feedback resistor divider to this pin.

### SOFT START TIME (SS)

The soft start time for all regulators can be adjusted by connecting this pin to an external resistor divider between VDDI and AGND pins.

### OSCILLATOR FREQUENCY (FREQ)

The oscillator frequency can be adjusted by connecting this pin to an external resistor divider between VDDI and AGND pins. This pin sets  $F_{\text{SW1}}$  value.

### REG8 VOLTAGE FEEDBACK INPUT FOR VOLTAGE REGULATION/PROGRAMMING (FB8)

Connect the feedback resistor divider to this pin, when voltage mode control is used. When current mode control is used, connect this pin between the LED string and an  $I_{\text{SET}}$  resistor to GND to force the operating current. Refer to [Figure 10](#) and [Figure 11](#). Exclude the components not used.

### REG8 BOOTSTRAP CAPACITOR INPUT PIN (BT8)

Connect a 0.01  $\mu\text{F}$  capacitor between this pin and SW8 pin to enhance the gate of the Synchronous Power MOSFET.

### REG8 REGULATED OUTPUT VOLTAGE PIN (VOUT8)

Connect this pin directly to the load directly and to the output filter as close to the pin as possible.

### REG8 SWITCHING NODE (SW8)

The inductor is connected between this pin and VIN pin.

### REG1 SWITCHING NODE (SW1)

The inductor is connected between this pin and VIN pin.

### REG1 REGULATED OUTPUT VOLTAGE BEFORE THE CUT-OFF SWITCH (VG)

REG1 regulated output voltage before the cutoff switch. This supplies the internal circuits and the gate drive.

#### **REG1 REGULATED OUTPUT VOLTAGE PIN (VOUT1) (34704A ONLY)**

Connect this pin directly to the load directly and to the output filter as close to the pin as possible.

#### **REG1 BOOTSTRAP CAPACITOR INPUT PIN (BT1)**

Connect a 1.0  $\mu$ F capacitor between this pin and SW1 pin to enhance the gate of the Switch Power MOSFET.

#### **I<sup>2</sup>C SERIAL INTERFACE CLOCK INPUT (SCL)**

I<sup>2</sup>C serial interface clock input.

#### **I<sup>2</sup>C SERIAL INTERFACE DATA INPUT (SDA)**

I<sup>2</sup>C serial interface data input

#### **POWER RESET OUTPUT SIGNAL (MICROPROCESSOR RESET) (RST)**

This is an open drain output and must be pulled up by an external resistor to a supply voltage like  $V_{IN}$ .

#### **REG7 COMPENSATION NETWORK CONNECTION (COMP7)**

REG7 compensation network connection.

#### **REG7 RESISTOR FEEDBACK NETWORK REFERENCE VOLTAGE (VREF7) (34704A ONLY)**

Connect this pin to the bottom of the feedback resistor divider.

#### **REG7 VOLTAGE FEEDBACK INPUT FOR VOLTAGE REGULATION/PROGRAMMING (FB7) (34704A ONLY)**

Connect the feedback resistor divider to this pin.

#### **REG7 EXTERNAL POWER MOSFET GATE DRIVE (DRV7) (34704A ONLY)**

REG7 external Power MOSFET gate drive.

#### **REG7 OUTPUT VOLTAGE RETURN PIN (VOUT7) (34704A ONLY)**

This is the discharge path of REG7 output voltage.

#### **REG6 VOLTAGE FEEDBACK INPUT FOR VOLTAGE REGULATION/PROGRAMMING (FB6) (34704A ONLY)**

Connect the feedback resistor divider to this pin.

#### **REG6 BOOTSTRAP CAPACITOR INPUT PIN (BT6) (34704A ONLY)**

Connect a 0.01  $\mu$ F capacitor between this pin and SW6 pin to enhance the gate of the Synchronous Power MOSFET.

#### **REG6 SWITCHING NODE (SW6) (34704A ONLY)**

The inductor is connected between this pin and the VIN pin.

#### **REG6 REGULATED OUTPUT VOLTAGE PIN (VOUT6) (34704A ONLY)**

Connect this pin directly to the load directly and to the output filter as close to the pin as possible.

#### **ANALOG GROUND (AGND)**

Analog ground of the IC.

#### **BATTERY VOLTAGE CONNECTION (VIN)**

Input decoupling /filtering is required for the device to operate properly.

#### **INTERNAL SUPPLY VOLTAGE (VDDI)**

Connect a 1.0  $\mu$ F low ESR decoupling filter capacitor between this pin and GND.

#### **BATTERY DETECTION (LION)**

Pull this pin high to VIN to indicate a connection to a Li-Ion battery.

#### **DUAL FUNCTION IC TURN ON/OFF (ONOFF)**

This is a hardware enable/disable for the 34704. It can be connected to a mechanical switch to turn the power On or Off.

#### **REG2 BOOST STAGE BOOTSTRAP CAPACITOR INPUT PIN (BT2U)**

Connect a 1.0  $\mu$ F capacitor between this pin and SW2U pin to enhance the gate of the Switch Power MOSFET.

#### **REG2 COMPENSATION NETWORK CONNECTION (COMP2)**

REG2 compensation network connection.

#### **REG2 VOLTAGE FEEDBACK INPUT FOR VOLTAGE REGULATION/PROGRAMMING (FB2)**

Connect the feedback resistor divider to this pin.

#### **REG2 BUCK STAGE BOOTSTRAP CAPACITOR INPUT PIN (BT2D)**

Connect a 1.0  $\mu$ F capacitor between this pin and SW2D pin to enhance the gate of the Switch Power MOSFET.

#### **REG2 POWER SUPPLY INPUT VOLTAGE (PVIN2)**

This is the connection to the drain of the high-side switch FET. Input decoupling /filtering is required for proper REG2 operation.

#### **REG2 BUCK STAGE SWITCHING NODE (SW2D)**

The inductor is connected between this pin and the SW2U pin.

#### **REG2 REGULATED OUTPUT VOLTAGE PIN (VOUT2)**

Connect this pin to the load and to the output filter as close to the pin as possible.

#### **REG2 BOOST STAGE SWITCHING NODE (SW2U)**

The inductor is connected between this pin and the SW2D pin.

#### **REG5 BOOST STAGE SWITCHING NODE (SW5U)**

The inductor is connected between this pin and the SW5D pin.

#### **REG5 REGULATED OUTPUT VOLTAGE PIN (VOUT5)**

Connect this pin to the load and to the output filter as close to the pin as possible.

#### **REG5 BUCK STAGE SWITCHING NODE (SW5D)**

The inductor is connected between this pin and the SW5U pin.

#### **REG5 POWER SUPPLY INPUT VOLTAGE (PVIN5)**

This is the connection to the drain of the high-side switch FET. Input decoupling /filtering is required for proper REG5 operation.

#### **REG5 BUCK STAGE BOOTSTRAP CAPACITOR INPUT PIN (BT5D)**

Connect a 1.0  $\mu$ F capacitor between this pin and SW5D pin to enhance the gate of the Switch Power MOSFET.

#### **REG5 VOLTAGE FEEDBACK INPUT FOR VOLTAGE REGULATION/PROGRAMMING (FB5)**

Connect the feedback resistor divider to this pin.

#### **REG5 COMPENSATION NETWORK CONNECTION (COMP5)**

REG5 compensation network connection.

#### **POWER GROUND CONNECTION FOR ALL OF THE REGULATORS EXCEPT REG7 (PGND)**

Power Ground Connection for all of the regulators except REG7.

## FUNCTIONAL INTERNAL BLOCK DESCRIPTION

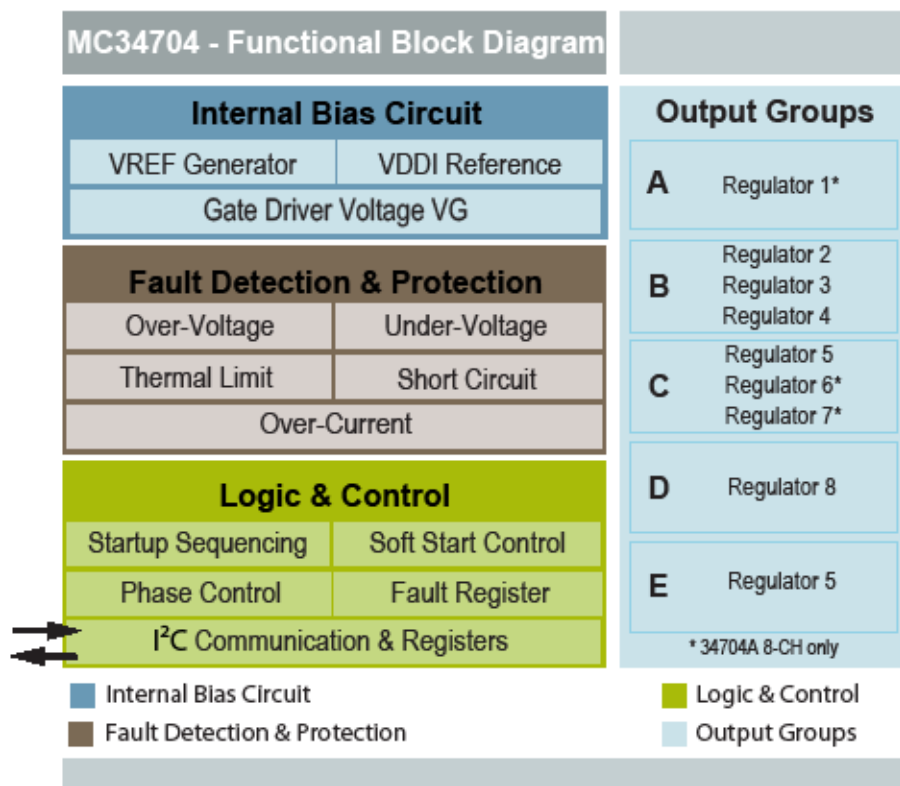


Figure 4. MC34704 Functional Internal Block Diagram

### INTERNAL BIAS CIRCUIT

#### Gate Driver Voltage (VG)

REG1/VG is the main regulator of the 34704 IC and will be used to supply internal circuitry and voltage biases through the VG output. It also provides the gate drive voltage for the rest of the regulators and itself.

See [Power-Up Sequence on page 28](#) for more details on how REG1 is a critical part of powering up the 34704. Based on this, REG1 will need extra circuitry to help it boot up until its output voltage is high enough that it can supply internal circuitry for the main control loop to take over.

REG1 VG starts up in peak current detect PFM mode and REG1 VG output starts rising. When the appropriate internal circuitry is alive and the switching frequency  $F_{SW1}$  is selected, the PWM control of REG1 can take over.

#### VREF Generator - Internal Reference

Each one of the regulators in the 34704 uses a DAC which is controlled by the I²C interface to generate a dynamic VREF voltage for setting the output voltage on each regulator.

#### VDDI Reference Voltage

The 34704 uses the internal VG voltage to provide a precise low current 2.5 V voltage that is meant to serve as reference voltage to derive the FREQ and SS voltage needed to set the switching frequency 1 (FSW1) and the soft start, respectively.

### FAULT DETECTION AND PROTECTION

#### Thermal Limit Detection

There is a thermal sensor for each regulator except REG7. All regulators of the corresponding group will shutdown if at least one of them reaches the thermal limit. If either REG2, REG3 or REG4 reaches its thermal limit, the whole part will shutdown immediately.

#### Overcurrent & Short-circuit Monitoring

The current limit circuitry has two levels of current limiting:

- A soft overcurrent limit (overcurrent limit): If the peak current reaches the typical overcurrent limit, the switcher will start a cycle-by-cycle operation to limit the current and a 10 ms current limit timer starts. The switcher will stay in this mode of operation until the part regains normal

operation, or shuts down after a failure to regain normal operation.

- A hard overcurrent limit (short-circuit limit) that is higher than the cycle by cycle limit at which the device reacts by shutting down the output immediately. This is necessary to prevent damage in case of a short-circuit. After that, only GrpB will attempt a one time retry after a time-out period of 10 ms and will go through a new soft start cycle

### Output Overvoltage/Undervoltage Monitoring

In the case of an output overvoltage/undervoltage, the user has two options that can be programmed through the I<sup>2</sup>C interface:

Response A: The output will switch off automatically and the 34704 would alert the processor through I<sup>2</sup>C that such an event happened.

Response B: The output will not switch off. Rather the 34704 communicates to the processor that an overvoltage/undervoltage condition has occurred and waits for the processor decision to either shutoff or not; in the mean time the control loop will try to fix itself.

NOTE: If Response A is set on any of the regulators from GrpB, and a OV/UV event occurs in the corresponding regulator, the complete device will shutdown and try to restart as long as the OV/UV is no longer present. This will also set the RST signal low until REG2, 3 and 4 are on regulation.

## LOGIC AND CONTROL

### Startup Sequencing

At power up, the VG regulator starts ramping up in peak detect mode. Meanwhile, VDDI is tracking VG until it reaches regulation and releases a POR signal that enables the internal circuitry and reads the FREQ and SS configuration to ramp up REG2, REG3 and REG4, that serve as the MPU main power supplies. Once the MPU is up, I<sup>2</sup>C communication is available to enable or disable GrpA, GrpC, GrpD and GrpE. An extra sequence can be configured for REG5, REG6 and REG7, changing the order in which they ramp up when enabled. [See Power-Up Sequence on page 28.](#)

### Soft Start Control

During power up the 34704 reads the SS terminal to configure a default soft start timing for all regulators when these are enabled. Soft start for REG5 to REG8 can be

changed via I<sup>2</sup>C at any time after power up has successfully completed.

### Phase Control

REG1 to REG5 use the main Switching frequency FSW1, which is configured through the FREQ terminal at power up. FSW1 uses 4 different phases of switching (clock is 80 degrees out of phase) to spread out the current draw by the individual converters from the input supply over time to reduce the peak input current demand. The remaining regulators use FSW2 which can be programmed at any time via I<sup>2</sup>C after a successful power up sequence.

### Fault Register

The 34704 has a dedicate fault register accessible via I<sup>2</sup>C which indicate which regulator is detecting a fault situation. In addition to this, each channel has its own fault register which indicates the type of fault detected in that regulator.

### I<sup>2</sup>C communication and Registers

The 34704 can communicate using a standard I<sup>2</sup>C, communication protocol or an accurate I<sup>2</sup>C protocol. During the first one, the device processes the given command as soon as it has received it. During the accurate data communication, the device requires that each read/write command be sent twice to validate the data. The 34704 provides a user accessible register map that allows various general IC configurations as well as independent control of each regulator, including fault flag registers and all configurable features for each regulator.

## OUTPUT GROUPS - REGULATORS

The 34704 is divided in 5 different groups which are arranged as follows:

- GrpA: Includes REG1<sup>(26)</sup> (VOUT1)
- GrpB: Includes REG2, REG3, and REG4
- GrpC: Includes REG5, REG6<sup>(26)</sup>, and REG7<sup>(26)</sup>
- GrpD: Includes REG8
- GrpE: This is a special group. It includes REG5 when GrpC/E power sequencing option#1 is chosen

Turning on/off each group would cause all contained regulators to turn on/off.

#### Notes

26. Only on 34704A

## REGULATOR OVERVIEW WITH EFFICIENCY ANALYSIS

### REG1 (34704A Only)

REG1 is a synchronous boost PWM voltage-mode control DC/DC regulator available only in the 34704A. Even though REG1 is a synchronous regulator, it is recommended to have a diode connected externally across its synchronous MOSFET. When the battery voltage is above REG1's output (>5.0 V) as the case might be when connected to the USB supply or wall adaptor, the REG1 power MOSFETs will be tri-stated and the voltage on the output will be Battery minus the diode drop. This will help maintain REG1's output to a maximum of 5.2 V and not allow it to drift all the way to 5.5 V.

The switcher will operate in DCM at very light loads to allow pulse skipping.

On the 34704A, when the appropriate command is received from the processor to turn on VOUT1, then the isolation FET of REG1 would turn on gradually to avoid any inrush current out of VG and to ramp the VOUT1 voltage in a controlled manner.

REG1 VOUT1 will be discharged every time GrpA is shutting down and it will be held low by the discharge FET as long as possible.

#### Characteristics

- It powers up directly from the battery
- Operates at a switching frequency equals to  $F_{SW1}$
- Drives integrated low  $R_{DS(on)}$  N-channel power MOSFETs (NHV\_HC) as its output stage
- It offers load disconnect from the input battery when the output is off (True Cutoff)
- The output is  $\pm 4\%$  accuracy
- Output voltage is set to 5.0 V by means of an internal resistor divider
- The output can be adjusted up or down at 2.5% for a total of 10% on each direction allowing Dynamic Voltage Scaling
- Uses a bootstrap network with an internal diode to power its synchronous MOSFET
- All gate drive circuits are supplied from REG1's own VG output.
- Uses integrated compensation
- The output is monitored for undervoltage and overvoltage conditions
- The output is monitored for overcurrent and short-circuit conditions
- The regulator is monitored for overtemperature conditions

#### Operation Modes

The VG output is always active as long as:

- The IC is not in an undervoltage lockout AND
- No shutdown signal through the  $\overline{ONOFF}$  pin is present AND

- There is no ALLOFF shutdown command through the I<sup>2</sup>C interface AND
- No faults exist that would cause the 34704 to shutdown  
The VOUT1 output will be active when:
- VG output is available AND
- There is no GrpA shutdown command through the I<sup>2</sup>C interface AND
- No faults exist that would cause the VOUT1 to shut down

### REG2

This is a 4-switch synchronous buck-boost PWM voltage-mode control DC/DC regulator.

See [Power-Up Sequence on page 28](#) for more details on when REG2 is powered up in the sequence.

The switcher will operate in DCM at very light loads to allow pulse skipping.

VOUT2 will be discharged every time the regulator is shutting down and it will be held low by the discharge FET as long as possible.

#### Characteristics

- It powers up directly from the battery
- Operates at a switching frequency equals to  $F_{SW1}$
- Drives integrated low  $R_{DS(on)}$  N-channel power MOSFETs (NHV\_HC) as its output stage
- The output is  $\pm 2\%$  accuracy
- Output voltage is adjustable by means of an external resistor divider
- The output can be adjusted up or down at 2.5% steps for a total of +17.5% to -20.0% on each direction allowing Dynamic Voltage Scaling
- Uses bootstrap networks with an internal diode to power its high-side MOSFETs
- All gate drive circuits are supplied from VG
- Uses external compensation
- The output is monitored for undervoltage and overvoltage conditions
- The output is monitored for overcurrent and short-circuit conditions
- The regulator is monitored for overtemperature conditions

#### Operation Modes

The switcher will be active when:

- VG is in regulation AND
- There is no GrpB shutdown command through the I<sup>2</sup>C interface AND
- No faults exist that would cause GrpB to shut down

### REG3

This is a synchronous buck PWM voltage-mode control DC/DC regulator.

See [Power-Up Sequence on page 28](#) for more details on when REG3 is powered up in the sequence.

The switcher will operate in DCM at very light loads to allow pulse skipping.

VOUT3 will be discharged every time the regulator is shutting down and it will be held low by the discharge FET as long as possible.

### Characteristics

- It powers up directly from the battery
- Operates at a switching frequency equals to  $F_{SW1}$
- Drives integrated low  $R_{DS(on)}$  N-channel power MOSFETs (NHV\_HC) as its output stage
- The output is  $\pm 4\%$  accuracy
- Output voltage is adjustable by means of an external resistor divider
- The output can be adjusted up or down at 2.5% steps to achieve from +17.5% to -20.0% on each direction allowing Dynamic Voltage Scaling using the  $I^2C$  DVS register.
- An extra fine voltage scaling in 0.5% steps helps to adjust down the output voltage as low as 40%.
- Uses a bootstrap network with an internal diode to power its switch MOSFET
- All gate drive circuits are supplied from VG.
- Uses integrated compensation.
- The output is monitored for undervoltage and overvoltage conditions
- The output is monitored for overcurrent and short-circuit conditions
- The regulator is monitored for overtemperature conditions

### Operation Modes

The switcher will be active when:

- VG is in regulation AND
- There is no GrpB shutdown command through the  $I^2C$  interface AND
- No faults exist that would cause GrpB to shut down

### REG4

This is a 4-switch synchronous buck-boost PWM voltage-mode control DC/DC regulator.

See [Power-Up Sequence on page 28](#) for more details on when REG4 is powered up in the sequence.

The switcher will operate in DCM at very light loads to allow pulse skipping.

VOUT4 will be discharged every time the regulator is shutting down and it will be held low by the discharge FET as long as possible.

### Characteristics

- It powers up directly from the battery
- Operates at a switching frequency equals to  $F_{SW1}$

- Drives integrated low  $R_{DS(on)}$  N-channel power MOSFETs (NHV\_HC) as its output stage
- The output is  $\pm 2\%$  accuracy
- Output voltage is adjustable by means of an external resistor divider
- The output can be adjusted up or down at 2.5% steps for a total of +17.5% to -20.0% on each direction allowing Dynamic Voltage Scaling.
- Uses bootstrap networks with an internal diode to power its high-side MOSFETs
- All gate drive circuits are supplied from VG.
- Uses external compensation
- The output is monitored for undervoltage and overvoltage conditions
- The output is monitored for overcurrent and short-circuit conditions
- The regulator is monitored for overtemperature conditions

### Operation Modes

The switcher will be active when:

- VG is in regulation AND
- There is no GrpB shutdown command through the  $I^2C$  interface AND
- No faults exist that would cause GrpB to shut down

### REG5

This is a 4-switch synchronous buck-boost PWM voltage-mode control DC/DC regulator.

See [Power-Up Sequence on page 28](#) for more details on when REG5 is powered up in the sequence.

The switcher will operate in DCM at very light loads to allow pulse skipping.

VOUT5 will be discharged every time the regulator is shutting down and it will be held low by the discharge FET as long as possible.

### Characteristics

- It powers up directly from the battery
- Operates at a switching frequency equals to  $F_{SW1}$
- Drives integrated low  $R_{DS(on)}$  N-channel power MOSFETs (NHV\_HC) as its output stage
- The output is  $\pm 2\%$  accuracy
- Output voltage is adjustable by means of an external resistor divider
- The output can be adjusted up or down at 2.5% steps for a total of +17.5% to -20.0% on each direction allowing Dynamic Voltage Scaling.
- Uses bootstrap networks with an internal diodes to power its high-side MOSFETs
- All gate drive circuits are supplied from VG.
- Uses external compensation
- The output is monitored for undervoltage and overvoltage conditions

- The output is monitored for overcurrent and short-circuit conditions
- The regulator is monitored for overtemperature conditions

### Operation Modes

The switcher will be active when:

- VG is in regulation AND
- There is no GrpC (OR GrpE) shutdown command through the I<sup>2</sup>C interface AND
- No faults exist that would cause GrpC (OR GrpE) to shut down

### REG6 (Only 34704A)

This is a synchronous boost PWM voltage-mode control DC/DC regulator.

See [Power-Up Sequence on page 28](#) for more details on when REG6 is powered up in the sequence.

The switcher will operate in DCM at very light loads to allow pulse skipping.

VOUT6 will be discharged every time the regulator is shutting down and it will be held low by the discharge FET as long as possible.

### Characteristics

- It powers up directly from the battery
- Operates at a switching frequency equals to  $F_{SW2}$
- Drives integrated low  $R_{DS(on)}$  N-channel power MOSFETs (NVHV\_LC) as its output stage
- It offers load disconnect from the input battery when the output is off (True Cut-Off)
- The output is  $\pm 4\%$  accuracy
- Output voltage is adjustable by means of an internal resistor divider
- The output can be adjusted up or down at 2.5% steps for a total of 10% on each direction allowing Dynamic Voltage Scaling
- Uses a bootstrap network with an internal diode to power its synchronous MOSFET
- All gate drive circuits are supplied from VG.
- Uses integrated compensation.
- The output is monitored for undervoltage and overvoltage conditions
- The output is monitored for overcurrent and short-circuit conditions
- The regulator is monitored for overtemperature conditions

### Operation Modes

The switcher will be active when:

- VG is in regulation AND
- There is no GrpC shutdown command through the I<sup>2</sup>C interface AND
- No faults exist that would cause GrpC to shut down

### REG7 (Only 34704A)

This is a none-synchronous buck-boost inverting PWM voltage-mode control DC/DC regulator.

See [Power-Up Sequence on page 28](#) for more details on when REG7 is powered up in the sequence.

The switcher will operate in DCM at very light loads to allow pulse skipping.

VOUT7 will be discharged every time the regulator is shutting down and it will be held high to ground by the discharge FET as long as possible.

### Characteristics

- It powers up directly from the battery
- Operates at a switching frequency equals to  $F_{SW2}$
- Drives an external P-channel power MOSFET
- The output is  $\pm 2\%$  accuracy
- Output voltage is adjustable by means of an external resistor divider
- The output can be adjusted up or down at 2.5% steps for a total of 10% on each direction allowing Dynamic Voltage Scaling.
- All gate drive circuits are supplied from  $V_G$
- Uses external compensation, the type is up to the designer
- The output is monitored for undervoltage and overvoltage conditions

### Operation Modes

The switcher will be active when:

- VG is in regulation AND
- There is no GrpC shutdown command through the I<sup>2</sup>C interface AND
- No faults exist that would cause GrpC to shut down

### REG8

This is a synchronous boost PWM voltage-mode control DC/DC regulator.

See [Power-Up Sequence on page 28](#) for more details on when REG8 is powered up in the sequence.

VOUT8 will be discharged every time the regulator is shutting down and it will be held to ground by the discharge FET as long as possible.

This regulator offers either voltage regulation for organic LEDs or current regulation for LCD backlighting LEDs. It provides either voltage or current feedback for these purposes through the same feedback pin.

The regulator cannot drive only 1LED with a forward voltage drop of less than the battery input voltage.

The processor would set the REG8 register through I<sup>2</sup>C before enabling REG8 to indicate if voltage regulation or current regulation will be used.

### Characteristics

- It powers up directly from the battery

- Operates at a switching frequency equals to  $F_{SW2}$
- Drives integrated low  $R_{DS(on)}$  N-channel power MOSFETs (NVHV\_LC) as its output stage
- It offers load disconnect from the input battery when the output is off (True Cut-Off)
- The output is  $\pm 4\%$  accuracy
- Output voltage is adjustable by means of an external resistor divider when in voltage regulation mode
- A 240 mV current limit comparator will be used to program/sense the voltage drop across the current setting resistor at the bottom of the LED string connected to the REG8 output when the current regulation mode is selected. This will be used to program the maximum current flowing and will regulate it
- The output can be adjusted up or down at 2.5% steps for a total of 10% on each direction allowing Dynamic Voltage Scaling
- Maximum output current is adjustable by means of an external resistor connected to the FB8 pin and then the output current can be scaled down from the set maximum in 16 steps through I<sup>2</sup>C interface
- Uses a bootstrap network with an internal diode to power its synchronous MOSFET
- All gate drive circuits are supplied from VG.
- Uses integrated compensation
- The output is monitored for overcurrent and short-circuit conditions
- The regulator is monitored for overtemperature conditions
- The output is monitored for undervoltage and overvoltage conditions

### Operation Modes

The switchers will be active when:

- VG is in regulation AND
- There is no GrpD shutdown command through the I<sup>2</sup>C interface AND
- No faults exist that would cause GrpD to shut down

### OVERALL EFFICIENCY ANALYSIS

In battery applications, it is highly recommended to power every single regulator directly from the battery to obtain full output capability:

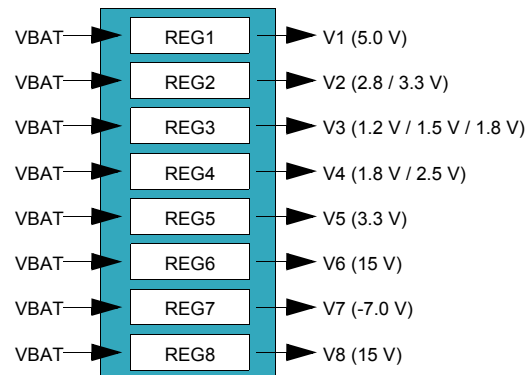


**Figure 5. Overall Efficiency Analysis**

Efficiency analysis includes the following losses:

- MOSFET Conduction Losses
- MOSFET Switching Losses (Except for REG7 due to external MOSFET and board layout dependence)
- MOSFET Gate Charging Losses
- MOSFET Deadtime Losses
- External Diode Losses (Only for REG7)
- Inductor Winding DC Losses
- Inductor Core Losses (Assumed to be 20% of DC Losses as a rule of thumb)
- Output AC Losses

### Efficiency Analysis

In this configuration, all of the regulators are supplied or powered directly with 3.6 V nominal, battery voltage.

Efficiency was calculated using the maximum allowed frequency of 1.5 MHz and 1.0 MHz for  $F_{SW1}$  and  $F_{SW2}$ , respectively, in this configuration. As a result, the following numbers are valid for worst case operation conditions.

The following table shows the detailed analysis for each regulator with V2 at 3.3 V, V3 at 1.2 V, and V4 at 1.8 V.

**Table 6. Regulator Analysis Table**

|                   | REG1   | REG2   | REG3   | REG4   | REG5   | REG6   | REG7   | REG8   |
|-------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| Vin (V)           | 3.60   | 3.60   | 3.60   | 3.60   | 3.60   | 3.60   | 3.60   | 3.60   |
| Vout (V)          | 5.00   | 3.30   | 1.20   | 1.80   | 3.30   | 15     | -7     | 15     |
| Iout_typ (A)      | 0.100  | 0.200  | 0.150  | 0.100  | 0.150  | 0.050  | 0.050  | 0.015  |
| Iout_max (A)      | 0.500  | 0.500  | 0.550  | 0.300  | 0.500  | 0.060  | 0.060  | 0.030  |
| DCR(mΩ)           | 230    | 230    | 230    | 310    | 230    | 230    | 230    | 230    |
| Cout (μF)         | 22     | 22     | 22     | 22     | 22     | 22     | 22     | 22     |
| ESR (mΩ)          | 9.00   | 9.00   | 9.00   | 9.00   | 9.00   | 9.00   | 9.00   | 9.00   |
| Fsw (kHz)         | 1500   | 1500   | 1500   | 1500   | 1500   | 1000   | 1000   | 1000   |
| Lout (μH)         | 1.50   | 1.50   | 1.50   | 1.50   | 1.50   | 4.70   | 4.70   | 4.70   |
| Iin_typ (A)       | 0.154  | 0.201  | 0.063  | 0.059  | 0.150  | 0.254  | 0.107  | 0.077  |
| Iin_max (A)       | 0.540  | 0.502  | 0.209  | 0.178  | 0.501  | 0.304  | 0.128  | 0.154  |
| ILout_peak (A)    | 0.724  | 0.510  | 0.649  | 0.444  | 0.512  | 0.444  | 0.443  | 0.297  |
| ICout_RMS (A)     | 0.212  | 0.005  | 0.074  | 0.076  | 0.0006 | 0.071  | 0.129  | 0.043  |
| Pout (W)          | 0.500  | 0.660  | 0.180  | 0.180  | 0.495  | 0.750  | 0.350  | 0.225  |
| Ploss On Chip (W) | 0.042  | 0.047  | 0.038  | 0.028  | 0.034  | 0.135  | 0.000  | 0.045  |
| Ploss Total (W)   | 0.044  | 0.049  | 0.041  | 0.030  | 0.035  | 0.145  | 0.027  | 0.047  |
| Pin (W)           | 0.544  | 0.709  | 0.221  | 0.210  | 0.530  | 0.895  | 0.377  | 0.272  |
| η (%)             | 91.90% | 93.12% | 81.48% | 85.91% | 93.33% | 60.00% | 69.00% | 64.00% |

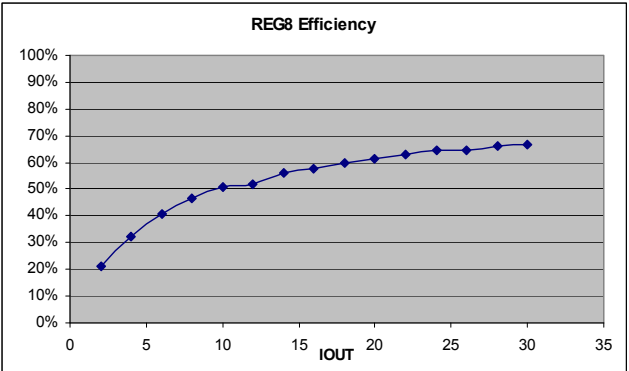
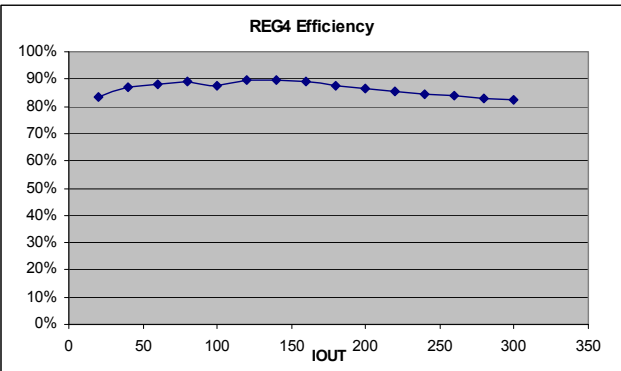
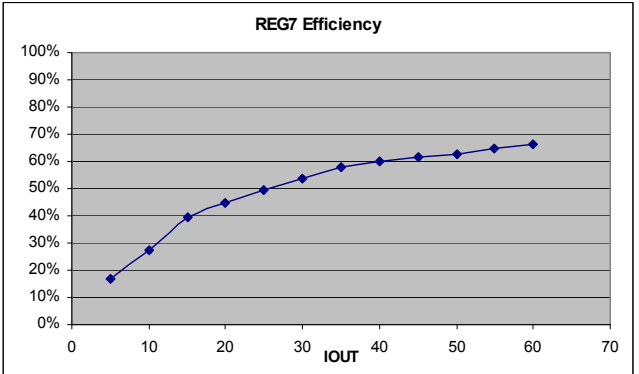
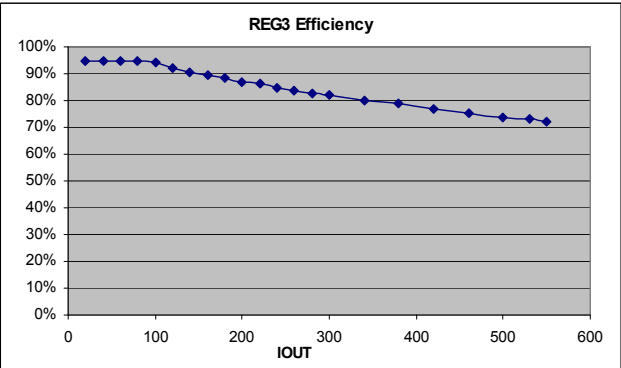
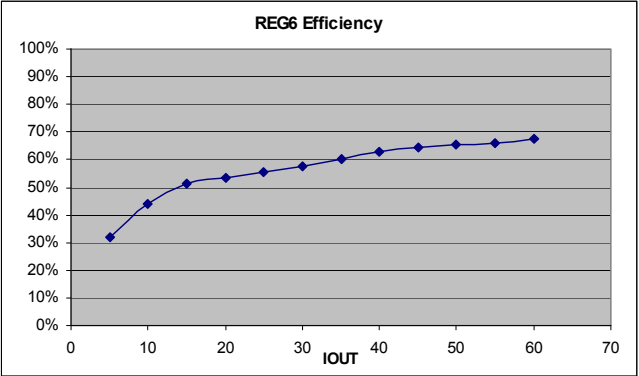
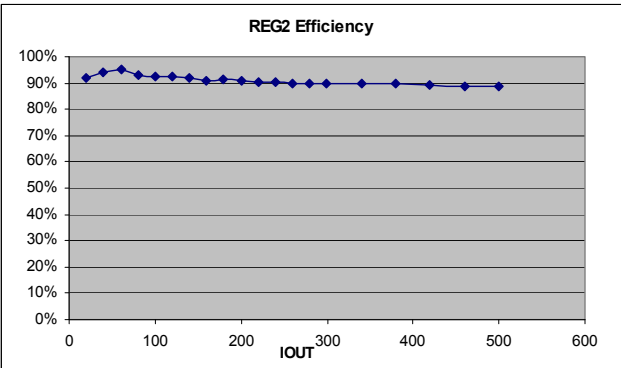
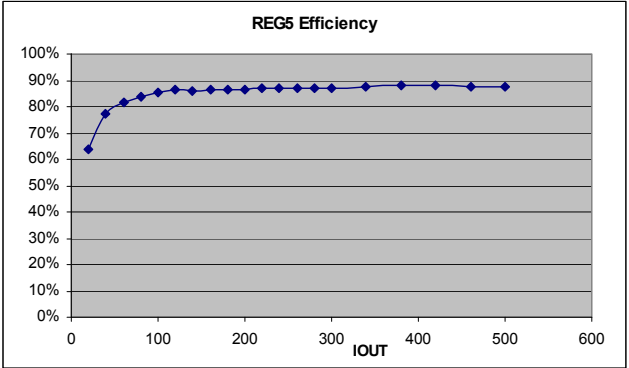
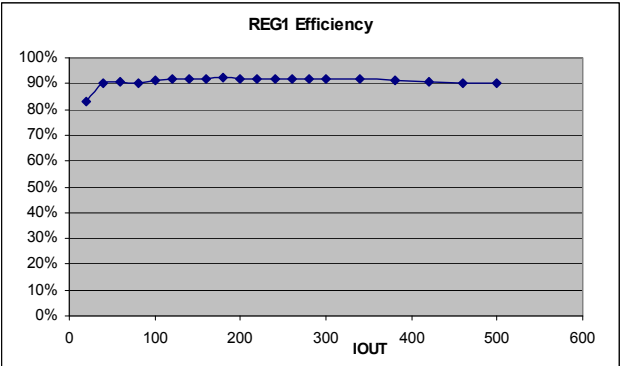
**Table 7. 34704A overall system efficiency 84%**

|                   | Overall System |
|-------------------|----------------|
| Pout (W)          | 3.340          |
| Ploss On Chip (W) | 0.369          |
| Ploss Total (W)   | 0.41           |
| Pin (W)           | 3.75           |
| η (%)             | 84.00%         |

**Table 8. 34704B overall system efficiency 89%**

|                   | Overall System |
|-------------------|----------------|
| Pout (W)          | 1.74           |
| Ploss On Chip (W) | 0.192          |
| Ploss Total (W)   | 0.202          |
| Pin (W)           | 1.942          |
| η (%)             | 89.6%          |

# MC34704 EFFICIENCY WAVEFORMS



## FUNCTIONAL DEVICE OPERATION

### OPERATIONAL MODES

#### POWER-UP SEQUENCE

Following is the power up sequence from a battery connection or a Power On signal through the ONOFF pin.

1. Battery initially connected to VIN.
2. LION pin is used to determine if a battery is being used (High for Li-Ion battery).
3. At initial power up from a cold start like the above with the battery first connected, the status of the ONOFF pin is ignored and 34704 moves forward to step (5).
4. After the cold start or battery insertion power up, activity on the ONOFF pin is used to determine if the device is enabled or disabled. If the device is disabled, then nothing happens. If the device is enabled then, 34704 moves forward to step (5).
5. The input battery UVLO signal de-asserts if the input voltage is above the UVLO rising threshold.
6. REG1 VG starts up in peak detect PFM and REG1 VG output starts rising.
7.  $V_{DDI}$  output voltage will start tracking REG1 VG output.
8. When REG1 VG output rises high enough such that  $V_{DDI}$  voltage is in regulation a POR signal is released and all internal circuitry can be enabled.  $I^2C$  communication will remain disabled for normal power up sequence. The values of the FREQ and SS pins are read at this point.
9. REG1 PWM control loop can take over control of REG1 output once the VG voltage reaches a certain threshold set internally.
10. When REG1 is in regulation, it will be used to supply the Power MOSFET gate voltage for all of the other regulators except REG7.
11. REG3 is enabled, then when REG3 is in regulation.
12. REG2 is enabled, then when REG2 is in regulation.
13. REG4 is enabled, then when REG4 is in regulation.
14.  $I^2C$  communication is enabled now since the processor supplies are up.
15. 34704 will de-assert the RST signal to indicate a "Power Good" after 10 ms of wait time. This output will be connected to the reset pin of the microprocessor.
16. The microprocessor then takes over and can enable REG1 VOUT1 and REG5 through REG8. The processor needs to send a command for REG8 mode of operation. The processor can also change REG5-8 soft start time before enabling them. The processor can also power down the system with an ALLOFF command.

For power sequencing needs, the different regulators are grouped based on their function and how they relate to each

other and the entire system. This makes power sequencing control a much easier task for the user where most of the group internal sequencing is now handled by the PMIC. All the processor has to do is to command the group and not each regulator.

The regulators groups are as follows:

- GrpA: Includes REG1 (VOUT1)
- GrpB: Includes REG2, REG3, and REG4
- GrpC: Includes REG5, REG6, and REG7
- GrpD: Includes REG8
- GrpE: This is a special group. It includes REG5 when GrpC/E power sequencing option#1 is chosen

#### SHUTDOWN SEQUENCES

- Processor can disable VOUT1 (GrpA) at any point it desires
- Processor can disable REG8 (GrpD) at any point it desires
- Processor can disable REG5 (GrpE) at any point it desires if sequencing option#1 is picked
- Processor can shutdown GrpC according to the power sequencing options 1, 2, 3, or 4 (see section "[I<sup>2</sup>C User Interface](#)")
- If any regulator in GrpC is shutting down due to a fault, the other regulators in GrpC will also shutdown by following the GrpC power sequencing options 1, 2, 3, or 4 (see section "[I<sup>2</sup>C User Interface](#)")
- If any regulator in GrpB is shutting down due to a fault, the other regulators in GrpB will also shutdown by following the processor supplies shutdown sequence. Then, GrpA, GrpC, GrpD, and GrpE (if applicable) will simultaneously shutdown keeping any sequencing within each group as necessary. VG will stay alive to perform a power up retry for GrpB but only for one time. If the power up cycle is successful, then normal operation is back. If the fault returns, then the shutdown sequence is repeated and then VG shuts down
- Processor can shutdown the 34704 by sending an "ALLOFF" command, then GrpA, GrpC, GrpD, and GrpE (if applicable) will simultaneously shutdown keeping any sequencing within each group as necessary. Then, GrpB will shutdown according to the processor supply shutdown sequence. Then, VG will shut down.
- The previous shutdown event can also happen through the ONOFF pin by pressing and holding the pin for a time period (programmable through  $I^2C$  with a default of 1sec)
- During battery depletion and when the input voltage passes the UVLO falling threshold, all of the outputs will be disabled without honouring the power down sequence This is to guarantee that the outputs are off and battery is not depleted further.

- In any of the previous shutdown sequences, VG output will stay alive to maintain internal circuitry and logic until all other regulators are off, then it will shut off.

## POWER SUPPLY

The battery voltage range is the following depending on the application:

- 1-cell Li-Ion/Polymer: 2.7 to 4.2 V. Typ value is 3.6 V
- USB supply or AC wall adapter: 4.5 to 5.5 V. Typ value is 5.0 V. This gives a total input voltage supply range of 2.7 to 5.5 V

For the regulators, each one will be supplied separately through its own power input.

## LION PIN

LION pin is always tied to VIN level.

## FREQUENCY SETTING PIN (FREQ PIN)

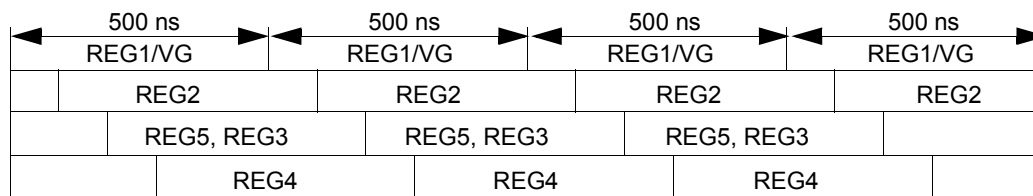
There are two switching frequencies on board the 34704, one for REG6, 7 & 8, and the other for the rest of the regulators. To avoid any jitter or interference problems by having two oscillators on board, the switching frequency will be derived from the main oscillator using a frequency divider.

The switching frequency will be selectable for all of the regulators. REG6, 7 & 8 switching frequency ( $F_{SW2}$ ) will be selectable through I<sup>2</sup>C to be between 250 kHz and 1.0 MHz in 250 kHz steps. The rest of the regulators switching frequency ( $F_{SW1}$ ) will be selectable through the FREQ pin and can be selected between 750 kHz and 2.0 MHz, in 250 kHz steps.

$F_{SW1}$  default value is 2.0 MHz. This value is obtained by tying the FREQ pin to VDDI.  $F_{SW2}$  default value is 500 kHz.

$F_{SW1}$  will be selectable through programming the FREQ pin with an external resistor divider connected between VDDI and AGND pins.  $F_{SW2}$  will only be selectable through I<sup>2</sup>C. Please refer to the "I<sup>2</sup>C Programmability" section.

The 34704 uses 4 different phases of switching (clock is 80 degrees out of phase) for  $F_{SW1}$  to spread out the current draw by the individual converters from the input supply over time to reduce the peak input current demand. This allows for better EMI performance and reduction in the input filter requirements.  $F_{SW1}$  has no phase relation with  $F_{SW2}$ . The following distribution is shown for  $F_{SW1}$  of 2.0 MHz. The regulators grouping is based on their maximum current draw and attempts to reduce the effect on the input current draw.



## SOFT START PIN (SS PIN)

Initially at power up, the soft start time will be set for all of the regulators through programming the SS pin with an external resistor divider connected between VDDI and AGND pins (see the [34704A Typical Application Diagram](#)).

After power up, the soft start value for REG5 through REG8 can be changed and programmed through I<sup>2</sup>C. REG2 through REG4 soft start value is only set by the SS pin and cannot be programmed through I<sup>2</sup>C.

See section "I<sup>2</sup>C Programmability" for more details.

## ONOFF PIN

This is a hardware enable/disable feature OR pin for the 34704:

- It can be connected to a mechanical switch to turn the power On or Off
- The device is power off by a command via the I<sup>2</sup>C interface as well
- The power off by hardware can be masked by a command via the I<sup>2</sup>C interface
- If the device is off and a falling edge is detected at the  $\overline{\text{ONOFF}}$  pin, the device starts up

- If and only if the device is on and the  $\overline{\text{ONOFF}}$  pin is pulled down for a time period (1s as a default and selectable to 2.0 sec, 1.5 sec, 1.0 sec or 0.5 sec via the I<sup>2</sup>C interface), then the device powers off after a second time period elapses unless it is masked by a command via the I<sup>2</sup>C interface:

- The second period is the same amount of time as the first period so that the counter can be shared
- When the first period elapses a shutdown flag is set to alert the processor that a shutdown signal has been activated. The  $\overline{\text{ONOFF}}$  pin can be released after this flag is set without affecting what will happen next
- A CPU can read out the shutdown flag to determine what to do
- Power off the device immediately by a command via I<sup>2</sup>C interface (ALLOFF command)
- Ignore the power off by sending a command via I<sup>2</sup>C interface to clear the shutdown flag

- Do nothing until the second time period expires and let the device power off by itself

The  $\overline{\text{ON/OFF}}$  pin is edge sensitive and activates on a falling edge. It is normally pulled high.

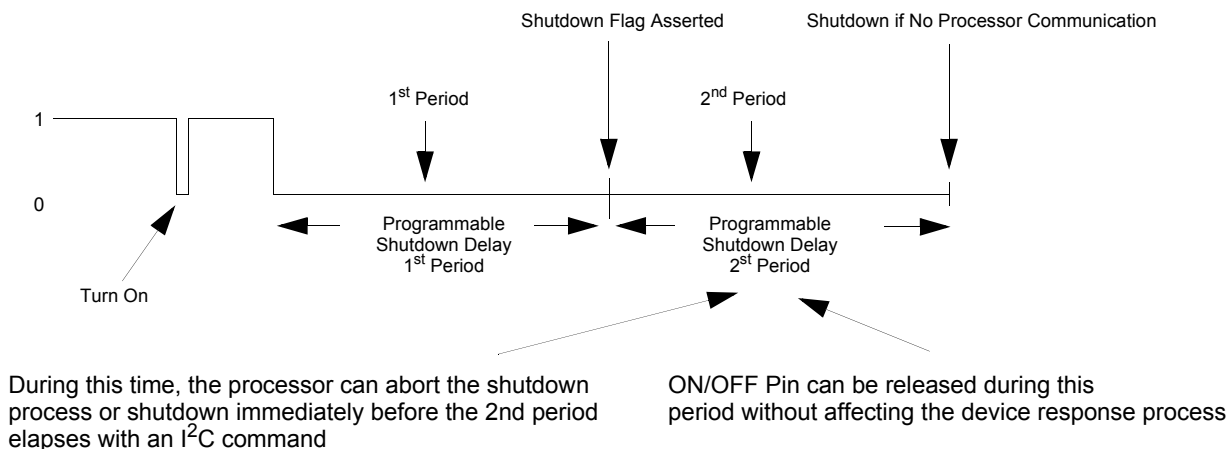


**Figure 6. Hardware Power Up/Down Timing**

## RST OUTPUT SIGNAL PIN

This is a power reset output signal. It is an open drain output that should be connected to the reset input of the microprocessor. An external pull up resistor should be connected to this output and is recommended to be pulled up to V2 for best performance (If this pin is pulled up to the VIN pin, then the 1.0  $\mu\text{A}$  shutdown current budget is not guaranteed)

At power up, the  $\overline{\text{RST}}$  pin is asserted (low) to keep the processor in “reset”. When VG, REG2, REG3, and REG4 are all in regulation (both OV and UV flags for each regulator are de-asserted) and no faults exist, the  $\overline{\text{RST}}$  output is de-asserted after a 10 ms delay to take the processor out of reset. Then the processor can go through its own internal power up sequence and can start communicating to the rest of the system.

If ANY of the above four regulators has any of the following faults: overtemperature, short-circuit, overcurrent for more than 10 ms, overvoltage in response A, undervoltage in response A, or is shutting down normally, the  $\overline{\text{RST}}$  output is asserted to put the processor back in reset. If ANY of the above four regulators has an overvoltage response B fault or an undervoltage response B fault, the  $\overline{\text{RST}}$  output will not be asserted (only the OV and UV flags will be available for the microprocessor to read).

## THERMAL LIMIT DETECTION

There is a thermal sensor for each regulator except REG7. It uses an external MOSFET.

## CURRENT LIMIT MONITORING

The current limit circuitry has two levels of current limiting:

- A soft overcurrent limit (overcurrent limit): If the peak current reaches the typical overcurrent limit, the switcher will start a cycle-by-cycle operation to limit the current and

a 10 ms current limit timer starts. The switcher will stay in this mode of operation until one of the following occurs:

- The current is reduced back to the normal level inside the 10 ms timer and in this case normal operation is gained back
- The output reaches the thermal shutdown limit and turns off
- The current limit timer expires without gaining normal operation at which point the output turns off. Then only for GrpB, at the end of a timeout period of 10 ms, the output will attempt to restart again but for one time only.
- The output current keeps increasing until it reaches the second overcurrent limit, see below for more details
- A hard overcurrent limit (short circuit limit) that is higher than the cycle by cycle limit at which the device reacts by shutting down the output immediately. This is necessary to prevent damage in case of a short-circuit. After that, only GrpB will attempt a one time retry after a timeout period of 10ms and will go through a new soft start cycle

## OUTPUT OVERVOLTAGE/UNDERVOLTAGE MONITORING

In the case of an output overvoltage/undervoltage, the user has two options that can be programmed through the I2C interface:

Response A: The output will switch off automatically and the 34704 would alert the processor through I2C that such an event happened.

Response B: The output will not switch off. Rather the 34704 communicates to the processor that an overvoltage/undervoltage condition has occurred and wait for the

processor decision to either shutoff or not, in the mean time the control loop will try to fix itself.

To avoid erroneous conditions, a 20  $\mu$ s filter will be implemented.

The OV/UV fault flag is masked during DVS until DVSSTAT flag is asserted "Done".

To keep the  $\overline{\text{RST}}$  output low during ramp up and until the soft start is done, the OV/UV protection is masked from reporting that the output is in regulation.

## LOGIC COMMANDS AND REGISTERS

### I<sup>2</sup>C USER INTERFACE

The 34704 communicates via I<sup>2</sup>C using a default device address \$54 to access all user registers and program all regulators features independently. Physical address is in a 7-bit format. The extra bit to complete the 8-bit indicates the

reading or writing mode as shown in [Figure 7](#) and [Figure 8](#). After each byte read or sent, the MC34704 answers with an Acknowledge bit, indicating the bite was transferred successfully.

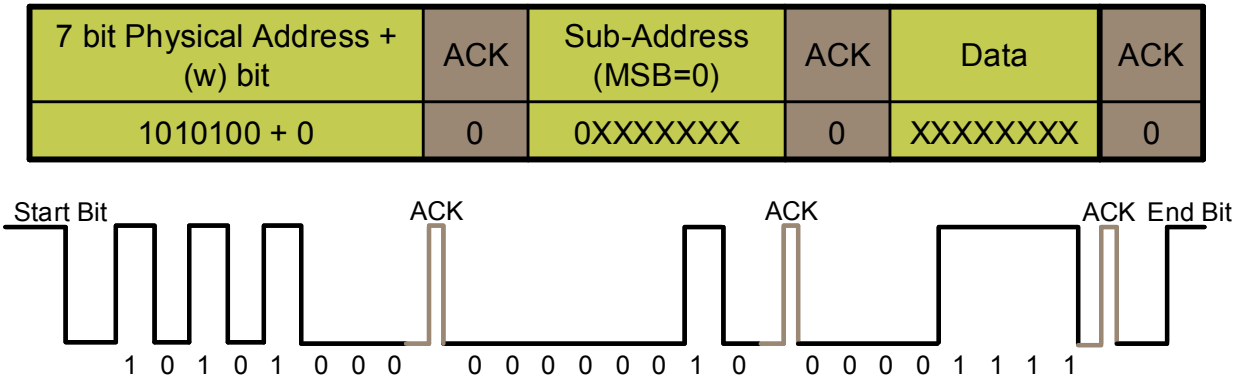


Figure 7. Writing sequence I<sup>2</sup>C bit stream

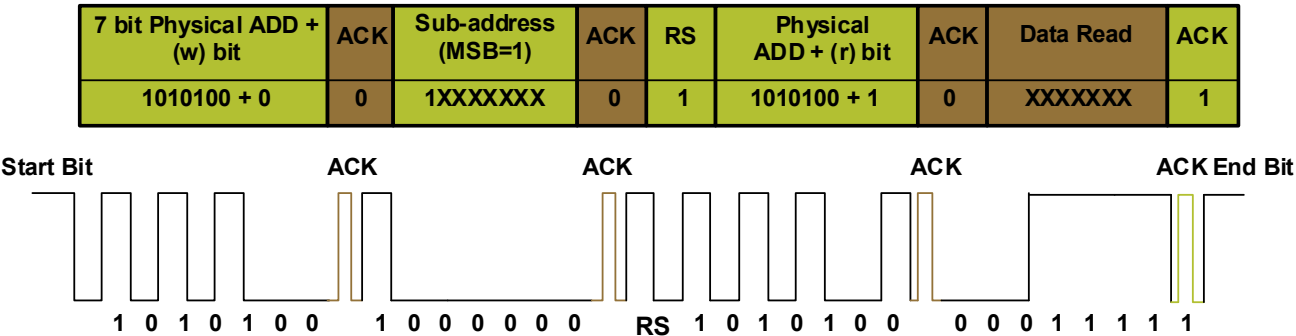


Figure 8. Reading sequence I<sup>2</sup>C bit stream

### USER PROGRAMMABLE REGISTERS

#### GrpC/E power sequencing setting (34704A Only)

The microprocessor can choose one of several voltage sequence options for the GrpC/E supply (REG5), high voltage supply (REG6), and negative voltage supply (REG7). For 3 of the sequencing options, REG5 supply is controlled

and tied with REG6 and REG7 in a preset power sequence. By default, only REG6 and REG7 are involved in the power sequence and REG5 is independently controlled with GrpE.

34704A assigns 2 bits to program the GrpC/E power sequencing options (*CCDSEQ[1:0]*). These bits value is latched in at GrpC power up and will not be allowed to change unless a power recycle happens.

| OPTION         | MSB | LSB | GRPC/E ENABLED                                                      | GRPC/E DISABLED                                                      |
|----------------|-----|-----|---------------------------------------------------------------------|----------------------------------------------------------------------|
| 1<br>(Default) | 0   | 0   | REG5 is independently controlled<br>REG6 and REG7 ramp up together. | REG5 is independently controlled<br>REG6 and REG7 ramp down together |

| OPTION | MSB | LSB | GRPC/E ENABLED                                             | GRPC/E DISABLED                                                 |
|--------|-----|-----|------------------------------------------------------------|-----------------------------------------------------------------|
| 2      | 0   | 1   | REG5 ramps up first<br>Then REG6 and REG7 ramp up together | REG5, REG6 and REG7 ramp down together                          |
| 3      | 1   | 0   | REG5, REG6, and REG7 ramp up together                      | REG5, REG6, and REG7 ramp down together                         |
| 4      | 1   | 1   | REG5 and REG6 ramp up together first.<br>Then ramp up REG7 | REG7 ramps down first.<br>Then REG5 and REG6 ramp down together |

### Switching frequency for REG6, 7 & 8

$F_{SW2}$  can be selected to be between 250 kHz and 1.0 MHz in 250 kHz steps. On the 34704B, FSW2 is just for REG8 since REG6 and 7 do not exist in this device.

34704 assigns 2 bits to program  $F_{SW2}$  ( $F_{SW2}[1:0]$ )

| FSW2             | MSB | LSB |
|------------------|-----|-----|
| 500kHz (Default) | 0   | 0   |
| 250kHz           | 0   | 1   |
| 750kHz           | 1   | 0   |
| 1000kHz          | 1   | 1   |

### Shutdown Hold (Delay) Time

The 34704 assigns 2 bits ( $SDDELAY[1:0]$ ) for the processor to program the shutdown delay time period

| Shutdown Delay   | MSB | LSB |
|------------------|-----|-----|
| 1.0sec (Default) | 0   | 0   |
| 0.5sec           | 0   | 1   |
| 1.5sec           | 1   | 0   |
| 2.0sec           | 1   | 1   |

Please refer to the /ONOFF pin description for more details

### Programming 34704 response to undervoltage/ overvoltage conditions on each regulator

There are two responses that can be programmed for an overvoltage/undervoltage condition:

**Response A:** When an overvoltage (undervoltage) event is detected, the concerned output shuts down and a register is flagged to alert the processor.

**Response B:** When an overvoltage/undervoltage event is detected, the concerned output will not shutdown, but the register is flagged to alert the processor. Then, the processor

can decide whether to shutdown the output or not. In the mean time, the concerned output control loop will be attempting to correct the error.

See [Output Overvoltage/Undervoltage Monitoring on page 30](#) for more details.

Response A and Response B share the same flag bit

34704 assigns 1 bit for this function ( $OVUVSETx$ ) where x corresponds to each regulator.

| OV/UV Response | bit |
|----------------|-----|
| A (Default)    | 0   |
| B              | 1   |

### Dynamic Voltage Scaling for each regulator

The customer can adjust each regulator's output dynamically with 2.5% step size. The total range of adjustability will vary depending on each regulator to accommodate different operating environments. Some regulators will utilize the full range of -20.00% to +17.50% and some regulators will only use the range of  $\pm 10.00\%$ . For details, see each regulator's section. Each 2.5% step takes 50  $\mu$ s before moving to the next step. REG8 only performs DVS when in voltage regulation mode.

During DVS, the Overvoltage and Undervoltage monitoring will not be active. In addition to that, these faults will be masked and not active for a DVS settling time period equal to 1ms. This DVS settling time will start after the DVSSTAT register is flagged indicating that the DVS cycle is done. This is to ensure that during DVS and soft start alike the output will not be tripped due to a momentary overvoltage or undervoltage fault. This is the same for Response A and Response B of the overvoltage/undervoltage fault monitoring.

34704 assigns 4 bits register to program the Dynamic Voltage Scaling for each regulator ( $DVSSETx[3:0]$ ) where x corresponds to each regulator.

| Percentage Change | MSB |   |   | LSB |
|-------------------|-----|---|---|-----|
| 0.00% (Default)   | 0   | 0 | 0 | 0   |
| +2.50%            | 0   | 0 | 0 | 1   |
| +5.00%            | 0   | 0 | 1 | 0   |
| +7.50%            | 0   | 0 | 1 | 1   |
| +10.00%           | 0   | 1 | 0 | 0   |
| +12.50%           | 0   | 1 | 0 | 1   |
| +15.00%           | 0   | 1 | 1 | 0   |
| +17.50%           | 0   | 1 | 1 | 1   |
| -20.00%           | 1   | 0 | 0 | 0   |
| -17.50%           | 1   | 0 | 0 | 1   |
| -15.00%           | 1   | 0 | 1 | 0   |
| -12.50%           | 1   | 0 | 1 | 1   |
| -10.00%           | 1   | 1 | 0 | 0   |
| -7.50%            | 1   | 1 | 0 | 1   |
| -5.00%            | 1   | 1 | 1 | 0   |
| -2.50%            | 1   | 1 | 1 | 1   |

#### On/Off Control for each group of regulators as defined previously and for the whole IC

34704 assigns 1 bit per group to turn each group on/off (ONOFFA, C, D, or E bits). Please note that GrpB does not have a dedicated enable register which is enabled by default.

| GrpA, C, D, or E ONOFF | bit |
|------------------------|-----|
| OFF (Default)          | 0   |
| ON                     | 1   |

Also, 34704 assigns 1 bit (ALLOFF) for disabling the whole IC through the I<sup>2</sup>C. (ALLOFF bit)

| ALL OFF         | bit |
|-----------------|-----|
| False (Default) | 0   |
| True            | 1   |

#### Soft Start Time

There are two set of bits for setting the soft start value for all of the regulators except REG1. The SSTM[1:0] bits reads the soft start value set by the SS pin and is used to initially set the soft start value for all of the regulators except REG1. Then, the SSSET bits for REG5 through REG8 can be used to change the soft start value for these regulators from the value set by the SSTM.

Here is how the SSTM bits interacts with the SSSETx register bits:

1. SSTM is set by a value read through the SS pin.
2. SSTM is copied into the bits SSSET5, SSSET6, SSSET7, and SSSET8.
3. The soft start time of REG2, REG3, and REG4 are only affected by the value of SSTM bits.
4. The soft start time of REG5, REG6, REG7, and REG8 are affected by the value of bits SSSET5, SSSET6, SSSET7, and SSSET8 respectively.

34704 assigns 2 bits to store the value programmed by the SS pin. Bits SSTM[1:0] can only be read by the user.

| Soft Start | MSB | LSB |
|------------|-----|-----|
| 0.5ms      | 0   | 0   |
| 2ms        | 0   | 1   |
| 8ms        | 1   | 0   |
| 32ms       | 1   | 1   |

34704 assigns 2 bits for REG5 through REG8 to program the soft start times for these regulators (SSSETx[1:0]) where x corresponds to each regulator from REG5 through REG8.

| Soft Start | MSB | LSB |
|------------|-----|-----|
| 0.5ms      | 0   | 0   |
| 2ms        | 0   | 1   |
| 8ms        | 1   | 0   |
| 32ms       | 1   | 1   |

#### REG8 Regulation Mode

The 34704 assigns 1 bit to indicate REG8's regulation mode (REG8MODE). The processor assigns this bit to either regulation mode before enabling the REG8 output.

| REG8 Regulation   | bit |
|-------------------|-----|
| Current (Default) | 0   |
| Voltage           | 1   |

#### When REG8 is current regulated, LED backlight current can be reduced from the maximum in 16 steps through the I<sup>2</sup>C interface

The maximum LED current can be set using the external resistor at the bottom of the LED string, then through I<sup>2</sup>C programming, this current value can be reduced in 16 steps.

34704 assigns 4 bits for this function (ILED[3:0])

The ILED setting is not a guaranteed characteristic from I<sub>MAX</sub>\* (1/16) to I<sub>MAX</sub>\* (9/16), due to an error amp common mode limitation.

| LED Current         | MSB |   |   | LSB |
|---------------------|-----|---|---|-----|
| $I_{MAX} * (1/16)$  | 0   | 0 | 0 | 0   |
| $I_{MAX} * (2/16)$  | 0   | 0 | 0 | 1   |
| $I_{MAX} * (3/16)$  | 0   | 0 | 1 | 0   |
| $I_{MAX} * (4/16)$  | 0   | 0 | 1 | 1   |
| $I_{MAX} * (5/16)$  | 0   | 1 | 0 | 0   |
| $I_{MAX} * (6/16)$  | 0   | 1 | 0 | 1   |
| $I_{MAX} * (7/16)$  | 0   | 1 | 1 | 0   |
| $I_{MAX} * (8/16)$  | 0   | 1 | 1 | 1   |
| $I_{MAX} * (9/16)$  | 1   | 0 | 0 | 0   |
| $I_{MAX} * (10/16)$ | 1   | 0 | 0 | 1   |
| $I_{MAX} * (11/16)$ | 1   | 0 | 1 | 0   |
| $I_{MAX} * (12/16)$ | 1   | 0 | 1 | 1   |
| $I_{MAX} * (13/16)$ | 1   | 1 | 0 | 0   |
| $I_{MAX} * (14/16)$ | 1   | 1 | 0 | 1   |
| $I_{MAX} * (15/16)$ | 1   | 1 | 1 | 0   |
| $I_{MAX}$ (Default) | 1   | 1 | 1 | 1   |

## ACCURATE I<sup>2</sup>C COMMUNICATION MODE

The 34704 assigns 1 bit to enable the Accurate I<sup>2</sup>C communication mode (ACCURATE). Setting this bit enables the Accurate mode in which each command and data should be sent 2 times to avoid false commands.

## USER ACCESSIBLE FLAG REGISTERS

### Cold Start Flag

The 34704 assigns 1 bit (*COLD*) to flag the processor that the power up was a result of battery insertion and not through *ONOFF* pin. This flag should be cleared after power up by the processor.

| Cold Start Flag   | bit |
|-------------------|-----|
| /ONOFF (Default)  | 0   |
| Battery Insertion | 1   |

### Shutdown Flag

The 34704 assigns 1 bit (*SHUTDOWN*) to flag the processor if a shutdown signal is received through the *ONOFF* pin and a programmable time period with a default of 1sec has elapsed.

| /ONOFF Status    | bit |
|------------------|-----|
| Normal (Default) | 0   |
| Shutdown         | 1   |

## Dynamic Voltage Scaling Status Flag

In addition and for each regulator, 34704 assigns 1 bit (*DVSSTATx*) to flag to the processor that the desired output voltage level set with the *DVSSETx* bits has been reached.

| DVS STATUS   | bit |
|--------------|-----|
| DVS Not Done | 0   |
| DVS Done     | 1   |

## USER ACCESSIBLE FAULT REGISTERS

### Overcurrent Fault Register

The 34704 assigns 1 bit for each regulator (*ILIMFx*) to indicate a fault due to overcurrent limit, where x corresponds to each regulator from REG1 to REG8, except REG7

| ILIMF | bit |
|-------|-----|
| False | 0   |
| True  | 1   |

### Short-circuit Fault Register

The 34704 assigns 1 bit for each regulator (*SCFx*) to indicate a fault due to short-circuit current limit, where x corresponds to each regulator from REG1 to REG8, except REG7

| SCF   | bit |
|-------|-----|
| False | 0   |
| True  | 1   |

### Overvoltage Fault Register

The 34704 assigns 1 bit for each regulator (*OVFx*) to indicate a fault due to overvoltage limit, where x corresponds to each regulator from REG1 to REG8

| OVF   | bit |
|-------|-----|
| False | 0   |
| True  | 1   |

### Undervoltage Fault Register

The 34704 assigns 1 bit for each regulator (*UVFx*) to indicate a fault due to undervoltage limit, where x corresponds to each regulator from REG1 to REG8.

| UVF   | bit |
|-------|-----|
| False | 0   |
| True  | 1   |

### Thermal Shutdown Fault Register

The 34704 assigns 1 bit for each regulator (*TSDFx*) to indicate a fault due to thermal limit, where x corresponds to each regulator from REG1 to REG8, except REG7

| TSDf  | bit |
|-------|-----|
| False | 0   |
| True  | 1   |

#### Regulator Fault Register

The 34704 assigns 1 bit for each regulator (*FAULTx*) to indicate that a fault had occurred on each regulator. The processor can just access this register periodically to determine system status. This reduces the access cycles. If a regulator fault register asserted, then the processor can access that regulator's registers to see what kind of fault had occurred.

| FAULT | bit |
|-------|-----|
| False | 0   |
| True  | 1   |

### SPECIAL REGISTERS

#### REG3 Fine Voltage Scaling Register

Regulator 3 has an additional fine output voltage scaling that enables to lower the output voltage in 0.5% steps. The 34704 assigns an 8-bit register (REG3DAC) to the REG3 Digital to analog converter for the FB3 voltage generation. Output voltage must be reduced gradually to avoid a OV/UV fault to occur.

#### REG7 Independent ON/OFF Control (Only on 34704A)

The 34704B provide two register to independently turn on REG7 when REG6 is not needed. Care must be taken when turning on REG7 to avoid inrush currents during regulator ramp-up. Following Process must be followed to assure successful turn on of REG7.

1. Set EN0 and clear DISCHR\_B on REG7CR0 register
2. After 1ms or more, set EN1 on REG7CR0 register
3. Set REG7DAC register to \$00
4. Gradually shift up REG7DAC register from \$00 to \$D9 to ramp-up the output voltage in a soft-start like wave. Soft start timing is dependant of I2C communication speed and number of bit you change per writing, for instance use 4,8 or 16 bits increase to ramp up the output voltage.

|     | Register Address | Code |
|-----|------------------|------|
| 1   | \$58             | \$50 |
| 2   | \$58             | \$D0 |
| 3   | \$59             | \$00 |
| 4   | \$59             | \$04 |
| 5   | \$59             | \$08 |
| 6   | \$59             | \$0C |
| ... | ...              | ...  |
| 55  | \$59             | \$D9 |

REG7 independent start up example

### REGISTER DESCRIPTION SUMMARY TABLE

| Register | ADDR | R/W | Bit Name | Bits | Description                                       |
|----------|------|-----|----------|------|---------------------------------------------------|
| GENERAL1 | \$01 | R/W | CCDSEQ   | 1:0  | GrpC/E power sequence selection                   |
|          |      |     | SDDELAY  | 3:2  | Hard shutdown delay timer selection               |
| GENERAL2 | \$02 | R/W | ONOFFx   | 3:0  | GrpA,C,D,E On/off bits                            |
|          |      |     | ALLOFF   | 4    | Soft shutdown bit (turn off all regulators)       |
| GENERAL3 | \$03 | R   | SSTIME   | 1:0  | Soft start configuration latch                    |
|          |      | R/W | COLDF    | 3    | Cold power up detection flag                      |
|          |      | R/W | SHTD     | 4    | Hard Shutdown detection flag                      |
| VGSET1   | \$04 | R/W | OVUVSET1 | 0    | Set REG1/VG response type to OV/UV                |
|          |      | R/W | DVSSET1  | 4:1  | REG1 DVS value setting                            |
| VGSET2   | \$05 | R   | DVSSTAT1 | 0    | DVS voltage level status flag                     |
|          |      | R   | -        | 5:1  | REG1 fault flags: Thermal SD, SC, ILim, UV and OV |
| REG2SET1 | \$06 | R/W | OVUVSET2 | 0    | Set REG2 response type to OV/UV                   |
|          |      | R/W | DVSSET2  | 4:1  | REG2 DVS value setting                            |

| Register | ADDR | R/W | Bit Name          | Bits | Description                                                       |
|----------|------|-----|-------------------|------|-------------------------------------------------------------------|
| REG2SET2 | \$07 | R   | DVSSTAT2          | 0    | DVS voltage level status flag                                     |
|          |      | R   | -                 | 5:1  | REG2 fault flags: Thermal SD, SC, ILim, UV and OV                 |
| REG3SET1 | \$08 | R/W | OVUVSET3          | 0    | Set REG3 response type to OV/UV                                   |
|          |      | R/W | DVSSET3           | 4:1  | REG3 DVS value setting                                            |
| REG3SET2 | \$09 | R   | DVSSTAT3          | 0    | DVS voltage level status flag                                     |
|          |      | R   | -                 | 5:1  | REG3 fault flags: Thermal SD, SC, ILim, UV and OV                 |
| REG4SET1 | \$0A | R/W | OVUVSET4          | 0    | Set REG4 response type to OV/UV                                   |
|          |      | R/W | DVSSET4           | 4:1  | REG4 DVS value setting                                            |
| REG4SET2 | \$0B | R   | DVSSTAT4          | 0    | DVS voltage level status flag                                     |
|          |      | R   | -                 | 5:1  | REG4 fault flags: Thermal SD, SC, ILim, UV and OV                 |
| REG5SET1 | \$0C | R/W | OVUVSET5          | 0    | Set REG5 response type to OV/UV                                   |
|          |      | R/W | DVSSET5           | 4:1  | REG5 DVS value setting                                            |
| REG5SET2 | \$0D | R/W | SSSET5            | 1:0  | REG5 Soft Start setting.                                          |
| REG5SET3 | \$0E | R   | DVSSTAT5          | 0    | DVS voltage level status flag                                     |
|          |      | R   | -                 | 5:1  | REG5 fault flags: Thermal SD, SC, ILim, UV and OV                 |
| REG6SET1 | \$0F | R/W | OVUVSET6          | 0    | Set REG6 response type to OV/UV                                   |
|          |      | R/W | DVSSET6           | 4:1  | REG6 DVS value setting                                            |
| REG6SET2 | \$10 | R/W | SSSET6            | 1:0  | REG6 Soft Start setting.                                          |
| REG6SET3 | \$11 | R   | DVSSTAT6          | 0    | DVS voltage level status flag                                     |
|          |      | R   | -                 | 5:1  | REG6 fault flags: Thermal SD, SC, ILim, UV and OV                 |
| REG7SET1 | \$12 | R/W | OVUVSET7          | 0    | Set REG7 response type to OV/UV                                   |
|          |      | R/W | DVSSET7           | 4:1  | REG7 DVS value setting                                            |
| REG7SET2 | \$13 | R/W | SSSET7            | 1:0  | REG7 Soft Start setting.                                          |
|          |      | R/W | FSW2              | 3:2  | REG6, 7 8, Frequency setting                                      |
| REG7SET3 | \$14 | R   | DVSSTAT7          | 0    | DVS voltage level status flag                                     |
|          |      | R   | -                 | 2:1  | REG7 fault flags: UV and OV                                       |
| REG8SET1 | \$15 | R/W | OVUVSET8          | 0    | Set REG8 response type to OV/UV                                   |
|          |      | R/W | DVSSET8           | 4:1  | REG8 DVS value setting                                            |
| REG8SET2 | \$16 | R/W | SSSET8            | 1:0  | REG8 Soft Start setting.                                          |
|          |      | R/W | REG8MODE          | 3:2  | Voltage or Current Regulation mode on REG8                        |
|          |      | R/W | ILED              | 6:4  | LED string current configuration during current regulation mode   |
| REG8SET3 | \$17 | R   | DVSSTAT8          | 0    | DVS voltage level status flag                                     |
|          |      | R   | -                 | 5:1  | REG8 fault flags: Thermal SD, SC, ILim, UV and OV                 |
| FAULTS   | \$18 | R   | FLT <sub>x</sub>  | 7:0  | First Level fault register for REG1 through REG8                  |
| I2CSET1  | \$19 | R/W | ACCURATE          | 0    | Accurate I2C communication mode enable                            |
| REG3DAC  | \$49 | R/W | 3DAC <sub>x</sub> | 7:0  | REG3 DAC reference voltage configuration for Fine voltage Scaling |
| REG7CR0  | \$58 | R/W | DISCHG_B          | 4    | Discharge enable for independent REG7 Control                     |
|          |      | R/W | EN                | 7:6  | Output Enable bits for Independent REG7 Control                   |
| REG7DAC  | \$59 | R/W | 7DAC <sub>x</sub> | 7:0  | REG7 DAC refence voltage configuration for REG7 Control           |

## I<sup>2</sup>C REGISTER DISTRIBUTION

Each regulator has a fault register that records any fault that occurs in that regulator. Then there is a regulator fault reporting register that the processor can access at all times to see if any fault had occurred.

There are also the IC general use registers. Those registers are also split between status reporting registers and processor programmable registers.

This distribution keeps each regulator's registers bundled together which makes it easier for the user to access one regulator at a time.

| Addr | Name     | D7      | D6        | D5    | D4           | D3           | D2       | D1          | D0       |          |
|------|----------|---------|-----------|-------|--------------|--------------|----------|-------------|----------|----------|
| \$00 | Reserved | -       |           |       |              |              |          |             |          |          |
| \$01 | GENERAL1 | -       |           |       |              | SDDELAY[1:0] |          | CCDSEQ[1:0] |          |          |
| \$02 | GENERAL2 | -       |           |       | ALLOFF       | ONOFFA       | ONOFFC   | ONOFFD      | ONOFFE   |          |
| \$03 | GENERAL3 | -       |           |       | SHTD         | COLDF        | -        | SSTIME[1:0] |          |          |
| \$04 | VGSET1   | -       |           |       | DVSSET1[3:0] |              |          |             |          | OVUVSET1 |
| \$05 | VGSET2   | -       |           | TSDF1 | SCF1         | ILIMF1       | UVF1     | OVF1        | DVSSTAT1 |          |
| \$06 | REG2SET1 | -       |           |       | DVSSET2[3:0] |              |          |             |          | OVUVSET2 |
| \$07 | REG2SET2 | -       |           | TSDF2 | SCF2         | ILIMF2       | UVF2     | OVF2        | DVSSTAT2 |          |
| \$08 | REG3SET1 | -       |           |       | DVSSET3[3:0] |              |          |             |          | OVUVSET3 |
| \$09 | REG3SET2 | -       |           | TSDF3 | SCF3         | ILIMF3       | UVF3     | OVF3        | DVSSTAT3 |          |
| \$0A | REG4SET1 | -       |           |       | DVSSET4[3:0] |              |          |             |          | OVUVSET4 |
| \$0B | REG4SET2 | -       |           | TSDF4 | SCF4         | ILIMF4       | UVF4     | OVF4        | DVSSTAT4 |          |
| \$0C | REG5SET1 | -       |           |       | DVSSET5[3:0] |              |          |             |          | OVUVSET5 |
| \$0D | REG5SET2 | -       |           |       |              |              |          | SSSET5[1:0] |          |          |
| \$0E | REG5SET3 | -       |           | TSDF5 | SCF5         | ILIMF5       | UVF5     | OVF5        | DVSSTAT5 |          |
| \$0F | REG6SET1 | -       |           |       | DVSSET6[3:0] |              |          |             |          | OVUVSET6 |
| \$10 | REG6SET2 | -       |           |       |              |              |          | SSSET6[1:0] |          |          |
| \$11 | REG6SET3 | -       |           | TSDF6 | SCF6         | ILIMF6       | UVF6     | OVF6        | DVSSTAT6 |          |
| \$12 | REG7SET1 | -       |           |       | DVSSET7[3:0] |              |          |             |          | OVUVSET7 |
| \$13 | REG7SET2 | -       |           |       |              | FSW2[1:0]    |          | SSSET7[1:0] |          |          |
| \$14 | REG7SET3 | -       |           |       |              |              | UVF7     | OVF7        | DVSSTAT7 |          |
| \$15 | REG8SET1 | -       |           |       | DVSSET8[3:0] |              |          |             |          | OVUVSET8 |
| \$16 | REG8SET2 | -       | ILED[3:0] |       |              |              | REG8MODE | SSSET8[1:0] |          |          |
| \$17 | REG8SET3 | -       |           | TSDF8 | SCF8         | ILIMF8       | UVF8     | OVF8        | DVSSTAT8 |          |
| \$18 | FAULTS   | FLT8    | FLT7      | FLT6  | FLT5         | FLT4         | FLT3     | FLT2        | FLT1     |          |
| \$19 | I2CSET1  | -       |           |       |              |              |          |             |          | ACCURATE |
| \$49 | REG3DAC  | 3DAC7   | 3DAC6     | 3DAC5 | 3DAC4        | 3DAC3        | 3DAC2    | 3DAC1       | 3DAC0    |          |
| \$58 | REG7CR0  | EN[1:0] |           | -     | DISCHG_B     | -            |          |             |          |          |
| \$59 | REG7DAC  | 7DAC7   | 7DAC6     | 7DAC5 | 7DAC4        | 7DAC3        | 7DAC2    | 7DAC1       | 7DAC0    |          |

34704A Register Distribution Map

| Addr      | Name     | D7   | D6        | D5    | D4           | D3           | D2       | D1          | D0       |
|-----------|----------|------|-----------|-------|--------------|--------------|----------|-------------|----------|
| \$00      | Reserved | -    |           |       |              |              |          |             |          |
| \$01      | GENERAL1 | -    |           |       |              | SDDELAY[1:0] |          | -           |          |
| \$02      | GENERAL2 | -    |           |       | ALLOFF       | -            | -        | ONOFFD      | ONOFFE   |
| \$03      | GENERAL3 | -    |           |       | SHTD         | COLDF        | -        | SSTIME[1:0] |          |
| \$04      | Reserved | -    |           |       |              |              |          |             |          |
| \$05      | VGSET2   | -    | -         | -     | -            | UVF1         | OVF1     | -           |          |
| \$06      | REG2SET1 | -    |           |       | DVSSET2[3:0] |              |          |             | OVUVSET2 |
| \$07      | REG2SET2 | -    | TSDF2     | SCF2  | ILIMF2       | UVF2         | OVF2     | DVSSTAT2    |          |
| \$08      | REG3SET1 | -    |           |       | DVSSET3[3:0] |              |          |             | OVUVSET3 |
| \$09      | REG3SET2 | -    | TSDF3     | SCF3  | ILIMF3       | UVF3         | OVF3     | DVSSTAT3    |          |
| \$0A      | REG4SET1 | -    |           |       | DVSSET4[3:0] |              |          |             | OVUVSET4 |
| \$0B      | REG4SET2 | -    | TSDF4     | SCF4  | ILIMF4       | UVF4         | OVF4     | DVSSTAT4    |          |
| \$0C      | REG5SET1 | -    |           |       | DVSSET5[3:0] |              |          |             | OVUVSET5 |
| \$0D      | REG5SET2 | -    |           |       |              |              |          | SSSET5[1:0] |          |
| \$0E      | REG5SET3 | -    | TSDF5     | SCF5  | ILIMF5       | UVF5         | OVF5     | DVSSTAT5    |          |
| \$0F-\$12 | Reserved | -    |           |       |              |              |          |             |          |
| \$13      | FSW2SET  | -    |           |       |              | FSW2[1:2]    |          | -           |          |
| \$14      | Reserved | -    |           |       |              |              |          |             |          |
| \$15      | REG8SET1 | -    |           |       | DVSSET8[3:0] |              |          |             | OVUVSET8 |
| \$16      | REG8SET2 | -    | ILED[3:0] |       |              |              | REG8MODE | SSSET8[1:0] |          |
| \$17      | REG8SET3 | -    |           | TSDF8 | SCF8         | ILIMF8       | UVF8     | OVF8        | DVSSTAT8 |
| \$18      | FAULTS   | FLT8 | -         | -     | FLT5         | FLT4         | FLT3     | FLT2        | FLT1     |
| \$19      | I2CSET1  | -    |           |       |              |              |          |             | ACCURATE |
| \$49      | REG3DAC  | DAC7 | DAC6      | DAC5  | DAC4         | DAC3         | DAC2     | DAC1        | DAC0     |

34704B Register Distribution Map

## COMPONENT CALCULATION

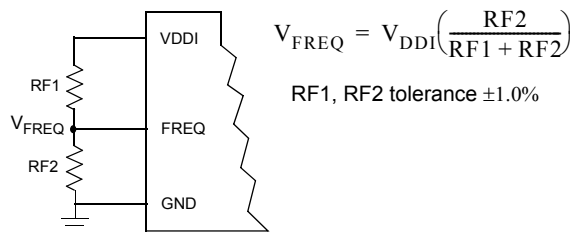
### F<sub>SW1</sub> AND GENERAL SOFT START CONFIGURATION

The 34704 uses F<sub>SW1</sub> as the switching frequency for REG1(VG) thru REG5, and this can be changed by applying a voltage between 0 to 2.5 V to the FREQ pin. If the FREQ pin is left unconnected, the 34704 starts up with a default frequency of 750 KHz. To configure the F<sub>SW1</sub>, use a 2 resistors voltage divider from VDDI to ground to set the voltage on the FREQ pin as indicated below:

| Ratio | F <sub>SW1</sub> [KHz] |
|-------|------------------------|
| 0     | 750                    |
| 9/32  | 1000                   |
| 13/32 | 1250                   |
| 17/32 | 1500                   |
| 21/32 | 1750                   |
| VDDI  | 2000                   |

#### Notes

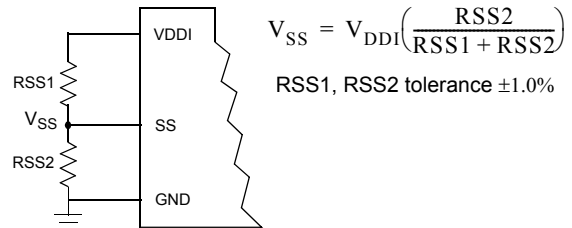
27. If an external voltage is used, F<sub>SW1</sub> can only be set during device startup.



Initially at power up, the soft start time will be set for all of the regulators through programming the SS pin with an external resistor divider connected between VDDI and AGND as follows:

| Ratio | Soft Start timing [ms] |
|-------|------------------------|
| 0     | 0.5                    |
| 11/32 | 2.0                    |
| 19/32 | 8.0                    |
| VDDI  | 32.0                   |

I<sub>DD</sub> max = 100μA



### REGULATORS POWER STAGE AND COMPENSATION CALCULATION

#### Regulator 1 and 6 (Synchronous Boost - internally compensated - REG1 is VG supply).

REG1 is a Synchronous Boost converter set to 5.0 V and Maximum current of 500 mA while REG6 is set to 15 V at 60 mA (on the 34704B, REG1 does not exist but similar circuitry is used to provide the internal VG voltage). They do not need an external compensation network, thus, the only components that need to be calculated are:

- **R1 and RB (Only REG6):** These two resistors help to set the output voltage to the desire value using a Vref=0.6 V, select R1 between 10 k and 100 K and then calculate RB as follows:

$$RB = \frac{R1}{\frac{Vo}{Vref} - 1} \quad [\Omega]$$

- **L:** A boost power stage can be designed to operate in CCM for load currents above a certain level usually 5 to 15% of full load. The minimum value of inductor to maintain CCM can be determined by using the following procedure:

1. Define  $I_{OB}$  as the minimum current to maintain CCM as 15% of full load.

$$L_{min} \geq \frac{V_o(D)(1-D)^2 T}{2I_{OB}} \quad (H)$$

where: D = Duty cycle  
Vo = Output Voltage  
T = Switching Period  
IOB = Boundary Current to achieve CCM

2. However the worst case condition for the boost power stage is when the input voltage is equal to one half of the output voltage, which results in the Maximum  $\Delta I_L$ , then:

$$L_{min} \geq \frac{V_o(T)}{16I_{OB}} \quad (H)$$

Note: On the 34704B Use the recommended 3.0uH inductor rated between 50 to 100 mA in order to have this regulator working in DCM. Rising the inductor value will make the regulator to begin working in CCM.

- **C<sub>OUT</sub>**: The three elements of output capacitor that contribute to its impedance and output voltage ripple are the ESR, the ESL and the capacitance C. The minimum capacitor value is approximately:

$$C_{OUT} \geq \frac{I_{o_{max}} D_{max}}{F_{sw} \Delta V_{O_r}} \quad (F)$$

where: Dmax = Maximum Duty cycle  
FSW = Switching Frequency

- Where  $\Delta V_{O_r}$  is the desired output voltage ripple.
- Now calculate the maximum allowed ESR to reach the desired  $\Delta V_{O_r}$ .

$$ESR \leq \frac{\Delta V_{O_r}}{\left( \frac{I_{o_{max}}}{1-D_{max}} + I_{OB} \right)} \quad [\Omega]$$

- **1CVG (Only Reg1)**: Use a 47uF capacitor from Ground to VG.
- **D1 (Only Reg1)**: Use a fast recovery schottky diode rated to 10V at 1A.

#### Regulator 2, 4 and 5 (Synchronous Buck-Boost regulator with external compensation)

These three regulators are 4-Switch synchronous buck-boost voltage mode control DC-DC regulator that can operate at various output voltage levels. Since each of the

regulators may work as a buck or a boost depending on the operating voltages, they need to be compensated in different ways for each situation.

Since the 34704 is meant to work using a Lilon battery, the operating input voltage range is set from 2.7 - 4.2 V, then the following scenarios are possible:

| Regulator | Vo    | Input voltage range | Operation |
|-----------|-------|---------------------|-----------|
| 2         | 2.8 V | 3.0 - 4.2           | Buck      |
|           | 3.3 V | 2.7 - 3.0           | Boost     |
|           | 3.3 V | 3.5 - 4.2           | Buck      |
| 4         | 1.8 V | 2.7 - 4.2           | Buck      |
|           | 2.5 V | 2.7 - 4.2           | Buck      |
| 5         | 3.3 V | 2.7 - 3.0           | Boost     |
|           | 3.3 V | 3.5 - 4.2           | Buck      |

- NOTE: Since these 3 regulators can work as a buck or a boost in a single application, a good practice to configure these regulators is to compensate for a boost scenario and then verify that the regulator is working in buck mode using that same compensation.

#### Compensating for Buck operation:

- **L**: A buck power stage can be designed to operate in CCM for load currents above a certain level usually 5 to 15% of full load. The minimum value of inductor to maintain CCM can be determined by using the following procedure:
  1. Define  $I_{OB}$  as the minimum current to maintain CCM between 10 to 15% of full load.

$$L_{min} \geq \frac{(V_o + I_{o_{max}}(R_{DS(ON)SFET} + R_L)D'_{min})T}{2I_{OB}} \approx D'_{MAX} T \frac{V_o}{2I_{OB}} \quad [H]$$

where: RDS(ON)SFET = Body Resistance of the Lowside Fet  
RL = Inductor Winding Resistance  
D'Min = Minimum Off Percentage given by 1- (Vin\_min/Vout\_max)  
D'max = Maximum Off Percentage given by 1- (Vin\_max/Vout\_min)

- **C<sub>OUT</sub>**: The three elements of output capacitor that contribute to its impedance and output voltage ripple are the ESR, the ESL and the capacitance C. A good approach to calculate the minimum real capacitance needed is to include the transient response analysis to control the maximum overshoot as desired.

1. First calculate the **dt<sub>I</sub>** (inductor current rising time) given by:

$$dtI = \frac{I_{o_{max}} T}{\Delta I_{ostep}} \quad [s]$$

Where the parameter  $\Delta I_{ostep}$  is the maximum current step during the current rising time and is define as:

$$\Delta I_{ostep} = \left( \frac{D_{max}}{F_{sw}} \right) \left( \frac{V_{in_{min}} - V_o}{L} \right) \quad [A]$$

2. Then the output capacitor can be chosen as follow:

$$C_{OUT} \leq \frac{I_{o_{max}} dtI}{\Delta V_{o_{max}}} \quad [A]$$

- Where  $\Delta V_{o_{max}}$  is the maximum allowed transient overshoot expressed as a percentage of the output voltage, typically from 3 to 5% of  $V_o$ .
3. Finally find the maximum allowed ESR to allow the desired transient response:

$$ESR_{max} = \frac{\Delta V_{o_r}(F_{sw})(L)}{V_o(1 - D_{min})} \quad [\Omega]$$

NOTE: Do not use the parameters  $\Delta V_{o_r}$  and  $\Delta V_{o_{max}}$  indistinctly, the first one indicates the output voltage ripple, while the second one is the maximum output voltage overshoot (transient response).

- **R1 and RB:** These two resistors help to set the output voltage to the desire value using a  $V_{ref}=0.6$  V, select R1 between 10 k and 100 K and then calculate RB as follows:

$$RB = \frac{R1}{\frac{V_o}{V_{ref}} - 1} \quad [\Omega]$$

- Compensation network. (C1,C2,C3, R2, R3): For compensating a buck converter, 3 important frequencies referring to the plant are:

1. Output LC filter cutoff frequency ( $F_{LC}$ ):

$$F_{LC} = \frac{1}{2\pi\sqrt{LC_{OUT}}} \quad [Hz]$$

2. Cutoff frequency due to capacitor ESR:

$$F_{ESR} = \frac{1}{2\pi(C_{OUT})ESR} \quad [Hz]$$

3. Crossover frequency (or bandwidth):

$$F_{BW} = \frac{F_{sw}}{10} \quad [Hz]$$

The Type 3 external compensation network will be in charge of canceling some of these poles and zeros to achieve stability in the system. The following poles and zeroes frequencies are provided by the type 3 compensation.

$$F_{PO} = F_{BW} \quad F_{Z1} = 0.9F_{LC} \quad F_{Z2} = 1.1F_{LC}$$

$$F_{P1} = F_{ESR} \quad F_{P2} = \frac{F_{SW}}{2}$$

The passive components associated to these frequencies are calculated with the following formulas.

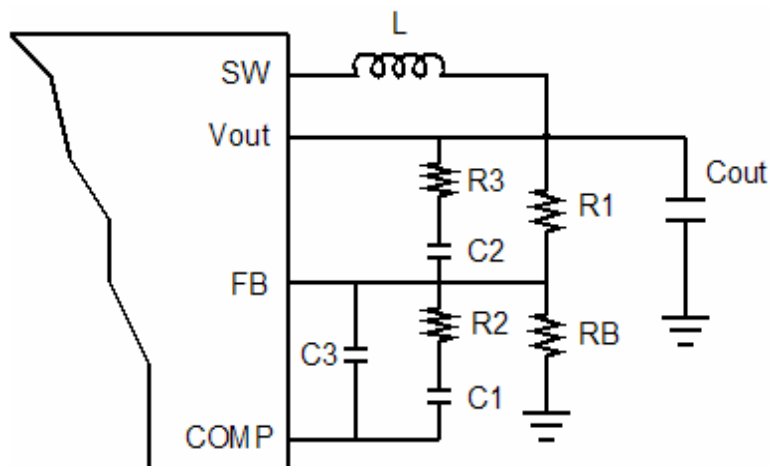
$$C1 = \frac{V_{in_{min}}}{V_{RAMP}} \left( \frac{1}{2\pi(F_{PO}R1)} \right)$$

$$C2 = \left( \frac{1}{2\pi(F_{Z2}R1)} \right)$$

$$R2 = \left( \frac{1}{2\pi(F_{Z1}C1)} \right)$$

$$R3 = \left( \frac{1}{2\pi(F_{P1}C2)} \right)$$

$$C3 = \left( \frac{1}{2\pi(F_{P2}R2)} \right)$$



On the 34704  $V_{RAMP}$  is half of 1.2 V since each operation mode spends only half the ramp.

### Compensating for boost operation:

- **L:** A boost power stage can be designed to operate in CCM for load currents above a certain level usually 5 to 15% of full load. The minimum value of inductor to maintain CCM can be determined by using the following procedure:

1. Define  $I_{OB}$  as the minimum current to maintain CCM between 10 to 15% of full load:

$$L_{min} \geq \frac{V_o(D)(1-D)^2 T}{2I_{OB}} \quad [H]$$

However the worst case condition for the boost power stage is when the input voltage is equal to one half of the output voltage, which results in the Maximum  $\Delta I_L$ , then:

$$L_{min} \geq \frac{V_o(T)}{16I_{OB}} \quad [H]$$

- **C<sub>OUT</sub>:** The three elements of output capacitor that contribute to its impedance and output voltage ripple are the ESR, the ESL and the capacitance C. The minimum capacitor value is approximately:

$$C_{OUT} \geq \frac{I_{o_{max}} D_{max}}{F_{sw} \Delta V_{O_r}} \quad [F]$$

- Where  $\Delta V_{O_r}$  is the desired output voltage ripple.
- Now calculate the maximum allowed ESR to reach the desired  $\Delta V_{O_r}$ :

$$ESR \leq \frac{\Delta V_{O_r}}{\left( \frac{I_{o_{max}}}{1-D_{max}} + I_{OB} \right)} \quad [\Omega]$$

- **R1 and RB:**

These two resistors help to set the output voltage to the desired value using a  $V_{ref}=0.6V$ , select R1 between 10k and 100K and then calculate RB as follows:

$$R_B = \frac{R_1}{\frac{V_o}{V_{REF}} - 1} \quad [\Omega]$$

- Compensation network. (C1,C2,C3, R2, R3)

For compensating a boost converter, 4 important frequencies referring to the plant are:

1. Output LC filter cutoff frequency ( $F_{LC}$ ):

$$F_{LC} = \frac{D'_{min}}{2\pi\sqrt{LC_{OUT}}} \quad [Hz]$$

- Where  $D'_{min}$  is the minimum off time percentage given by:

$$D'_{min} = \frac{V_{in_{min}}}{V_{out_{max}}}$$

2. Cutoff frequency due to capacitor ESR:

$$F_{ESR} = \frac{1}{2\pi(C_{OUT})ESR} \quad [Hz]$$

3. The right plane zero frequency:

$$RHP_Z = \frac{(D'_{min})^2 R_{LOAD}}{2\pi L} \quad [Hz]$$

4. Crossover frequency (or bandwidth): select this frequency as far away from the  $RHP_Z$  as much as possible:

$$F_{BW} \ll \frac{RHP_Z}{6} \quad [Hz]$$

The Type 3 external compensation network will be in charge of canceling some of these poles and zeros to achieve stability in the system. The following poles and zeroes frequencies are provided by the type 3 compensation:

$$F_{PO} = F_{BW} \quad F_{Z1} = 0.9F_{LC} \quad F_{22} = 1.1F_{LC}$$

$$F_{P1} = F_{ESR} \quad F_{2P} = \frac{F_{SW}}{2}$$

The passive components associated to these frequencies are calculated with the following formulas

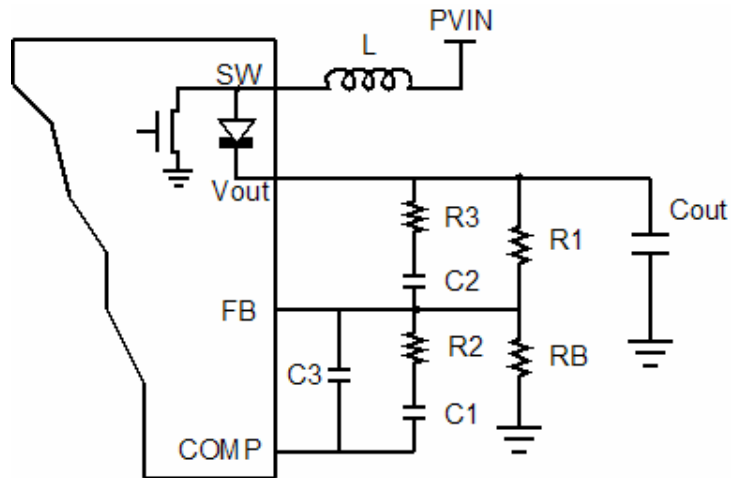
$$C1 = \frac{V_{in_{min}}}{V_{RAMP}} \left( \frac{1}{D'_{min}} \right)^2 \left( \frac{1}{2\pi(F_{PO}R1)} \right)$$

$$C2 = \left( \frac{1}{2\pi(F_{Z2}R1)} \right)$$

$$R2 = \left( \frac{1}{2\pi(F_{Z1}C1)} \right)$$

$$R3 = \left( \frac{1}{2\pi(F_{P1}C2)} \right)$$

$$C3 = \left( \frac{1}{2\pi(F_{P2}R2)} \right)$$



On the 34704  $V_{RAMP}$  is half of 1.2 V since each operation mode spends only half the ramp.

### Regulator 3 (Synchronous Buck - internally compensated)

- **L:** A buck power stage can be designed to operate in CCM for load currents above a certain level usually 5 to 15% of full load. The minimum value of inductor to maintain CCM can be determined by using the following procedure:
  1. Define  $I_{OB}$  as the minimum current to maintain CCM between 10 to 15% of full load.

$$L_{min} \geq \frac{(V_o + I_{o_{max}}(R_{DS(on)LSFET} + R_L)(D'_{min})T}{2I_{OB}}$$

$$L_{min} \geq D'T \frac{V_o}{2I_{OB}} \quad [H]$$

- **C<sub>OUT</sub>:** The three elements of output capacitor that contribute to its impedance and output voltage ripple are the ESR, the ESL and the capacitance C. A good approach to calculate the minimum real capacitance needed is to include the transient response analysis to control the maximum overshoot as desired.

- First calculate the  $dt_I$  (inductor current rising time) given by:

$$dt_I = \frac{I_{o_{max}}T}{\Delta I_{ostep}} \quad [s]$$

Where the parameter  $\Delta I_{ostep}$  is the maximum current step during the current rising time and is define as:

$$\Delta I_{ostep} = \left( \frac{D_{max}}{F_{sw}} \right) \left( \frac{V_{in_{min}} - V_o}{L} \right) \quad [A]$$

- Then the output capacitor can be chosen as follow:

$$C_{OUT} \leq \frac{I_{o_{max}}dt_I}{\Delta V_{o_{max}}} \quad [F]$$

Where  $\Delta V_{o_{max}}$  is the maximum allowed transient overshoot expressed as a percentage of the output voltage, typically from 3 to 5% of  $V_o$ .

- Finally find the maximum allowed ESR to allow the desired transient response:

$$ESR_{max} = \frac{\Delta V_{o_r}(F_{sw})(L)}{V_o(1 - D_{min})} \quad [\Omega]$$

NOTE: do not use the parameters  $\Delta V_{o_r}$  and  $\Delta V_{o_{max}}$  indistinctly, the first one indicates the output voltage ripple, while the second one is the maximum output voltage overshoot (transient response).

- **R1 and RB:** These two resistors help to set the output voltage to the desire value using a  $V_{REF}=0.6$  V, select R1 between 10 k and 100 K and then calculate RB as follows:

$$RB = \frac{R1}{\frac{V_o}{V_{ref}} - 1} \quad [\Omega]$$

### Regulator 8 (Synchronous Boost - internally compensated -Voltage or current feedback)

REG8 is a Synchronous Boost converter set to 15V with a maximum current of 30 mA and can be used with voltage

feedback using the standard voltage divider configuration, or can be programmed to work with a current feedback configuration to control the current flowing through a LED string. It does not need external compensation network, thus the only components that need to be calculated are:

- **L:** A boost power stage can be designed to operate in CCM for load currents above a certain level usually 5 to 15% of full load. The minimum value of inductor to maintain CCM can be determined by using the following procedure:
- Define  $I_{OB}$  between 60 to 80% of the maximum current rating to maintain CCM as 15% of full load:

$$L_{min} \geq \frac{V_o(D)(1-D)^2 T}{2I_{OB}} \quad [H]$$

However the worst case condition for the boost power stage is when the input voltage is equal to one half of the output voltage, which results in the Maximum  $\Delta I_L$ , then:

$$L_{min} \geq \frac{V_o(T)}{16I_{OB}} \quad [H]$$

- **C<sub>OUT</sub>:** The three elements of output capacitor that contribute to its impedance and output voltage ripple are the ESR, the ESL and the capacitance C. The minimum capacitor value is approximately:

$$C_{OUT} \geq \frac{I_{o_{max}} D_{max}}{F_{sw} \Delta V_{O_r}} \quad [F]$$

- Where  $\Delta V_{O_r}$  is the desired output voltage ripple.
- Now calculate  $\Delta V_{O_r}$  the maximum allowed ESR to reach the desired.

$$ESR \leq \frac{\Delta V_{O_r}}{\left( \frac{I_{o_{max}}}{1-D_{max}} + I_{OB} \right)} \quad [\Omega]$$

- **R1 and RB (for Voltage feedback control):** These two resistors help to set the output voltage to the desired value using a  $V_{REF}=0.6$  V, select R1 between 10k and 100K and then calculate RB as follows:

$$RB = \frac{R1}{\frac{V_o}{V_{ref}} - 1} \quad [\Omega]$$

- **RS (For current feedback control with LED string):** This resistor is attached at the end of the LED string and it

controls the amount of current flowing through it. To calculate this resistor, set the maximum current you want to flow through the string and use the following formula:

$$RS = \frac{V_{ref}}{I_o} \quad [\Omega]$$

Where  $V_{REF}=230$  mV is the maximum internal reference voltage in current mode control that is reflected on the FB8 pin.

When Input voltage is equal to or higher than  $V_{OUT8}$ , a reverse bias diode is needed from the switching node to the output in order to cause a drop from the Input to the output, see Figure 9 below:

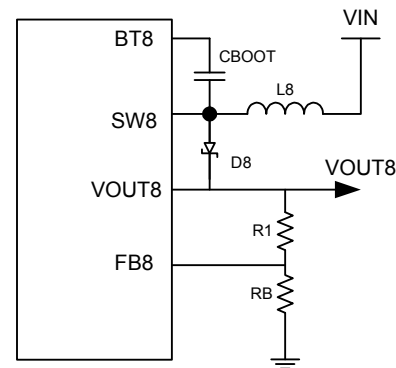


Figure 9. Reverse Bias Diode

#### Regulator 7 (Inverter controller - external compensation needed)

REG7 is a non-synchronous buck/boost inverting PWM voltage-mode control DC-DC regulator that drive an external P-MOSFET to supply a typical voltage of -7.0 V at a maximum current of 60 mA.

- **P-MOSFET:** The peak current of the MOSFET is assumed to be  $I_D$ , which is obtained by the following formula, define  $I_{OB}$  between 60 to 80% of the maximum current rating.

$$I_Q \geq I_{L_{peak}} = \frac{-(I_o + I_{OB})}{1-D}$$

And the voltage rating is given by:

$$V_Q = V_{in} - V_o$$

- **Diode D7:** The peak value of the diode current is  $I_{FSM}$  which should also be higher than  $I_{L_{peak}}$ . The average current rating should be higher than the output current low and the repetition reverse voltage  $V_{RRM}$  is given by:

$$V_{RRM} \geq V_{in} - V_o$$

- **L:** The minimum value of inductor to maintain CCM can be determined by using the following procedure:

$$L_{min} \geq \frac{-V_o T}{2I_{o_{max}}} \left( \frac{V_{in_{min}}}{V_o - V_{in_{min}}} \right)^2 \quad [H]$$

- **C<sub>OUT</sub>:** The three elements of output capacitor that contribute to its impedance and output voltage ripple are the ESR, the ESL and the capacitance C. The minimum capacitor value is approximately:

$$C_{OUT} \geq \frac{I_{o_{max}} D_{max}}{F_{SW} \Delta V_{o_r}} \quad [F]$$

- Where  $\Delta V_{o_r}$  is the desired output voltage ripple.
- Now calculate the maximum allowed ESR to reach the desired.

$$ESR \leq \frac{\Delta V_{o_r}}{\left( \frac{I_{o_{max}}}{1 - D_{max}} + \frac{I_{OB}}{1 - D} \right)} \quad [\Omega]$$

- **R1 and RB:** These two resistors help to set the output voltage to the desired value using a  $V_{FB7}=0.6V$ , select R1 between 10 k and 150 K and then calculate RB as follows:

$$RB = \frac{0.9}{1.5 - V_o - 0.9} R1 \quad [\Omega]$$

NOTE: RB is not grounded, instead is connected to VREF7 pin ( $V_{REF7}=1.5 V$ ) which provide a positive voltage to assure a positive voltage at the FB7 pin.

- Compensation network. (C1,C2,C3, R2, R3)

For compensating a buck converter, 4 important frequencies referring to the plant are:

- Output LC filter cutoff frequency ( $F_{LC}$ ):

$$F_{LC} = \frac{D'_{min}}{2\pi \sqrt{LC_{OUT}}} \quad [Hz]$$

Where  $D'_{min}$  is the minimum off time percentage given by:

$$D'_{min} = \frac{V_{in_{min}}}{|V_{out_{max}}|}$$

- Cutoff frequency due to capacitor ESR:

$$F_{ESR} = \frac{1}{2\pi (C_{OUT}) ESR} \quad [Hz]$$

- The right plane zero frequency:

$$RHP_Z = \frac{(D'_{min})^2 R_{LOAD}}{D \cdot 2\pi L} \quad [Hz]$$

- Crossover frequency (or bandwidth): select this frequency as far away from the  $RHP_Z$  as much as possible:

$$F_{BW} \ll \frac{RHP_Z}{6} \quad [Hz]$$

The Type 3 external compensation network will be in charge of canceling some of these poles and zeros to achieve stability in the system. The following poles and zeroes frequencies are provided by the type 3 compensation:

$$F_{PO} = F_{BW} \quad F_{Z1} = 0.9F_{LC} \quad F_{22} = 1.1F_{LC}$$

$$F_{P1} = F_{ESR} \quad F_{2P} = \frac{F_{SW}}{2}$$

The passive components associated to these frequencies are calculated with the following formulas.

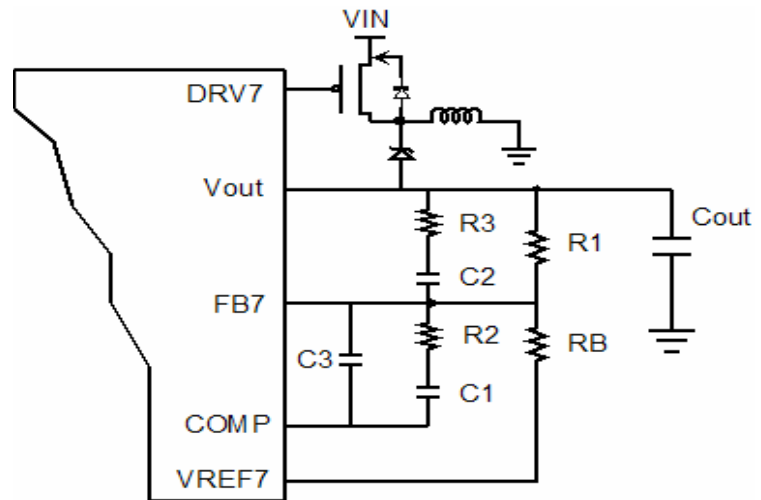
$$C1 = \frac{V_{in\_min}}{V_{RAMP}} \left( \frac{1}{D'_{min}{}^2} \right) \left( \frac{1}{2\pi(F_{PO}R1)} \right)$$

$$C2 = \left( \frac{1}{2\pi(F_{Z2}R1)} \right)$$

$$R2 = \left( \frac{1}{2\pi(F_{Z1}C1)} \right)$$

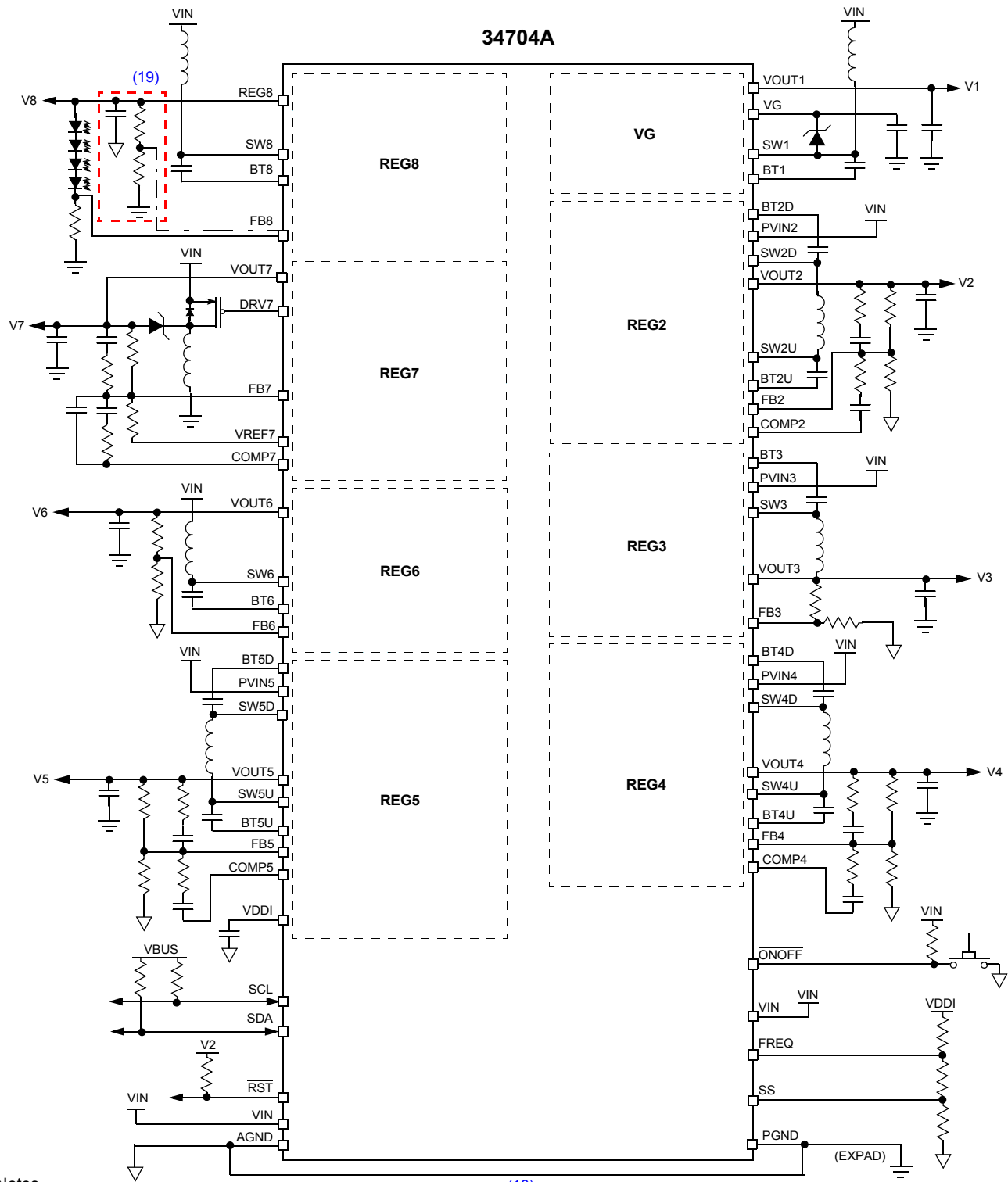
$$R3 = \left( \frac{1}{2\pi(F_{p1}C2)} \right)$$

$$C3 = \left( \frac{1}{2\pi(F_{P2}R2)} \right)$$



On the 34704  $V_{RAMP}$  is half of 1.2 V since each operation mode spends only half the ramp.

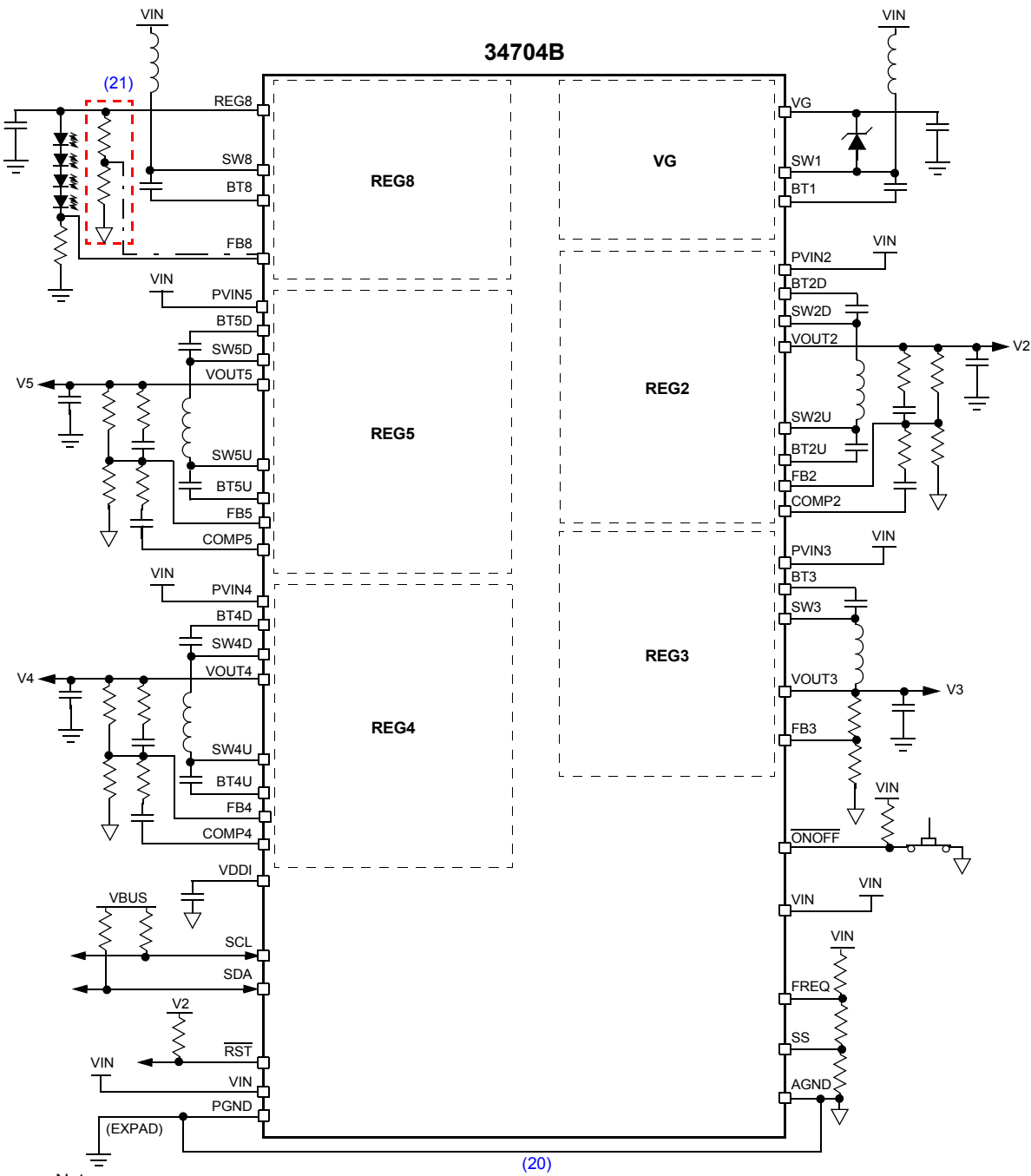
## TYPICAL APPLICATIONS



### Notes

18. AGND(S) & PGND(S) SHOULD BE CONNECTED TOGETHER AS CLOSE TO THE IC AS POSSIBLE
19. REFER TO THE FB8 FUNCTIONAL PIN DESCRIPTION ON PAGE 17.

Figure 10. 34704A Typical Application Diagram

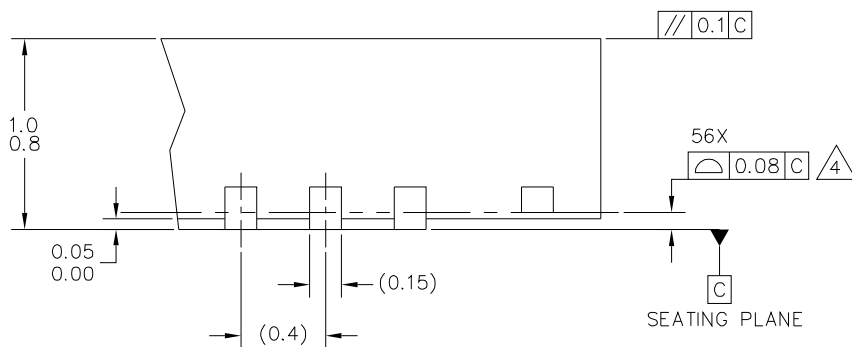


- Notes
- 20. AGND(S) & PGND(S) SHOULD BE CONNECTED TOGETHER AS CLOSE TO THE IC AS POSSIBLE
  - 21. REFER TO THE FB8 FUNCTIONAL PIN DESCRIPTION ON PAGE 17.

Figure 11. 34704B Typical Application Diagram



### PACKAGE DIMENSIONS (CONTINUED)



DETAIL G  
VIEW ROTATED 90°CW

|                                                                               |  |                    |                          |                            |        |
|-------------------------------------------------------------------------------|--|--------------------|--------------------------|----------------------------|--------|
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| TITLE:<br><br>QFN, THERMALLY ENHANCED,<br>7 X 7 X 0.9, 0.4 PITCH, 56 TERMINAL |  |                    | DOCUMENT NO: 98ASA00712D |                            | REV: 0 |
|                                                                               |  |                    | STANDARD: NON-JEDEC      |                            |        |
|                                                                               |  |                    | 31 MAR 2014              |                            |        |



## PACKAGE DIMENSIONS (CONTINUED)

### NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THIS IS A NON-JEDEC REGISTERED PACKAGE.
4.  COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.2 MM.

|                                                                           |                                      |                            |
|---------------------------------------------------------------------------|--------------------------------------|----------------------------|
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|                                                                           | STANDARD: NON-JEDEC                  |                            |
|                                                                           | 31 MAR 2014                          |                            |

## REVISION HISTORY

| REVISION | DATE    | DESCRIPTION OF CHANGES                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|----------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2.0      | 4/2008  | <ul style="list-style-type: none"> <li>Initial Release</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 3.0      | 6/2008  | <ul style="list-style-type: none"> <li>Revised <a href="#">34704 Simplified Application Diagram on page 1</a></li> <li>Revised <a href="#">34704 Internal Block Diagram on page 3</a></li> <li>Revised <a href="#">34704 Pin Definitions on page 4</a></li> <li>Revised <a href="#">34704A Typical Application Diagram on page 49</a> and <a href="#">34704B Typical Application Diagram on page 49</a></li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 4.0      | 6/2009  | <ul style="list-style-type: none"> <li>Updated category from Advance Information to Technical Data.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 5.0      | 1/2010  | <ul style="list-style-type: none"> <li>Added Max I<sup>2</sup>C Speed as 400kHz to dynamic electrical characteristics table</li> <li>Added Device Physical address to dynamic electrical characteristics table.</li> <li>Added register Definition summary table</li> <li>Changed REG7 name definition on Functional Description table to "Inverter boost"</li> <li>Added efficiency Plots</li> <li>Clarified GrpC and E Shutdown Sequence</li> <li>Clarified REG8 Voltage/Current Regulation Mode on feature list.</li> <li>Clarified Pulse Skipping operation.</li> <li>Added minimum Fine Scaling value at 40%</li> <li>Corrected Register Vs Bit notation on I<sup>2</sup>C user interface section.</li> <li>Added I<sup>2</sup>C reading and writing Bit stream sequence example.</li> <li>Added ACCURATE Bit definition</li> <li>Revised Pin Definitions Table for Pins 3, 11, 35, 40, 46 and 53</li> <li>Removed Li-ion battery references throughout document.</li> <li>Added Feedback Reference Voltage and Feedback Reference Voltage on Current Regulation Mode to Table 4.</li> </ul> |
| 6.0      | 9/2011  | <ul style="list-style-type: none"> <li>Revised Note 2 on page 7.</li> <li>Changed F<sub>22</sub> to F<sub>22</sub> and F<sub>2P</sub> to F<sub>P2</sub> on page 42.</li> <li>Revised step 1 under "Compensating for Buck operation" section on page 40.</li> <li>Updated the formula for C1 on page 42.</li> <li>Revised step 1 under "Compensating for boost operation" section on page 43.</li> <li>Revised step 1 under "Regulator 3 (Synchronous Buck - internally compensated)" section on page 44.</li> <li>Revised I<sub>OB</sub> definition under "Regulator 8 (Synchronous Boost - internally compensated -Voltage or current feedback)" section on page 45.</li> <li>Revised P-MOSFET description under "Regulator 7 (Inverter controller - external compensation needed)" section on page 46.</li> </ul>                                                                                                                                                                                                                                                                               |
| 7.0      | 12/2011 | <ul style="list-style-type: none"> <li>Changed <math>\overline{\text{RST}}</math> Leakage Current from 1 mA to 1 <math>\mu</math>A in the <b>Static Electrical Characteristics</b> table on <a href="#">page 9</a>.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|          | 4/2013  | <ul style="list-style-type: none"> <li>No technical changes. Revised back page. Updated document properties. Added SMARTMOS sentence to first paragraph.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 8.0      | 12/2014 | <ul style="list-style-type: none"> <li>Updated case outline (changed 98ASA10751D to 98ASA00712D) as per PCN 16331</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

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