DESCRIPTION

Demonstration circuit 1098 supports a family of 10/12/14-BIT 125 MSPS ADCs. Each assembly features one member of this family of high speed, high dynamic range ADCs.

The versions of 1098 demo board are listed in Table 1. Depending on the required resolution, sample rate and input frequency, the DC1098 is supplied with the appropriate A/D and with an optimized input circuit. The circuitry on the analog inputs is optimized for analog input frequencies below 70 MHz or from 70 MHz to 140MHz. For higher input frequencies, contact the factory for support.

Design files for this circuit board are available. Call the LTC factory.

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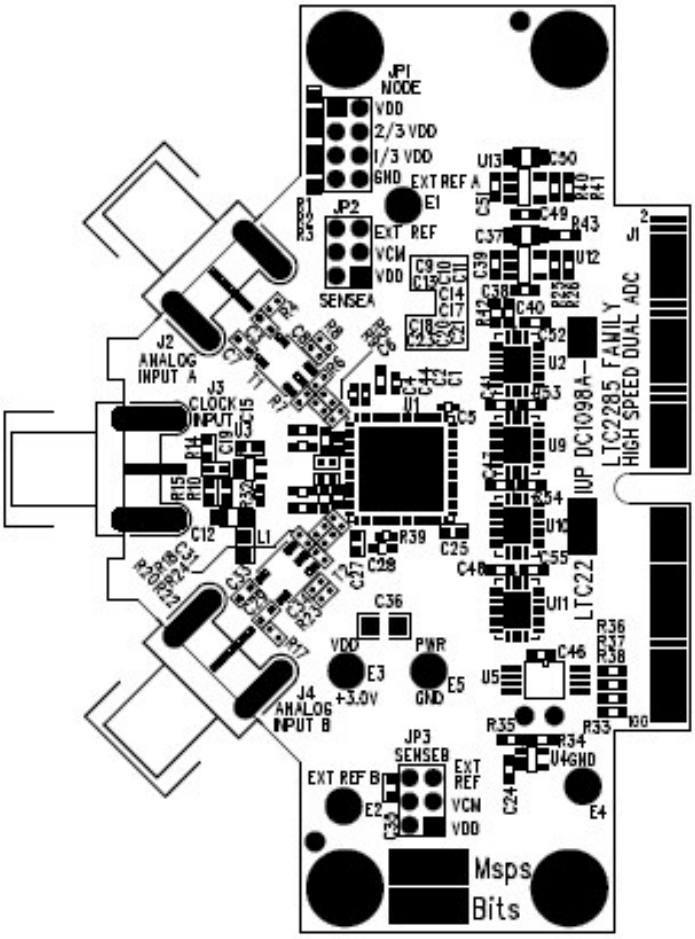


Table 1. DC1098A Variants

DC1098 VARIANTS	ADC PART NUMBER	RESOLUTION*	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
1098A-A	LTC2281	10-Bit	125 MSPS	1MHz - 70MHz
1098A-B	LTC2283	12-Bit	125 MSPS	1MHz - 70MHz
1098A-C	LTC2295	14-Bit	125 MSPS	1MHz -70MHz
1098A-D	LTC2291	10-Bit	125 MSPS	70MHz -140MHz
1098A-E	LTC2293	12-bit	125 MSPS	70MHz -140MHz
1098A-F	LTC2295	14-Bit	125 MSPS	70MHz -140MHz

Table 2. Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Supply Voltage	Depending on sampling rate and the A/D converter provided, this supply must provide up to 200mA.	Optimized for 3.0V [2.7V ⇔3.6V min/max]
Analog Input Range	Depending on Sense Pin Voltage	$1V_{PP}$ to $2V_{PP}$
Logic Input Voltages	Minimum Logic High	2.4V
	Maximum Logic Low	0.8V
Logic Output Voltage (74VCX245 output buffer, V_{cc} = 2.5V)	Minimum Logic High @ -1.6mA	2.3V (33Ω Series terminations)
	Maximum Logic Low @ 1.6mA	0.7V (33Ω Series terminations)
Sampling Frequency (Convert Clock Frequency)	See Table 1	
Convert Clock Level	50 Ω Source Impedance, AC coupled or ground referenced (Convert Clock input is capacitor coupled on board and terminated with 50Ω.)	$2V_{P-P}$ ⇔$2.5V_{P-P}$ Sine Wave or Square wave (See Note 1)
Resolution	See Table 1	
Input Frequency Range	See Table 1	
SFDR	See Applicable Data Sheet	
SNR	See Applicable Data Sheet	

Note 1: For sample rates below 20MSPS a square wave must be used to achieve full performance.

QUICK START PROCEDURE

Demonstration circuit 1098 is easy to set up to evaluate the performance of most members of the LTC2285 family of Dual A/D converters – LTC2281, LTC2283, and LTC2285. Refer to the latest DC1098 schematic for new variants.

Refer to Figure 1 for proper measurement equipment setup and follow the procedure below.

SETUP

If a DC890 FastDAACS Data Acquisition and Collection System was supplied with the DC1098 demonstration circuit, follow the DC890 Quick Start Guide to install the required software and for connecting the DC890 to the DC1098 and to a PC running Windows98, 2000 or XP.

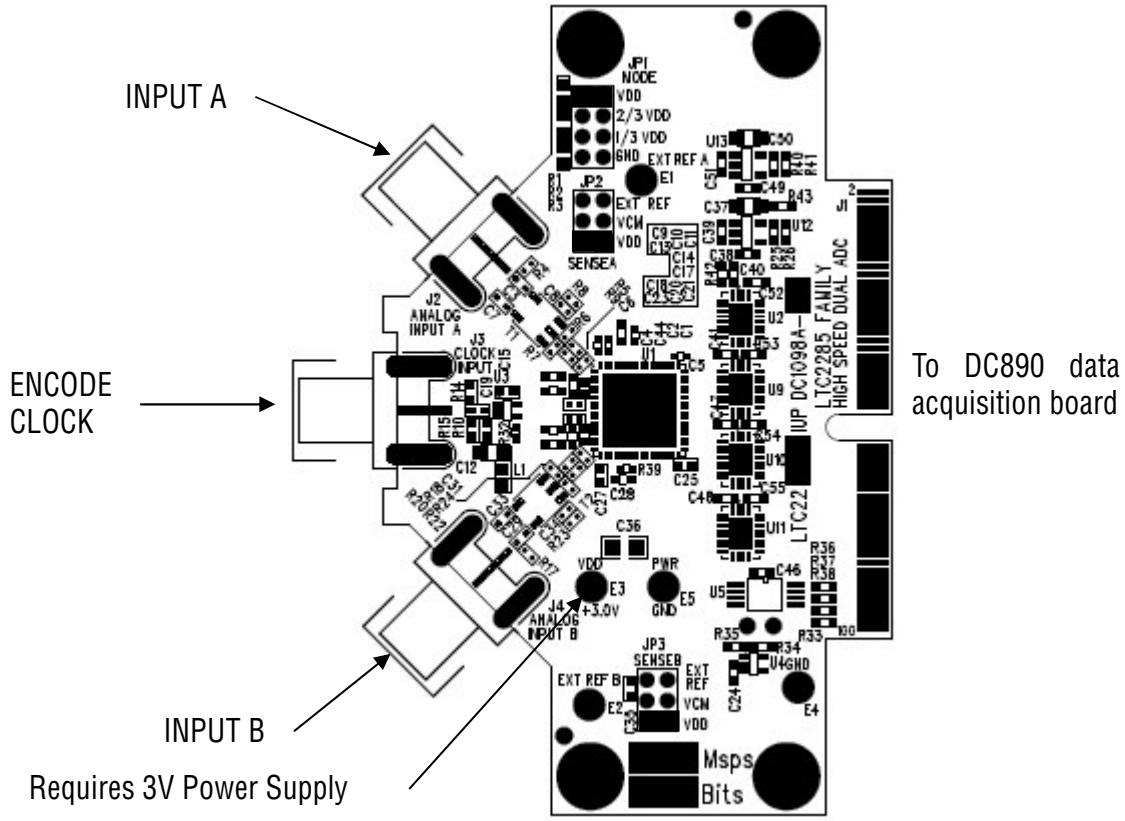


Figure 1. DC1098 Setup

DC1098 DEMONSTRATION CIRCUIT BOARD JUMPERS

The DC1098 demonstration circuit board should have the following jumper settings as default: (as per figure 1)

JP1: Mode: Vdd. 2s complement, Clock duty stabilizer off (see data sheet for function of Mode pin.)

JP2: Sense A: Vdd, (2V P-P input range)

JP3: Sense B: Vdd, (2V P-P input range)

APPLYING POWER AND SIGNALS TO THE DC1098 DEMONSTRATION CIRCUIT BOARD:

If a DC890 is used to acquire data from the DC1098, the DC890 should be powered up FIRST, before applying +3V across the pins marked "+3.0V" and "PWR GND" on the DC1098. However, the output buffers on DC1098 will not be enabled until power is applied to DC890. The DC1098 demonstration circuit requires up to 200 mA depending on the sampling rate and the A/D converter supplied.

ENCODE CLOCK

NOTE: This is not a logic compatible input. It is terminated with 50 Ohms.

Apply an encode clock to the SMA connector on the DC1098 demonstration circuit board marked "J3 CLOCK INPUT". This input is connected to ground through a 50Ω resistor, and followed by a blocking capacitor. For the best noise performance, the CLOCK INPUT must be driven with a very low jitter source. When using a sinusoidal generator, the amplitude should be as large as possible, up to $3V_{P-P}$ or 13 dBm. Using band pass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. Data sheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broad band noise. Low phase noise Agilent 8644B generators are used with TTE band pass filters for both the Clock input and the Analog input.

A square wave encode clock is recommended for sample rates lower than 20MSPS. This is because the lower slew rate of a sinusoidal encode clock translates to increased clock jitter and hence lower SNR.

The Encode Clock can be driven with a 2.5V CMOS Logic Level square wave if R14 is replaced with an acceptable load for the drive capability of the logic. Note that logic devices are generally not able to drive cable. A barrel is recommended for logic drive. If a cable is used, the cable carrying the clock signal must be terminated to maintain the signal integrity of the Encode Clock Source and the signal source must be able to drive the 0 to 2.5V square wave signal into 50Ω load.

ANALOG INPUT NETWORK

Apply the analog input signals of interest to the SMA connectors on the DC1098 demonstration circuit board marked “ANALOG INPUT (A and B)”. These inputs are capacitively coupled to ETC1-1-13 Balun transformers on high input frequency versions, or directly coupled through ETC1-1T Flux coupled transformers on low input frequency versions.

For optimal distortion and noise performance the RC network on the analog inputs are optimized for different analog input frequencies on the different versions of the DC1098. Refer to table 1. For input frequencies below about 70MHz, the circuit in Fig. 2 is recommended. For input frequencies above 70MHz and below 170MHz, the circuit in Fig. 3 is recommended.

For input frequencies between 250MHz and 500MHz, the circuit in Fig. 4 is recommended. For input frequencies greater than 250MHz contact the factory for support.

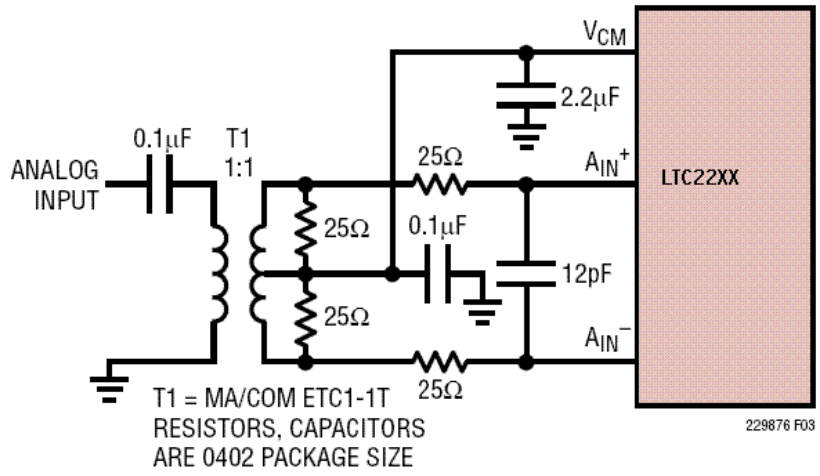


Figure 2. Analog Front End Circuit For 1MHz < A_{IN} < 70MHz (1 of 2)

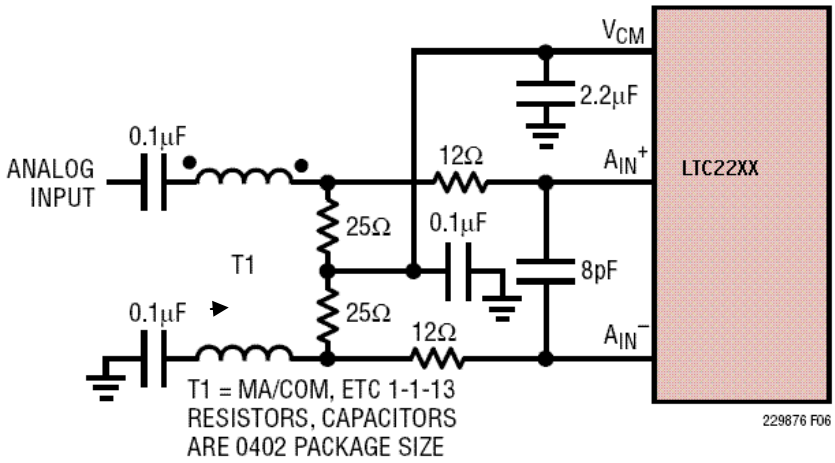


Figure 3. Analog Front End Circuit For 70MHz < A_{IN} < 170MHz (1 of 2)

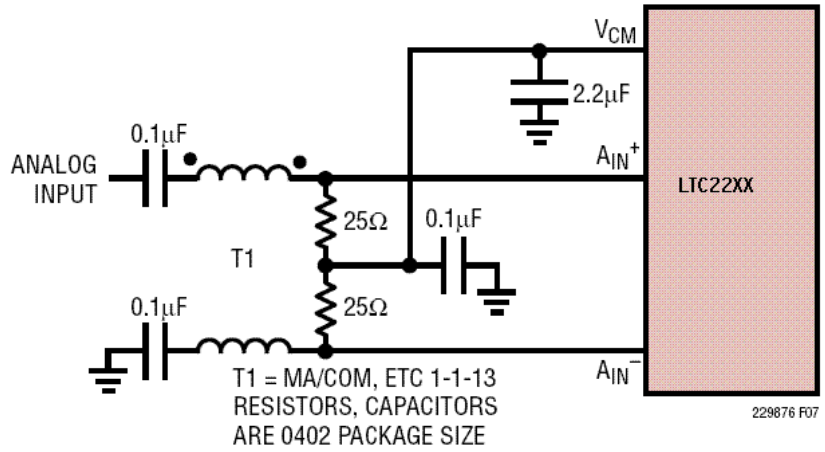


Figure 4. Analog Front End Circuit For 170MHz < A_{IN} < 300MHz

Note that relative aperture measurements require removal of these networks, or the results will simply show the relative phase through the RC network. The measure of relative phase further requires a resistive power divider, and matched cables, or the results will be misleading. Any relative phase measurements should be confirmed by reversing the signals to confirm that the relative delay is not due to the external network.

If relative phase measurements produce results of greater that a fraction of a picosecond, please consult the factory for assistance.

Channel to Channel Crosstalk on this demo board is better than -110 dB for input frequencies below 140 MHz.

DATA COLLECTION

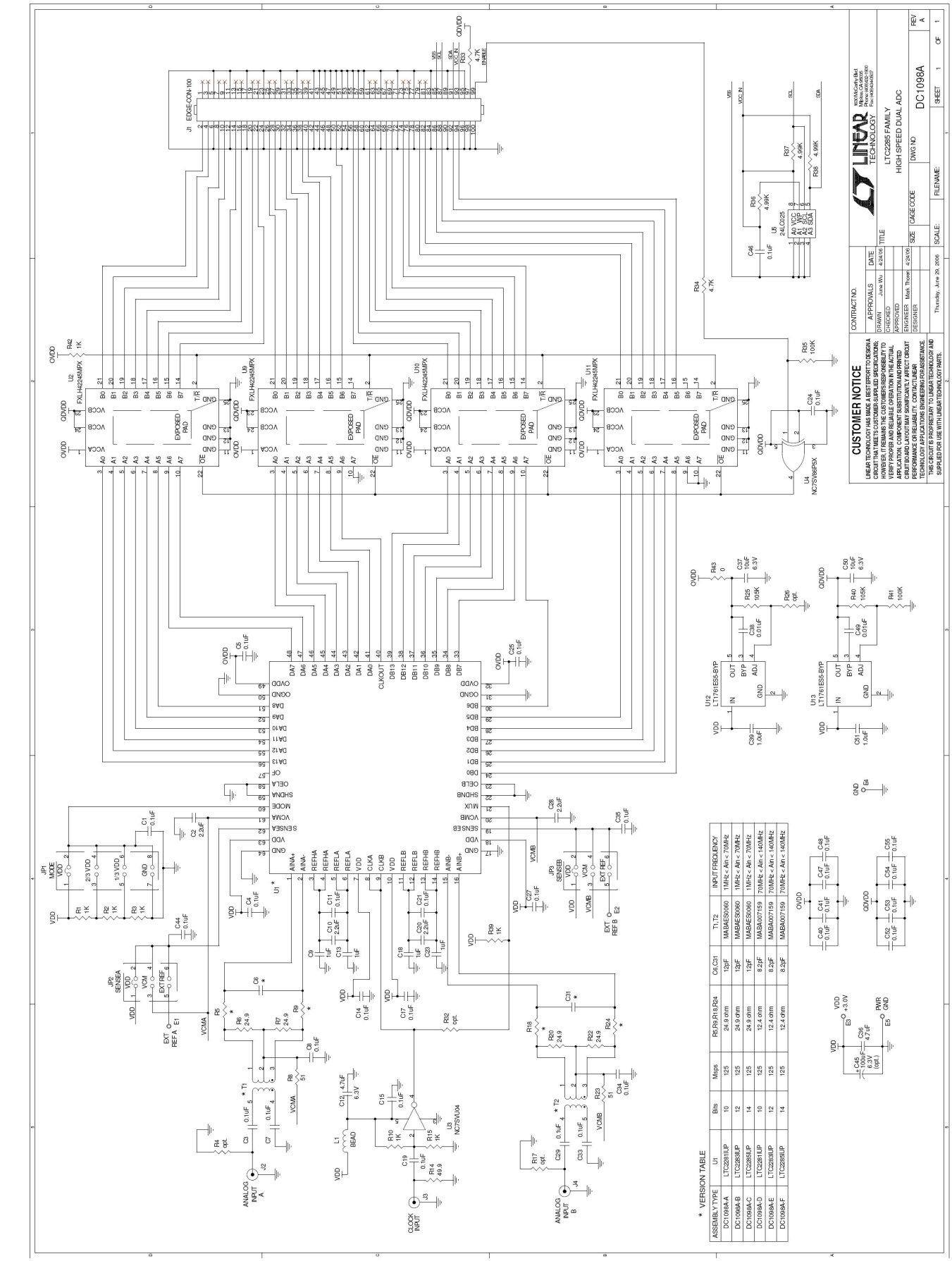
The conversion clock output and the parallel data for both ADC channels are available on J1. This connector is designed to mate with a Samtec model MEC8-150-02-L-D-EM2 receptacle. It is recommended that this receptacle be used if something other than a DC890 board is used to collect data.

DC890 QuickEval-II Data Acquisition Board uses the *PScope System Software* provided or downloaded from the Linear Technology website at http://www.linear.com/software/. If a DC890 was provided, follow the Quick Start Guide and the instructions below.

To start the data collection software if "*PScope.exe*", is installed (by default) in \Program Files\LTC\PScope\, double click the PScope Icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

Configure PScope for the appropriate variant of the DC1098 demonstration circuit by selecting the correct A/D Converter as installed on the DC1098. Under the "Configure" menu, go to "Device." Under the "Device" pull down menu, select device, LTC2280 through LTC2299. When evaluating 12-Bit parts, select the appropriate LTC22XX part in the Device List and PScope will automatically blank the last two LSBs when using a DC1098 supplied with a 14-Bit part.

If everything is hooked up properly, powered, and a suitable convert clock is present, clicking the "Collect" button should result in time and frequency plots displayed in the PScope window. The two channel mode in Pscope provides a page for each channel, and a page showing the frequency domain plots of both channels. An additional window called "X-channel" displays relative phase and amplitude of the two channels. This can be used to gauge crosstalk, or validate relative aperture delay. Additional information and help for *PScope* is available in the DC890 Quick Start Guide and in the online help available within the *PScope* program itself.


LINEAR TECHNOLOGY
LTC2285 FAMILY
HIGH SPEED DUAL ADC
DC1098A
CUSTOMER NOTICE
LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.
THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.
* VERSION TABLE
ASSEMBLY TYPE | U1 | Bits | Msps | R5,Rg,R18,R24 | C6,C31 | T1,T2 | INPUT FREQUENCY
DC1098A-A | LTC2281IUP | 10 | 125 | 24.9 ohm | 12pF | MABAES0060 | 1MHz < Ain < 70MHz
DC1098A-B | LTC2285IUP | 12 | 125 | 24.9 ohm | 12pF | MABAES0060 | 1MHz < Ain < 70MHz
DC1098A-C | LTC2285IUP | 14 | 125 | 24.9 ohm | 12pF | MABAES0060 | 1MHz < Ain < 70MHz
DC1098A-D | LTC2281IUP | 10 | 125 | 12.4 ohm | 8.2pF | MABA007159 | 70MHz < Ain < 140MHz
DC1098A-E | LTC2285IUP | 12 | 125 | 12.4 ohm | 8.2pF | MABA007159 | 70MHz < Ain < 140MHz
DC1098A-F | LTC2285IUP | 14 | 125 | 12.4 ohm | 8.2pF | MABA007159 | 70MHz < Ain < 140MHz