# Voltage Output, High or Low Side Measurement, Bi-Directional Zerø-Drift Series CURRENT SHUNT MONITOR

**Check for Samples: INA199A1, INA199B1, INA199A2, INA199B2, INA199A3, INA199B3**

## FEATURES

- **WIDE COMMON-MODE RANGE: –0.3V to 26V**
- **OFFSET VOLTAGE: ±150μV (Max)**
  **(Enables shunt drops of 10mV full-scale)**
- **ACCURACY**
  - **±1.5% Gain Error (Max over temperature)**
  - **0.5μV/°C Offset Drift (Max)**
  - **10ppm/°C Gain Drift (Max)**
- **CHOICE OF GAINS:**
  - **INA199A1/B1: 50V/V**
  - **INA199A2/B2: 100V/V**
  - **INA199A3/B3: 200V/V**
- **QUIESCENT CURRENT: 100μA (max)**
- **PACKAGES: SC70, THIN QFN-10**

## APPLICATIONS

- **NOTEBOOK COMPUTERS**
- **CELL PHONES**
- **TELECOM EQUIPMENT**
- **POWER MANAGEMENT**
- **BATTERY CHARGERS**
- **WELDING EQUIPMENT**

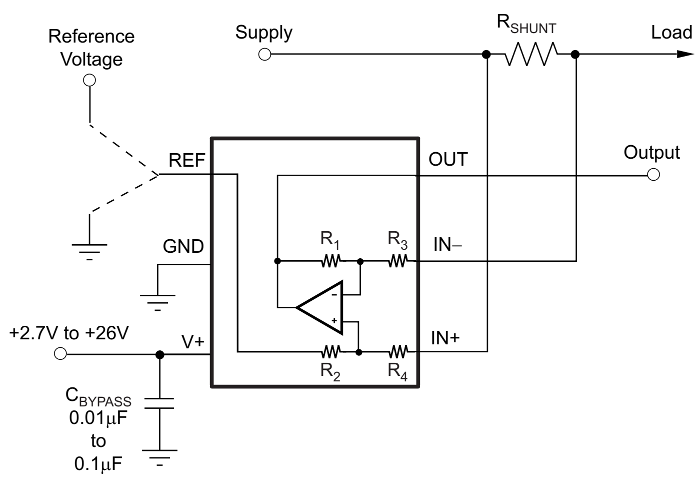
## DESCRIPTION

The INA199 series of voltage output current shunt monitors can sense drops across shunts at common-mode voltages from –0.3V to 26V, independent of the supply voltage. Three fixed gains are available: 50V/V, 100V/V, and 200V/V. The low offset of the Zerø-Drift architecture enables current sensing with maximum drops across the shunt as low as 10mV full-scale.

These devices operate from a single +2.7V to +26V power supply, drawing a maximum of 100μA of supply current. All versions are specified from –40°C to +105°C, and offered in both SC70 and thin QFN-10 packages.

**PRODUCT FAMILY TABLE**

| PRODUCT | GAIN | $R_3$ AND $R_4$ | $R_1$ AND $R_2$ |
|---|---|---|---|
| INA199A1/B1 | 50 | 20kΩ | 1MΩ |
| INA199A2/B2 | 100 | 10kΩ | 1MΩ |
| INA199A3/B3 | 200 | 5kΩ | 1MΩ |



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE INFORMATION(1)

| PRODUCT | GAIN | PACKAGE-LEAD | PACKAGE DESIGNATOR | PACKAGE MARKING |
|---|---|---|---|---|
| INA199A1 | 50V/V | SC70-6 | DCK | OBG |
| | | Thin QFN-10 | RSW | NSJ |
| INA199B1 | 50V/V | SC70-6 | DCK | SEB |
| | | Thin QFN-10 | RSW | SHV |
| INA199A2 | 100V/V | SC70-6 | DCK | OBH |
| | | Thin QFN-10 | RSW | NTJ |
| INA199B2 | 100V/V | SC70-6 | DCK | SEG |
| | | Thin QFN-10 | RSW | SHW |
| INA199A3 | 200V/V | SC70-6 | DCK | OBI |
| | | Thin QFN-10 | RSW | NUJ |
| INA199B3 | 200V/V | SC70-6 | DCK | SHE |
| | | Thin QFN-10 | RSW | SHX |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

| | | VALUE | UNIT |
|---|---|---|---|
| Supply Voltage | | +26 | V |
| Analog Inputs, $V_{IN+}$, $V_{IN–}$(2) | Differential ($V_{IN+}$) – ($V_{IN–}$) | –26 to +26 | V |
| | Common-mode(3) | GND – 0.3 to +26 | V |
| REF Input | | GND – 0.3 to (V+) + 0.3 | V |
| Output(3) | | GND – 0.3 to (V+) + 0.3 | V |
| Input Current Into All Pins(3) | | 5 | mA |
| Operating Temperature | | –40 to +125 | °C |
| Storage Temperature | | –65 to +150 | °C |
| Junction Temperature | | +150 | °C |
| ESD Ratings: (version A) | Human Body Model (HBM) | 4000 | V |
| | Charged-Device Model (CDM) | 1000 | V |
| | Machine Model (MM) | 200 | V |
| ESD Ratings: (version B) | Human Body Model (HBM) | 1500 | V |
| | Charged-Device Model (CDM) | 1000 | V |
| | Machine Model (MM) | 100 | V |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) $V_{IN+}$ and $V_{IN–}$ are the voltages at the IN+ and IN– pins, respectively.
(3) Input voltage at any pin may exceed the voltage shown if the current at that pin is limited to 5mA.

## ELECTRICAL CHARACTERISTICS

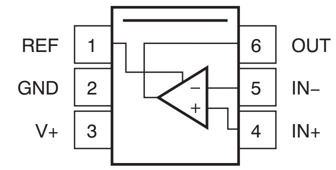
**Boldface** limits apply over the specified temperature range, **$T_A$ = –40°C to +105°C.**
At $T_A$ = +25°C, $V_S$ = +5V, $V_{IN+}$ = 12V, $V_{SENSE}$ = $V_{IN+}$ – $V_{IN–}$, and $V_{REF}$ = $V_S$/2, unless otherwise noted.

| PARAMETER | | CONDITIONS | INA199A1, INA199B1, INA199A2, INA199B2, INA199A3, INA199B3 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **INPUT** | | | | | | |
| **Common-Mode Input Range** | **$V_{CM}$** | **Version A** | **–0.3** | | **26** | **V** |
| | | **Version B** | **–0.1** | | **26** | **V** |
| **Common-Mode Rejection** | **CMR** | **$V_{IN+}$ = 0V to +26V, $V_{SENSE}$ = 0mV** | **100** | **120** | | **dB** |
| Offset Voltage, RTI (1) | $V_{OS}$ | $V_{SENSE}$ = 0mV | | ±5 | ±150 | μV |
| **vs Temperature** | **$dV_{OS}/dT$** | | | **0.1** | **0.5** | **μV/°C** |
| vs Power Supply | PSR | $V_S$ = +2.7V to +18V, $V_{IN+}$ = +18V, $V_{SENSE}$ = 0mV | | ±0.1 | | μV/V |
| Input Bias Current | $I_B$ | $V_{SENSE}$ = 0mV | | 28 | | μA |
| Input Offset Current | $I_{OS}$ | $V_{SENSE}$ = 0mV | | ±0.02 | | μA |
| **OUTPUT** | | | | | | |
| Gain | G | | | | | |
| INA199A1 | | | | 50 | | V/V |
| INA199A2 | | | | 100 | | V/V |
| INA199A3 | | | | 200 | | V/V |
| **Gain Error** | | **$V_{SENSE}$ = –5mV to 5mV** | | **±0.03** | **±1.5** | **%** |
| **vs Temperature** | | | | **3** | **10** | **ppm/°C** |
| Nonlinearity Error | | $V_{SENSE}$ = –5mV to 5mV | | ±0.01 | | % |
| Maximum Capacitive Load | | No Sustained Oscillation | | 1 | | nF |
| **VOLTAGE OUTPUT (2)** | | **$R_L$ = 10kΩ to GND** | | | | |
| **Swing to V+ Power-Supply Rail** | | | | **(V+) – 0.05** | **(V+) – 0.2** | **V** |
| **Swing to GND** | | | | **($V_{GND}$) + 0.005** | **($V_{GND}$) + 0.05** | **V** |
| **FREQUENCY RESPONSE** | | | | | | |
| Bandwidth | GBW | $C_{LOAD}$ = 10pF, INA199A1 and INA199B1 | | 80 | | kHz |
| | | $C_{LOAD}$ = 10pF, INA199A2 and INA199B2 | | 30 | | kHz |
| | | $C_{LOAD}$ = 10pF, INA199A3 and INA199B3 | | 14 | | kHz |
| Slew Rate | SR | | | 0.4 | | V/μs |
| **NOISE, RTI (1)** | | | | | | |
| Voltage Noise Density | | | | 25 | | nV/√Hz |
| **POWER SUPPLY** | | | | | | |
| **Operating Voltage Range** | **$V_S$** | | **+2.7** | | **+26** | **V** |
| | | –20°C to +85°C | +2.5 | | +26 | V |
| Quiescent Current | $I_Q$ | $V_{SENSE}$ = 0mV | | 65 | 100 | μA |
| **Over Temperature** | | | | | **115** | **μA** |
| **TEMPERATURE RANGE** | | | | | | |
| Specified Range | | | –40 | | +105 | °C |
| Operating Range | | | –40 | | +125 | °C |
| Thermal Resistance | $\theta_{JA}$ | | | | | |
| SC70 | | | | 250 | | °C/W |
| Thin QFN | | | | 80 | | °C/W |

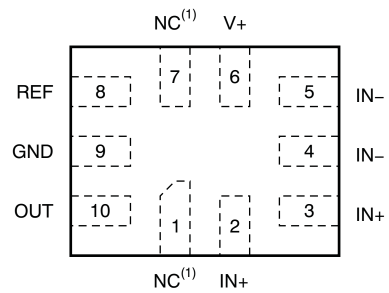
(1) RTI = Referred-to-input.
(2) See Typical Characteristic curve, *Output Voltage Swing vs Output Current* (Figure 6).

## PIN CONFIGURATIONS

**DCK PACKAGE**
**SC70-6**
**(TOP VIEW)**




**RSW PACKAGE**
**Thin QFN-10**
**(TOP VIEW)**




(1) NC = no connection.

## TYPICAL CHARACTERISTICS

Performance measured with the INA199A3 at $T_A$ = +25°C, $V_S$ = +5V, $V_{IN+}$ = 12V, and $V_{REF}$ = $V_S$/2, unless otherwise noted.

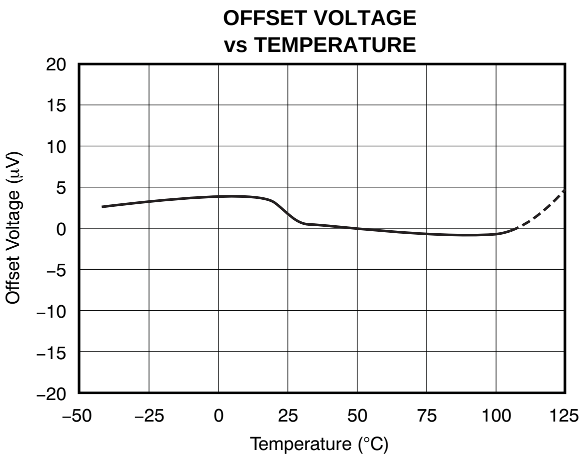



**Figure 1.**

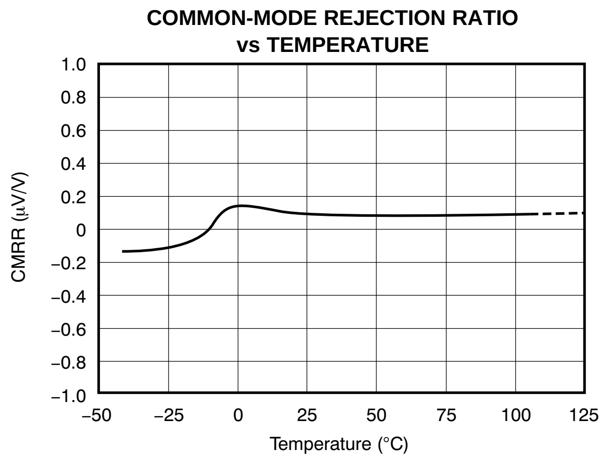



**Figure 2.**

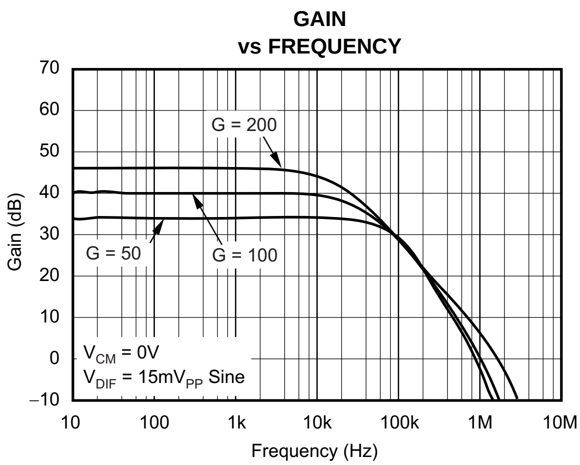



**Figure 3.**

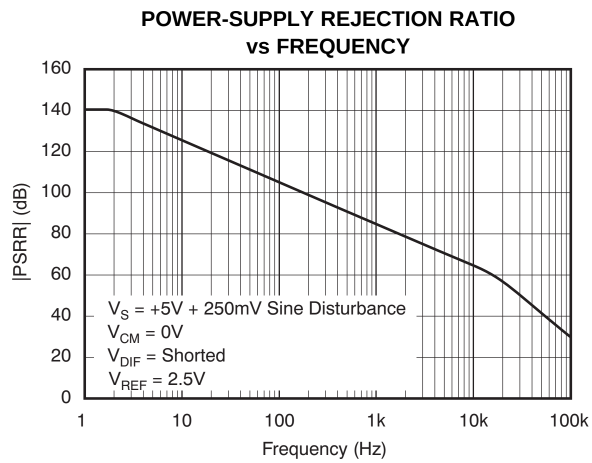



**Figure 4.**

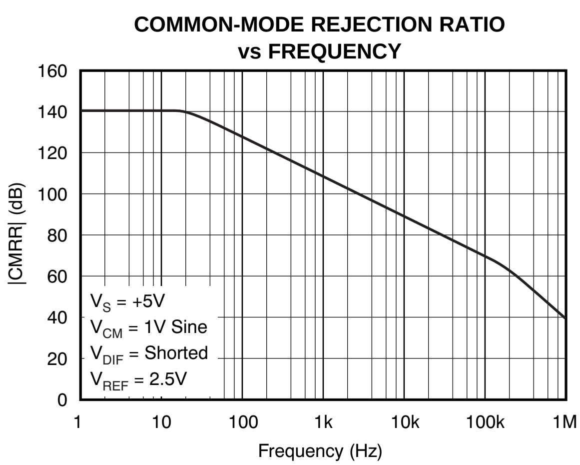



**Figure 5.**

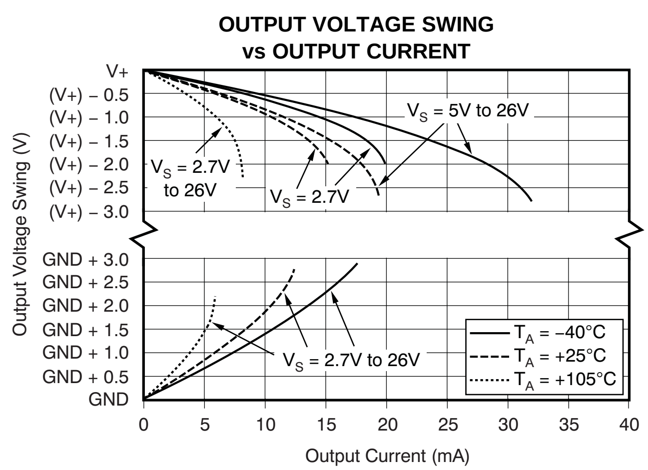



**Figure 6.**

## TYPICAL CHARACTERISTICS (continued)

Performance measured with the INA199A3 at $T_A$ = +25°C, $V_S$ = +5V, $V_{IN+}$ = 12V, and $V_{REF}$ = $V_S$/2, unless otherwise noted.

**OUTPUT VOLTAGE SWING vs OUTPUT CURRENT ($V_S$ = 2.5V)**

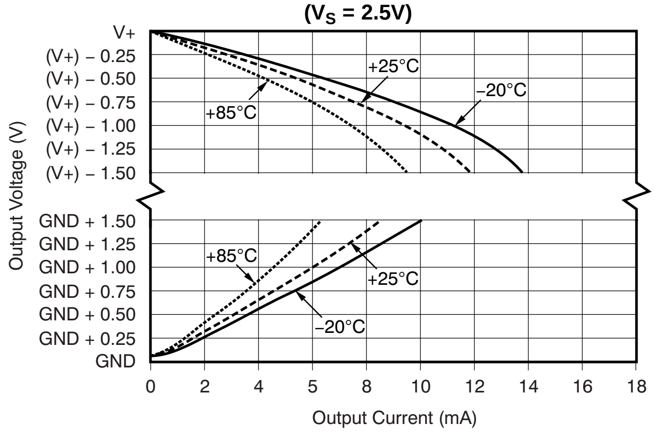



**Figure 7.**

**INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE with SUPPLY VOLTAGE = +5V**

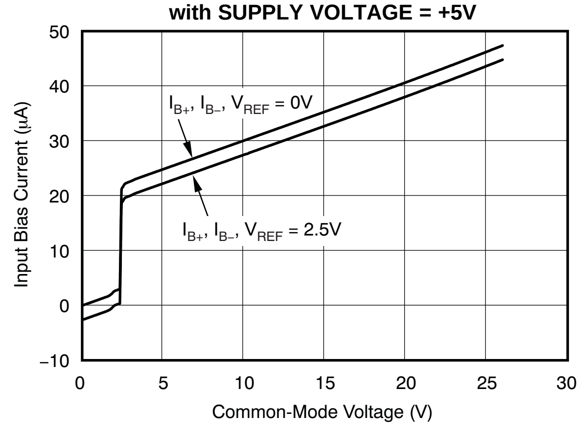



**Figure 8.**

**INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE with SUPPLY VOLTAGE = 0V (Shutdown)**

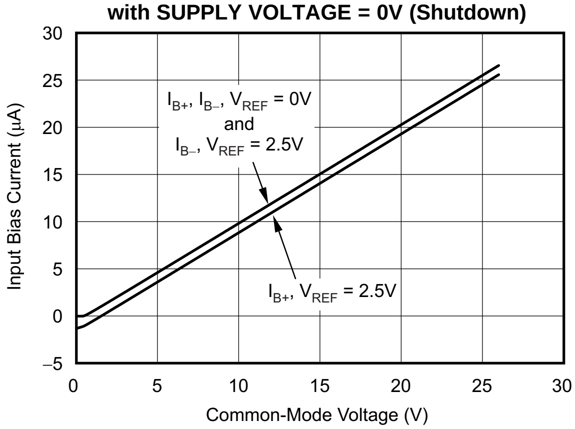



**Figure 9.**

**INPUT BIAS CURRENT vs TEMPERATURE**

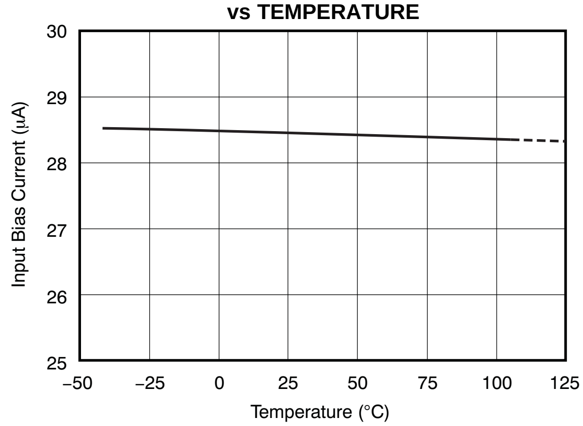



**Figure 10.**

**QUIESCENT CURRENT vs TEMPERATURE**

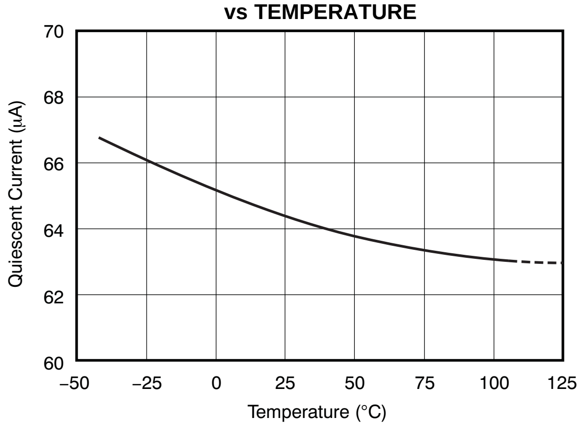



**Figure 11.**

**INPUT-REFERRED VOLTAGE NOISE vs FREQUENCY**

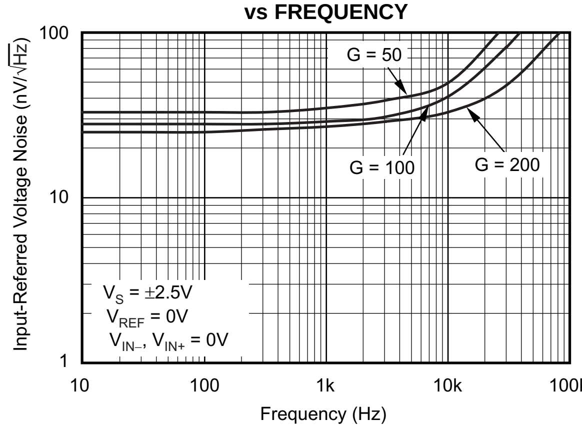



**Figure 12.**

## TYPICAL CHARACTERISTICS (continued)

Performance measured with the INA199A3 at $T_A$ = +25°C, $V_S$ = +5V, $V_{IN+}$ = 12V, and $V_{REF}$ = $V_S$/2, unless otherwise noted.

**0.1Hz to 10Hz VOLTAGE NOISE (Referred-to-Input)**

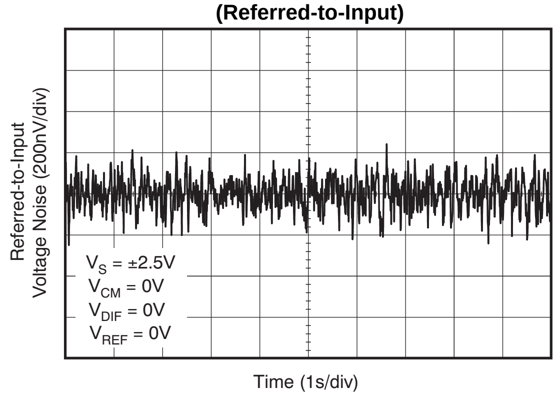



**Figure 13.**

**STEP RESPONSE (10mV$_{PP}$ Input Step)**

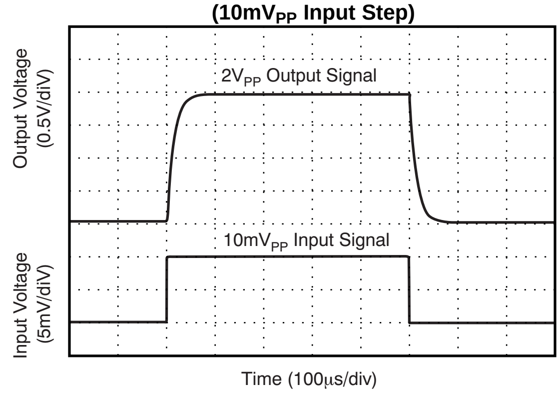



**Figure 14.**

**COMMON-MODE VOLTAGE TRANSIENT RESPONSE**

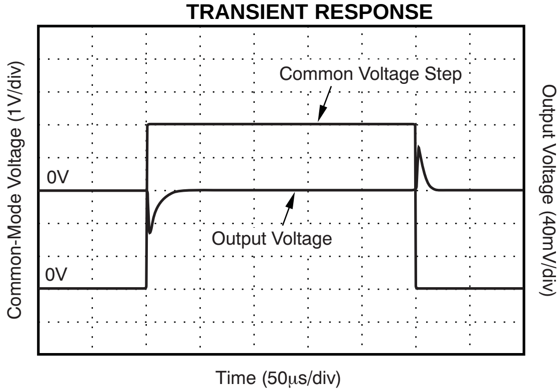



**Figure 15.**

**INVERTING DIFFERENTIAL INPUT OVERLOAD**

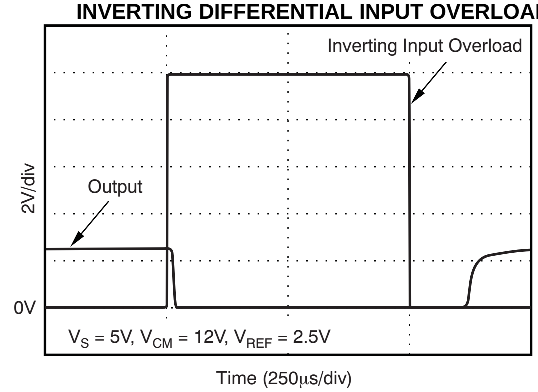



**Figure 16.**

**NONINVERTING DIFFERENTIAL INPUT OVERLOAD**

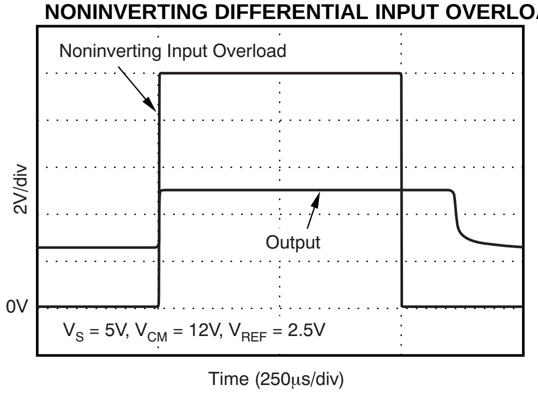



**Figure 17.**

**START-UP RESPONSE**

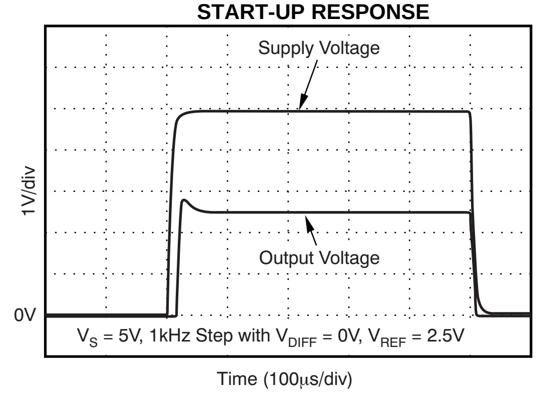



**Figure 18.**

## TYPICAL CHARACTERISTICS (continued)

Performance measured with the INA199A3 at $T_A$ = +25°C, $V_S$ = +5V, $V_{IN+}$ = 12V, and $V_{REF}$ = $V_S$/2, unless otherwise noted.

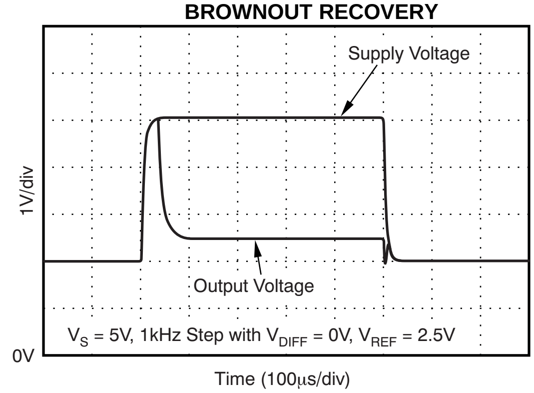



**Figure 19.**

# APPLICATION INFORMATION

## BASIC CONNECTIONS

Figure 20 shows the basic connections for the INA199. The input pins, IN+ and IN–, should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

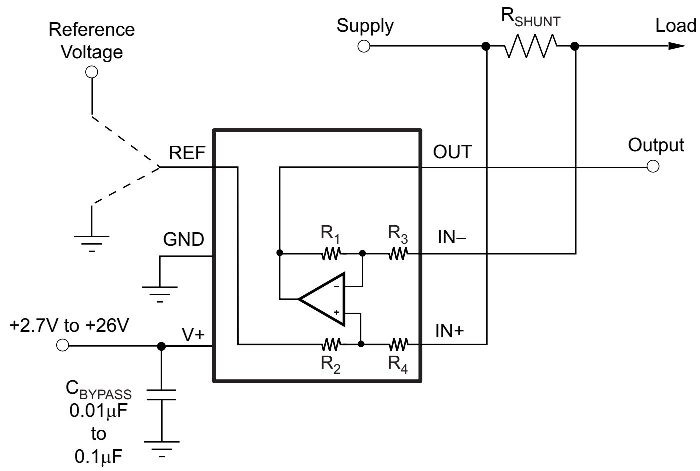



**Figure 20. Typical Application**

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

On the RSW package, two pins are provided for each input. These pins should be tied together (that is, tie IN+ to IN+ and tie IN– to IN–).

## POWER SUPPLY

The input circuitry of the INA199 can accurately measure beyond its power-supply voltage, V+. For example, the V+ power supply can be 5V, whereas the load power-supply voltage can be as high as +26V. However, the output voltage range of the OUT terminal is limited by the voltages on the power-supply pin. Note also that the INA199 can withstand the full –0.3V to +26V range in the input pins, regardless of whether the device has power applied or not.

## SELECTING $R_S$

The zero-drift offset performance of the INA199 offers several benefits. Most often, the primary advantage of the low offset characteristic enables lower full-scale drops across the shunt. For example, non-zero-drift current shunt monitors typically require a full-scale range of 100mV.

The INA199 series of current-shunt monitors give equivalent accuracy at a full-scale range on the order of 10mV. This accuracy reduces shunt dissipation by an order of magnitude with many additional benefits.

Alternatively, there are applications that must measure current over a wide dynamic range that can take advantage of the low offset on the low end of the measurement. Most often, these applications can use the lower gain of 50 or 100 to accommodate larger shunt drops on the upper end of the scale. For instance, an INA199A1 operating on a 3.3V supply could easily handle a full-scale shunt drop of 60mV, with only 150μV of offset.

## UNIDIRECTIONAL OPERATION

Unidirectional operation allows the INA199 to measure currents through a resistive shunt in one direction. The most frequent case of unidirectional operation sets the output at ground by connecting the REF pin to ground. In unidirectional applications where the highest possible accuracy is desirable at very low inputs, bias the REF pin to a convenient value above 50mV to get the device output swing into the linear range for zero inputs.

A less frequent case of unipolar output biasing is to bias the output by connecting the REF pin to the supply; in this case, the quiescent output for zero input is at quiescent supply. This configuration would only respond to negative currents (inverted voltage polarity at the device input).

## BIDIRECTIONAL OPERATION

Bidirectional operation allows the INA199 to measure currents through a resistive shunt in two directions. In this case, the output can be set anywhere within the limits of what the reference inputs allow (that is, between 0V to V+). Typically, it is set at half-scale for equal range in both directions. In some cases, however, it is set at a voltage other than half-scale when the bidirectional current is nonsymmetrical.

The quiescent output voltage is set by applying voltage to the reference input. Under zero differential input conditions the output assumes the same voltage that is applied to the reference input.

## INPUT FILTERING

An obvious and straightforward filtering location is at the device output. However, this location negates the advantage of the low output impedance of the internal buffer. The only other filtering option is at the device input pins. This location, though, does require consideration of the ±30% tolerance of the internal resistances. Figure 21 shows a filter placed at the inputs pins.

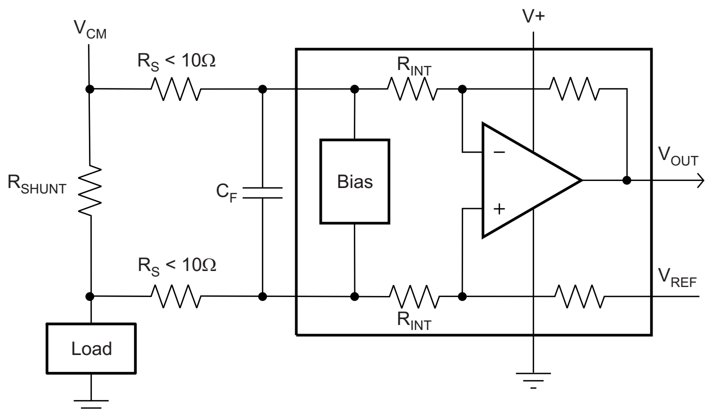



**Figure 21. Filter at Input Pins**

The addition of external series resistance, however, creates an additional error in the measurement so the value of these series resistors should be kept to 10Ω or less if possible to reduce impact to accuracy. The internal bias network shown in Figure 21 present at the input pins creates a mismatch in input bias currents when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed at the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. The amount of error these external filter resistor add to the measurement can be calculated using Equation 2 where the gain error factor is calculated using Equation 1.

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance value as well as the internal input resistors, R3 and R4 (or $R_{INT}$ as shown in Figure 21). The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. The equation used to calculate the expected deviation from the shunt voltage to what is seen at the device input pins is given in Equation 1:

$$\text{Gain Error Factor} = \frac{(1250 \times R_{INT})}{(1250 \times R_S) + (1250 \times R_{INT}) + (R_S \times R_{INT})}$$

where:

$R_{INT}$ is the internal input resistor (R3 and R4), and

$R_S$ is the external series resistance. (1)

With the adjustment factor equation including the device internal input resistance, this factor varies with each gain version, as shown in Table 1. Each individual device gain error factor is shown in Table 2.

**Table 1. Input Resistance**

| PRODUCT | GAIN | $R_{INT}$ (kΩ) |
|---|---|---|
| INA199A1 | 50 | 20 |
| INA199B1 | 50 | 20 |
| INA199A2 | 100 | 10 |
| INA199B2 | 100 | 10 |
| INA199A3 | 200 | 5 |
| INA199B3 | 200 | 5 |

**Table 2. Device Gain Error Factor**

| PRODUCT | SIMPLIFIED GAIN ERROR FACTOR |
|---|---|
| INA199A1 | $\frac{20,000}{(17 \times R_S) + 20,000}$ |
| INA199B1 | $\frac{20,000}{(17 \times R_S) + 20,000}$ |
| INA199A2 | $\frac{10,000}{(9 \times R_S) + 10,000}$ |
| INA199B2 | $\frac{10,000}{(9 \times R_S) + 10,000}$ |
| INA199A3 | $\frac{1000}{R_S + 1000}$ |
| INA199B3 | $\frac{1000}{R_S + 1000}$ |

The gain error that can be expected from the addition of the external series resistors can then be calculated based on Equation 2:

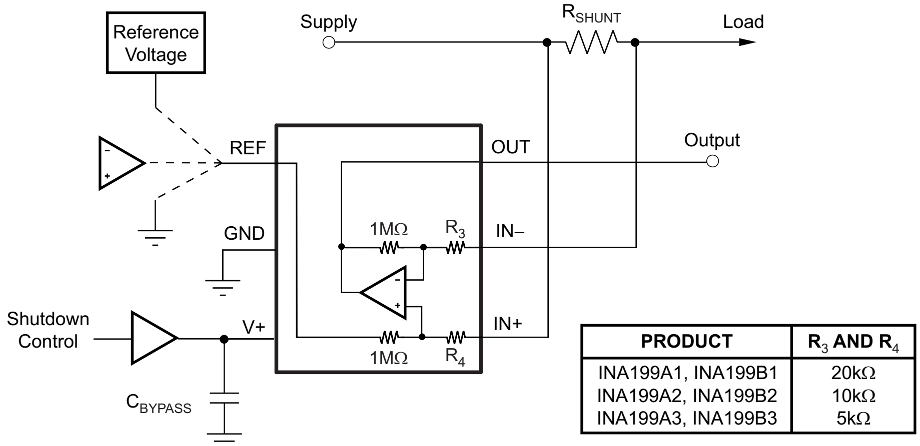
$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \qquad (2)$$

For example, using an INA199A2 or INA199B2 and the corresponding gain error equation from Table 2, a series resistance of 10Ω results in a gain error factor of 0.991. The corresponding gain error is then calculated using Equation 2, resulting in a gain error of approximately 0.89% solely because of the external 10Ω series resistors. Using an INA199A1 or INA199B1 with the same 10Ω series resistor results in a gain error factor of 0.991 and a gain error of 0.84% again solely because of these external resistors.

## SHUTTING DOWN THE INA199 SERIES

While the INA199 series does not have a shutdown pin, the low power consumption allows powering from the output of a logic gate or transistor switch that can turn on and turn off the INA199 power-supply quiescent current.

However, in current shunt monitoring applications. there is also a concern for how much current is drained from the shunt circuit in shutdown conditions. Evaluating this current drain involves considering the simplified schematic of the INA199 in shutdown mode shown in Figure 22.




| PRODUCT | $R_3$ AND $R_4$ |
|---|---|
| INA199A1, INA199B1 | 20kΩ |
| INA199A2, INA199B2 | 10kΩ |
| INA199A3, INA199B3 | 5kΩ |

NOTE: 1MΩ paths from shunt inputs to reference and INA199 outputs.

**Figure 22. Basic Circuit for Shutting Down INA199 with Grounded Reference**

Note that there is typically slightly more than 1MΩ impedance (from the combination of 1MΩ feedback and 5kΩ input resistors) from each input of the INA199 to the OUT pin and to the REF pin. The amount of current flowing through these pins depends on the respective ultimate connection. For example, if the REF pin is grounded, the calculation of the effect of the 1MΩ impedance from the shunt to ground is straightforward. However, if the reference or op amp is powered while the INA199 is shut down, the calculation is direct; instead of assuming 1MΩ to ground, however, assume 1MΩ to the reference voltage. If the reference or op amp is also shut down, some knowledge of the reference or op amp output impedance under shutdown conditions is required. For instance, if the reference source behaves as an open circuit when it is unpowered, little or no current flows through the 1MΩ path.

Regarding the 1MΩ path to the output pin, the output stage of a disabled INA199 does constitute a good path to ground; consequently, this current is directly proportional to a shunt common-mode voltage impressed across a 1MΩ resistor.

As a final note, when the device is powered up, there is an additional, nearly constant, and well-matched 25μA that flows in each of the inputs as long as the shunt common-mode voltage is 3V or higher. Below 2V common-mode, the only current effects are the result of the 1MΩ resistors.

## REF INPUT IMPEDANCE EFFECTS

As with any difference amplifier, the INA199 series common-mode rejection ratio is affected by any impedance present at the REF input. This concern is not a problem when the REF pin is connected directly to most references or power supplies. When using resistive dividers from the power supply or a reference voltage, the REF pin should be buffered by an op amp.

In systems where the INA199 output can be sensed differentially, such as by a differential input analog-to-digital converter (ADC) or by using two separate ADC inputs, the effects of external impedance on the REF input can be cancelled. Figure 23 depicts a method of taking the output from the INA199 by using the REF pin as a reference.

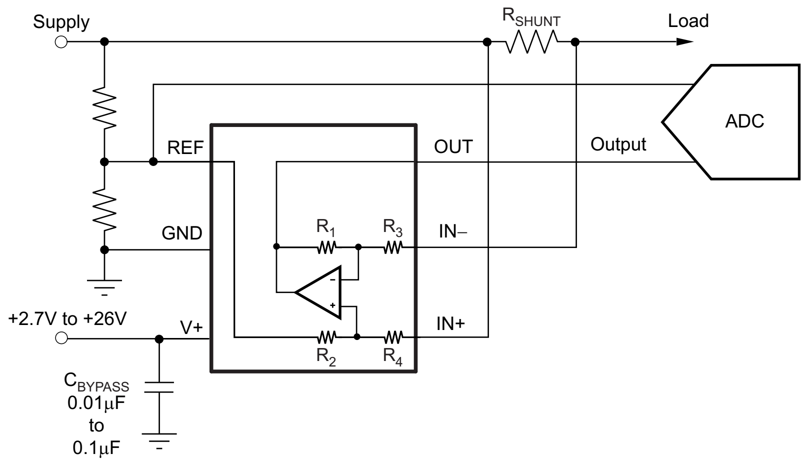



**Figure 23. Sensing INA199 to Cancel Effects of Impedance on the REF Input**

## USING THE INA199 WITH COMMON-MODE TRANSIENTS ABOVE 26V

With a small amount of additional circuitry, the INA199 series can be used in circuits subject to transients higher than 26V, such as automotive applications. Use only zener diode or zener-type transient absorbers (sometimes referred to as *Transzorbs*); any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors as shown in Figure 24 as a working impedance for the zener. It is desirable to keep these resistors as small as possible, most often around 10Ω. Larger values can be used with an effect on gain that is discussed in the section on input filtering. Because this circuit limits only short-term transients, many applications are satisfied with a 10Ω resistor along with conventional zener diodes of the lowest power rating that can be found. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

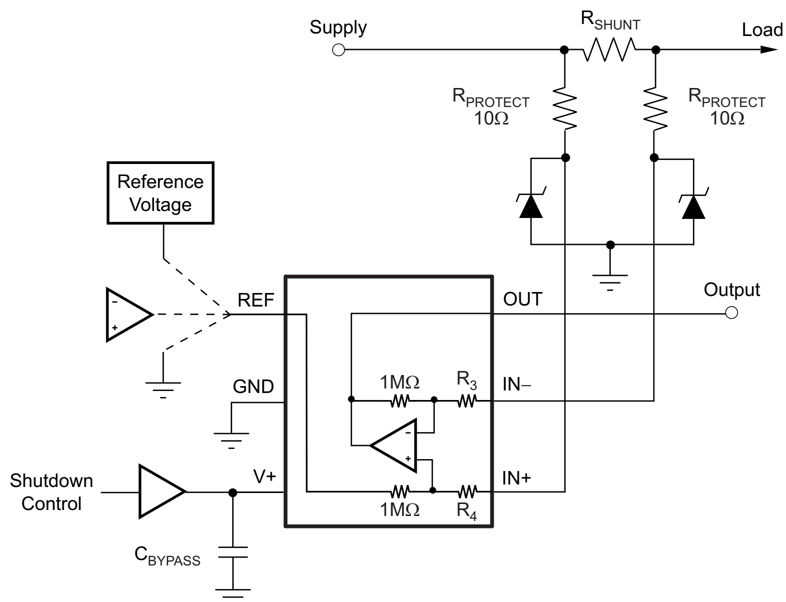



**Figure 24. INA199 Transient Protection Using Dual Zener Diodes**

In the event that low-power zeners do not have sufficient transient absorption capability and a higher power transzorb must be used, the most package-efficient solution then involves using a single transzorb and back-to-back diodes between the device inputs. This method is shown in Figure 25. The most space-efficient solutions are dual series-connected diodes in a single SOT-523 or SOD-523 package. In both examples shown in Figure 24 and Figure 25, the total board area required by the INA199 with all protective components is less than that of an SO-8 package, and only slightly greater than that of an MSOP-8 package.

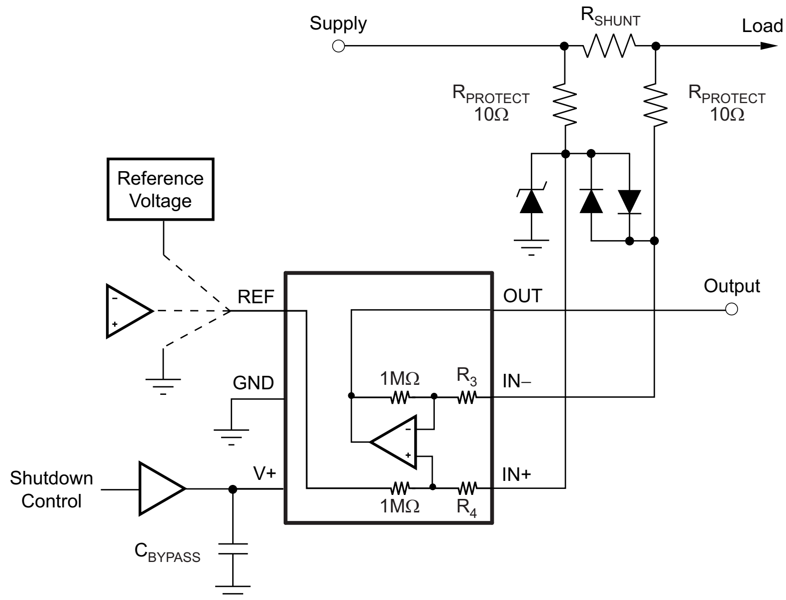



**Figure 25. INA199 Transient Protection Using a Single Transzorb and Input Clamps**

## IMPROVING TRANSIENT ROBUSTNESS

Applications involving large input transients with excessive dV/dt above 2kV per microsecond present at the device input pins may cause damage to the internal ESD structures on version A devices. This potential damage is a result of the internal latching of the ESD structure to ground when this transient occurs at the input. With significant current available in most current-sensing applications, the large current flowing through the input transient-triggered, ground-shorted ESD structure quickly results in damage to the silicon. External filtering can be used to attenuate the transient signal prior to reaching the inputs to avoid the latching condition. Care must be taken to ensure that external series input resistance does not significantly impact gain error accuracy. For accuracy purposes, these resistances should be kept under 10Ω if possible. Ferrite beads are recommended for this filter because of their inherently low dc ohmic value. Ferrite beads with less than 10Ω of resistance at dc and over 600Ω of resistance at 100MHz to 200MHz are recommended. The recommended capacitor values for this filter are between 0.01µF and 0.1µF to ensure adequate attenuation in the high-frequency region. This protection scheme is shown in Figure 26.

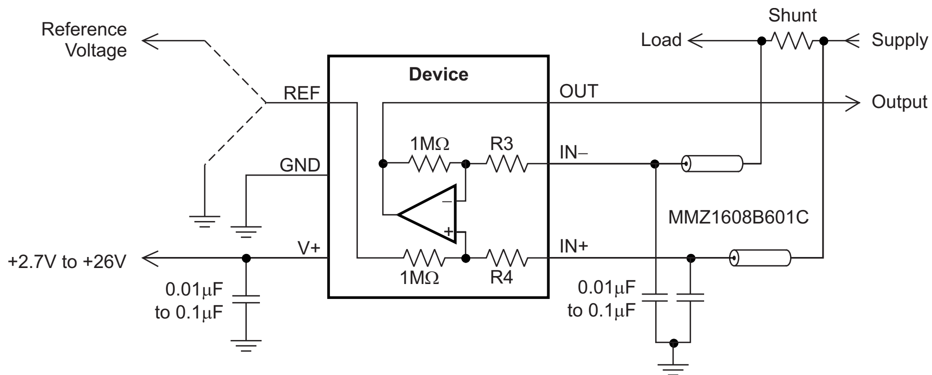



**Figure 26. Transient Protection**

To minimize the cost of adding these external components to protect the device in applications where large transient signals may be present, version B devices are now available with new ESD structures that are not susceptible to this latching condition. Version B devices are incapable of sustaining these damage causing latched conditions so they do not have the same sensitivity to the transients that the version A devices have, thus making the version B devices a better fit for these applications.

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision C (August 2012) to Revision D** **Page**

- Changed Frequency Response, *Bandwidth* parameter in Electrical Characteristics table ..... 3
- Updated Figure 21 ..... 10
- Updated Figure 22 ..... 12

**Changes from Revision B (February 2010) to Revision C** **Page**

- Added INA199Bx gains to fourth Features bullet ..... 1
- Added INA199Bx data to Product Family Table ..... 1
- Added INA199Bx data to Package Information table ..... 2
- Added silicon version B ESD ratings data to Absolute Maximum Ratings table ..... 2
- Added silicon version B data to Input, *Common-Mode Input Range* parameter of Electrical Characteristics table ..... 3
- Added QFN package information to *Temperature Range* section of *Electrical Characteristics* table ..... 3
- Updated Figure 3 ..... 5
- Updated Figure 9 ..... 6
- Updated Figure 12 ..... 6
- Changed last paragraph of the *Selecting* $R_S$ section to cover both INA199Ax and INA199Bx versions ..... 9
- Changed *Input Filtering* section ..... 10
- Added *Improving Transient Robustness* section ..... 16

**Changes from Revision A (June 2009) to Revision B** **Page**

- Deleted ordering information content from Package/Ordering table ..... 2
- Updated DCK pinout drawing ..... 4

**Changes from Original (May 2009) to Revision A** **Page**

- Added *ordering number* and *transport media, quantity* columns to *Package/Ordering Information* table ..... 2

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| INA199A1DCKR | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| INA199A1DCKT | ACTIVE | SC70 | DCK | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| INA199A1RSWR | ACTIVE | UQFN | RSW | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| INA199A1RSWT | ACTIVE | UQFN | RSW | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| INA199A2DCKR | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| INA199A2DCKT | ACTIVE | SC70 | DCK | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| INA199A2RSWR | ACTIVE | UQFN | RSW | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| INA199A2RSWT | ACTIVE | UQFN | RSW | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| INA199A3DCKR | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| INA199A3DCKT | ACTIVE | SC70 | DCK | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| INA199A3RSWR | ACTIVE | UQFN | RSW | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| INA199A3RSWT | ACTIVE | UQFN | RSW | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| INA199B1DCKR | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| INA199B1DCKT | ACTIVE | SC70 | DCK | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| INA199B2DCKR | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| INA199B2DCKT | ACTIVE | SC70 | DCK | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| INA199B3DCKR | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| INA199B3DCKT | ACTIVE | SC70 | DCK | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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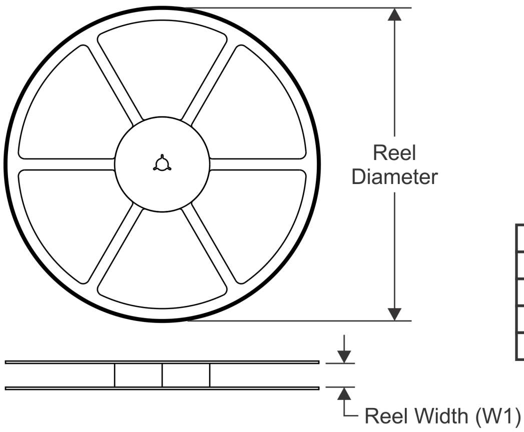
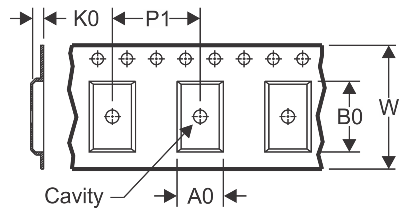
## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

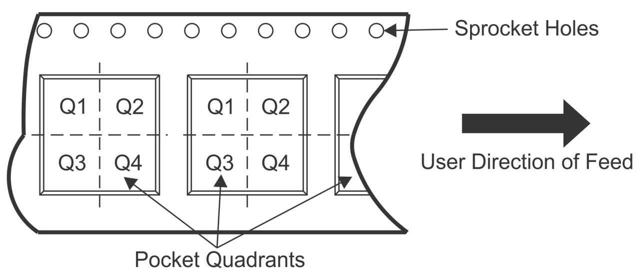



### TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

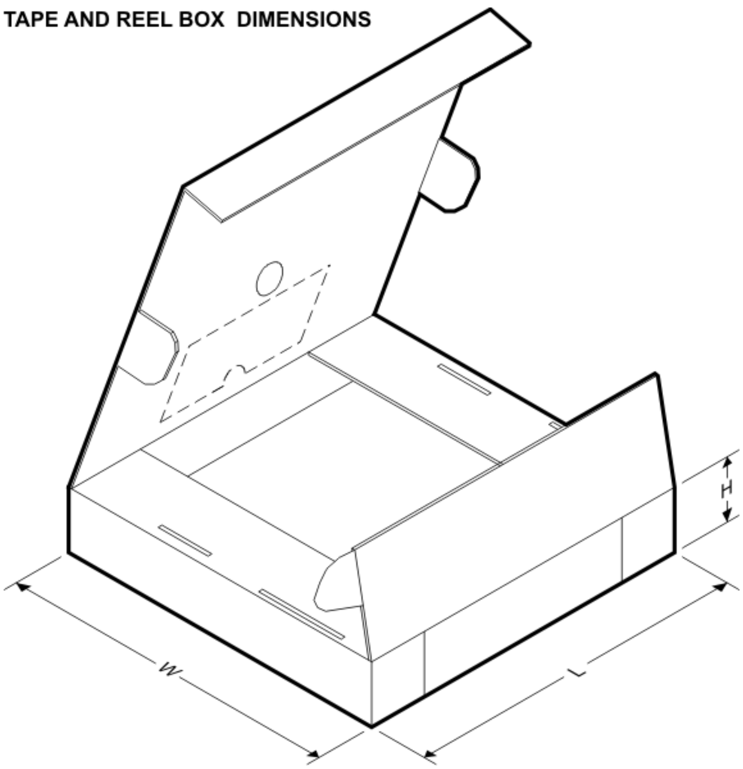



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| INA199A1DCKR | SC70 | DCK | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199A1DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199A1DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| INA199A1DCKT | SC70 | DCK | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199A1DCKT | SC70 | DCK | 6 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199A1RSWR | UQFN | RSW | 10 | 3000 | 179.0 | 8.4 | 1.7 | 2.1 | 0.7 | 4.0 | 8.0 | Q1 |
| INA199A1RSWT | UQFN | RSW | 10 | 250 | 179.0 | 8.4 | 1.7 | 2.1 | 0.7 | 4.0 | 8.0 | Q1 |
| INA199A2DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| INA199A2DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199A2DCKR | SC70 | DCK | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199A2DCKT | SC70 | DCK | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199A2DCKT | SC70 | DCK | 6 | 250 | 180.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| INA199A2DCKT | SC70 | DCK | 6 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199A2RSWR | UQFN | RSW | 10 | 3000 | 179.0 | 8.4 | 1.7 | 2.1 | 0.7 | 4.0 | 8.0 | Q1 |
| INA199A2RSWT | UQFN | RSW | 10 | 250 | 179.0 | 8.4 | 1.7 | 2.1 | 0.7 | 4.0 | 8.0 | Q1 |
| INA199A3DCKR | SC70 | DCK | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199A3DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199A3DCKT | SC70 | DCK | 6 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| INA199A3DCKT | SC70 | DCK | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199A3RSWR | UQFN | RSW | 10 | 3000 | 179.0 | 8.4 | 1.7 | 2.1 | 0.7 | 4.0 | 8.0 | Q1 |
| INA199A3RSWT | UQFN | RSW | 10 | 250 | 179.0 | 8.4 | 1.7 | 2.1 | 0.7 | 4.0 | 8.0 | Q1 |
| INA199B1DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199B1DCKT | SC70 | DCK | 6 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199B2DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199B2DCKT | SC70 | DCK | 6 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199B3DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199B3DCKT | SC70 | DCK | 6 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |

## TAPE AND REEL BOX DIMENSIONS

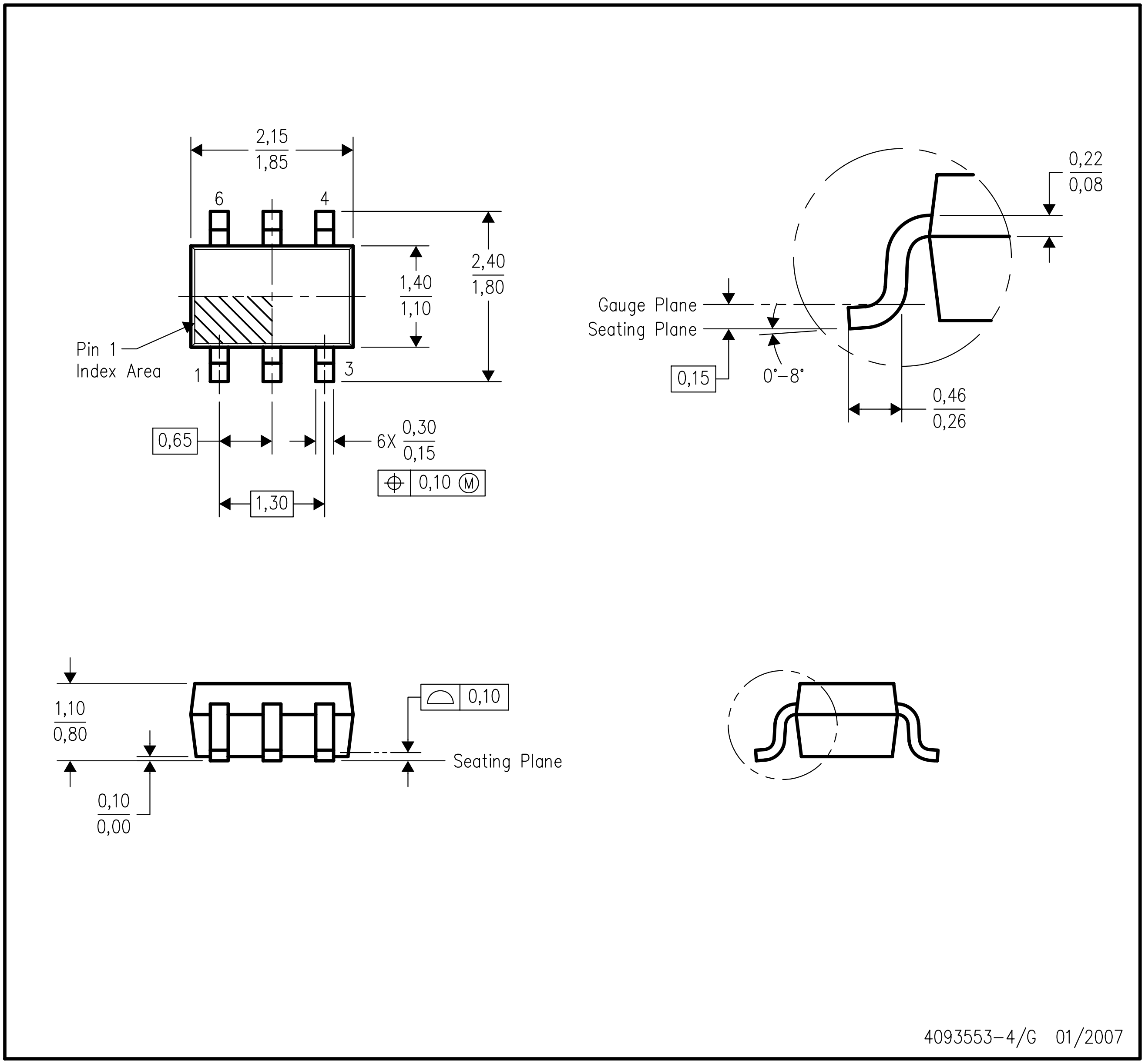



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| INA199A1DCKR | SC70 | DCK | 6 | 3000 | 195.0 | 200.0 | 45.0 |
| INA199A1DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| INA199A1DCKR | SC70 | DCK | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| INA199A1DCKT | SC70 | DCK | 6 | 250 | 195.0 | 200.0 | 45.0 |
| INA199A1DCKT | SC70 | DCK | 6 | 250 | 180.0 | 180.0 | 18.0 |
| INA199A1RSWR | UQFN | RSW | 10 | 3000 | 203.0 | 203.0 | 35.0 |
| INA199A1RSWT | UQFN | RSW | 10 | 250 | 203.0 | 203.0 | 35.0 |
| INA199A2DCKR | SC70 | DCK | 6 | 3000 | 202.0 | 201.0 | 28.0 |

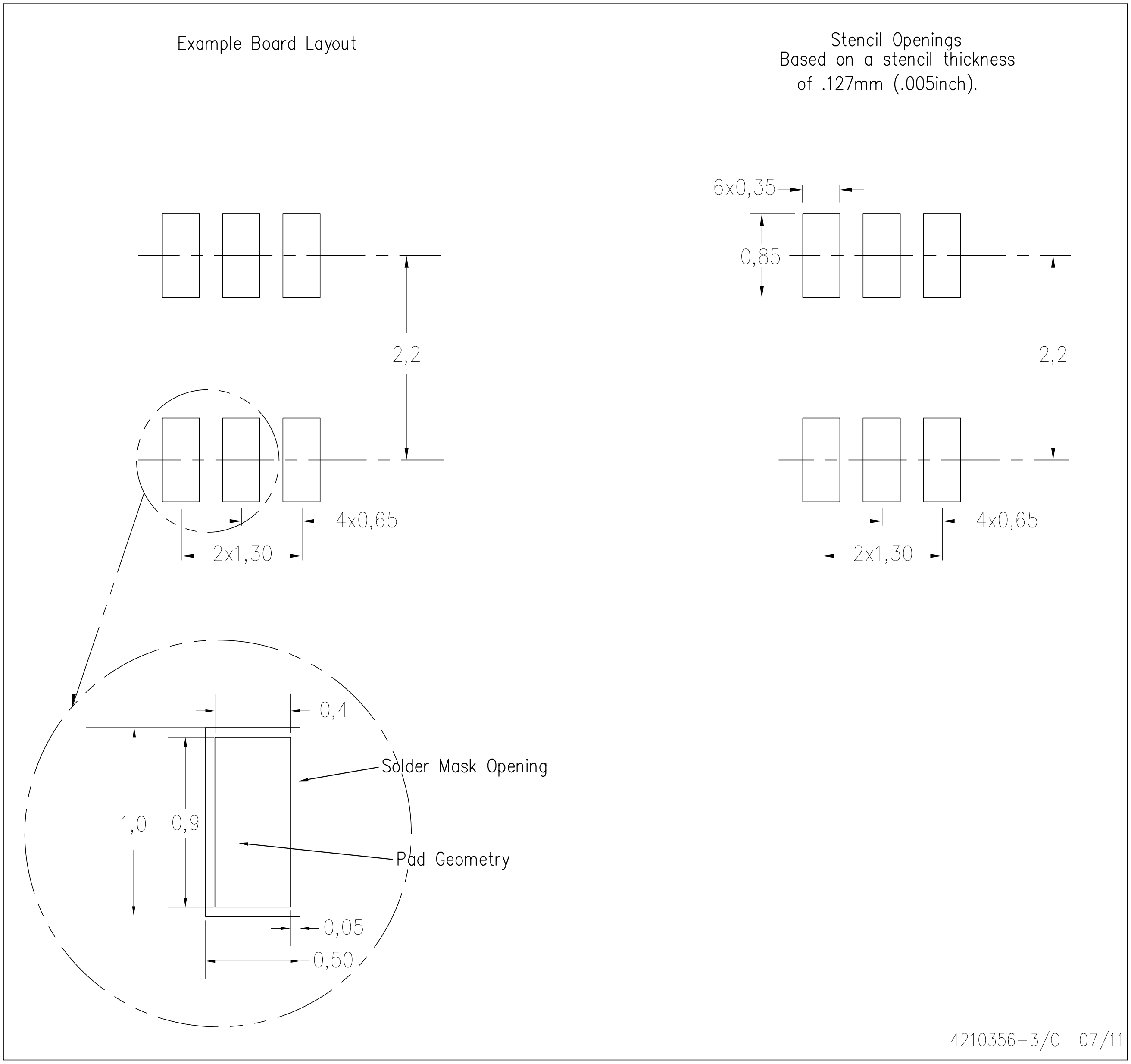
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| INA199A2DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| INA199A2DCKR | SC70 | DCK | 6 | 3000 | 195.0 | 200.0 | 45.0 |
| INA199A2DCKT | SC70 | DCK | 6 | 250 | 195.0 | 200.0 | 45.0 |
| INA199A2DCKT | SC70 | DCK | 6 | 250 | 202.0 | 201.0 | 28.0 |
| INA199A2DCKT | SC70 | DCK | 6 | 250 | 180.0 | 180.0 | 18.0 |
| INA199A2RSWR | UQFN | RSW | 10 | 3000 | 203.0 | 203.0 | 35.0 |
| INA199A2RSWT | UQFN | RSW | 10 | 250 | 203.0 | 203.0 | 35.0 |
| INA199A3DCKR | SC70 | DCK | 6 | 3000 | 195.0 | 200.0 | 45.0 |
| INA199A3DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| INA199A3DCKT | SC70 | DCK | 6 | 250 | 180.0 | 180.0 | 18.0 |
| INA199A3DCKT | SC70 | DCK | 6 | 250 | 195.0 | 200.0 | 45.0 |
| INA199A3RSWR | UQFN | RSW | 10 | 3000 | 203.0 | 203.0 | 35.0 |
| INA199A3RSWT | UQFN | RSW | 10 | 250 | 203.0 | 203.0 | 35.0 |
| INA199B1DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| INA199B1DCKT | SC70 | DCK | 6 | 250 | 180.0 | 180.0 | 18.0 |
| INA199B2DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| INA199B2DCKT | SC70 | DCK | 6 | 250 | 180.0 | 180.0 | 18.0 |
| INA199B3DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| INA199B3DCKT | SC70 | DCK | 6 | 250 | 180.0 | 180.0 | 18.0 |

DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



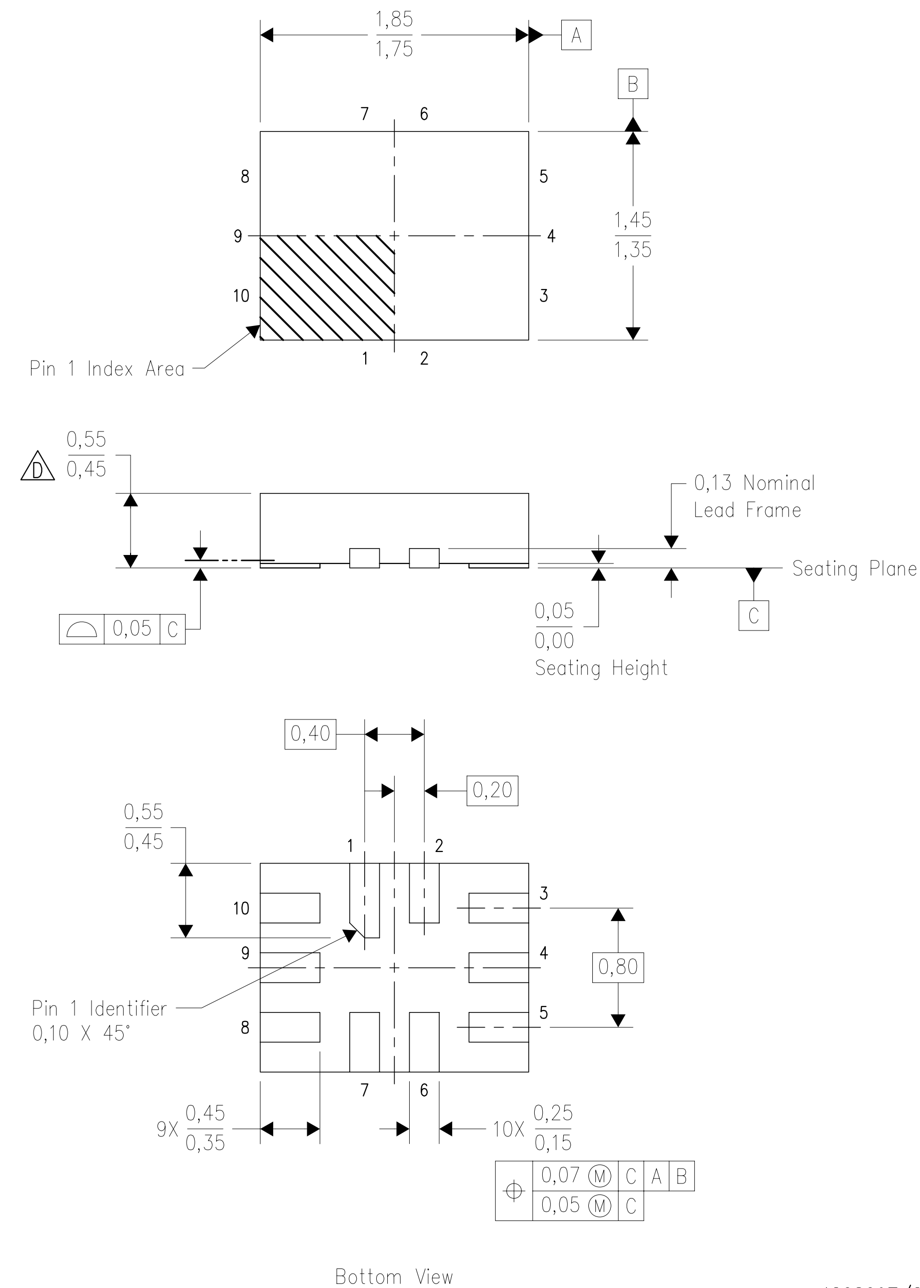

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE




NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

RSW (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD




4208097/C 07/2008

NOTES:

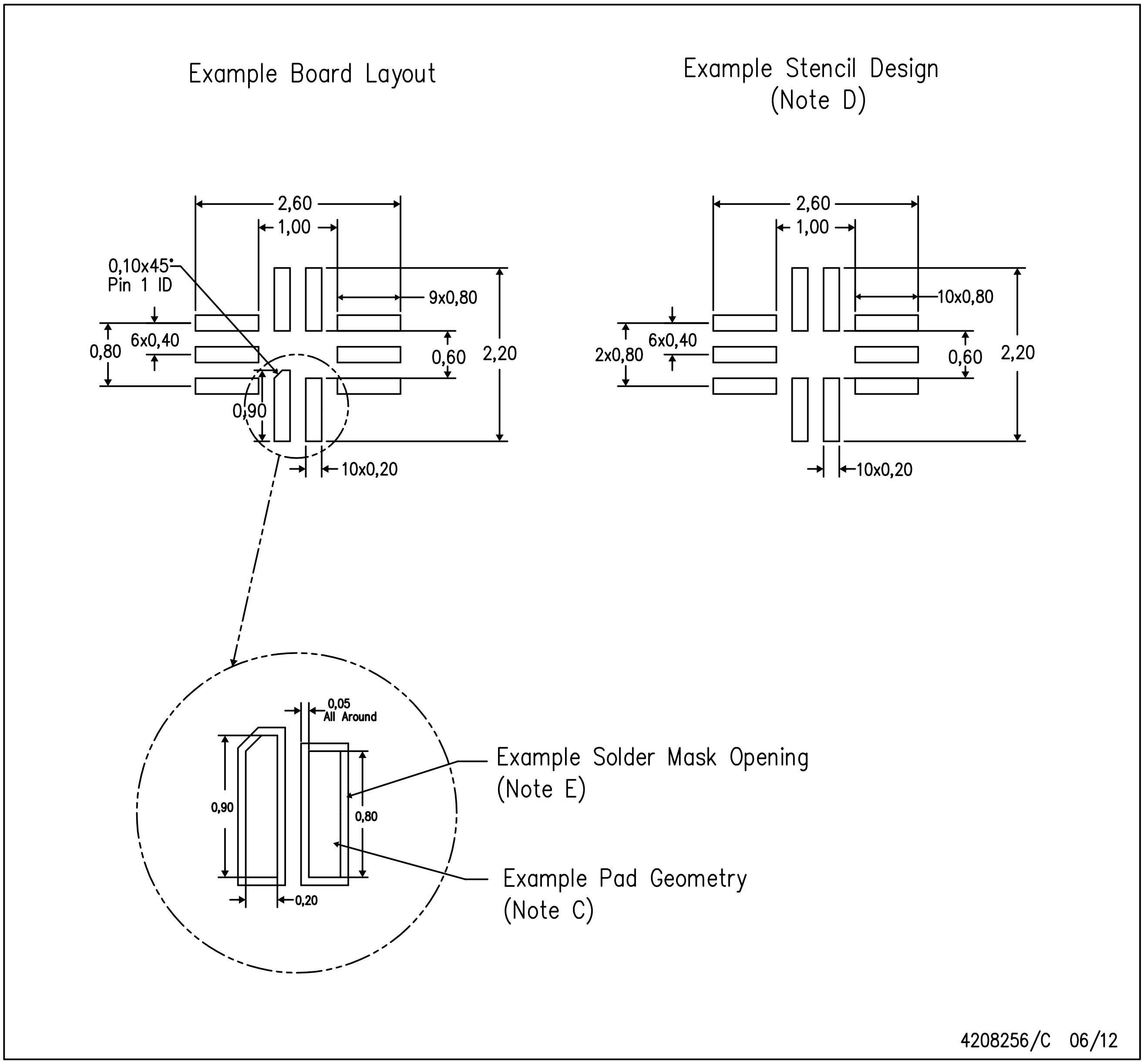
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.

B. This drawing is subject to change without notice.

C. QFN (Quad Flatpack No–lead) package configuration.

D. This package complies to JEDEC MO–288 variation UDEE, except minimum package height.

RSW (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.