

# Power MOSFET, 40 A



PRODUCT SUMMARY				
$V_{DSS}$	500 V			
R <sub>DS(on)</sub>	0.106 Ω			
I <sub>D</sub>	40 A			
Туре	Modules - MOSFET			
Package	SOT-227			

#### **FEATURES**

- Fully isolated package
- · Easy to use and parallel
- · Low on-resistance
- Dynamic dV/dt rating
- · Fully avalanche rated
- Simple drive requirements
- · Low drain to case capacitance
- · Low internal inductance
- UL approved file E78996





- · Designed for industrial level
- · Material categorization: For definitions of compliance please see www.vishav.com/doc?99912

#### **DESCRIPTION**

Third Generation Power MOSFETs from Vishay Semiconductors provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-227 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 500 W. The low thermal resistance of the SOT-227 contribute to its wide acceptance throughout the industry.

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS
Continuous drain surrent at V 10 V		T <sub>C</sub> = 25 °C	40	
Continuous drain current at V <sub>GS</sub> 10 V	I <sub>D</sub>	T <sub>C</sub> = 90 °C	29	Α
Pulsed drain current	I <sub>DM</sub> <sup>(1)</sup>		150	
Dower discipation	В	T <sub>C</sub> = 25 °C	543	W
Power dissipation	P <sub>D</sub>	T <sub>C</sub> = 90 °C	261	VV
Gate to source voltage	V <sub>GS</sub>		± 20	V
Single pulse avalanche energy	E <sub>AS</sub> (2)		400	mJ
Repetitive avalanche current	I <sub>AR</sub> (1)		13	Α
Repetitive avalanche energy	E <sub>AR</sub> (1)		42	mJ
Peak diode recovery dV/dt	dV/dt (3)		10	V/ns
Operating junction and storage temperature range	T <sub>J</sub> , T <sub>Stg</sub>		- 55 to + 150	°C
Insulation withstand voltage (AC-RMS)	V <sub>ISO</sub>		2.5	kV
Mounting torque		M4 screw, on terminals and heatsink	1.3	Nm

#### **Notes**

- (1) Repetitive rating; pulse width limited by maximum junction temperature (see fig. 18)
- $^{(2)}$  Starting  $T_J$  = 25 °C, L = 500  $\mu H,\,R_g$  = 2.4  $\Omega,\,I_{AS}$  = 40 A (see fig. 18)
- $^{(3)}$   $I_{SD} \leq 40$  A,  $dI_F/dt \leq 200$  A/µs,  $V_{DD} \stackrel{<}{\leq} V_{(BR)DSS}, \, T_J \leq 150 \,\, ^{\circ}C$



THERMAL - MECHANICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Junction and storage temperature range	T <sub>J</sub> , T <sub>Stg</sub>		- 55	-	150	°C
Junction to case	R <sub>thJC</sub>		-	-	0.23	°C/W
Case to heatsink	R <sub>thCS</sub>	Flat, greased surface	-	0.05	-	C/VV
Weight			-	30	-	g
Mounting torque			-	-	1.3	Nm
Case style			SOT-227			

<b>ELECTRICAL CHARACTERISTCS</b> (T <sub>J</sub> = 25 °C unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Drain to source breakdown voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1.0 mA	500	-	-	V
Breakdown voltage temperature coefficient	$\Delta V_{(BR)DSS}/\Delta T_{J}$	Reference to 25 °C, I <sub>D</sub> = 1 mA	-	0.65	-	V/°C
Static drain to source on-resistance	R <sub>DS(on)</sub> (1)	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 23 A	-	106	130	mΩ
Gate threshold voltage	M	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	2	3	4	V
Gate theshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$ , $T_J = 125  ^{\circ} C$	-	1.9	-	]
Forward transconductance	9 <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 23 A	-	29	-	S
		V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V	-	0.5	50	μΑ
Drain to source leakage current	I <sub>DSS</sub>	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	30	500	
		V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C	-	0.2	3	mA
Gate to source forward leakage		V <sub>GS</sub> = 20 V	-	-	200	nΛ
Gate to source reverse leakage	I <sub>GSS</sub>	V <sub>GS</sub> = - 20 V	-	-	- 200	nA
Total gate charge	Qg	I <sub>D</sub> = 38 A		280	420	
Gate to source charge	Q <sub>gs</sub>	V <sub>DS</sub> = 400 V	-	37	55	nC
Gate to drain ("Miller") charge	Q <sub>gd</sub>	V <sub>GS</sub> = 10 V; see fig. 15 and 19 <sup>(1)</sup>	-	150	220	1
Turn-on delay time	t <sub>d(on)</sub>		-	143	-	
Rise time	$t_r$ $V_{DD} = 250 \text{ V}, I_D = 40 \text{ A}, R_g = 2.4 \Omega,$		-	33	-	]
Turn-off delay time	t <sub>d(off)</sub>	L = 500 μH, diode used: 60APH06	-	107	-	ns
Fall time	t <sub>f</sub>		-	36	-	
Turn-on delay time	t <sub>d(on)</sub>		-	145	-	
Rise time	t <sub>r</sub>	$V_{DD} = 250 \text{ V}, I_D = 40 \text{ A}, R_g = 2.4 \Omega,$	-	35	-	
Turn-off delay time	t <sub>d(off)</sub>	L = 500 $\mu$ H, T <sub>J</sub> = 125 °C, diode used: 60APH06	-	110	-	ns
Fall time	t <sub>f</sub>		-	40	-	
Internal source inductance	L <sub>S</sub>	Between lead, and center of die contact	-	5	-	nH
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	-	6900	-	
Output capacitance	Coss	V <sub>DS</sub> = 25 V	-	1600	-	pF
Reverse transfer capacitance	C <sub>rss</sub>	f = 1.0 MHz, see fig. 14	-	580	-	1

#### Note

 $^{(1)}~$  Pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%$ 



SOURCE-DRAIN RATINGS AND CHARACTERISTICS						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Continuous source current (body diode)	IS	MOSFET symbol showing the integral reverse	ı	-	38	A
Pulsed source current (body diode)	I <sub>SM</sub> <sup>(1)</sup>	p-n junction diode.	-	-	150	
Diode forward voltage V <sub>SD</sub> (2)	V (2)	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 38 A, V <sub>GS</sub> = 0 V	=	0.9	1.31	V
	VSD (=)	$T_J = 125  ^{\circ}\text{C},  I_S = 38  \text{A},  V_{GS} = 0  \text{V}$	=.	0.75	-	
Reverse recovery time	t <sub>rr</sub>		=.	560	-	ns
Reverse recovery current	I <sub>rr</sub>	$T_J = 25  ^{\circ}\text{C}, \ I_F = 40  \text{A}; \ dI_F/dt = 100  \text{A/}\mu\text{s}^{(2)}$	=.	40	-	Α
Reverse recovery charge	Q <sub>rr</sub>		-	11	-	μC
Reverse recovery time	t <sub>rr</sub>		-	680	-	ns
Reverse recovery current	I <sub>rr</sub>	$T_J = 25  ^{\circ}\text{C}, \ I_F = 40  \text{A}; \ dI_F/dt = 100  \text{A/}\mu\text{s}^{(2)}$	-	47	-	Α
Reverse recovery charge	Q <sub>rr</sub>	1	-	16	-	μC
Forward turn-on time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> + L <sub>D</sub> )				

#### **Notes**

- (1) Repetitive rating; pulse width limited by maximum junction temperature (see fig. 18)
- (2) Pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %

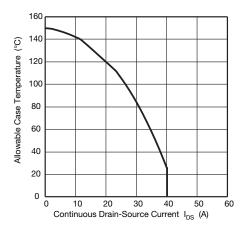


Fig. 1 - Maximum DC MOSFET Drain-Source Current vs. Case Temperature

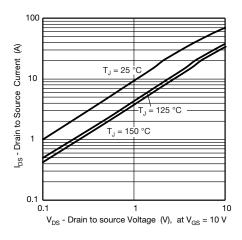


Fig. 2 - Typical Drain-to-Source Current Output Characteristics;  $V_{\text{GS}} = 10~\text{V}$ 

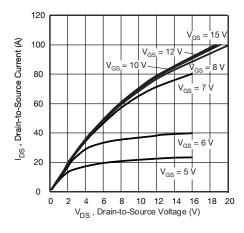


Fig. 3 - Typical Drain-to-Source Current Output Characteristics at  $T_J = 25\ ^{\circ}\text{C}$ 

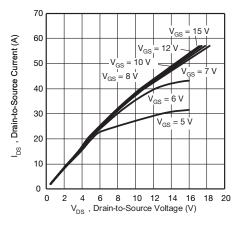


Fig. 4 - Typical Drain-to-Source Current Output Characteristics at  $T_J = 125\ ^{\circ}\text{C}$ 



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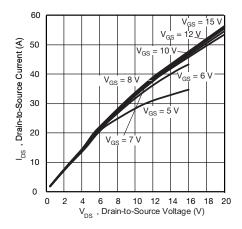


Fig. 5 - Typical Drain-to-Source Current Output Characteristics at  $T_{\rm J}$  = 150  $^{\circ}$ C

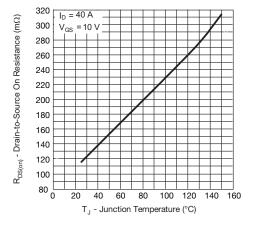


Fig. 6 - Normalized On-Resistance vs. Temperature

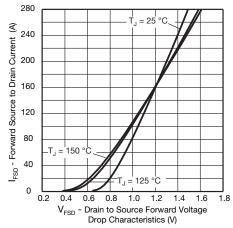


Fig. 7 - Typical Body Diode Forward Voltage Drop Characeristics

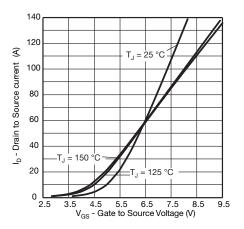


Fig. 8 - Typical MOSFET Transfer Characteristics

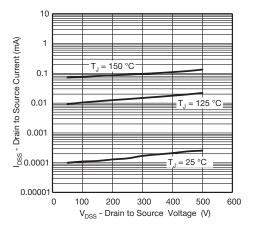


Fig. 9 - Typical MOSFET Zero Gate Voltage Drain Current

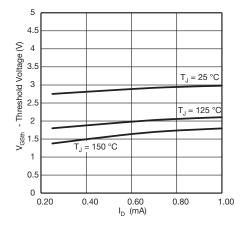


Fig. 10 - Typical MOSFET Threshold Voltage



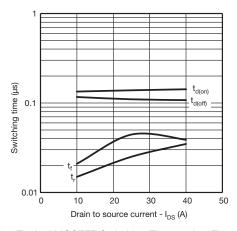


Fig. 11 - Typical MOSFET Switching Time vs. I<sub>DS</sub>, T<sub>J</sub> = 125 °C, V<sub>DD</sub> = 250 V, V<sub>GS</sub> = 10 V, L = 500  $\mu$ H, R<sub>G</sub> = 2.4  $\Omega$  Diode used 60APH06

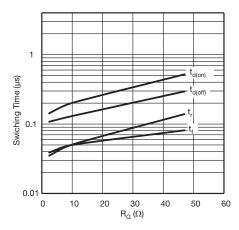


Fig. 12 - Typical MOSFET Switching Time vs. R<sub>G</sub>, T<sub>J</sub> = 125 °C, I<sub>DS</sub> = 40 A , V<sub>DD</sub> = 250 V, V<sub>GS</sub> = 10 V, L = 500  $\mu$ H Diode used 60APH06

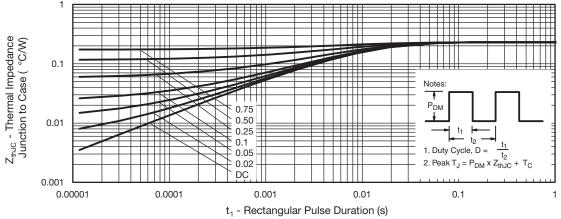


Fig. 13 - Maximum Thermal Impedance Z<sub>thJC</sub> Characteristics, MOSFET

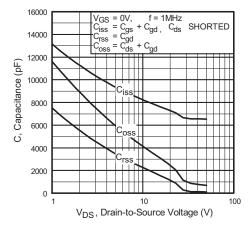


Fig. 14 - Typical Capacitance vs. Drain to Source Voltage

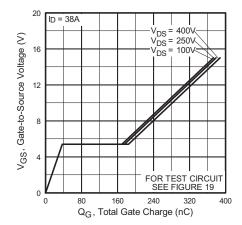


Fig. 15 - Typical Gate Charge vs. Gate to Source Voltage

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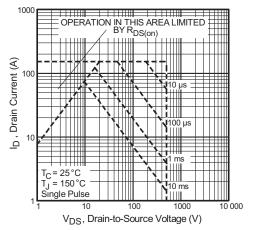


Fig. 16 - Maximum Safe Operating Area

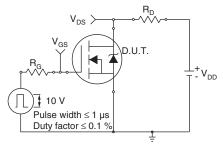


Fig. 17 - Switching Time Test Circuit

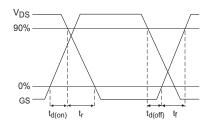


Fig. 18 - Switching Time Waveforms

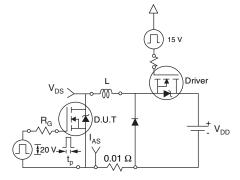


Fig. 19 - Unclamped Inductive Test Circuit

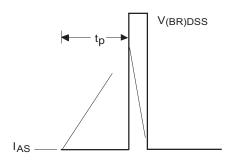


Fig. 20 - Unclamped Inductive Waveforms

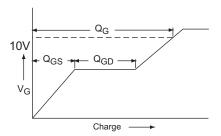


Fig. 21 - Basic Gate Charge Waveform

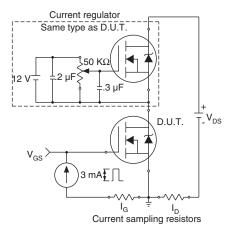


Fig. 22 - Gate Charge Test Circuit

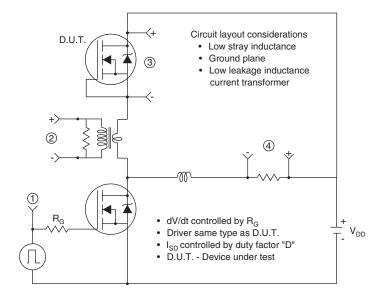
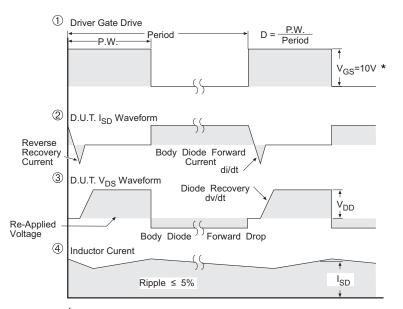


Fig. 23 - Peak Diode Recovery dV/dt Test Circuit

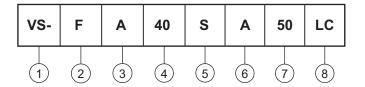


\*  $V_{GS}$  = 5V for Logic Level Devices

Fig. 24 - For N-Channel Power MOSFETs

#### **ORDERING INFORMATION TABLE**

Device code



- 1 Vishay Semiconductors product
- 2 Power MOSFET
- 3 A = Generation 3, MOSFET silicon die
- 4 Current rating (40 = 40 A)
- 5 Single switch
- 6 Package indicator (SOT-227)
- 7 Voltage rating (50 = 500 V)
- 8 LC = Low charge

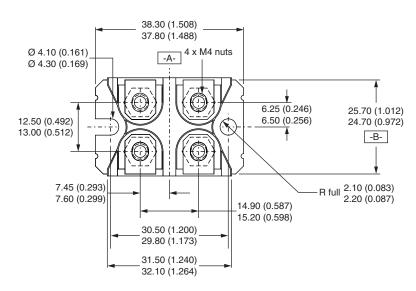
CIRCUIT CONFIGURATION				
CIRCUIT	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING		
Single switch	S	D (3)  3 2 (D) (G) (O) (D)  4 4 1 (S) (S) (G) (G)		

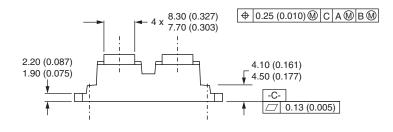
LINKS TO RELATED DOCUMENTS					
Dimensions www.vishay.com/doc?95423					
Packaging information	www.vishay.com/doc?95425				

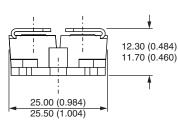


### **SOT-227 Generation II**

#### **DIMENSIONS** in millimeters (inches)







#### Note

• Controlling dimension: millimeter



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Vishay

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