# 0.3 Ω, Low Voltage Dual SPDT Analog Switches

## DESCRIPTION

The DG2535E and DG2733E are low voltage, low on-resistance, dual single-pole/double-throw (SPDT) monolithic CMOS analog switches designed for high performance switching of analog signals. Combining low-power, high speed, low on-resistance, and small package size, the DG2535E and DG2733E are ideal for portable and battery powered applications.

The DG2535E and DG2733E have an operation range from 1.65 V to 5.5 V single supply. The DG2535E has two separate control pins for independent control of the two SPDT switches. The DG2733E has an EN pin to enable the device when the logic is high.

The DG2535E and DG2733E have guaranteed 1.65 V logic compatible, allowing easy interface with low voltage DSP or MCU control logic.

The switches conduct signals within the power rails equally well in both directions when on, and blocks up to the power supply level when off. Break-before-make is guaranteed.

The DG2535E and DG2733E are built on Vishay Siliconix's sub micron CMOS low voltage process technology and provide greater than 400 mA latch-up protection, as tested per JESD78A.

The DG2535E and DG2733E are available in lead (Pb)-free 10-lead DFN and SOIC packages.

## FEATURES

- 1.65 V to 5.5 V single power operation
- 0.3 Ω typ. switch on resistance at V+ = 5 V
- Fast switching:
  $t_{ON}$ = 55 ns at 2.7 V, $t_{OFF}$ = 15 ns at 2.7 V
- Latch-up current > 400 mA (JESD78)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE

## BENEFITS

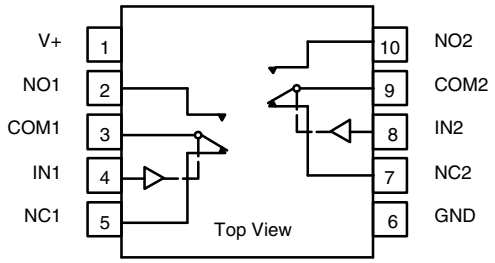
- Low switch resistance
- Low voltage logic compatible
- Wide operation voltage range
- Fast switching time

## APPLICATIONS

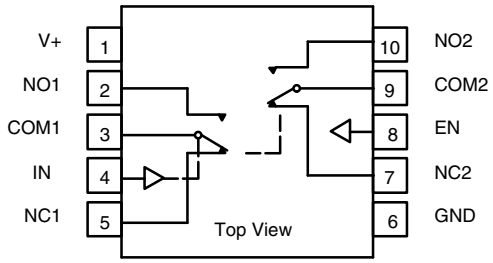
- Audio and video signal routing
- Battery operated systems
- Relay replacement
- Automatic test equipment
- Process control and automation
- Data acquisition systems
- Meters and instruments
- Medical and healthcare systems
- PCMCIA cards
- Communication systems

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG2535E




DG2733E




| TRUTH TABLE DG2535E | | |
|---|---|---|
| IN1, IN2 | NC1, NC2 | NO1, NO2 |
| 0 | ON | OFF |
| 1 | OFF | ON |

| TRUTH TABLE DG2733E | | | |
|---|---|---|---|
| IN | EN | NC1, NC2 | NO1, NO2 |
| 0 | 1 | ON | OFF |
| 1 | 1 | OFF | ON |
| 0 | 0 | OFF | OFF |
| 1 | 0 | OFF | OFF |

| ORDERING INFORMATION | | |
|---|---|---|
| **TEMP. RANGE** | **PACKAGE** | **PART NUMBER** |
| -40 °C to +85 °C | MSOP10 | DG2535EDQ-T1-GE3 |
| | | DG2733EDQ-T1-GE3 |
| | DFN-10 | DG2535EDN-T1-GE4 |
| | | DG2733EDN-T1-GE4 |

| **ABSOLUTE MAXIMUM RATINGS** ($T_A$ = 25 °C, unless otherwise noted) | | | | |
|---|---|---|---|---|
| **PARAMETER** | | **SYMBOL** | **LIMIT** | **UNIT** |
| Reference to GND | V+ | | -0.3 V to +6 V | V |
| | IN, COM, NC, NO [a] | | -0.3 V to (V+ + 0.3) | |
| Current (any terminal except NO, NC or COM) | | | 30 | mA |
| Continuous current (NO, NC, or COM) | | | ± 300 | |
| Peak current (pulsed at 1 ms, 10 % duty cycle) | | | ± 500 | |
| Storage temperature (D suffix) | | | -65 to +150 | °C |
| Power dissipation (packages) [b] | miniQFN10 [c] | | 208 | mW |
| Latch up current | | JESD78A | > 400 | mA |
| ESD - HBM | | ANSI / ESDA / JEDEC® JS-001 | > 5000 | V |
| ESD - CDM | | JESD22-C101 | > 1000 | |
| ESD - MM | | JESD22-A115 | > 200 | |

**Notes**

a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 4 mW/C above 70 °C.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

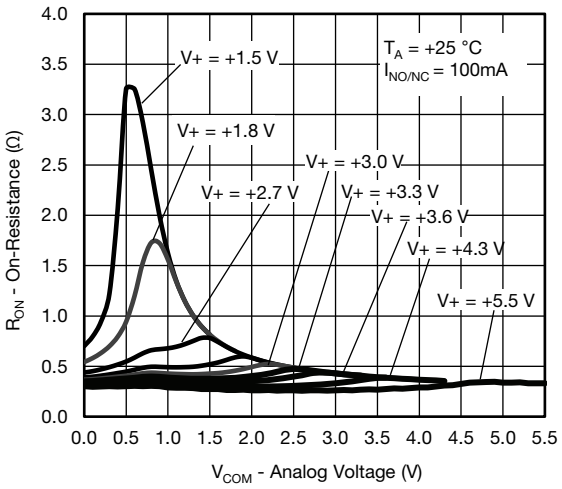
## SPECIFICATIONS

| PARAMETER | SYMBOL | TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 3 V, ± 10 %, $V_{IN}$ = 0.4 V or 1.65 V [e] | TEMP. [a] | LIMITS -40 °C to +85 °C MIN. [b] | TYP. [c] | MAX. [b] | UNIT |
|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | |
| Analog signal range [d] | $V_{analog}$ | $R_{DS(on)}$ | Full | 0 | - | V+ | V |
| On-resistance | $R_{DS(on)}$ | V+ = 2.7 V, $I_{NO/NC}$ = 100 mA, $V_{COM}$ = 0.5 V | Room | - | 0.5 | 0.7 | Ω |
| | | V+ = 2.7 V, $I_{NO/NC}$ = 100 mA, $V_{COM}$ = 1.5 V | | | | | |
| | | V+ = 2.7 V, $I_{NO/NC}$ = 100 mA, $V_{COM}$ = 0.5 V | Full | - | 0.6 | - | |
| | | V+ = 2.7 V, $I_{NO/NC}$ = 100 mA, $V_{COM}$ = 1.5 V | | | | | |
| | | V+ = 5.5 V, $I_{NO/NC}$ = 100 mA, $V_{COM}$ = 0.9 V | Room | - | 0.3 | 0.5 | |
| | | V+ = 5.5 V, $I_{NO/NC}$ = 100 mA, $V_{COM}$ = 2.5 V | | | 0.25 | | |
| | | V+ = 5.5 V, $I_{NO/NC}$ = 100 mA, $V_{COM}$ = 0.9 V | Full | - | 0.4 | - | |
| | | V+ = 5.5 V, $I_{NO/NC}$ = 100 mA, $V_{COM}$ = 2.5 V | | | | | |
| $R_{ON}$ match [d] | $\Delta R_{ON}$ | V+ = 2.7 V, $I_{NO/NC}$ = 100 mA, $V_{COM}$ = 0.5 V, 1.5 V | Room | - | 0.06 | 0.08 | |
| | | V+ = 5.5 V, $I_{NO/NC}$ = 100 mA, $V_{COM}$ = 0.9 V, 2.5 V | | | | | |
| $R_{ON}$ resistance flatness [d] | $R_{ON}$ flatness | V+ = 2.7 V, $I_{NO/NC}$ = 100 mA, $V_{COM}$ = 0.5 V, 1.5 V | Room | - | - | 0.15 | |
| Switch off leakage current | $I_{NO/NC(off)}$ | V+ = 5 V, $V_{NO/NC}$ = 0.5 V / 4.5 V, $V_{COM}$ = 4.5 V / 0.5 V | Room | -8 | - | 8 | nA |
| | | | Full | -50 | - | 50 | |
| | $I_{COM(off)}$ | | Room | -8 | - | 8 | |
| | | | Full | -50 | - | 50 | |
| Channel-on leakage current | $I_{COM(on)}$ | V+ = 5 V, $V_{NO/NC}$ = $V_{COM}$ = 4.5 V / 0.5 V | Room | -10 | - | 10 | |
| | | | Full | -50 | - | 50 | |
| **Digital Control** | | | | | | | |
| Input high voltage | $V_{INH}$ | V+ = 3 V | Full | 1.65 | - | - | V |
| Input low voltage | $V_{INL}$ | | Full | - | - | 0.4 | |
| Input high voltage | $V_{INH}$ | V+ = 5 V | Full | 1.8 | - | - | |
| Input low voltage | $V_{INL}$ | | Full | - | - | 0.6 | |
| Input capacitance | $C_{IN}$ | | Full | - | 6 | - | pF |
| Input current | $I_{INL}$ or $I_{INH}$ | $V_{IN}$ = 0 or V+ | Full | -1 | - | 1 | µA |
| **Dynamic Characteristics** | | | | | | | |
| Break-Before-Make time [e] | $t_{BBM}$ | V+ = 3.6 V, $V_{NO}$, $V_{NC}$ = 1.5 V, $R_L$ = 50 Ω, $C_L$ = 35 pF | Room | 1 | 15 | - | ns |
| Turn-on time [e] | $t_{ON}$ | | Room | - | 28 | 78 | |
| | | | Full | - | - | 80 | |
| Turn-off time [e] | $t_{OFF}$ | | Room | - | 13 | 58 | |
| | | | Full | - | - | 60 | |
| Off-isolation [d] | OIRR | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 100 kHz | Room | - | -70 | - | dB |
| Crosstalk [d] | $X_{TALK}$ | | | - | -90 | - | |
| 3 dB bandwidth [d] | | $R_L$ = 50 Ω, $C_L$ = 5 pF | Room | - | 120 | - | MHz |
| NO, NC off capacitance [d] | $C_{NO(off)}$ | $V_{IN}$ = 0 V, or V+, f = 1 MHz | Room | - | 40 | - | pF |
| | $C_{NC(off)}$ | | | - | 40 | - | |
| Channel on capacitance [d] | $C_{NO(on)}$ | | | - | 120 | - | |
| | $C_{NC(on)}$ | | | - | 120 | - | |
| **Power Supply** | | | | | | | |
| Power supply range | V+ | | - | 1.65 | - | 5.5 | V |
| Power supply current | I+ | $V_{IN}$ = 0 or V+ | Full | - | - | 1 | µA |

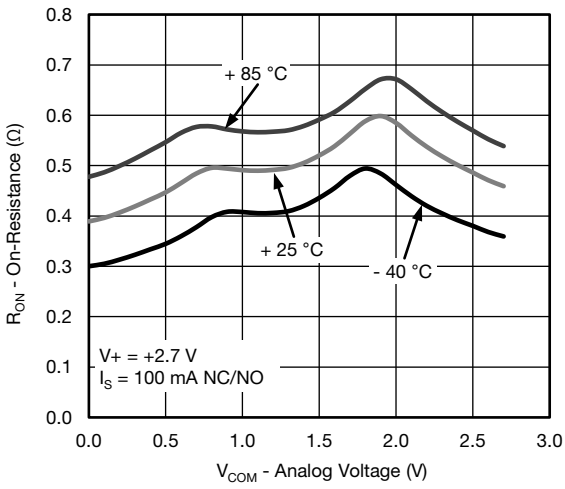
**Notes**

a. Room = 25 °C, Full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, not subjected to production test.
e. $V_{IN}$ = input voltage to perform proper function.

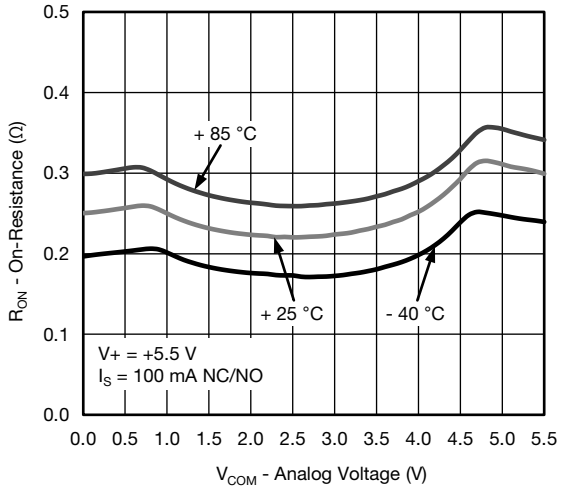
## TYPICAL CHARACTERISTICS ($T_A$ = 25 °C, unless otherwise noted)



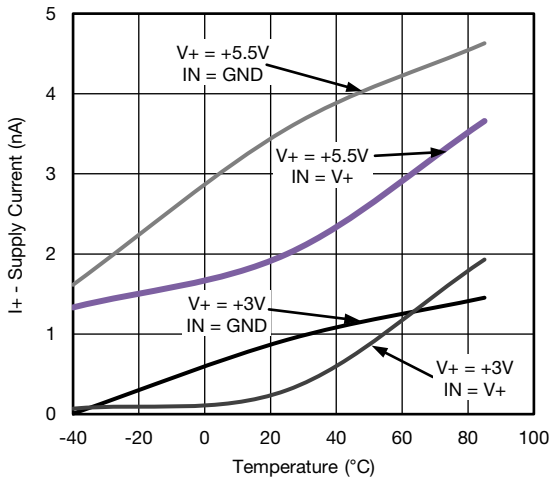

**$R_{ON}$ vs. $V_{COM}$ and Supply Voltage**




**$R_{ON}$ vs. Analog Voltage and Temperature**

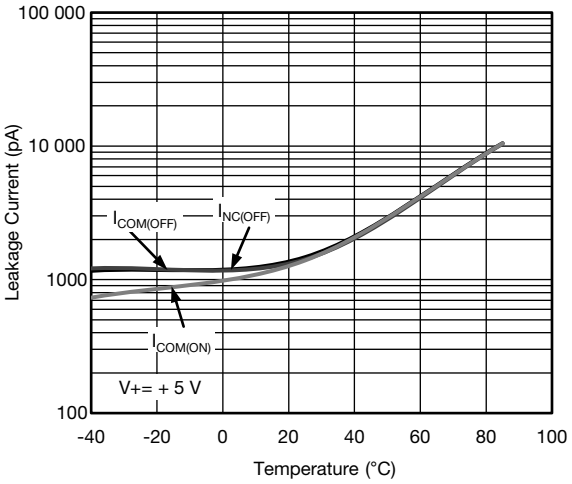



**$R_{ON}$ vs. Analog Voltage and Temperature**

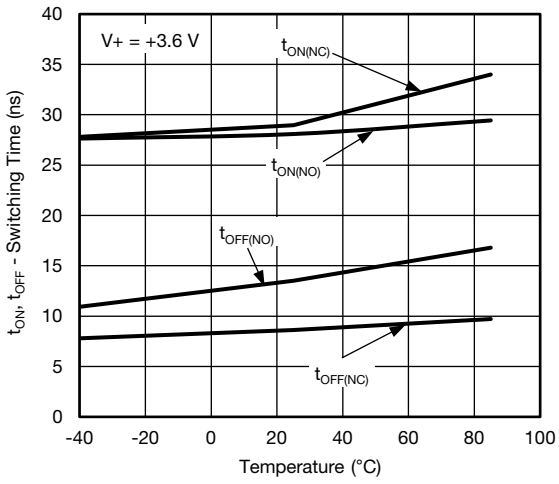



**Supply Current vs. Temperature**

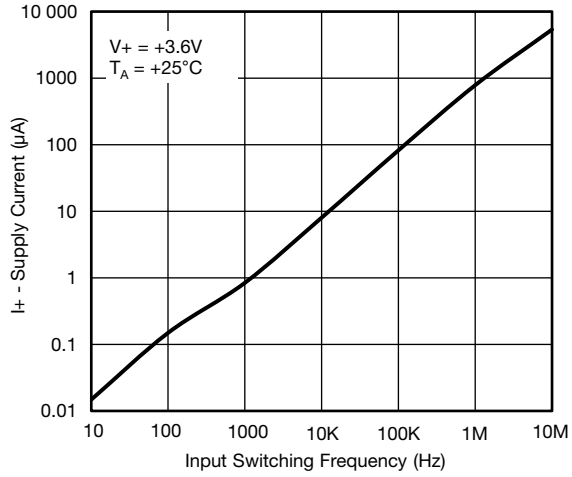
## TYPICAL CHARACTERISTICS ($T_A$ = 25 °C, unless otherwise noted)



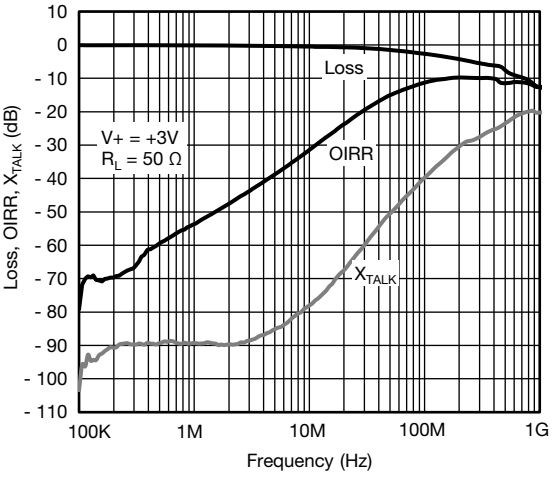

**Leakage Current vs. Temperature**



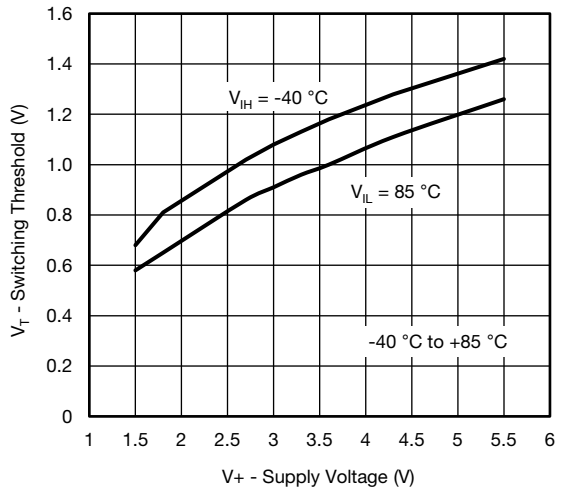

**Switching Time vs. Temperature**



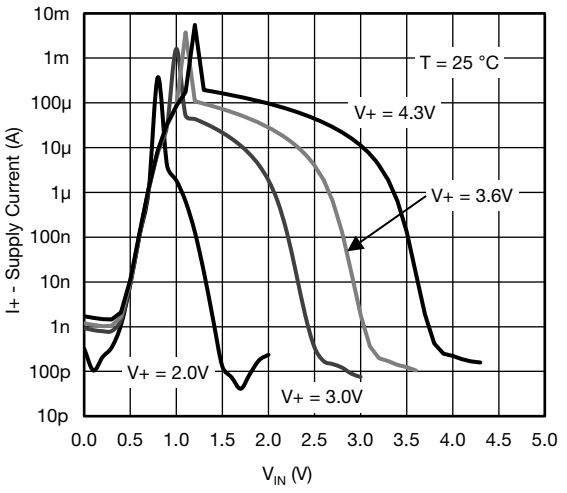

**Supply Current vs. Switching Frequency**




**Insertion Loss, Off-Isolation Crosstalk vs. Frequency**

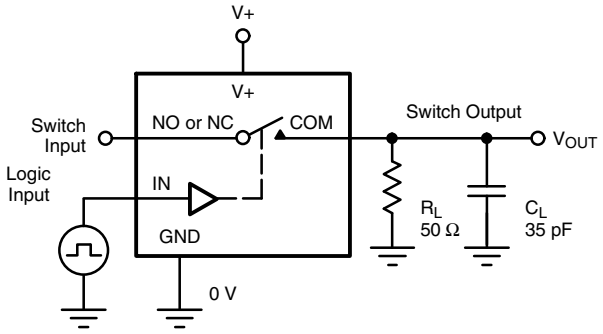



**Switching Threshold vs. Supply Voltage**



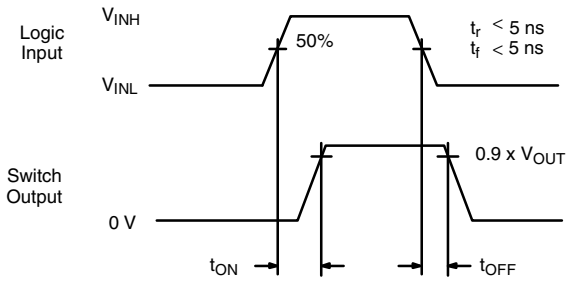

**Supply Current vs. $V_{IN}$**

## TEST CIRCUITS



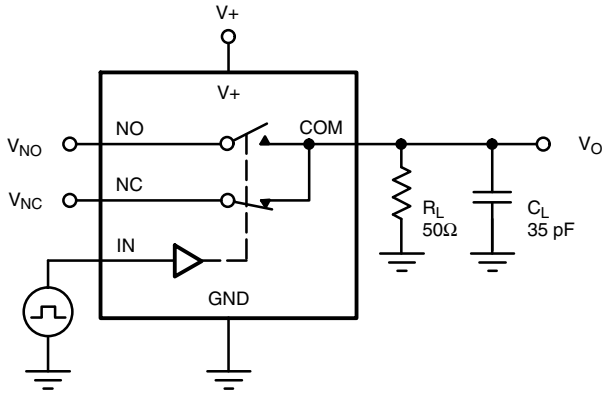

$C_L$ (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$




Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

**Fig. 1 - Switching Time**




$C_L$ (includes fixture and stray capacitance)

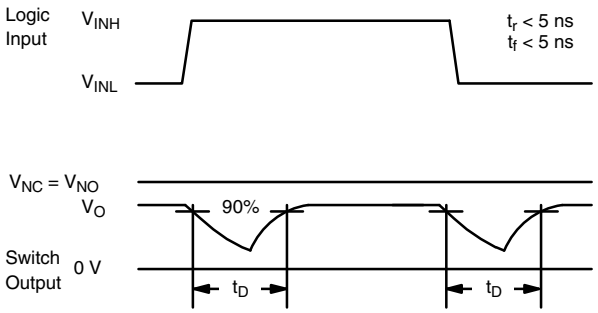



**Fig. 2 - Break-Before-Make Interval**

## TEST CIRCUITS

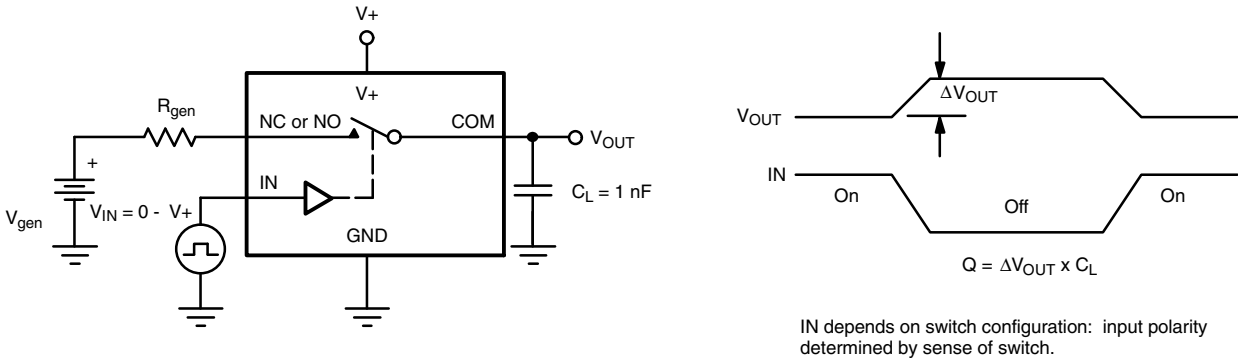



**Fig. 3 - Charge Injection**

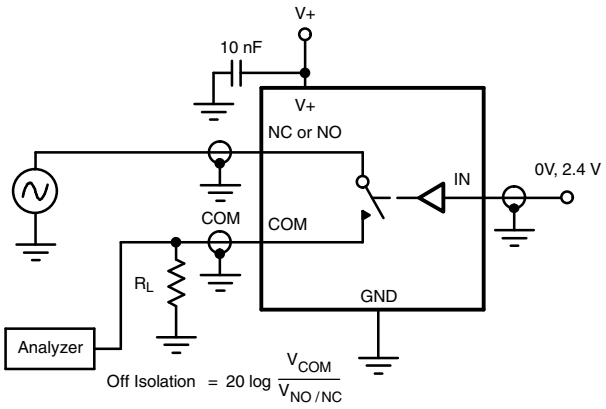



**Fig. 4 - Off-Isolation**

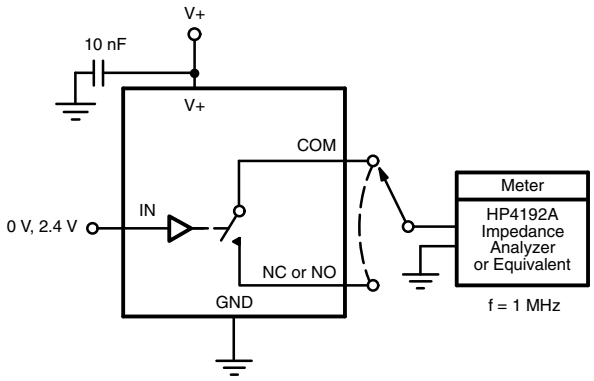
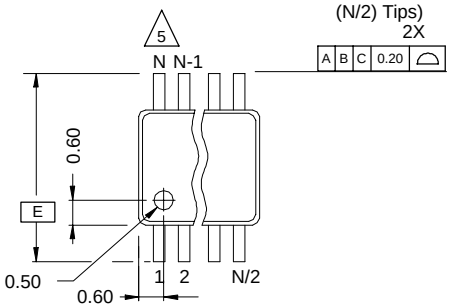


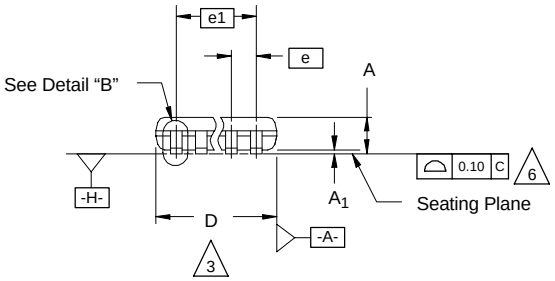

**Fig. 5 - Channel Off/On Capacitance**

## MSOP: 10-LEADS

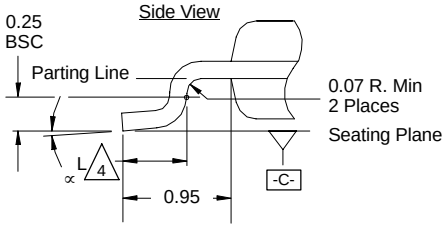
**JEDEC Part Number: MO-187, (Variation AA and BA)**



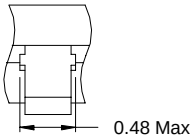

Top View



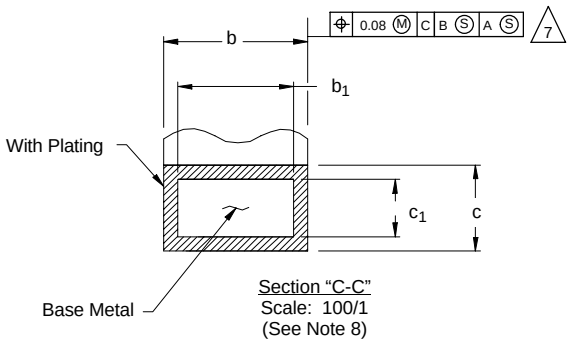

Side View



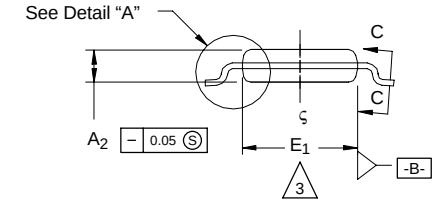

Detail "A"
(Scale: 30/1)




Detail "B"
(Scale: 30/1)
Dambar Protrusion




Section "C-C"
Scale: 100/1
(See Note 8)




End View

NOTES:

1. Die thickness allowable is $0.203 \pm 0.0127$.
2. Dimensioning and tolerances per ANSI.Y14.5M-1994.
3. Dimensions "D" and "$E_1$" do not include mold flash or protrusions, and are measured at Datum plane -H- , mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimension is the length of terminal for soldering to a substrate.
5. Terminal positions are shown for reference only.
6. Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
7. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
8. Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
9. Controlling dimension: millimeters.
10. This part is compliant with JEDEC registration MO-187, variation AA and BA.
11. Datums -A- and -B- to be determined Datum plane -H- .
12. Exposed pad area in bottom side is the same as teh leadframe pad size.

**N = 10L**

| Dim | MILLIMETERS | | | Note |
|---|---|---|---|---|
| | Min | Nom | Max | |
| **A** | - | - | 1.10 | |
| **$A_1$** | 0.05 | 0.10 | 0.15 | |
| **$A_2$** | 0.75 | 0.85 | 0.95 | |
| **b** | 0.17 | - | 0.27 | 8 |
| **$b_1$** | 0.17 | 0.20 | 0.23 | 8 |
| **c** | 0.13 | - | 0.23 | |
| **$c_1$** | 0.13 | 0.15 | 0.18 | |
| **D** | 3.00 BSC | | | 3 |
| **E** | 4.90 BSC | | | |
| **$E_1$** | 2.90 | 3.00 | 3.10 | 3 |
| **e** | 0.50 BSC | | | |
| **$e_1$** | 2.00 BSC | | | |
| **L** | 0.40 | 0.55 | 0.70 | 4 |
| **N** | 10 | | | 5 |
| ∝ | 0° | 4° | 6° | |

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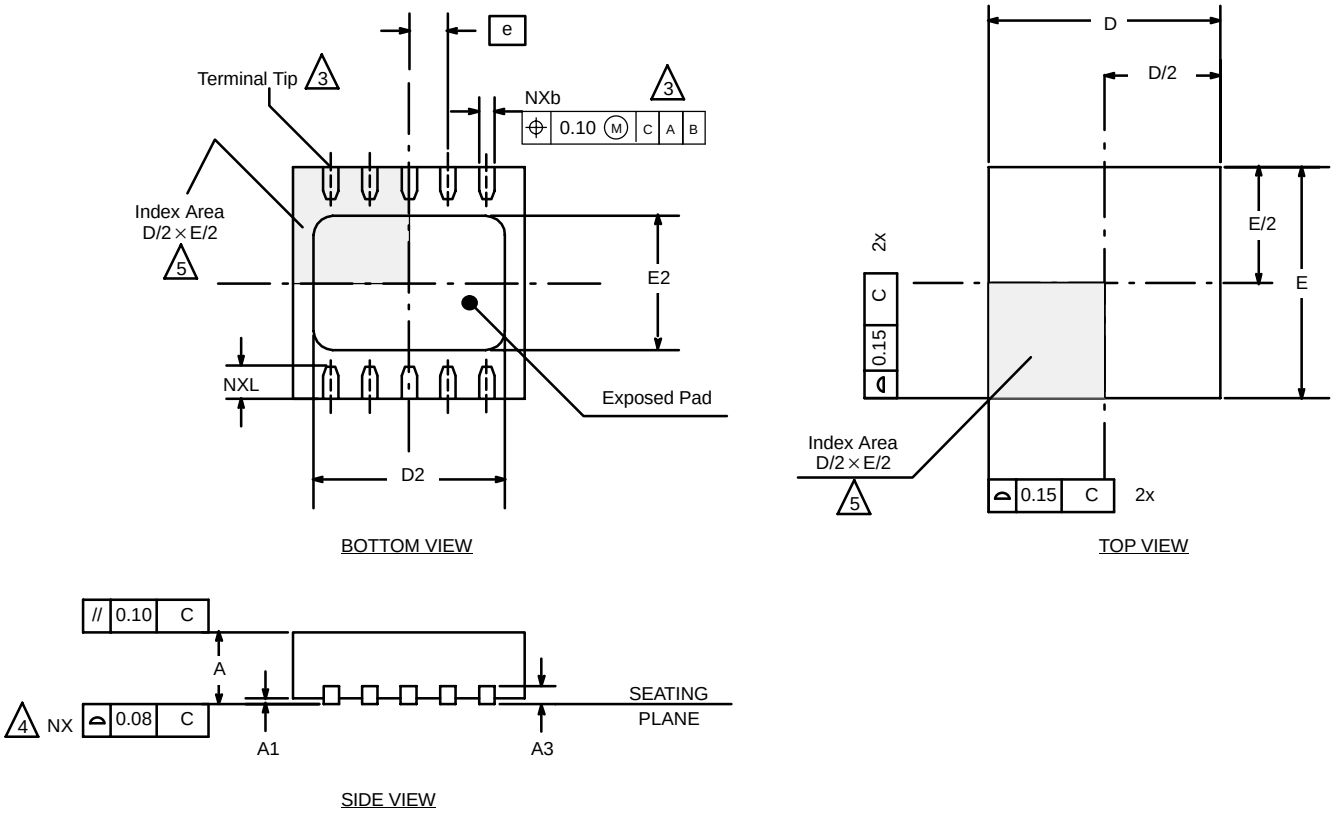
DWG: 5867

## DFN-10 LEAD (3 X 3)




NOTES:

1. All dimensions are in millimeters and inches.
2. N is the total number of terminals.
3. Dimension b applies to metallized terminal and is measured between 0.15 and 0.30 mm from terminal tip.
4. Coplanarity applies to the exposed heat sink slug as well as the terminal.
5. The pin #1 identifier may be either a mold or marked feature, it must be located within the zone iindicated.

| Dim | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| **A** | 0.80 | 0.90 | 1.00 | 0.031 | 0.035 | 0.039 |
| **A1** | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| **A3** | | 0.20 BSC | | | 0.008 BSC | |
| **b** | 0.18 | 0.23 | 0.30 | 0.007 | 0.009 | 0.012 |
| **D** | | 3.00 BSC | | | 0.118 BSC | |
| **D2** | 2.20 | 2.38 | 2.48 | 0.087 | 0.094 | 0.098 |
| **E** | | 3.00 BSC | | | 0.118 BSC | |
| **E2** | 1.49 | 1.64 | 1.74 | 0.059 | 0.065 | 0.069 |
| **e** | | 0.50 BSC | | | 0.020 BSC | |
| **L** | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |

*Use millimeters as the primary measurement.

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DWG: 5943

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