



# Overvoltage-Protection Controllers with Internal FET

## General Description

The MAX4943–MAX4946/MAX4949 family of overvoltage-protection devices feature a low 80mΩ (typ) R<sub>ON</sub> internal FET and protect low-voltage systems against voltage faults up to +28V. These devices also drive an optional external pFET to protect down to -28V when connected to a load with reverse current protection. When the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to the protected components.

All switches feature a minimum 1.2A current-limit protection. During a short-circuit occurrence, the MAX4944B and MAX4945B place the switch in a latching state where the switch turns off and remains off. For the autoretry devices, the switch turns off and continuously checks after a 15ms (typ) retry time.

The overvoltage thresholds (OVLO) are preset to 7.4V, 6.35V, 5.8V, 4.56V, or 8.9V. The undervoltage-lockout (UVLO) thresholds are preset to 2.45V and 4.15V. When the input voltage drops below the undervoltage-lockout (UVLO) threshold, the devices enter a low-current standby mode. (See the *Ordering Information/Selector Guide* for more details on UVLO/OVLO).

All devices are offered in a small, 8-pin μDFN (2mm x 2mm) package and are specified for operation over the -40°C to +85°C temperature range.

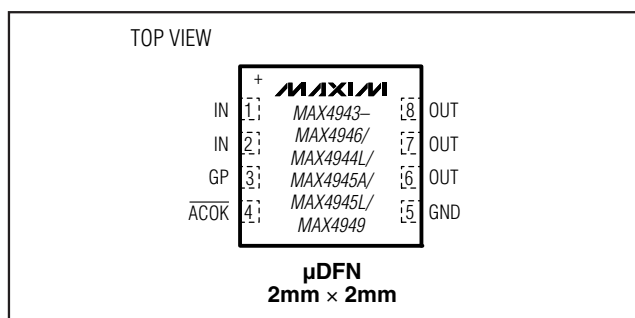
## Applications

Cell Phones                      PDAs and Palmtop Devices  
Digital Still Cameras      MP3 Players

## Features

- ◆ Input Voltage Protection Up to +28V
- ◆ Integrated nFET Switch
- ◆ Preset Overvoltage Protection Trip Level
  - 7.40V (MAX4943)
  - 6.35V (MAX4944)
  - 5.80V (MAX4945)
  - 4.56V (MAX4946)
  - 8.90V (MAX4949)
- ◆ Low-Current Undervoltage-Lockout Mode
- ◆ Short-Circuit Protection (Latching/Autoretry)
- ◆ Internal 15ms (typ) Startup Delay and Retry Times
- ◆ Input Voltage Power-Good Logic Output
- ◆ Thermal-Shutdown Protection
- ◆ Small, 8-Pin (2mm x 2mm) μDFN Package

## Pin Configuration



## Ordering Information/Selector Guide

PART	PIN-PACKAGE	TOP MARK	PKG CODE	UVLO (V)	OVLO (V)	OVERCURRENT MODE
MAX4943ELA+T*	8 μDFN	ABA	L822-1	4.15	7.40	Retry
MAX4944ELA+T	8 μDFN	ABB	L822-1	4.15	6.35	Retry
MAX4944BELA+T*	8 μDFN	ABC	L822-1	4.15	6.35	Latching
MAX4944LELA+T	8 μDFN	ABD	L822-1	2.45	6.35	Retry
MAX4945ELA+T**	8 μDFN	ABE	L822-1	4.15	5.80	Retry
MAX4945AELA+T**	8 μDFN	ADW	L822-1	4.15	5.80	Retry
MAX4945BELA+T*	8 μDFN	ABF	L822-1	4.15	5.80	Latching
MAX4945LELA+T	8 μDFN	ABG	L822-1	2.45	5.80	Retry
MAX4946ELA+T	8 μDFN	ABH	L822-1	2.45	4.56	Retry
MAX4949ELA+T	8 μDFN	ADT	L822-1	2.45	8.90	Latching

**Note:** All devices are specified over the -40°C to +85°C operating temperature range.

+Denotes a lead-free/RoHS-compliant package.

T = Tape-and-reel package.

\*Future product—contact factory for availability.

\*\*The OVLO is 6.10V (max) for the MAX4945ELA+T and .6.0V (max) for the MAX4945AELA+T.



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## ABSOLUTE MAXIMUM RATINGS

IN .....	-0.3V to +30V	Operating Temperature Range .....	-40°C to +85°C
OUT .....	-0.3V to (IN + 0.3V)	Junction Temperature .....	+150°C
GP .....	-0.3V to +12V	Storage Temperature Range .....	-65°C to +150°C
IN to GP .....	-0.3V to +22V	Lead Temperature (soldering, 10s) .....	+300°C
ACOK .....	-0.3V to +6V		
Continuous Power Dissipation (T <sub>A</sub> = +70°C)			
8-Pin $\mu$ DFN (derate 4.8mW/°C above +70°C) .....	381mW		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>IN</sub> = +5V (MAX4943/MAX4944\_/MAX4945\_/MAX4949), V<sub>IN</sub> = +3V (MAX4946), T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V <sub>IN</sub>			2.2		28.0	V
Input Supply Current	I <sub>IN</sub>	V <sub>IN</sub> = 3V (MAX4946)			50	150	$\mu$ A
		V <sub>IN</sub> = 5V, all remaining parts			50	150	
UVLO Supply Current	I <sub>UVLO</sub>	V <sub>IN</sub> = 2.2V				30	$\mu$ A
IN Undervoltage Lockout	V <sub>UVLO</sub>	(V <sub>IN</sub> falling)	MAX4943/MAX4944/ MAX4944B/MAX4945/ MAX4945A/ MAX4945B	3.90	4.15	4.40	V
			MAX4944L/MAX4945L/ MAX4946/MAX4949	2.30	2.45	2.60	
IN Undervoltage-Lockout Hysteresis					1		%
Overvoltage Trip Level	V <sub>OVLO</sub>	(V <sub>IN</sub> rising)	MAX4943	7.00	7.4	7.80	V
			MAX4944_	6.00	6.35	6.70	
			MAX4945/MAX4945B/L	5.50	5.80	6.10	
			MAX4945A	5.50	5.80	6.00	
			MAX4946	4.30	4.56	4.82	
			MAX4949	8.20	8.90	9.60	
IN Overvoltage Hysteresis					1		%
Switch On-Resistance	R <sub>ON</sub>	V <sub>IN</sub> = 3V (MAX4946), I <sub>OUT</sub> = 1A			80	200	m $\Omega$
		V <sub>IN</sub> = 5V, all remaining parts, I <sub>OUT</sub> = 1A			80	200	
Overcurrent Protection Threshold	I <sub>LIM</sub>	MAX4943-MAX4946	T <sub>A</sub> = +25°C	1.2	1.7	4.0	A
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>	1.2	1.7	4.0	
		MAX4949	T <sub>A</sub> = +25°C	2.0	3.5	5.0	
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>	2.0	3.0	5.0	
GP Clamp Voltage	I <sub>GPD</sub>	(V <sub>IN</sub> - V <sub>GP</sub> ), V <sub>IN</sub> = 28V		13	16	19	V
GP Pulldown Resistor	R <sub>GPD</sub>				50		k $\Omega$

# Overvoltage-Protection Controllers with Internal FET

MAX4943-MAX4946/MAX4944L/MAX4945A/MAX4945L/MAX4949

## ELECTRICAL CHARACTERISTICS (continued)

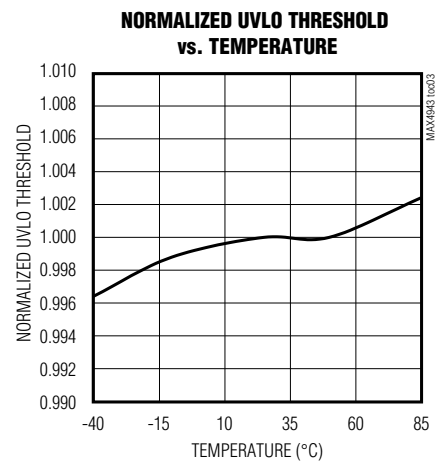
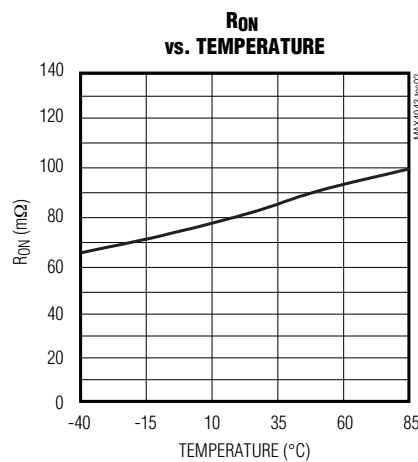
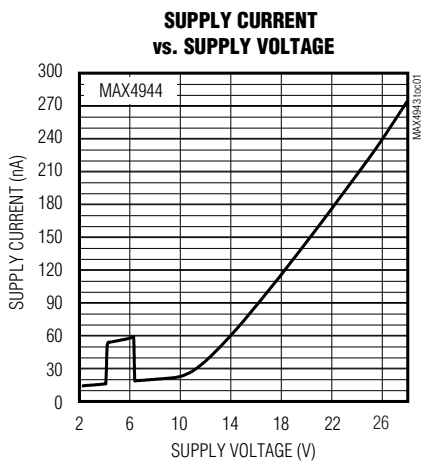
( $V_{IN} = +5V$  (MAX4943/MAX4944\_/MAX4945\_/MAX4949),  $V_{IN} = +3V$  (MAX4946),  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACOK Output-Low Voltage	$V_{OL}$	$I_{SINK} = 1mA$			0.4	V
ACOK High-Leakage Current		$V_{ACOK} = 5.5V$			1	$\mu A$
Thermal Shutdown				+175		$^{\circ}C$
Thermal-Shutdown Hysteresis				40		$^{\circ}C$
Load Capacitor					300	$\mu F$
<b>TIMING CHARACTERISTICS (Figure 2)</b>						
Debounce Time	$t_{INDBC}$	Time from $V_{UVLO} < V_{IN} < V_{OVLO}$ to charge-pump enable		15		ms
Switch Turn-On Time	$t_{ON}$	$V_{UVLO} < V_{IN} < V_{OVLO}$ , $R_{LOAD} = 100\Omega$ , $C_{LOAD} = 300\mu F$ , $V_{OUT} =$ from 10% of $V_{OUT}$ to 80% of $V_{OUT}$		6		ms
ACOK Assertion Time	$t_{ACOK}$	$V_{UVLO} < V_{IN} < V_{OVLO}$ , to $\overline{ACOK}$ low		30		ms
Switch Turn-Off Time	$t_{OFF}$	$V_{IN} < V_{UVLO}$ or $V_{IN} > V_{OVLO}$ , to internal switch off		2	20	$\mu s$
		Overcurrent fault to internal switch turn-off		10		$\mu s$
Autoretry Time	$t_{RETRY}$	From overcurrent fault to internal switch turn-on		15		ms

**Note 1:** All specifications are 100% production tested at  $T_A = +25^{\circ}C$ , unless otherwise noted. Specifications are over  $-40^{\circ}C$  to  $+85^{\circ}C$  and are guaranteed by design.

## Typical Operating Characteristics

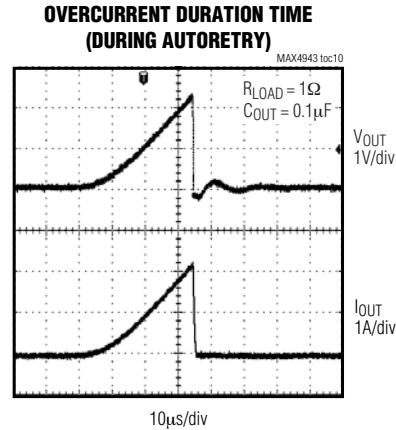
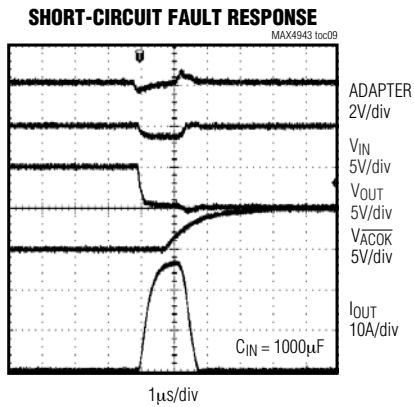
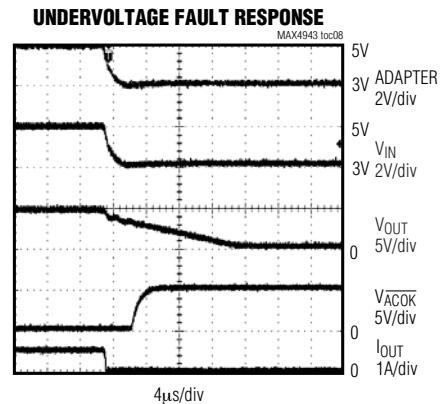
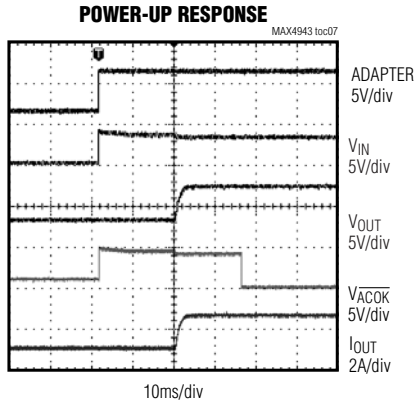
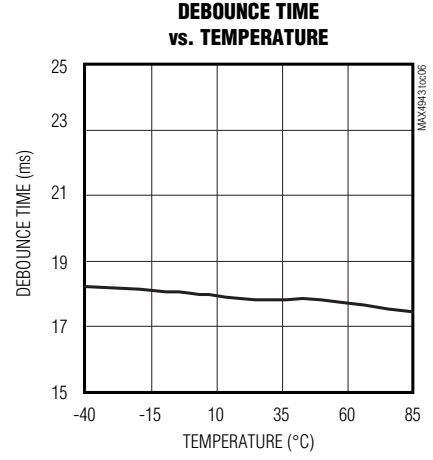
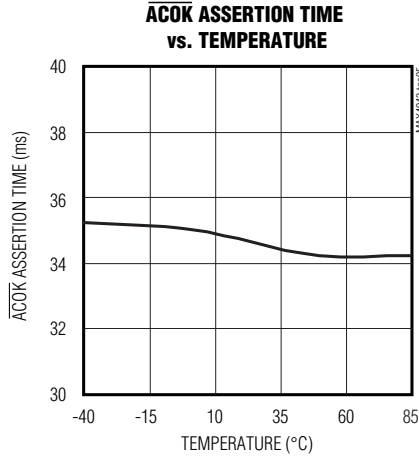
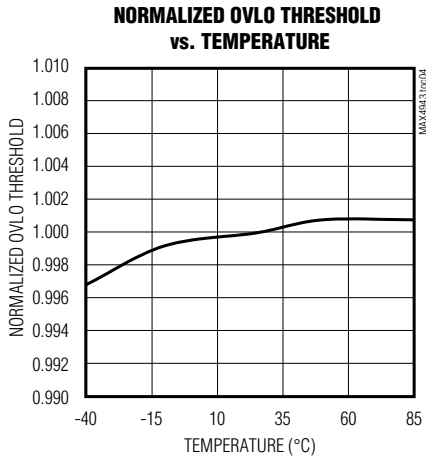
( $T_A = +25^{\circ}C$ , unless otherwise noted.)



# Overvoltage-Protection Controllers with Internal FET

## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



# Overvoltage-Protection Controllers with Internal FET

## Pin Description

PIN	NAME	FUNCTION
1, 2	IN	Voltage Input. IN powers the charge pump required to turn on the internal switch. When the correct adapter is plugged in, a 15ms (typ) debouncer prevents false turn-on of the internal switch. Bypass IN to GND with a 1 $\mu$ F ceramic capacitor as close as possible to the device to enable $\pm 15$ kV (HBM) ESD protection on IN.
3	GP	pFET Gate-Drive Output. GP pulls the external pFET gate down when the input is above ground.
4	$\overline{\text{ACOK}}$	Active-Low Open-Drain Adapter-Voltage Indicator Output. $\overline{\text{ACOK}}$ is driven low after the adapter voltage is stable between $V_{\text{UVLO}}$ and $V_{\text{OVLO}}$ for 30ms (typ). Connect a pullup resistor from $\overline{\text{ACOK}}$ to the logic I/O voltage of the host system.
5	GND	Ground
6, 7, 8	OUT	Output Voltage. Output of internal switch. Short all pins together for proper operation.

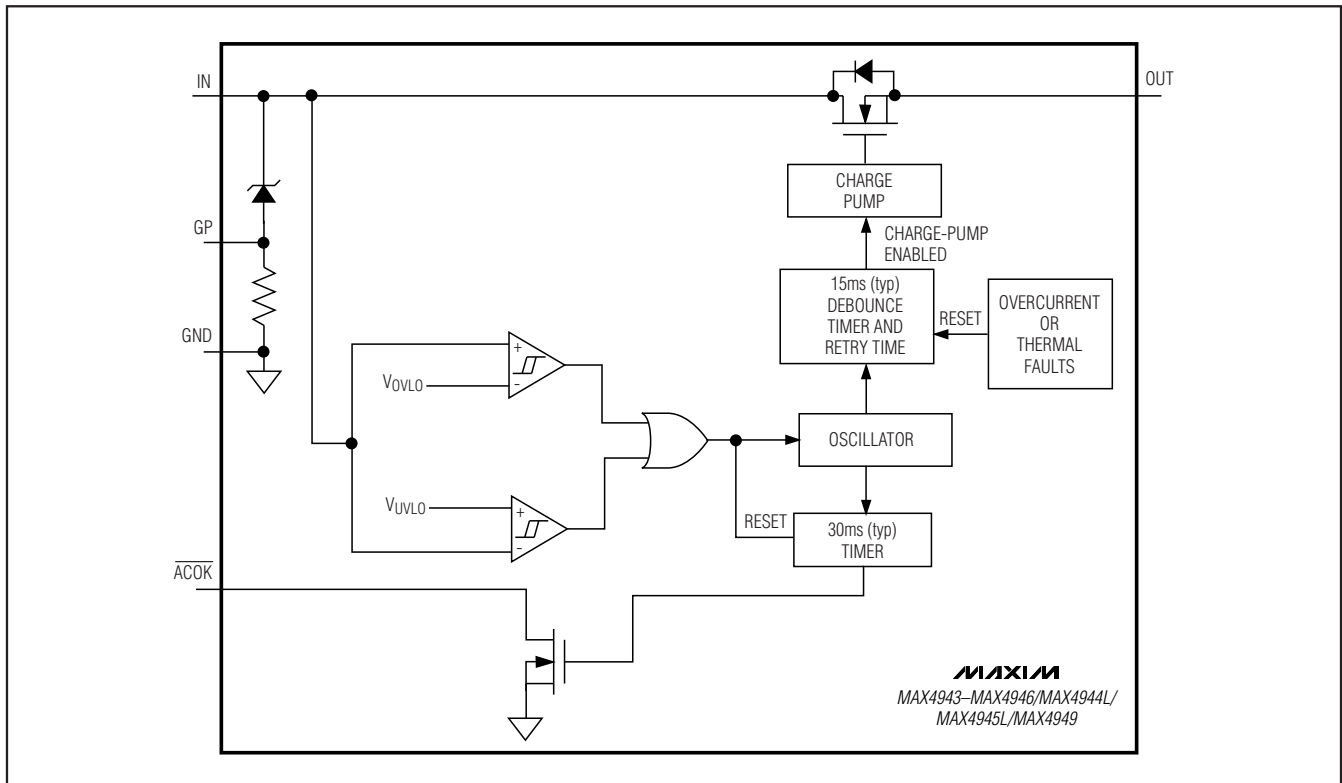


Figure 1. Functional Diagram

## Detailed Description

The MAX4943-MAX4946/MAX4949 overvoltage-protection devices feature a low  $R_{\text{ON}}$  internal FET and protect low-voltage systems against voltage faults up to +28V. If the input voltage exceeds the overvoltage threshold, the internal MOSFET is turned off to prevent damage to the protected components. These devices also drive an

optional external pFET to protect down to -28V. If the adapter voltage drops below ground, the pFET turns off to prevent damage to the protected components due to negative voltage exposure. The internal charge pump's 15ms (typ) debounce time prevents false turn-on of the internal switch during startup. An open-drain, active-low logic output is available to signal that a successful power-up has occurred.

MAX4943-MAX4946/MAX4944L/MAX4945A/MAX4945L/MAX4949

# Overvoltage-Protection Controllers with Internal FET

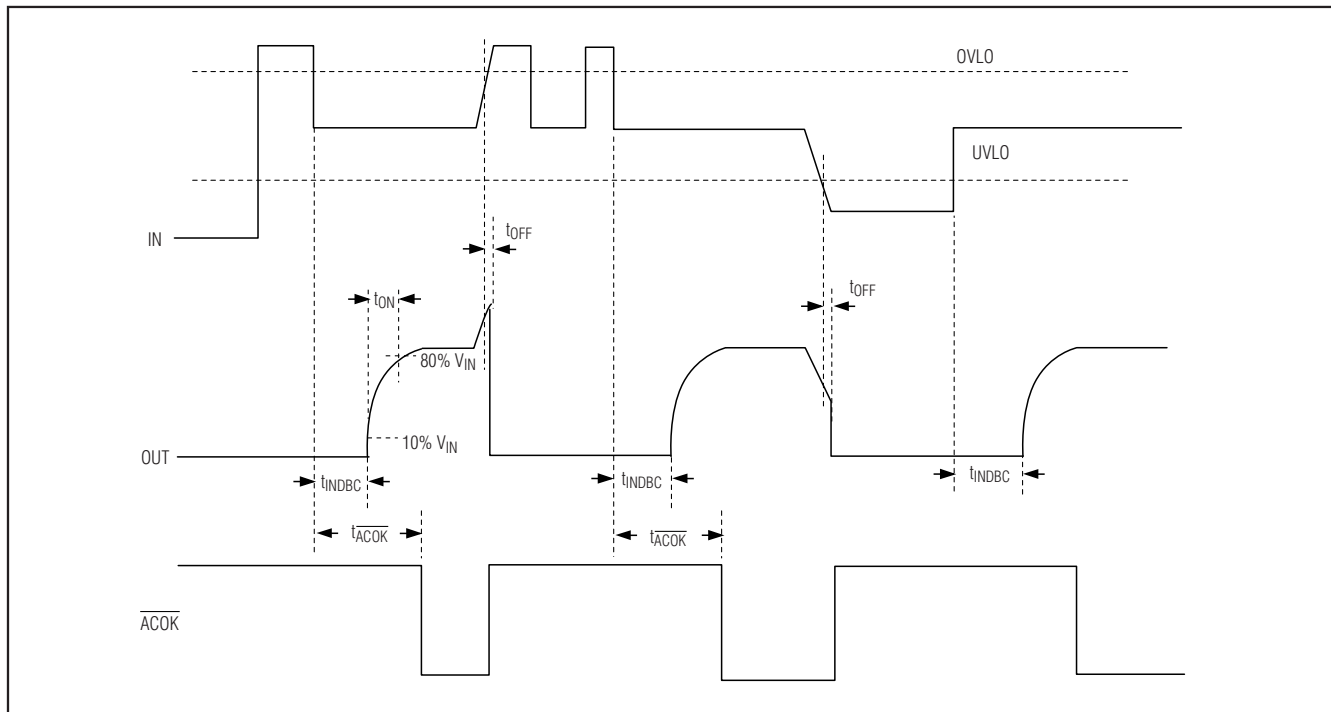


Figure 2. Timing Diagram

## Device Operation

The MAX4943–MAX4946/MAX4949 have an internal oscillator and charge pump that control the turn-on of the internal switch. The internal oscillator controls the timers that enable the turn-on of the charge pump and controls the state of the open-drain  $\overline{\text{ACOK}}$  output. If  $V_{\text{IN}} < V_{\text{UVLO}}$  or if  $V_{\text{IN}} > V_{\text{OVLO}}$ , the internal oscillator remains off, thus disabling the charge pump. If  $V_{\text{UVLO}} < V_{\text{IN}} < V_{\text{OVLO}}$ , the internal charge pump is enabled. The charge-pump startup, after a 15ms (typ) internal delay, turns on the internal switch (see Figure 2).  $\overline{\text{ACOK}}$  is held high during startup until the  $\overline{\text{ACOK}}$  30ms (typ) blanking period expires. At this point, the device is in its on state.

At any time, if  $V_{\text{IN}}$  drops below  $V_{\text{UVLO}}$  or rises above  $V_{\text{OVLO}}$ ,  $\overline{\text{ACOK}}$  is pulled high and the charge pump is disabled.

## Internal Switch

The MAX4943–MAX4946/MAX4949 incorporate an internal nFET with a 80m $\Omega$  (typ)  $R_{\text{ON}}$ . The switch is internally driven by a charge pump that generates a 5V

voltage above the input voltage. The internal switch is equipped with 1.2A (min) current-limit protection that turns off the switch within 10 $\mu\text{s}$  (typ) during an overcurrent fault condition.

## Autoretry

The MAX4943–MAX4946 have an overcurrent autoretry function that turns on the switch again after a 15ms (typ) retry time (see Figure 3). If the faulty load condition is still present after the blanking time, the switch turns off again and the cycle is repeated. The fast turn-off time and 15ms retry time result in a very low duty cycle to keep power consumption low. If the faulty load condition is not present, the switch remains on.

## Latch

The MAX4944B/MAX4945B/MAX4949 do not have the autoretry function, and the switch latches off after an overcurrent fault. The switch remains off until the overcurrent fault has been removed. The switch turns back on when the adapter voltage goes below  $V_{\text{UVLO}}$  and then returns to the valid operating range.

# Overvoltage-Protection Controllers with Internal FET

MAX4943-MAX4946/MAX4944L/MAX4945A/MAX4945L/MAX4949

## GP GATE Drive

When the input voltage goes above ground, GP pulls low and turns on the pFET. An internal clamp protects the pFET by ensuring that the GP to IN voltage does not exceed 19V (max) when the input (IN) rises to +28V.

## Undervoltage Lockout (UVLO)

The MAX4944L/MAX4945L/MAX4946/MAX4949 have a 2.45V (typ) undervoltage-lockout threshold ( $V_{UVLO}$ ), while the remaining devices have a 4.15V (typ)  $V_{UVLO}$  threshold. When  $V_{IN}$  is less than  $V_{UVLO}$ ,  $\overline{ACOK}$  is high impedance.

## Overvoltage-Lockout Thresholds (OVLO)

The MAX4943 has a 7.4V (typ) overvoltage threshold ( $V_{OVLO}$ ), the MAX4944\_ has a 6.35V (typ)  $V_{OVLO}$  threshold, the MAX4945\_ has a 5.80V (typ)  $V_{OVLO}$  threshold, the MAX4946 has a 4.56V (typ)  $V_{OVLO}$  threshold, and the MAX4949 has a 8.90V (typ)  $V_{OVLO}$  threshold. When  $V_{IN}$  is greater than  $V_{OVLO}$ ,  $\overline{ACOK}$  is high impedance.

## $\overline{ACOK}$

$\overline{ACOK}$  is an active-low, open-drain output that asserts low when  $V_{UVLO} < V_{IN} < V_{OVLO}$  for the 30ms (typ) period. Connect a pullup resistor from  $\overline{ACOK}$  to the logic I/O voltage of the host system. During a short-circuit fault,  $\overline{ACOK}$  may deassert due to  $V_{IN}$  not being in the valid operating voltage range.

## Thermal-Shutdown Protection

The MAX4943-MAX4946/MAX4949 feature thermal-shutdown circuitry. The internal switch turns off when the junction temperature exceeds +175°C (typ) and immediately goes into a fault mode. The device exits thermal shutdown after the junction temperature cools by 40°C (typ).

## Applications Information

### IN Bypass Capacitor

For most applications, bypass IN to GND with a 1 $\mu$ F ceramic capacitor as close as possible to the device to enable  $\pm 15$ kV (HBM) ESD protection on the pin. If  $\pm 15$ kV is not required, there is no capacitor required at IN. If the power source has significant inductance due to long lead length, take care to prevent overshoots due to the LC tank circuit and provide protection if necessary to prevent exceeding the +30V absolute maximum rating on IN.

### Reverse Polarity Protection

The optional external pFET can provide reverse polarity protection down to -28V (for a 30V pFET), if the protect-

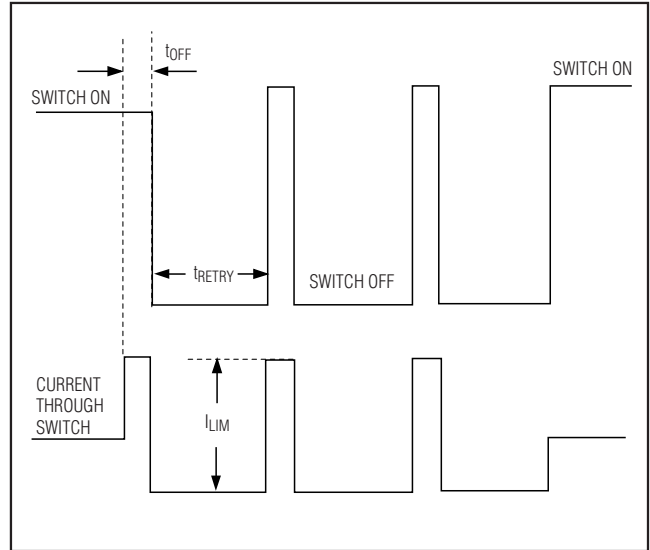


Figure 3. Autoretry Timing Diagram

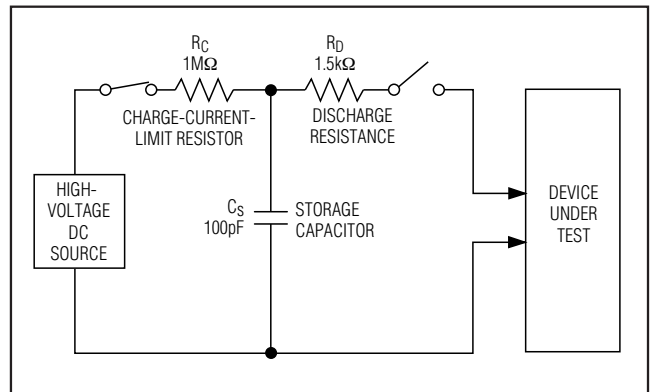


Figure 4. Human Body ESD Test Model

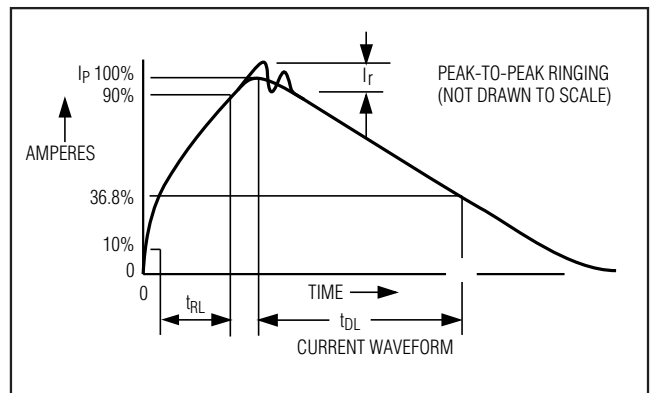


Figure 5. Human Body Current Waveform

# Overvoltage-Protection Controllers with Internal FET

ed device does not allow current to flow into OUT. The pFET is turned off when the voltage between GP and IN is less than the pFET gate threshold voltage.

### ESD Test Conditions

ESD performance depends on a number of conditions. The MAX4943-MAX4946/MAX4949 are specified for ±15kV (HBM) typical ESD resistance on IN when IN is bypassed to ground with a 1µF ceramic capacitor.

### Human Body Model

Figure 4 shows the Human Body Model and Figure 5 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

### IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The MAX4943-MAX4946/MAX4949 are specified for ±15kV Air-Gap Discharge and ±8kV Contact Discharge IEC 61000-4-2 on the IN pin when IN is bypassed to ground with a 1µF ceramic capacitor.

The major difference between tests done using the Human Body Model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2, due to lower series resistance.

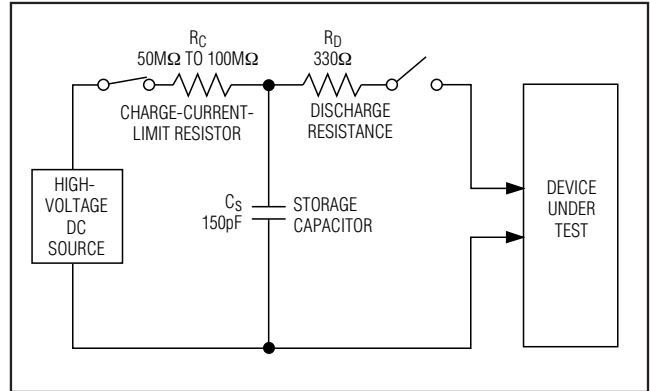


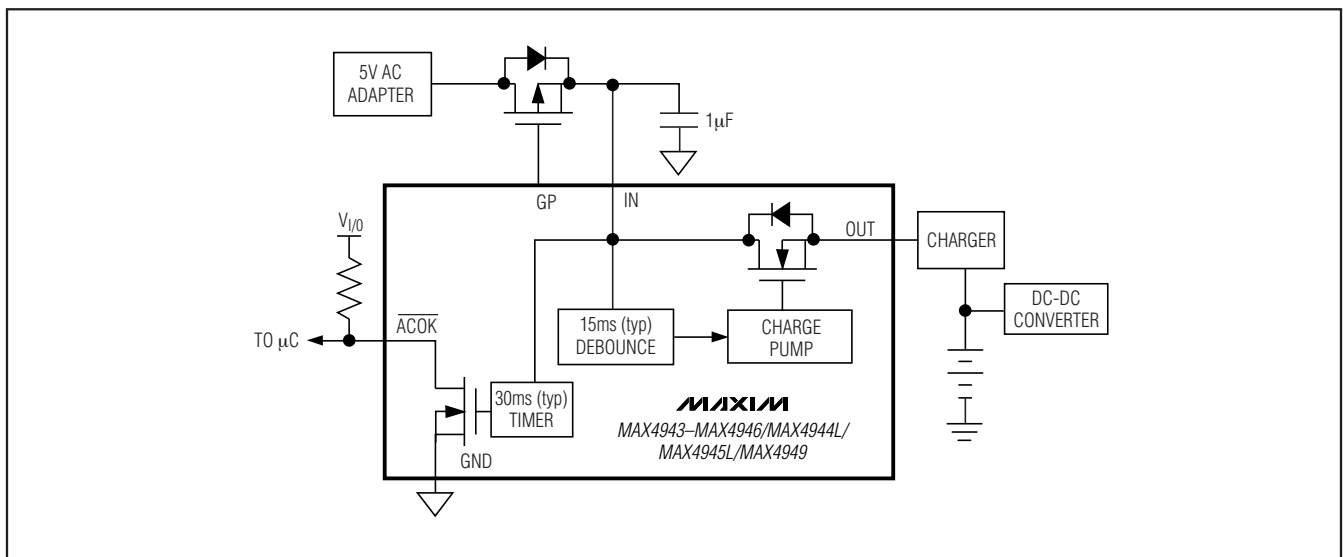
Figure 6. IEC 61000-4-2 ESD Test Model

Hence, the ESD withstand voltage measured to IEC 61000-4-2 generally is lower than that measured using the Human Body Model. Figure 6 shows the IEC 61000-4-2 model. The Contact Discharge method connects the probe to the device before the probe is charged. The Air-Gap Discharge test involves approaching the device with a charged probe.

### Chip Information

PROCESS: BiCMOS

### Typical Operating Circuit





# Overvoltage-Protection Controllers with Internal FET

## Package Information

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 $\mu$ DFN	L822-1	<a href="#">21-0164</a>

MAX4943-MAX4946/MAX4944L/MAX4945A/MAX4945L/MAX4949

# Overvoltage-Protection Controllers with Internal FET

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	7/07	—	1, 2, 3
3	6/08	Added MAX4945A to the <i>Ordering Information/Selector Guide</i> and <i>Electrical Characteristics</i> tables	1, 2

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