PAC5556
Data Sheet

Power Application Controller®

Configurable Analog Front End™

Application Specific Power Drivers™

Arm® Cortex®-M0 Controller Core

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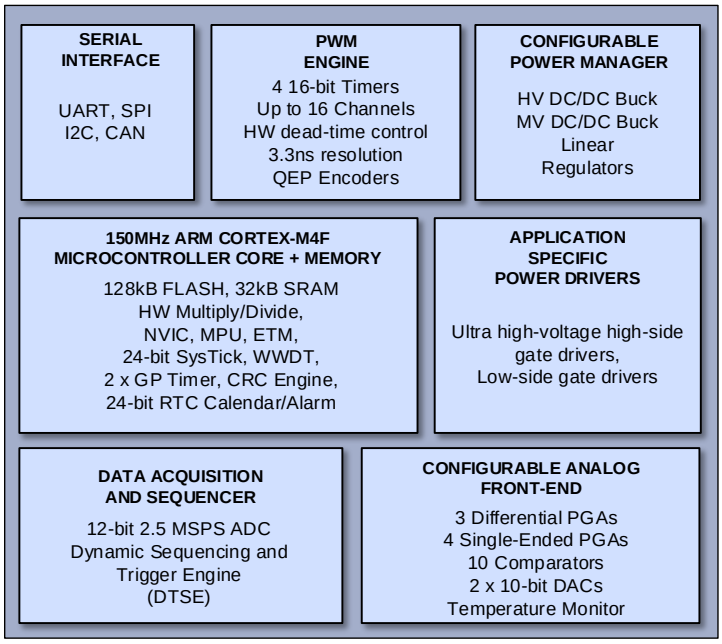
1 GENERAL DESCRIPTION

The PAC5556 is a Power Application Controller® (PAC) product that is optimized for high-voltage, high-speed BLDC or PMSM motor control. The PAC5556 integrates a 150MHz Arm® Cortex®-M4F 32-bit microcontroller core with a highly-configurable Power Manager, Active-Semi's Configurable Analog Front-End™ and Application Specific Power Drivers™ to form the most compact microcontroller-based power and motor control and drive solution available.

The PAC5556 microcontroller features 128kB of embedded FLASH and 32kB of SRAM memory, a 2.5MSPS analog-to-digital converter (ADC) with programmable auto-sampling of up to 24 conversion sequences, 3.3V IO, flexible clock control system, PWM and general-purpose timers and several serial communications interfaces.

The Configurable Power Manager (CPM) provides "all-in-one" efficient power management solution for multiple types of power sources. It features a configurable high-voltage buck controller (HV-BUCK), a configurable medium-voltage switching regulator (MV-BUCK), and four linear regulated voltage supplies. The Application Specific Power Drivers (ASPD) are 600V power drivers designed for half bridge, H-bridge, 3-phase, and general-purpose driving. The Configurable Analog Front End (CAFE) comprises differential programmable gain amplifiers, single-ended programmable gain amplifiers, comparators, digital-to-analog converters, and I/Os for programmable and inter-connectible signal sampling, feedback amplification, and sensor monitoring of multiple analog input signals.

Figure 1-1 Power Application Controller



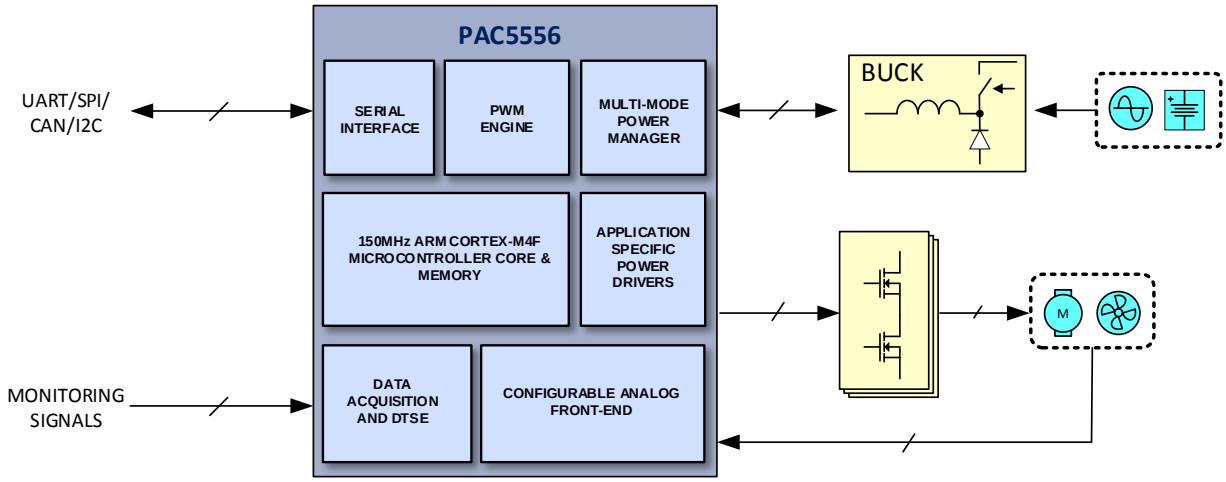
The PAC5556 is available in a 52-pin, 10x10mm QFN package.

2 PAC FAMILY APPLICATIONS

The PAC5556 is ideal for 120VAC/240VAC or up to 600VDC powered BLDC or PMSM motor applications. Target applications for this device include:

- AC Fans
- Ceiling Fans
- White Goods
- Compressors
- Water Pumps

Figure 2-1 Simplified Application Diagram



3 PRODUCT SELECTION SUMMARY

Table 3-1 Product Selection Summary

PART NUMBER	PIN PKG	POWER MANAGER		CONFIGURABLE ANALOG FRONT END					APPLICATION SPECIFIC POWER DRIVERS		MICROCONTROLLER						PRIMARY APPLICATION
		INPUT VOLTAGE	CONFIGURABLE POWER	DIFF-PGA	PGA	COMPARATOR	DAC	ADC CHANNEL	VBST/VSRC	POWER DRIVER	SPEED (MHz)	FLASH (kB)	SRAM (kB)	GPIO	PWM CHANNEL	COMM	
PAC5556	52-pin 10x10 QFN	Up to 600V	Y	3	4	10	2	11	630V/ 610V	3 LS @ 1A 3 HS @ 0.25A/ 0.5A	150	128	32	26	16 (3.3 V)	UART SPI CAN I2C SWD JTAG	3 half-bridge 3 phase control Sensored BLDC, Sensorless BEMF, Sensorless FOC

Notes: DIFF-PGA = differential programmable gain amplifier; HS = high-side, LS = low-side, PGA = programmable gain amplifier, VSRC = Bootstrap Voltage Source

4 ORDERING INFORMATION

Table 4-1 Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PINS	PACKING
PAC5556QX	-40°C to 125°C	QFN1010-52	52 + Exposed Pad	Tray

5 FEATURES

5.1 Feature Overview

- Configurable Power Manager
  - AC line input or DC supply up to 600V
  - 8µA hibernate I_Q
  - 600V DC/DC buck controller (HV-BUCK)
  - 5V DC/DC buck regulator (MV-BUCK)
  - 4 Linear regulators with power and hibernate management
  - Power and temperature monitor, warning, fault detection
- Proprietary Configurable Analog Front-End
  - 10 Analog Front-End IO pins
  - 3 Differential Programmable Gain Amplifiers
  - 4 Single-ended Programmable Gain Amplifiers
  - Programmable Over-Current Protection
  - 10 Comparators, 2 DACs (10-bit)
  - Integrated VM ADC Sampling
- Proprietary Application Specific Power Drivers
  - 3 600V high-side gate drivers with 0.25A/0.5A gate driving capability
  - 3 low-side gate drivers with 1A/1A gate driving capability
  - Configurable fault protection
  - Cycle by cycle current limit control (CBCCTL)
- 150MHz Arm® Cortex®-M4F 32-bit Microcontroller Core
  - Single-cycle 32-bit x 32-bit hardware multiplier
  - 32-bit hardware divider
  - DSP Instructions and Saturation Arithmetic Support
  - Integrated sleep and deep sleep modes
  - Single-precision Floating Point Unit (FPU)
  - 8-region Memory Protection Unit (MPU)
  - Nested Vectored Interrupt Controller (NVIC) with 32 Interrupts with 8 levels of priority
  - 24-Bit SysTick Timer
  - Wake-up Interrupt Controller (WIC) allowing power-saving sleep modes
  - Clock-gating allowing low-power operation
  - Embedded Trace Macrocell (ETM) for in-system debugging at real-time without breakpoints

- Memory
  - 128kB FLASH
  - 32kB SRAM with ECC
  - 2 x 1kB INFO FLASH area for manufacturing information
  - 1 x 1kB INFO FLASH area for user parameter storage and application configuration or code
- Analog to Digital Converter (ADC)
  - 12-bit resolution
  - 2.5MSPS
  - Programmable Dynamic Triggering and Sampling Engine (DTSE)
- I/O
  - 3.3V Digital I/O or Analog Input for ADC
  - Configurable weak pull-up and pull-down
  - Configurable drive strength (6mA to 25mA minimum)
  - Dedicated Integrated IO power supply (3.3V)
  - Flexible peripheral MUX allowing each IO pin to be configured with one of up to 8 peripheral functions
  - Flexible Interrupt Controller
- Flexible Clock Control System (CCS)
  - 300MHz PLL from internal 1.25% oscillator
  - 20MHz Ring Oscillator
  - 20MHz External Clock Input
- Timing Generators
  - Four 16-bit timers with up to 32 PWM/CC blocks
    - 16 Programmable Hardware Dead-time generators
    - Up to 300MHz input clock for high-resolution PWM
  - 16-bit Windowed Watchdog Timer (WWDT)
  - 24-bit Real-time Clock (RTC) with Calendar and Alarm Functions
  - 24-bit SysTick Timer
  - 2 x 24-bit General-purpose count-down timers with interrupt
  - Wake-up timer for sleep modes from 0.125s to 8s
- Communication Peripherals
  - 3 x USART
    - SPI or UART modes
    - SPI Master/Slave, up to 25MHz
    - UART, up to 1Mbps
  - I2C Master/Slave
  - CAN 2.0B Controller

- Debug
  - Single Wire Debugger (SWD)
  - JTAG
  - Embedded Trace Macrocell (ETM)
- 4-Level User-Configurable Code Protection
- 96-bit Unique ID
- CRC Engine
  - Offloads software for communications and safety protocol through hardware acceleration
  - Configurable Polynomial (CRC-16 or CRC-8)
  - Configurable Input Data Width, Input and Output Reflection
  - Programmable Seed Value

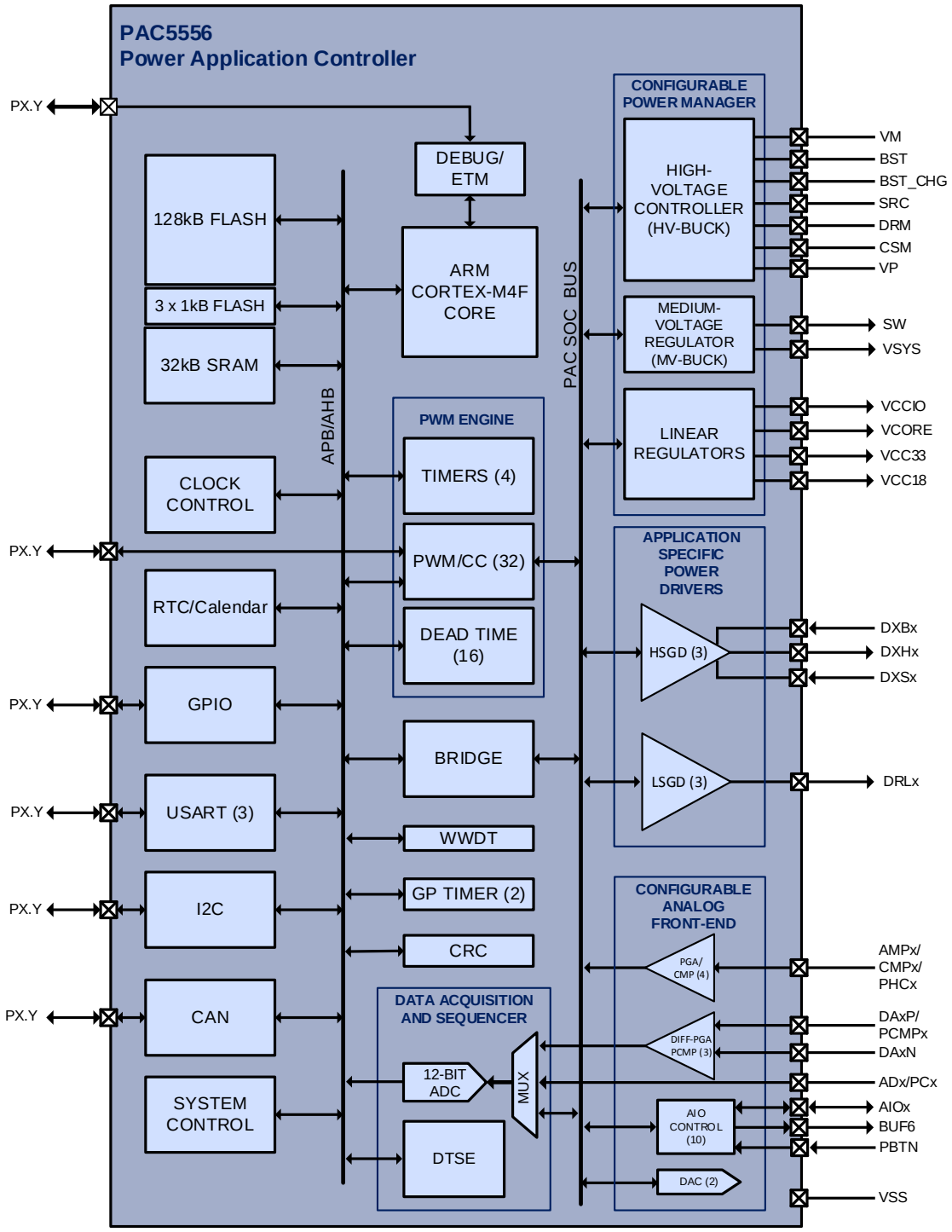
6 ABSOLUTE MAXIMUM RATINGS

Table 6-1 Absolute Maximum Ratings

PARAMETER			VALUE	UNIT
VM to VSS			-0.3 to 605	V
BST/DXBx to VSS			-0.3 to 630	V
BST to SRC, DXBx to DXSx			-0.3 to 20	V
SRC/DXSx to VSS			-10 to 610	V
DRM to SRC, DXHx to DXSx			-0.3 to 20	V
DXSx allowable offset slew rate (dV_{DXSx}/dt)			-50 to 50	V/ns
DRLx to VSS			-0.3 to V_P + 0.3	V
VP to VSS			-0.3 to 18	V
SW to VSS			-0.3 to V_P + 0.3	V
CSM to VP			-0.3 to 0.3	V
CSM to VSS			-0.3 to V_P + 1.0	V
BST_CHG to VSS			-0.3 to 42	V
VSYS, AIO6 to VSS			-0.3 to 6	V
VCC33, VCCIO to VSS			-0.3 to 4.1	V
VCORE to VSS			-0.3 to 1.44	V
VCC18 to VSS			-0.3 to 2.5	V
AIO<9:7>, AIO<5:0> to VSS			-0.3 to V_{SYS} + 0.3	V
PE<x>, PF<x> to VSS			-0.3 to V_{CCIO} + 0.3	V
PE<x>, PF<x> pin injection current			25	mA
PE<x>, PF<x> sum of all pin injection current			50	mA
VSS RMS Current			0.2	A_{RMS}
Electrostatic Discharge (ESD)	Human body model (JEDEC)	All pins (except VM)	2	kV
		VM	1	kV
	Charge device model (JEDEC)		1	kV

7 ARCHITECTURAL BLOCK DIAGRAM

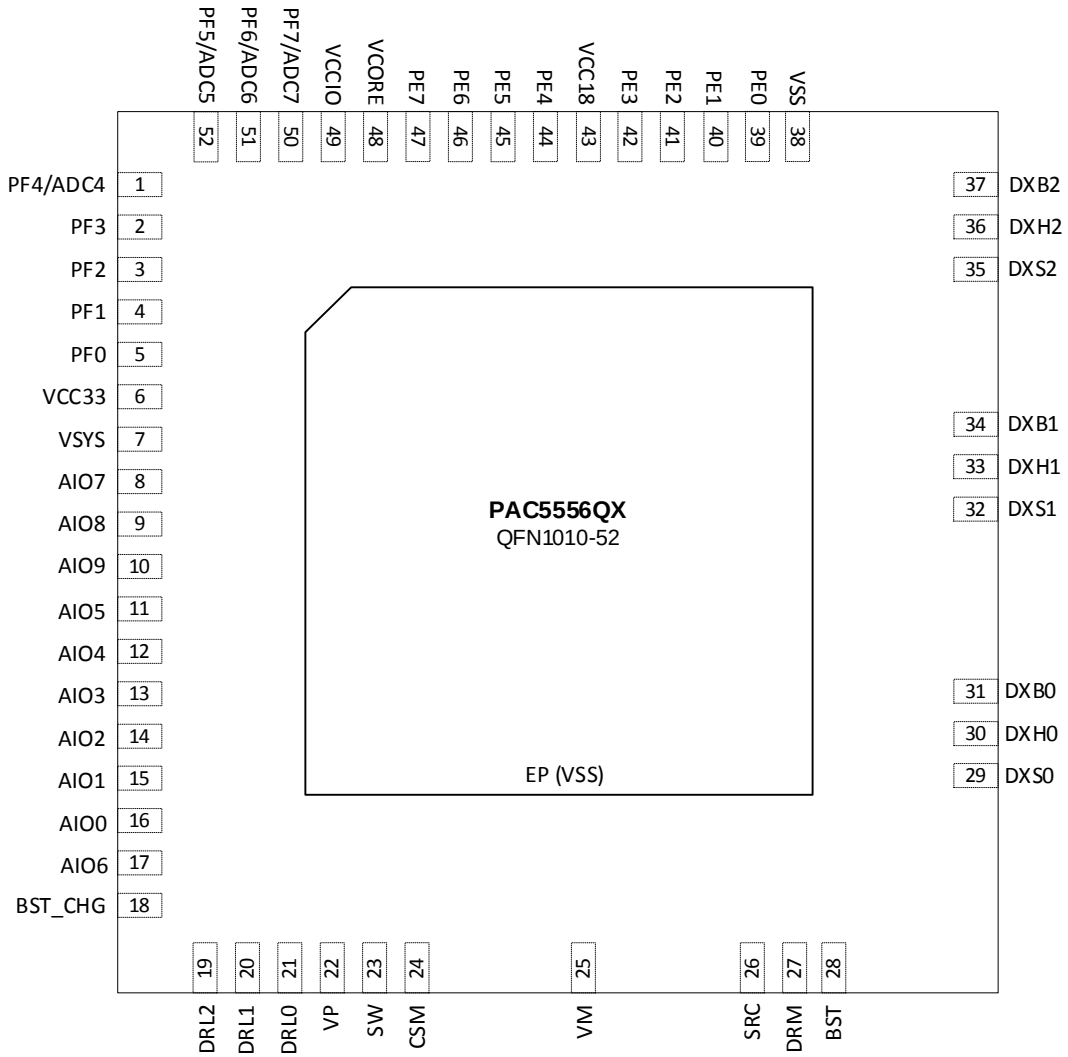
Table 7-1 Architectural Block Diagram



8 PIN CONFIGURATION

8.1 PAC5556QX Pin Configuration (QFN1010-52 Package)

Figure 8-1 PAC5556QX Pin Configuration (QFN1010-52 Package)



9 PIN DESCRIPTION

9.1 Power and Ground Pin Description

Table 9-1 Multi-Mode Power Manager and System Pin Description

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
VCC33	6	Power	Internally generated 3.3V power supply. Connect to a 2.2µF or higher value ceramic capacitor from V_{CC33} to V_{SSA}.
VSYS	7	Power	5V power supply for the medium-voltage buck regulator. Connect to a 22 µF /6.3V or higher ceramic capacitor from V_{SYS} to V_{SS}.
BST_CHG	18	Power	Boot-strap capacitor charge pin. Connect to DC/DC boot-strap capacitor. Connect to a 220pF/50V ceramic capacitor from V_{SYS} to V_{SS}.
VP	22	Power	Main power supply. Provides power to the power drivers as well as voltage feedback path for the switching supply. Connect a properly sized supply bypass capacitor in parallel with a 4.7 µF ceramic capacitor in parallel with a 220µF aluminum capacitor from V_P to V_{SS} for voltage loop stabilization. This pin requires good capacitive bypassing to V_{SS}, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin.
SW	23	Power	Switch node for the medium-voltage buck regulator.
CSM	24	Power	High-Voltage Buck Regulator Switching supply current sense input. Connect to the positive side of the current sense resistor.
VM	25	Power	High-Voltage Buck Regulator supply controller input. Connect a 0.1µF higher value ceramic capacitor from VM to VSS. This pin requires good capacitive bypass to V_{SS}, so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin.
SRC	26	Power	High-Voltage Buck Regulator Source. Connect to the source of the high-side power MOSFET of the high-voltage buck regulator.
DRM	27	Power	High-Voltage Buck Regulator gate driver. Connect to the gate of the high-side power MOSFET of the high-voltage buck regulator.
BST	28	Power	High-Voltage Buck Regulator bootstrap input. Connect a 2.2µF/25V or higher value ceramic capacitor from BST to SRC. The ceramic capacitor must be connected with a shorter than 10mm trace to the device pin.
VSS	38	Power	Ground.
VCC18	43	Power	Internally generated 1.8V power supply. Connect a 2.2 µF or higher value ceramic capacitor from V_{CC18} to V_{SSA}.
VCORE	48	Power	Internally generated digital logic 1.2V power supply. Connect a 2.2 µF or higher value ceramic capacitor from V_{CORE} to V_{SSA}.
VCCIO	49	Power	Internally generated digital I/O 3.3V power supply. Connect a 4.7 µF or higher value ceramic capacitor from V_{CCIO} to V_{SSA}.
EP (VSS)	EP	Power	Exposed pad. Must be connected to V_{SS} in a star ground configuration. Connect to a large PCB copper area for power dissipation heat sinking.

9.2 Signal Manager Pin Description

Table 9-2 Signal Pin Description

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION
AIO7	8	AIO7	I/O	Analog front end I/O 7.
		AMP7	Analog	PGA input 7.
		CMP7	Analog	Comparator input 7.
		PHC7	Analog	Phase comparator input 7.
AIO8	9	AIO8	I/O	Analog front end I/O 8.
		AMP8	Analog	PGA input 8.
		CMP8	Analog	Comparator input 8.
		PHC8	Analog	Phase comparator input 8.
AIO9	10	AIO9	I/O	Analog front end I/O 9.
		AMP9	Analog	PGA input 9.
		CMP9	Analog	Comparator input 9.
		PHC9	Analog	Phase comparator input 9.
AIO5	11	AIO5	I/O	Analog front end I/O 5.
		DA54P	Analog	Differential PGA 54 positive input.
		AMP5	Analog	PGA input 5.
AIO4	12	AIO4	I/O	Analog front end I/O 4.
		DA54N	Analog	Differential PGA 54 negative input.
		AMP4	Analog	PGA input 4.
AIO3	13	AIO3	I/O	Analog front end I/O 3.
		DA32P	Analog	Differential PGA 32 positive input.
		AMP3	Analog	PGA input 3.
AIO2	14	AIO2	I/O	Analog front end I/O 2.
		DA32N	Analog	Differential PGA 32 negative input.
		AMP2	Analog	PGA input 2.
AIO1	15	AIO1	I/O	Analog front end I/O 1.
		DA10P	Analog	Differential PGA 10 positive input.
		AMP1	Analog	PGA input 1.
AIO0	16	AIO0	I/O	Analog front end I/O 0.
		DA10N	Analog	Differential PGA 10 negative input.
		AMP0	Analog	PGA input 0.
AIO6	17	AIO6	I/O	Analog front end I/O 6.
		AMP6	Analog	PGA input 6.
		CMP6	Analog	Comparator input 6.
		BUF6	Analog	Buffer output 6.
		PBTN	Analog	Push button input.

9.3 Driver Manager Pin Description

Table 9-3 Driver Manager Pin Description

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
DRL2	19	Analog	Low-side gate driver 2.
DRL1	20	Analog	Low-side gate driver 1.
DRL0	21	Analog	Low-side gate driver 0.
DXS0	29	Analog	Ultra-high-voltage high-side gate driver source 0.
DXH0	30	Analog	Ultra-high-voltage high-side gate driver 0.
DXB0	31	Analog	Ultra-high-voltage high-side gate driver bootstrap 0. Connect a 1µF or higher value ceramic capacitor from DXB0 to DXS0. This pin requires good capacitive bypass so it must be connected with a 10mm or shorter trace.
DXS1	32	Analog	Ultra-high-voltage high-side gate driver source 1.
DXH1	33	Analog	Ultra-high-voltage high-side gate driver 1.
DXB1	34	Analog	Ultra-high-voltage high-side gate driver bootstrap 1. Connect a 1µF or higher value ceramic capacitor from DXB1 to DXS1. This pin requires good capacitive bypass so it must be connected with a 10mm or shorter trace.
DXS2	35	Analog	Ultra-high-voltage high-side gate driver source 2.
DXH2	36	Analog	Ultra-high-voltage high-side gate driver 2.
DXB2	37	Analog	Ultra-high-voltage high-side gate driver bootstrap 2. Connect a 1µF or higher value ceramic capacitor from DXB2 to DXS2. This pin requires good capacitive bypass so it must be connected with a 10mm or shorter trace.

9.4 I/O Ports Pin Description

Table 9-4 I/O Ports Pin Description

PIN NAME	PIN NUMBER	FUNCTION	TYPE	DESCRIPTION[1]
PF4/ADC4	1	PF4	I/O	I/O port PF4.
		ADC4	Analog	ADC channel ADC4.
PF3	2	PF3	I/O	I/O port PF3.
PF2	3	PF2	I/O	I/O port PF2.
PF1	4	PF1	I/O	I/O port PF1.
PF0	5	PF0	I/O	I/O port PF0.
PE0	39	PE0	I/O	I/O port PE0.
PE1	40	PE1	I/O	I/O port PE1.
PE2	41	PE2	I/O	I/O port PE2.
PE3	42	PE3	I/O	I/O port PE3.
PE4	44	PE4	I/O	I/O port PE4.
PE5	45	PE5	I/O	I/O port PE5.
PE6	46	PE6	I/O	I/O port PE6.
PE7	47	PE7	I/O	I/O port PE7.
PF7/ADC7	50	PF7	I/O	IO port PF7.
		ADC7	Analog	Analog channel ADC7.
PF6/ADC6	51	PF6	I/O	I/O port PF6.
		ADC6	Analog	Analog channel ADC6.
PF5/ADC5	52	PF5	I/O	IO port PF5.
		ADC5	Analog	Analog channel ADC5.

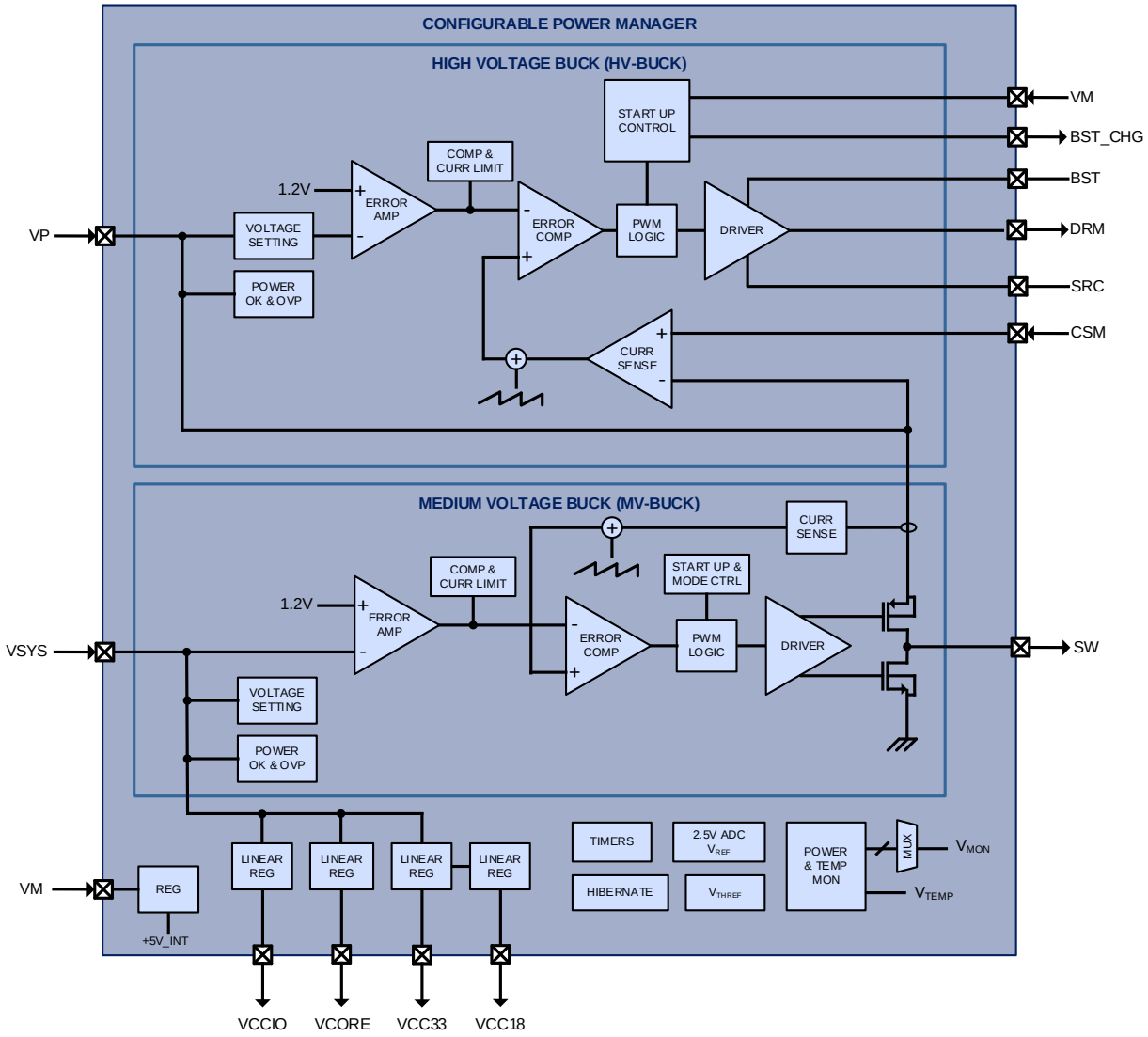
[1] For a full description of all of the pin configurations for each digital I/O, see the PAC55XX Family User Guide for the Peripheral MUX.

10 CONFIGURABLE POWER MANAGER (CPM)

10.1 Features

- 600V Switching Controller (HV-BUCK)
- 5V Switching Regulator (MV-BUCK) with integrated FET
- 4 linear regulators with power and hibernate management
- V_{REF} for ADC
- Power and temperature monitor, warning, and fault detection

Figure 10-1 CPM Block Diagram



10.2 Functional Description

- The Configurable Power Manager (600V Switching Controller (HV-BUCK)
- 5V Switching Regulator (MV-BUCK) with integrated FET
- 4 linear regulators with power and hibernate management
- V_{REF} for ADC
- Power and temperature monitor, warning, and fault detection

Figure 10-1) is optimized to efficiently provide “all-in-one” power management required by the PAC and associated application circuitry. It incorporates a high-voltage DC/DC controller that is used to convert power from a DC input source to generate a main supply output V_P. There is also an integrated medium-voltage buck DC/DC regulator to generate V_{SYS}.

Four other linear regulators provide V_{CCIO}, V_{CC33}, V_{CORE} and V_{CC18} supplies for 3.3V I/O, 3.3V mixed signal, 1.9V microcontroller core circuitry and MCU FLASH. The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

10.3 High-Voltage Supply Controller (HV-BUCK)

The PAC5556 contains a 600V High-Voltage Supply Controller (Buck DC/DC). This power supply is used to supply the various regulators in the PAC5556, as well as generating the V_P gate drive voltage for the Application Specific Driver Manager (ASPD).

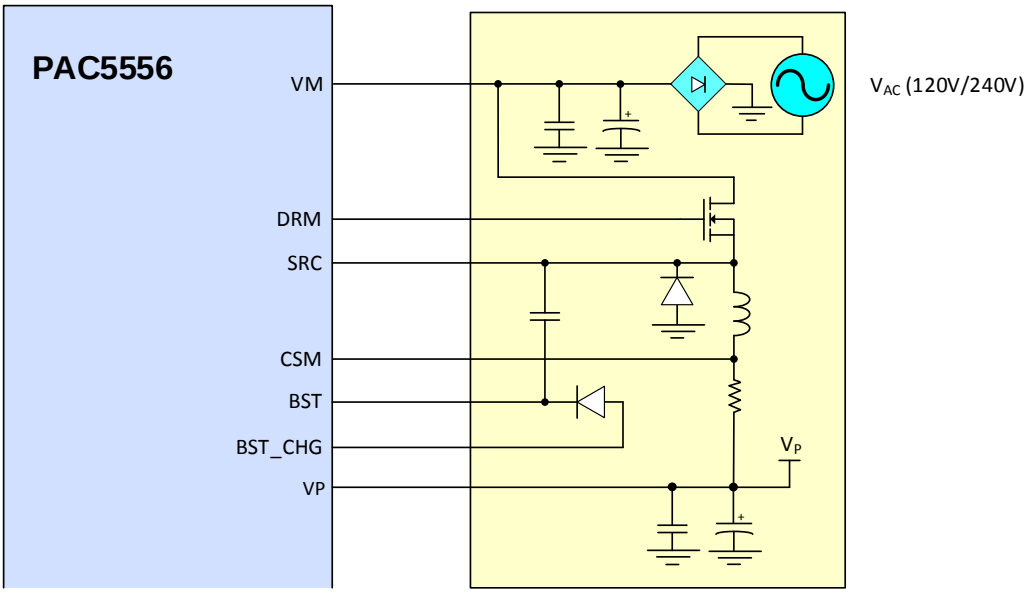
The HV-BUCK controller converts the motor voltage (V_M) to the gate driver and IC system supply (V_P). The VM input is the HV-BUCK supply regulator input and is connected to the rectified DC motor voltage source. The BST and SRC pins are connected to the boot-strap and source nodes of the power supply, respectively. The BST_CHG pin is used to initially charge the boot-strap capacitor in the HV-BUCK.

The V_P regulation voltage is initially set to 15V during start up, and may be reconfigured to be 12V by the microcontroller after initialization. When V_P is lower than the target regulation voltage, the internal feedback control circuitry causes the inductor current to increase to raise V_P. Conversely, when V_P is higher than the regulation voltage, the feedback loop control causes the inductor current to decrease to lower V_P. The feedback loop is internally stabilized. The output current capability of the switching supply is determined by the external current sense resistor. The inductor current signal is sensed differentially between the CSM pin and V_P, and has a peak current limit threshold of 0.2V.

The CPM may be used to supply both AC offline or DC supplied applications of up to 600VDC.

The diagram below shows an example of the PAC5556 with a 120Hz/240Hz AC application.

Figure 10-2 HV-BUCK with AC Supply



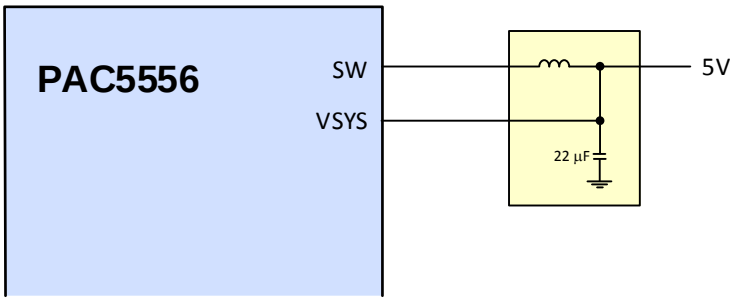
The switching frequency and output voltage of the HV-BUCK can be reconfigured by the MCU. The switching frequency can be configured to be between 25kHz and 125kHz and the gate drive output voltage can be configured to 12V or 15V.

10.4 Medium-Voltage Buck Regulator (MV-BUCK)

The PAC5556 contains a Medium-Voltage Buck Switching Regulator that generates a 5V/200mA supply for the device, as well as PCB functions.

The SW pin is the switch node of the Buck regulator. The Power MOSFET is integrated, so connect this pin to VSYS through an external inductor. The VSYS pin is the 5V regulator output, which should be bypassed to ground with a 22µF ceramic capacitor.

Figure 10-3 MV-BUCK Switching Regulator Example

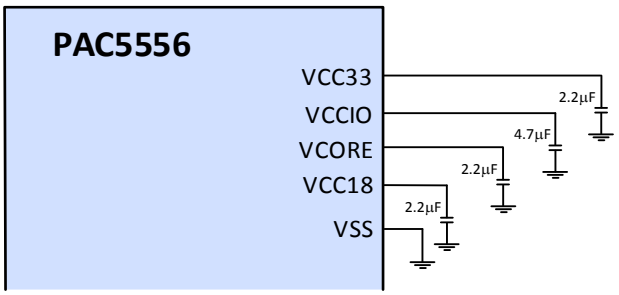


The output of VSYS is fixed at 5V and the switching frequency is 1.33MHz.

10.5 Linear Regulators

The CPM includes four additional linear regulators. VSYS supplies these three regulators. Once VSYS is above 4V, these four additional linear regulators for VCCIO, VCC33, VCC18 and VCORE supplies sequentially power up.

Figure 10-4 Linear Regulators Example



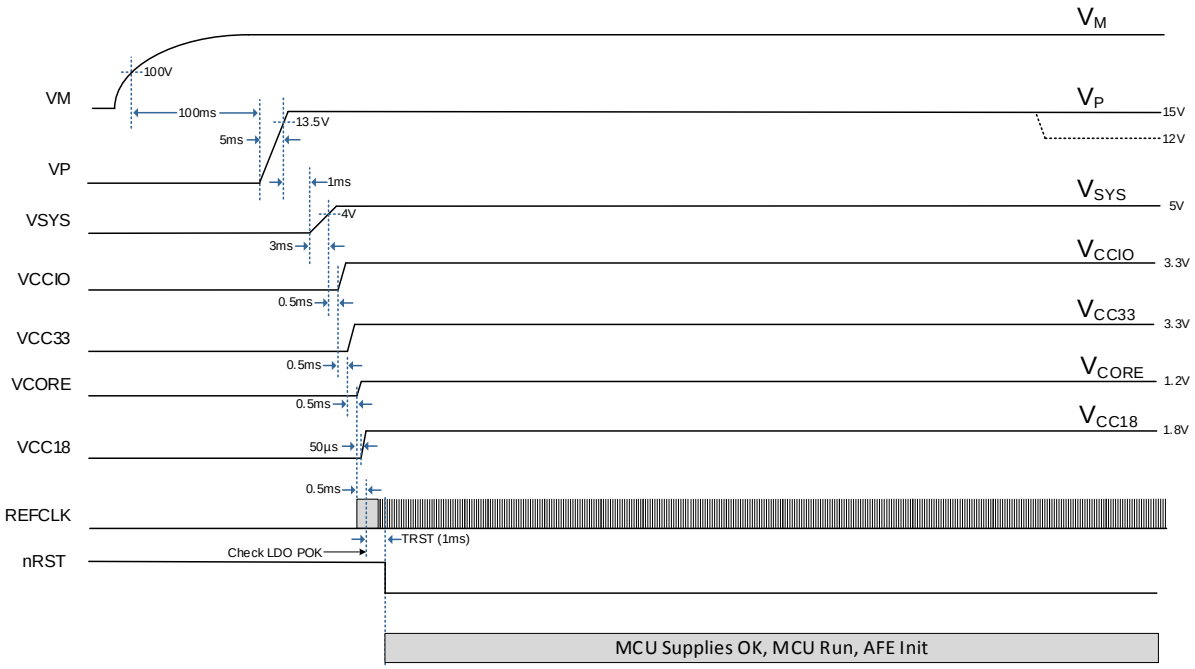
The figure above shows typical circuit connections for the linear regulators. The VCCIO regulator generates a dedicated 3.3V supply for the MCU IO. The VCC33 regulator generates a 3.3V supply for the analog peripherals in the MCU and the VCC18 LDO. The VCORE regulator generates a 1.2V supply for the MCU digital logic. The VCC18 regulator supplies a 1.8V supply for the MCU FLASH.

When VSYS, VCCIO, VCC33, and VCORE are all above their respective power good thresholds, and the configurable power on reset duration has expired, the microcontroller is initialized.

10.6 Power-up Sequence

The CPM follows a typical power up sequence as in the Figure 10-5 below.

Figure 10-5 Power-Up Sequence



A typical sequence begins with power being applied to VM. When VM reaches 100V, the HV-BUCK controller is started. After the boot-strap capacitor is charged VP starts to rise. VP rises to 90% of the target setting of 15V (13.5V) within 5ms, then there is a 1ms delay and then the MV-BUCK is started. When the VSYS output of the MVBK rises to 4V, then there is a 0.5ms delay and the VCCIO LDO is enabled. Then there is a 0.5ms delay and the VCC33 LDO is enabled. Then there is a 0.5ms delay and the VCORE LDO is enabled. The VCC18 LDO starts after 50µs after VCORE.

There is then a 0.5ms delay and the power good threshold of all LDOs is checked. If all are OK, then there is an additional 1ms delay (TRST), then the POR signal is asserted to the MCU and it begins executing firmware.

During the firmware initialization process, the MCU may change the VP output voltage setting from the 15V default to 12V.

10.7 Hibernate Mode

The PAC5556 can go into an ultra-low power hibernate mode via the microcontroller firmware or via the optional push button (PBTN, see *Push Button* description in *Configurable Analog Front End*). In hibernate mode, only a minimal amount of current is used by V_M (typically 8µA at 170VDC), and the CPM controller and all internal regulators are shut down to eliminate power drain from the output supplies. The system exits hibernate mode after a wake-up timer duration (configurable from 125ms to 8s or infinite) has expired or, if push button enabled, after an additional push button event has been detected. When exiting the hibernate mode, the power manager goes through the start up cycle and the microcontroller is reinitialized. Only the persistent power manager status bits (resets and faults) are retained during hibernation.

10.8 Power Monitor

Whenever any of the V_{SYS}, V_{CCIO}, V_{CC33}, or V_{CORE} power supplies fall below their respective power good threshold voltage, a fault event is detected and the microcontroller is reset. The microcontroller stays in the reset state until V_{SYS}, V_{CCIO}, V_{CC33}, and V_{CORE} supplies are all good again and the reset time has expired.

These power supplies may also be monitored by the ADC. The PWRMON MUX allows the user to select which channels may be monitored by the ADC. The channels that may be monitored are shown below:

- V_{CORE}
- V_{CORE} * 4/10
- V_{CC33} * 4/10
- V_{CCIO} * 4/10
- V_{SYS} * 4/10
- VMS[2]
- VPTAT[3]
- VMS (buffered)

For details on how to select the power monitor channels using the ADC, see the section below on ADC Analog Input.

[2] VMS is the scaled value of the VM power supply input. For more information on how to convert this value to volts, see the PAC5556 Device User Guide.
[3] VPTAT is the internal temperature sensor value. For more information on how to convert this value to degrees C, see the PAC5556 Device User Guide.

10.9 Electrical Characteristics

Table 10-1 High-Voltage Buck Controller Electrical Characteristics

(V_M = 330V, V_P = 15V and T_J = 25°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
V_M	Motor voltage range			0		600	V
$I_{HIB;VM}$	V_M hibernate mode supply current	HIB = 1	VM = 170V		8	16	µA
			VM = 330V		18		
$V_{UVLOR;VM}$	V_M UVLO rising				82		V
$V_{UVLOF;VM}$	V_M UVLO falling				62		V
V_{SRC}	Level-shifted driver source voltage range	Repetitive, 10µs pulse		-10		605	V
		Steady state		0		600	V
V_{BST}	BST pin voltage range	Repetitive, 10µs pulse		1		625	V
$V_{BS;BST}$	Boot-strap supply voltage range	Steady state		9		620	V
		V_{BST}, relative to V_{SRC}		9		20	V
$V_{UVLOR;BST}$	Boot-strap UVLO rising threshold				7		V
$V_{UVLOF;BST}$	Boot-strap UVLO falling threshold				6.2		V
V_{DRM_MINON}	DRM minimum on time				200		ns
V_{DRM_MINOFF}	DRM minimum off time				1200		ns
$V_{REF;VP}$	V_P output regulation voltage	V_P = 15V		-5%	15	5%	V
$k_{POKR;VP}$	V_P power OK threshold	V_P rising			91		%
		V_P falling			87		%
$k_{OVPR;VP}$	V_P OV protection threshold	V_P rising			130		%
$f_{SWM;DRM}$	Switching frequency programmable range			25		125	kHz
I_{SRC}	Source node current output				100		mA
I_{SNK}	Sink node current output				200		mA
$V_{UVLOR;VP}$	V_P UVLO rising				10		V
$V_{UVLOF;VP}$	V_P UVLO falling				8		V
$V_{CSM;ILIM}$	CSM current limit threshold			-10%	0.2	10%	V
	HV-BUCK inductor value				680		µH
R_{DSG}	Discharge resistance				1		kΩ

Table 10-2 Medium-Voltage Buck Controller Electrical Characteristics

(V_M = 330V, V_P = 15V and T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{VSYS}	V_{SYS} output voltage accuracy		-3%	5	3%	V
F_{SW}	Switching frequency		-5%	1.33	5%	MHz
$I_{VSYS;LIM}$	V_{SYS} current limit		320		450	mA
$V_{POK;VSYS}$	V_{SYS} power OK threshold	Rising	4.25	4.5	4.75	V
		Falling		4.2		V
	V_{SYS} power OK blanking delay			10		µs
	MV-BUCK inductor value	Current rating of at least 750mA	6.8 - 20%		10 + 20%	µH
$V_{UVLO;VSYS}$	V_{SYS} UVLO	Rising		4.5		V
		Falling		4.2		V
$V_{OVP;VSYS}$	V_{SYS} OVP	Rising		5.5		V
		Falling		5.2		V
$R_{DSCH;VSYS}$	V_{SYS} discharge resistance			2.5		kΩ

Table 10-3 Linear Regulators Electrical Characteristics

(V_P = 12V and T_A = -40°C to 125°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CCIO}	V_{CCIO} output voltage	Load = 1mA	-3%	3.3	3%	V
V_{CCIO}	V_{CCIO} output voltage	Load = 1mA	-3%	3.3	3%	V
V_{CORE}[4]	V_{CORE} output voltage	Load = 1mA	-3%	1.2	3%	V
V_{CC18}	V_{CC18} output voltage			1.8		V
$I_{LIM;VCCIO}$	V_{CCIO} current limit		40	65		mA
$I_{LIM;VCC33}$	V_{CC33} current limit		40	65		mA
$I_{LIM;VCORE}$	V_{CORE} current limit		40	65		mA
	LDO current fold back			50		%
$t_{POK;BLANK}$	Power OK blanking delay	V_{CCIO}, V_{CC33}, V_{CORE}		10		µs
R_{DISCH}	Output discharge resistance	LDO off		300		Ohm
C_{VCCIO}	VCCIO stable output capacitance		1		10	µF
C_{VCC33}	VCC33 stable output capacitance		1		10	µF
C_{VCORE}	VCORE stable output capacitance		1		10	µF
$V_{LDO;POK}$	LDO power OK rising threshold	Hysteresis = 10%	85	90	95	%

Table 10-4 Power Monitor Electrical Characteristics

(T_A = -40°C to 125°C unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
k_{MON}	Power monitoring voltage	V_{CORE}		1		V/V
		V_{SYS}, V_{CCIO}, V_{CC33}		0.4		

[4] Note that the VCORE LDO may not have any other loads. The only connection to the VCORE pin should be a bypass capacitor to ground.

10.10 Typical Performance Characteristics

(T_A = 25ºC unless otherwise specified)

Figure 10-6 VDDIO LDO Voltage vs. Current

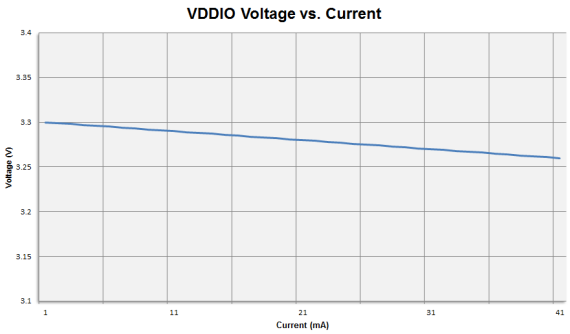


Figure 10-7 VCC33 LDO Voltage vs. Current

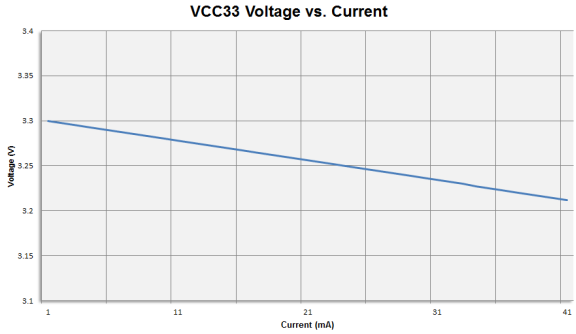
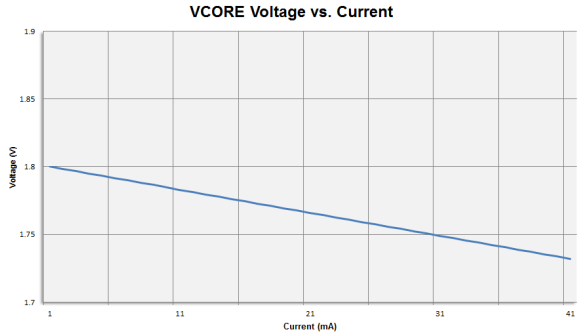


Figure 10-8 VCORE LDO Voltage vs. Current



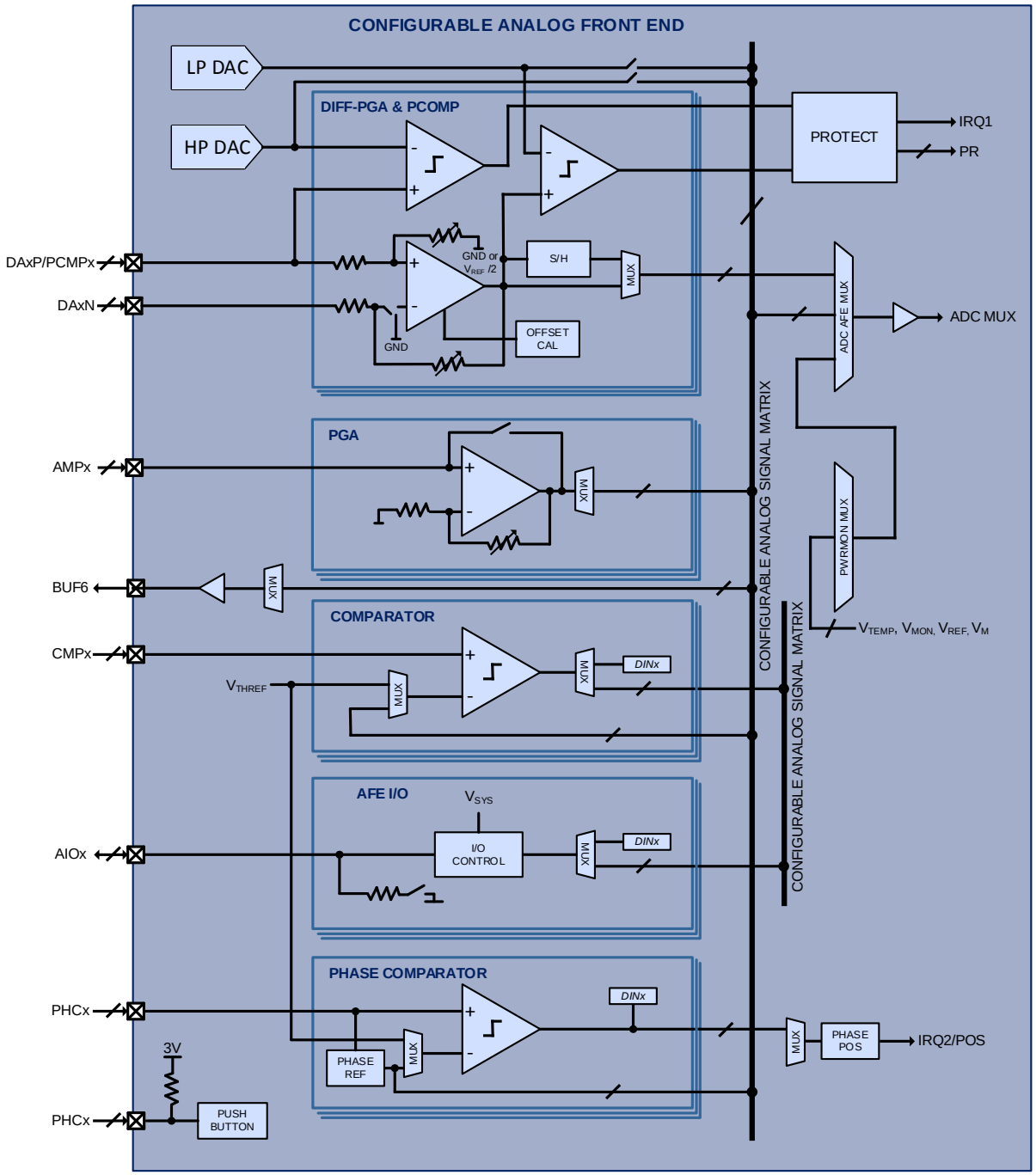
11 CONFIGURABLE ANALOG FRONT END (CAFE)

11.1 Features

- 10 Configurable Analog I/O signals
  - Gain mode, comparator mode, I/O mode, special mode
- 3 High-Performance, Configurable Differential Amplifiers
- 4 High-Performance, Configurable Single-Ended Amplifiers
- Two high-speed comparators with protection functions
- Phase to phase, phase to center-tap modes
- Bi-directional, asymmetric configurable comparator hysteresis
- Push-button input for entering/exiting hibernate mode
- Integrated VM sampling using ADC

11.2 Block Diagram

Figure 11-1 Configurable Analog Front End



11.3 Functional Description

The device includes a Configurable Analog Front End™ (CAFE, Figure 11-1) accessible through 10 analog and I/O pins. These pins can be configured to form flexible interconnected circuitry made up of 3 differential programmable gain amplifiers, 4 single-ended programmable gain amplifiers, 10 protection comparators, and one buffer output.

Each of these pins can also be programmed as analog feed-through pins, or as analog front end I/O pins that can function as digital inputs or digital open-drain outputs. The PAC proprietary configurable analog signal matrix (CASM) and configurable digital signal matrix (CDSM) allow real time asynchronous analog and digital signals to be routed in flexible circuit connections for different applications. A push button function is provided for optional push button on, hibernate, and off power management function.

11.4 Differential Programmable Gain Amplifier (DA)

The DAxP and DAxN pin pair are positive and negative inputs, respectively, to a differential programmable gain amplifier. The differential gain can be programmable to be 1x, 2x, 4x, 8x, 16x, 32x, and 48x for zero-ohm signal source impedance. The differential programmable gain amplifier has -0.3V to 2.5V input common mode range, and its output can be configured for routing directly to the ADC pre-multiplexer, or through a sample-and-hold circuit synchronized with the ADC auto-sampling mechanism. Each differential amplifier is accompanied by offset calibration circuitry, and two protection comparators for protection event monitoring. The programmable gain differential amplifier is optimized for use with signal source impedance lower than 500Ω and with matched source impedance on both positive and negative inputs for minimal offset. The effective gain is scaled by 13.5k / (13.5k + R_{SOURCE}), where R_{SOURCE} is the matched source impedance of each input.

Each differential amplifier is connected to a pair of AIO pins on the PAC5556. AIO<1:0> are connected to one differential amplifier; AIO<3:2> are connected to one differential amplifier and AIO<5:4> are connected to one differential amplifier.

11.5 Single-Ended Programmable Gain Amplifier (AMP)

Each AMPx input goes to a single-ended programmable gain amplifier with signal relative to V_{SS}. The amplifier gain can be programmed to be 1x, 2x, 4x, 8x, 16x, 32x, and 48x, or as analog feed-through. The programmable gain amplifier output is routed via a multiplexer to the configurable analog signal matrix CASM.

11.6 General Purpose Comparator (CMP)

The general-purpose comparator takes the CMPx input and compares it to either the programmable threshold voltage (V_{THREF}) or a signal from the configurable analog signal matrix CASM. The comparator has 0V to V_{SYS} input common mode range, and its polarity-selectable output is routed via a multiplexer to either a data input bit or the configurable digital signal matrix CDSM.

11.7 Phase Comparator (PHC)

The phase comparator takes the PHCx input and compares it to either the programmable threshold voltage (VTHREF) or a signal from the configurable analog signal matrix CASM. The comparison signal can be set to a phase reference signal generated by averaging the PHCx input voltages. In a three-phase motor control application, the phase reference signal acts as a virtual center tap for BEMF detection. The PHCx inputs are optionally fed through to the CASM. The PHC inputs can be compared to the virtual center-tap, or phase to phase for the most efficient BEMF zero-cross detection. The phase comparators have configurable asymmetric hysteresis.

The phase comparator has 0V to V_{SYS} input common mode range, and its polarity-selectable output is routed to a data input bit and to the phase/position multiplexer synchronized with the auto-sampling sequencers.

11.8 Protection Comparator (PCMP)

Two protection comparators are provided in association with each differential programmable gain amplifier, with outputs available to trigger protection events and accessible as read-back output bits. The high-speed protection (HP) comparator compares the AIO<n+1> pin to the 10-bit HP DAC output voltage, with full scale voltage of 2.5V. The limit protection (LP) comparator compares the differential programmable gain amplifier output to the 10-bit LP DAC output voltage, with full scale voltage of 2.5V.

Each protection comparator has a mask bit to prevent or allow it to trigger the main microcontroller interrupt IRQ1. Each protection comparator also has one mask bit to prevent or allow it to activate protection event PR. This protection event can be used directly by protection circuitry in the Application Specific Power Drivers (ASPD) to protect devices being driven.

11.9 Analog Output Buffer (BUF)

A subset of the signals from the configurable analog signal matrix CASM can be multiplexed to the AIO6 pin for external use. The buffer offset voltage can be minimized with the built-in swap function.

11.10 Analog Front End I/O (AIO)

The PAC5556 has 10 AIOx pins that are available. When in digital IO mode, each of these pins can be configured to be a digital input or digital open-drain output. The AIOx input or output signal can be set to a data input or output register bit, or multiplexed to one of the signals in the configurable digital signal matrix CDSM.

The signal can be set to active high (default) or active low, with V_{SYS} supply rail. Where $AIO_{6,7,8,9}$ supports microcontroller interrupt for external signals. Each has two mask bits to prevent or allow rising or falling edge of its corresponding digital input to trigger second microcontroller interrupt IRQ2.

11.11 Push Button (PBTN)

When the user commands the PAC5556 into hibernate mode, the device is put into a very low-power state and the MCU is not powered. To exit from hibernate mode, the user may use the push-button (PBTN) to wake the system up.

When enabled, the PBTN can be used to detect a user active-low push button event and will wake-up the system from hibernate mode.

In addition, PBTN can also be used as a hardware reset for the microcontroller when it is held low for longer than 8s during normal operation. The PBTN input is active low and has a 55kΩ pull-up resistor to 3V.

11.12 HP DAC and LP DAC

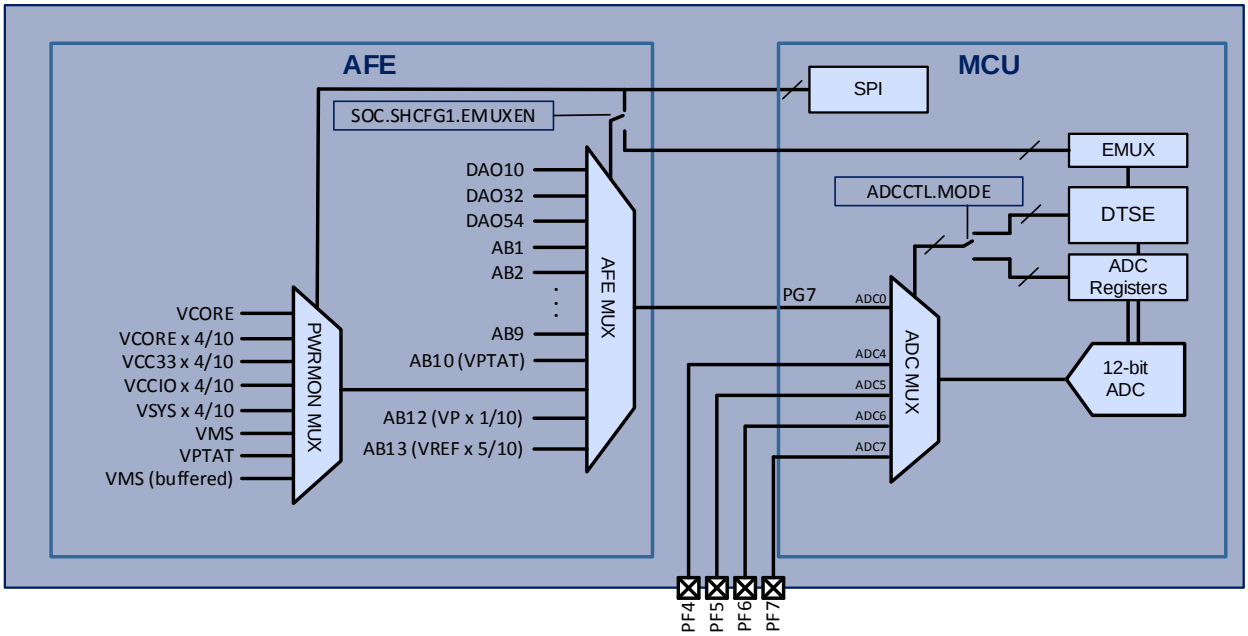
The 10-bit HP DAC can be used as the comparison voltage for the high-speed protection (HP) comparators, or routed for general purpose use via the AB2 signal in the CASM. The HP DAC output full scale voltage is 2.5V.

The 10-bit LP DAC can be used as the comparison voltage for the limit protection (LP) comparators, or routed for general purpose use via the AB3 signal in the CASM. The LP DAC output full scale voltage is 2.5V.

11.13 ADC Analog Input

The PAC5556 has several different Analog Input channels that may be used for analog-to-digital conversion. The diagram below shows the hierarchy of muxes that are available for analog signal sampling.

Figure 11-2 ADC Analog Input Muxes



The PAC5556 contains three hierarchical muxes:

- ADC MUX
- AFE MUX
- PWRMON MUX

The ADC MUX is an 8-channel MUX local to the ADC on MCU that is directly controlled by either by registers in the MCU, or automatically by the ADC sequencer. The output of the ADC MUX is sampled by the ADC. The ADC0 input to the ADC MUX is connected to the AFE MUX through IO PG7. The ADC MUX input channels ADC4-ADC7 are directly connected to package pins on the PAC5556 as shown below:

- ADC0: PG7
- ADC4: PF4
- ADC5: PF5
- ADC6: PF6
- ADC7: PF7

The AFE MUX is a 16-to-1 multiplexer that selects between the 3 differential programmable gain amplifier outputs, AB1 through AB9, temperature monitor signal (VPTAT), power monitor signal (from the PWRMON MUX), attenuated VP voltage and VREF. The output of the AFE MUX is connected to channel ADC0 on the ADC MUX on the MCU. The ADC AFE MUX can be directly controlled or automatically scanned by the ADC DTSE through the high-speed EMUX channel select.

The PWRMON MUX is an 8-channel MUX that selects between the internal regulators on the PAC5556 for diagnostic purposes. The output of the PWRMON MUX is connected to channel AB11 on the AFE MUX. The MUX channel select is available through the SPI SOC bus between the MCU and AFE.

For more information on controlling the various MUXes for ADC and ADC sequencer sampling, see the PAC5556 Device User Guide.

11.14 Configurable Analog Signal Matrix (CASM)

The CASM has 9 general purpose analog signals labeled AB1 through AB9 that can be used for:

- Routing the single-ended programmable gain amplifier or analog feed-through output to AB1 through AB9
- Routing an analog signal via AB1, AB2, or AB3 to the negative input of a general-purpose comparator or phase comparator
- Routing the 10-bit HP DAC output to AB2
- Routing the 10-bit LP DAC output to AB3
- Routing analog signals via AB1 through AB12 to the ADC pre-multiplexer
- Routing phase comparator feed-through signals to AB7, AB8, and AB9, and averaged voltage to AB1

11.15 Configurable Digital Signal Matrix (CDSM)

The CDSM has 7 general purpose bi-directional digital signals labeled DB1 through DB7 that can be used for:

- Routing the AIOx input to or output signals from DB1 through DB7
- Routing the general-purpose comparator output signals to DB1 through DB7

11.16 Cycle-by-cycle Current Limit

The PAC5556 contains hardware support for cycle by cycle current limit. The user may configure this feature to use the LPCOMP DAC as the current threshold. The CAFE will automatically perform duty cycle truncation to lower current at any time the associated phase current is greater than the setting of the LPCOMP DAC.

11.17 Integrated VM ADC Sampling

The PAC5556 contains integrated sampling of the VM (motor voltage) input using the ADC without having to dedicate an external pin to this sampling circuit on the PCB.

To sample the VM motor voltage (called VMS), the user should select the VMS voltage on the PWRMON MUX, and set the ADC AFE MUX to AB11 (PWRMON) and may use the ADC to sample channel ADC0 to read this value.

In INFO FLASH, there are two linear sampling points for the VM ADC input: VMS100 and VMS200. These contain calibrated values for two sample points of VM = 100V and VM = 200V.

To calculate the actual VM sampling point, using the equation below.

- VM = 100 * (VMS_ADC[5] - VMS100) / (VMS200 - VMS100) + 100V

These can be used to calibrate the measured VM voltage and can be used by algorithms that need an accurate VM voltage for control.

For more information on how to set the device registers to read VMS, see the Application Note on this topic.

[5] Power monitor sampled VMS voltage in ADC counts

11.18 Temperature Warnings and Faults

The PAC5556 integrates a temperature sensor that is used for temperature protection and monitoring. The PAC5556 monitors the device temperature during operation for temperature warnings and faults.

If the device temperature reaches 140°C, the device enters the temperature warning state. When in this state, the device will continue to operate normally. The user may enable a maskable interrupt to notify the MCU of this event. While in the temperature warning state, if the temperature falls below 125°C, the device exits the temperature warning state.

If the device temperature reaches 165°C, the device enters the temperature fault state. When this state is entered, the Power Manager disables all of the power supplies, the ASPD and CAFE are disabled. The Power Manager will also set fault bits for the over-temperature and power supply failure conditions. While in this state, if the temperature falls below 155°C then the device will re-start the power supplies and the MCU will re-start. The MCU may check the fault bits to determine that this condition occurred when it is initializing itself.

For more details on temperature warning and fault handling, see the PAC5556 Device User Guide.

11.19 Temperature Monitoring

The PAC5556 has an integrated temperature sensor that may be sampled by the ADC in the MCU.

The voltage of the temperature sensor is called VPTAT. The PAC5556 stores calibration values for the temperature sensor in INFO FLASH. The MCU may calculate the device temperature by sampling VPTAT and using the calibration values stored in INFO FLASH.

For more information on how to calculate device temperature from VPTAT see the PAC5556 Device User Guide.

For details on how to select the temperature sensor channel using the ADC, see the section above on ADC Analog Input and the PAC5556 Device User Guide.

11.20 Voltage Reference

The reference block includes a 1.2V high-precision reference voltage used internally and for all the LDOs. There is also a high-accuracy 2.5V programmable reference for the ADC V_{REF} on the MCU. There is also a 4-level programmable threshold voltage V_{THREF} (0.1V, 0.2V, 0.5V, and 1.25V).

11.21 Electrical Characteristics

Table 11-1 Differential PGA (DA) Electrical Characteristics (AIO<5:0>)

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;DA}$	Input common mode range		-0.3		2.5	V
$V_{OLR;DA}$	Output linear range		0.1		V_{SYS} - 0.1	V
$V_{SHR;DA}$	Sample and hold range		0.1		3.5	V
$I_{CC;DA}$	Operating supply current	Each enabled amplifier		150	300	µA
$V_{OS;DA}$	Input offset voltage	Gain = 8x	-8		8	mV
$k_{CMRR;DA}$	Common mode rejection ratio		50	80		dB
	Slew rate	Gain = 8x	10			V/µs
$R_{INDIF;DA}$	Differential input impedance			27		kΩ
$t_{ST;DA}$	Settling time	To 1% of final value			360	ns
$A_{VZI;DA}$	Differential amplifier gain (zero ohm source impedance)	Gain = 1x		1		%
		Gain = 2x		2		
		Gain = 4x		4		
		Gain = 8x, $V_{DAxP} = V_{DAxN} = 0V$, T_A = 25°C	-2		2	
		Gain = 16x		16		
		Gain = 32x		32		
		Gain = 48x		48		

Table 11-2 Single-Ended PGA (AMP) Electrical Characteristics (AIO<9:6>)

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;AMP}$	Input common mode range		0		V_{SYS}	V
$V_{OLR;AMP}$	Output linear range		0.1		V_{SYS} - 0.1	V
$I_{CC;AMP}$	Operating supply current	Each enabled amplifier		80	120	µA
$V_{OS;AMP}$	Input offset voltage	Gain = 8x	-10		10	mV
	Slew rate	Gain = 1x	10			V/µs
$t_{ST;AMP}$	Settling time	To 1% of final value			360	ns
$A_{V;AMP}$	Amplifier gain	Gain = 1x		1		%
		Gain = 2x		2		
		Gain = 4x		4		
		Gain = 8x, V_{AMPx} = 125mV, T_A = 25°C	-2		2	
		Gain = 16x		16		
		Gain = 32x		32		
		Gain = 48x		48		
$t_{ST;AMP}$	Settling time	To 1% of final value			360	ns

Table 11-3 General Purpose Comparator (CMP) Electrical Characteristics (AIO<9:6>)

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;CMP}$	Input common mode range		0		V_{SYS}	V
$I_{CC;CMP}$	Operating supply current	Each enabled comparator		35	70	µA
$V_{OS;CMP}$	Input offset voltage		-10		10	mV
$V_{HYS;CMP}$	Hysteresis			22		mV
$t_{DEL;CMP}$	Comparator delay				1	µs
$t_{DELMODE;CMP}$	Mode change blanking delay			10		µs

Table 11-4 Phase Comparator (PHC) Electrical Characteristics (AIO<9:6>)

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;PHC}$	Input common mode range		0		V_{SYS}	V
$I_{CC;PHC}$	Operating supply current	Each enabled comparator		35	70	µA
$V_{OS;PHC}$	Input offset voltage		-10		10	mV
$V_{HYS;PHC}$	Hysteresis			22		mV
$t_{DEL;PHC}$	Comparator delay	10mV difference input			1	µs

Table 11-5 Special Mode Electrical Characteristics (AIO<9:7>)

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;SPEC}$	Input common mode range		0		V_{SYS}	V
$I_{CC;SPEC}$	Operating supply current	Each enabled comparator		80	120	µA
$V_{HSYS;SPEC}$	Comparator Hysteresis, HYSMODE = 0	AIO<9:7>HYS = 00b (0mV)		0		mV
		AIO<9:7>HYS = 01b (6mV)	4	6	8	mV
		AIO<9:7>HYS = 10b (12mV)	9	12	15	mV
		AIO<9:7>HYS = 11b (24mV)	18	24	30	mV
	Comparator Hysteresis, HYSMODE = 1	AIO<9:7>HYS = 00b (0mV)		0		mV
		AIO<9:7>HYS = 01b (24mV)	18	24	30	mV
		AIO<9:7>HYS = 10b (48mV)	36	48	60	mV
		AIO<9:7>HYS = 11b (96mV)	72	96	120	mV

Table 11-6 Special Mode Electrical Characteristics (AIO6)

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ICMR;SPEC}$	Input common mode range		0		V_{SYS}	V
$I_{CC;SPEC6}$	Operating supply current			60	120	µA
$V_{INOFF;SPEC6}$	Input offset voltage		-20		20	mV
$I_{OUT;SPEC6}$	Output current			2		mA

Table 11-7 Analog Front End (AIO) Electrical Characteristics (AIO<9:0>)

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{AIO}	Pin voltage range		0		5	V
$V_{IH;AIO}$	High-level input voltage		2.2			V
$V_{IL;AIO}$	Low-level input voltage				0.8	V
$R_{PD;AIO}$	Pull-down resistance	Input mode		1		MΩ
$V_{OL;AIO}$	Low-level output voltage	I_{AIOx}=10mA, open-drain output mode			0.3	V
$I_{OL;AIO}$	Low-level output sink current	V_{AIOx} = 0.4V, open-drain output mode	6	14		mA
$I_{LK;AIO}$	High-level output leakage current	V_{AIOx} = 5V, open-drain output mode		0	10	µA

Table 11-8 Push Button (PBTN) Electrical Characteristics (AIO6)

(T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I;PBTN}$	Input voltage range		0		5	V
$V_{IH;PBTN}$	High-level input voltage		2.2			V
$V_{IL;PBTN}$	Low-level input voltage				0.8	V
$R_{PU;PBTN}$	Pull-up resistance	To 3V, push-button input mode		50		kΩ

Table 11-9 HP DAC and LP DAC Electrical Characteristics

(T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DACREF}	DAC reference voltage	TA = 25°C	-0.5%	2.5	0.5%	V
		TA = -40°C to 105°C	-0.9%	2.5	0.9%	
	HP 10-bit DAN INL		-2		2	LSB
	HP 10-bit DAC DNL		-1		1	LSB
	LP 10-bit DAC INL		-2		2	LSB
	LP 10-bit DAC DNL		-1		1	LSB

Table 11-10 Temperature Protection

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_{WARN}	Temperature warning threshold			140		ºC
$T_{WARN;HYS}$	Temperature warning hysteresis			15		ºC
$T_{WARN;BLANK}$	Temperature warning blanking			10		µs
T_{FAULT}	Temperature fault threshold			165		ºC
$T_{FAULT;HYS}$	Temperature fault hysteresis			15		ºC
$T_{FAULT;BLANK}$	Temperature fault blanking			10		µs

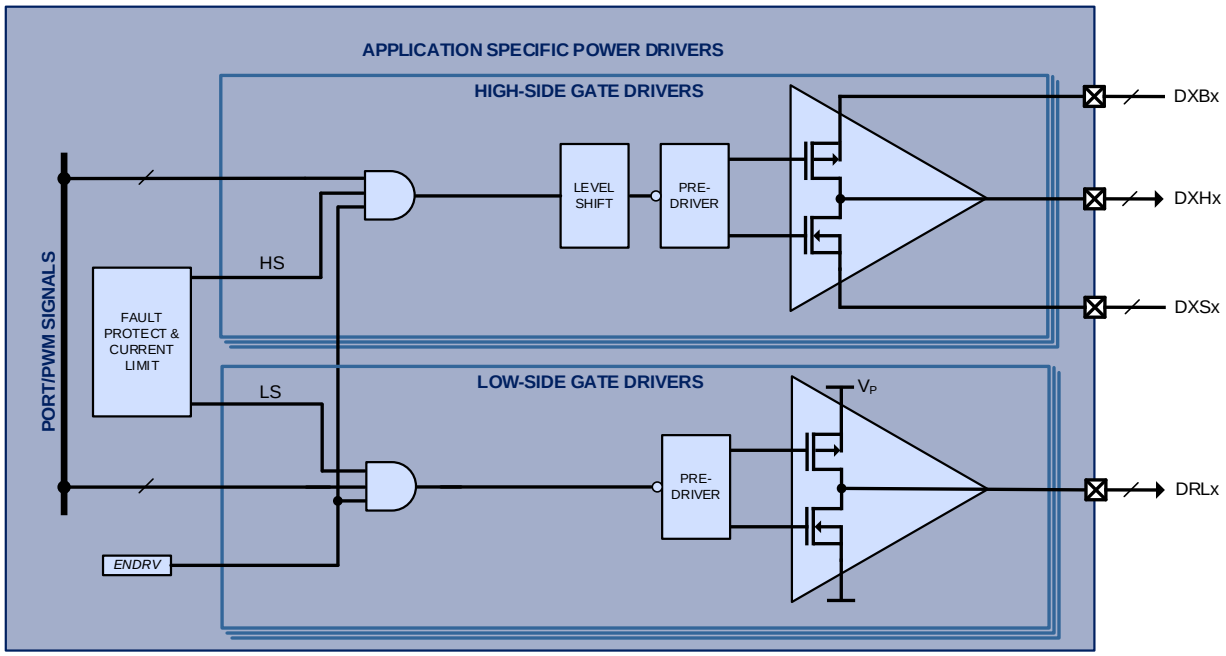
12 APPLICATION SPECIFIC POWER DRIVERS (ASPD)

12.1 Features

- 3 high-side gate drivers with 250mA sink and 500mA source current
- 3 low-side gate drivers with 1A sink and 1A source current
- Fast fault protection
- Cycle-by-cycle current limit function
- Configurable driver break-before-make (BBM) safety function

12.2 Block Diagram

Figure 12-1 Application Specific Power Drivers



12.3 Functional Description

The Application Specific Power Drivers™ (ASPD, Figure 12-1) module handles power driving for power and motor control applications. The ASPD contains three low-side gate drivers (DRLx), three ultra-high-side gate drivers (DXHx). Each gate driver can drive an external IGBT switch in response to high-speed control signals from the microcontroller ports, and a pair of high-side and low-side gate drivers can form a half-bridge driver.

Figure 12-2 below shows typical gate driver connections and Table 12-1 shows the ASPD available resources. The ASPD gate drivers support up to a 600V source supply.

Figure 12-2 Typical Gate Driver Connections

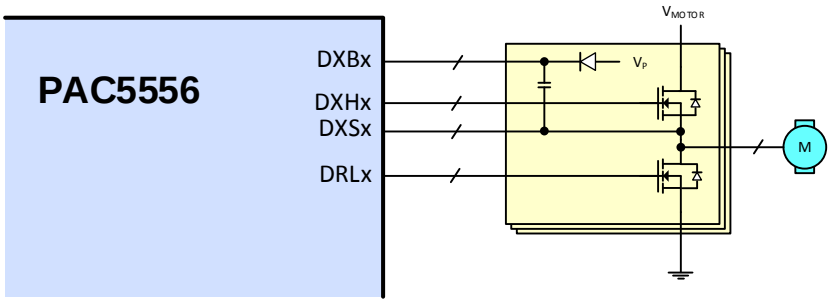


Table 12-1 Power Driver Resources

PART NUMBER	LOW-SIDE GATE DRIVER		HIGH-SIDE GATE DRIVER		
	DRLx	SOURCE/SINK CURRENT	DXHx	SOURCE/BOOTSTRAP SUPPLY	SOURCE/SINK CURRENT
PAC5556	3	1A/1A	3	610V/630V	0.25A/0.5A

The ASPD includes built-in configurable fault protection for the internal gate drivers.

12.4 Low-Side Gate Driver

The DRLx low-side gate driver drives the gate of an external IGBT switch between the low-level power ground rail and high-level V_P supply rail. The DRLx output pin has sink and source output current capability of 1A. Each low-side gate driver is controlled by a microcontroller port signal.

12.5 High-Side Gate Driver

The DXHx high-side gate driver drives the gate of an external MOSFET or IGBT switch between its low-level DXSx driver source rail and its high-level DXBx bootstrap rail. The DXSx pin can go up to 610V. The DXHx output pin has sink output current capability of 0.25A and source output current capability of 0.5A. The DXBx bootstrap pin can have a maximum operating voltage of 20V relative to the DXSx pin. The DXSx pin is designed to tolerate momentary switching negative spikes down to -10V without affecting the DXHx output state. Each high-side gate driver is controlled by a microcontroller port signal.

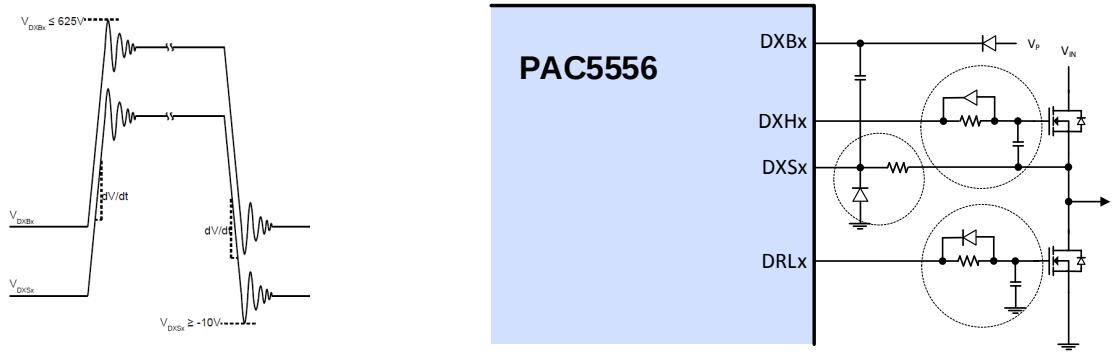
For bootstrapped high-side operation, connect an appropriate capacitor between DXBx and DXSx and a properly rated bootstrap diode from V_P to DXBx.

12.6 High-Side Switching Transients

Typical high-side switching transients are shown in Figure 12-3 below. To ensure functionality and reliability, the DXSx and DXBx pins must not exceed the peak and undershoot limit values shown. This should be verified by probing the DXSx and DXBx pins directly relative to VSS pin. A small resistor and diode clamp for the DXSx pin can be used to make sure that the pin voltage stays within the negative limit value. In addition, the high-side slew rate dV/dt must be kept within ±50V/ns for DXSx. This can be achieved by adding a resistor-diode pair in series, and an optional capacitor in parallel with the power switch gate. The parallel capacitor also provides a low impedance and close gate shunt against coupling from the switch drain.

These optional protection and slew rate control are shown in Figure 12-3.

Figure 12-3 Gate Driver Switching Transients



(a) High-Side Switching Transients

(b) Optional Transient Protection and Slew Rate Control

12.7 Gate Driver Fault Protection

The ASPD incorporates a configurable fault protection mechanism using protection signal from the Configurable Analog Front End (CAFE), designated as protection event 1 (PR) signal.

The DRL0/DRL1/DRL2 drivers are designated as low-side group 1. The DXH0/DXH1/DXH2 gate drivers are designated as high-side group 1. The PR signal from the CAFE can be used to disable low-side group 1, high-side group 1, or both depending on the PR mask bit settings.

12.8 Gate Driver Pull Down

When the PAC5556 is powered-up, the input PWM from the MCU to the ASPD can be in an unknown state. To avoid any incorrect gate driver output, the ASPD includes pull-down resistors for the gate driver output as follows.

The high-side gate driver (DXHx) is pulled down to its source (DXSx) with a 5k resistor. The low-side gate driver (DRLx) is pulled down to ground using a 5k resistor.

12.9 Electrical Characteristics

Table 12-2 Gate Driver Electrical Characteristics

(V_M = 330V, V_P = 15V, and T_A = -40°C to 105°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Low-Side Gate Drivers (DRLx pins)						
$V_{OH;DRL}$	High-level output voltage	I_{DRLx} = -50mA	V_P-0.5			V
$V_{OL;DRL}$	Low-level output voltage	I_{DRLx} = 50mA			0.35	V
$I_{OHPK;DRL}$	Output high source current	10µs pulse		-1		A
$I_{OLPK;DRL}$	Output low sink current	10µs pulse		1		A
High-Side Gate Drivers (DXHx, DXBx and DXSx pins)						
V_{DXS}	Level-shift driver source voltage range	Repetitive, 10µs pulse	-10		605	V
		Steady state	0		600	V
V_{DXB}	Bootstrap pin voltage range	Repetitive, 10µs pulse	1		625	V
		Steady state	9		620	V
$V_{BS;DXB}$	Bootstrap supply voltage range	V_{DXBx}, relative to V_{DXSx}	9		20	V
$V_{UVLO;DXB}$	Bootstrap UVLO threshold	V_{DXBx} rising, relative to respective V_{DXSx}, Hysteresis = 0.5V	7	8	9	V
$I_{BS;DXB}$	Bootstrap supply current			25	50	µA
$I_{OS;DXB}$	Offset supply current	V_{DXBx} = V_{DXSx} = 600V			10	µA
$V_{OH;DXH}$	High-Level output voltage	I_{DXHx} = -20mA	V_{DXBx}-1			V
$V_{OL;DXH}$	Low-level output voltage	I_{DXHx} = 40mA			V_{DXSx}+0.6	V
$I_{OHPK;DXH}$	High-level pulsed peak source current	10µs pulse		-0.25		A
$I_{OLPK;DXH}$	Low-level pulsed peak sink current	10µs pulse		0.5		A

13 SOC CONTROL SIGNALS

The MCU has access to the Analog Sub-system on the PAC5556 through certain digital peripherals. The functions that the MCU may access from the Analog Sub-System are:

- High-side and Low-side Gate Drivers
- SPI Interface for Analog Register Access
- ADC EMUX
- Analog Sub-system Interrupts

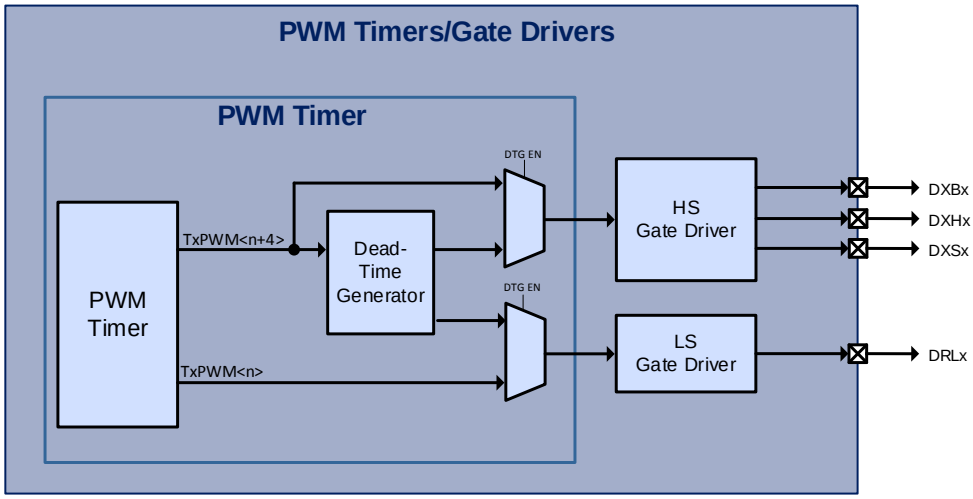
13.1 High-side and Low-Side Gate Drivers

The high-side and low-side gate drivers on the PAC5556 are controlled by PWM outputs of the timer peripherals on the MCU. The timer peripheral generates the PWM output. The PWM timer may be configured to generate a complementary PWM output (high-side and low-side gate drive signals) with hardware controlled dead-time.

These signals are sent to the gate drivers in the Analog Sub-system that create the high and low side gate drivers for the external inverter.

The diagram below shows the block diagram of the PWM timer, DTG and ASPD gate drivers.

Figure 13-1 SOC Signals for Gate Drivers



Each timer peripheral that drives the DTG and ASPD Gate Drivers has two PWM outputs that are connected to the gate drivers: TxPWM<n> and TxPWM<n+4>. If the Dead-Time Generator is disabled TxPWM<n> is connected to the DRLx gate driver output and TxPWM<n+4> is connected to the DXHx gate driver output. If the DTG is enabled, the TxPWM<n+4> is used to generate the complementary high-side and low-side output. For applications that drive half-bridge or full-bridge topologies, the DTG will be enabled to allow a complementary output with dead-time insertion.

Table 13-1 PWM to ASPD Gate Driver Options (DTG Enabled)

Gate Driver	Timer PWM Input	GPIO Port/Pin
Complementary Pair		
DXH0	TBPWM4	PC4
DRL0	TBPWM0	PB0
Complementary Pair		
DXH1	TBPWM5	PC5
DRL1	TBPWM1	PB1
Complementary Pair		
DXH2	TBPWM6	PC6
DRL2	TBPWM2	PB2

Note in the table above that each phase has a complementary pair that is optimized for driving one half-bridge. Each half-bridge uses a pair of timer outputs that have dead-time insertion between them. The complementary pairs are grouped together in this table.

13.2 SPI SOC Bus

The SPI SOC bus is used for reading and writing registers in the Analog Sub-System. The PAC5523 allows both USARTA and USARTB to be used as the SPI master to read and write registers in the Analog Sub-System.

The table below shows which peripherals and which IO pins should be used for this interface.

Table 13-2 SPI SOC Bus Connections

SPI Signal	USART Signal	IO Pin
SCLK	USASCLK	PA3
	USBSCLK	
MOSI	USAMOSI	PA4
	USBMOSI	
MISO	USAMISO	PA5
	USBMISO	
SS	USASS	PA6
	USBSS	

13.3 ADC EMUX

The ADC EMUX is a write-only serial bus that the ADC DTSE uses for instructing the CAFE to perform MUX changes, activate Sample and Hold, etc.

The table below shows the MCU pins that are used by the ADC EMUX in the PAC5556.

Table 13-3 SPI SOC Bus Connections

EMUX Signal	Description	IO Pin
EMUXC	EMUX Clock	PA2
EMUXD	EMUX Data	PA1

13.4 Analog Interrupts

The Analog sub-system has two interrupts that it can generate for different conditions. The table below shows the two different interrupts, the interrupt conditions and the IO pin that the interrupts are connected to.

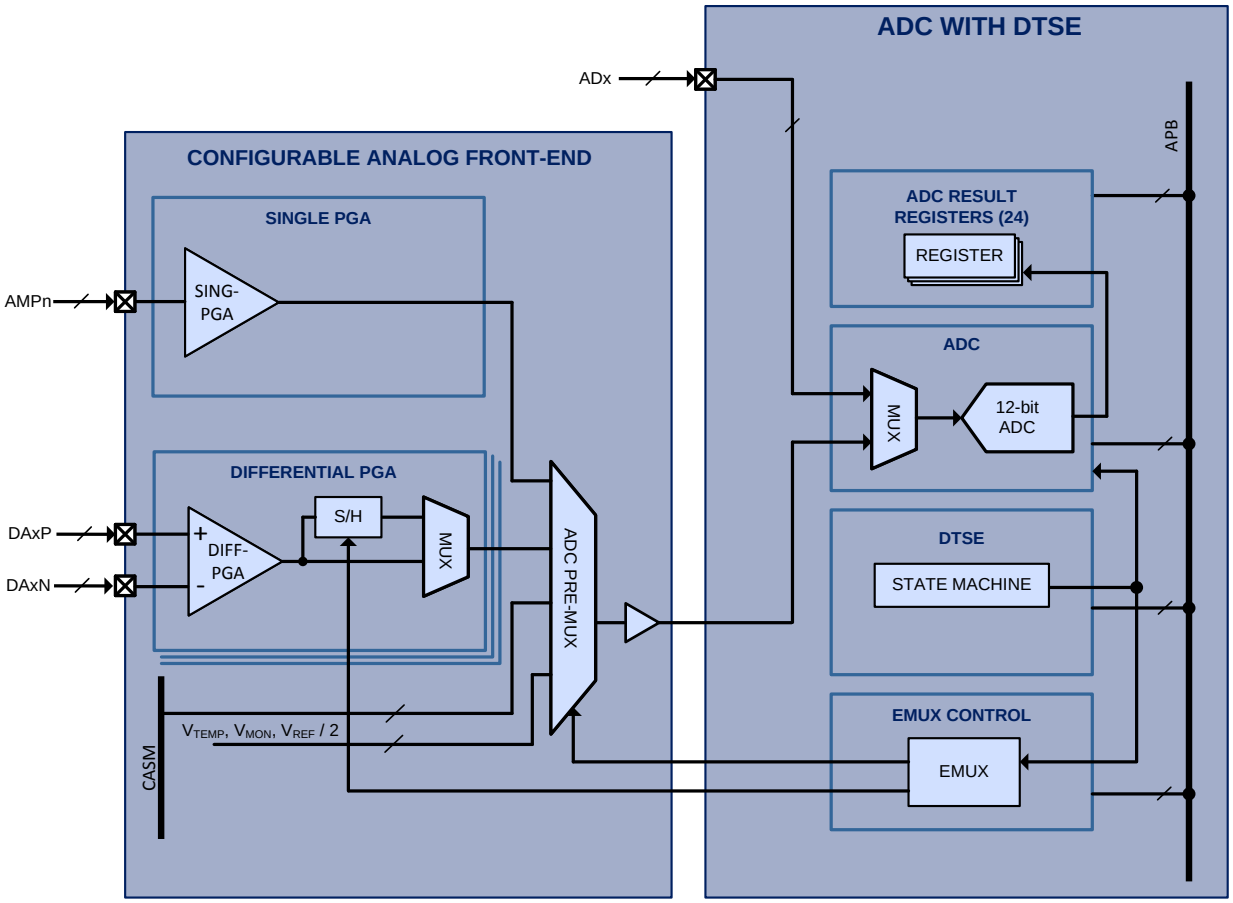
Table 13-4 Analog Interrupts

Analog IRQ	Interrupt Conditions	IO Pin
IRQ1	HPCOMP/LPCOMP Comparator Protection for Over-current and Over-Voltage events	PA7
IRQ2	BEMF and Special Mode Comparator, including phase to phase comparator, AIO6/AIO7/AIO8/AIO9 interrupt	PA0

14 ADC/DTSE

14.1 ADC Block Diagram

Figure 14-1 ADC with DTSE



14.2 Functional Description

14.2.1 ADC

The analog-to-digital converter (ADC) is a 12-bit successive approximation register (SAR) ADC with 400ns conversion time and up to 2.5 MSPS capability. The integrated analog multiplexer allows selection from up to 8 direct ADx inputs, and from up to 10 analog inputs signals in the Configurable Analog Front End (CAFE), including up to 3 differential input pairs as well as temperature and V_{REF} / 2.

The ADC contains a power down mode, and the user may configure the ADC to interrupt the MCU for the completion of a conversion when in manual mode. The ADC may be configured for either repeating or non-repeating conversions or conversion sequences.

14.2.2 Dynamic Triggering and Sample Engine

The Dynamic Triggering and Sample Engine (DTSE) is a highly-configurable automatic sequencer that allows the user to configure automatic sampling of their application-specific analog signals without any interaction from the micro-controller core. The DTSE also contains a pseudo-DMA engine that copies each of up to 24 conversion results to dedicated memory space and can interrupt the MCU when complete.

The DTSE has up to 32 input triggers, from PWM Timers A, B, C and D for either the rising, falling or rising and falling PWM edges. The user may also force any trigger sequence by writing a register via firmware. The user can configure the DTSE to chain from 1 to 24 conversions to any PWM trigger.

The DTSE has a flexible interrupt structure that allows up to 24 interrupts to be configured at the completion of any individual conversion. The user may configure one of four different IRQ signals when generating an interrupt during sequence conversions. The IRQ may be generated at the end of a conversion sequence, or at the end of a series of conversions. The user may select one of four IRQs for conversions, and each may be assigned a different interrupt priority.

Each of the 24 conversions has dedicated results registers, so that the pseudo-DMA engine has dedicated storage for each of the conversion results.

14.2.3 EMUX Control

A dedicated low latency interface controllable by the DTSE or register control allows changing the ADC pre-multiplexer and asserting/de-asserting the S/H circuit in the Configurable Analog Front-End (CAFE), allowing back to back conversions of multiple analog inputs without microcontroller interaction.

For more information on the ADC and DTSE, see the PAC55XX Family User Guide.

14.3 Electrical Characteristics

Table 14-1 ADC and DTSE Electrical Characteristics

(V_P = 12V, V_{SYS} = 5V and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
ADC						
f_{ADCCLK}	ADC conversion clock input				40	MHz
$f_{ADCCONV}$	ADC conversion time				16	ADCCLK
		f_{ADCCLK} = 40MHz; PCx, PDx, PEx, PFx, PGx pins			400	ns
		f_{ADCCLK} = 40MHz; AIO[9:0] pins			800	ns
t_{ADCSH}	ADC sample and hold time	f_{ADCCLK} = 40MHz			100	ns
					4	ADCCLK
C_{ADCIC}	ADC input capacitance	ADC MUX input		1		pF
	ADC resolution			12		bits
	ADC effective resolution		10.5			bits
	ADC differential non-linearity (DNL)	F_{ADCCLK} = 25MHz		±0.5		LSB
		F_{ADCCLK} = 40MHz		±0.75		LSB
	ADC integral non-linearity (INL)	F_{ADCCLK} = 25MHz		±0.5		LSB
		F_{ADCCLK} = 40MHz		±0.75		LSB
	ADC offset error			0.6		%FS
	ADC gain error			0.12		%FS
REFERENCE VOLTAGE						
V_{REFADC}	ADC reference input voltage	VREF = 2.5V		2.5		V
EMUX CLOCK SPEED						
$f_{EMUXCLK}$	EMUX gine clock input				50	MHz

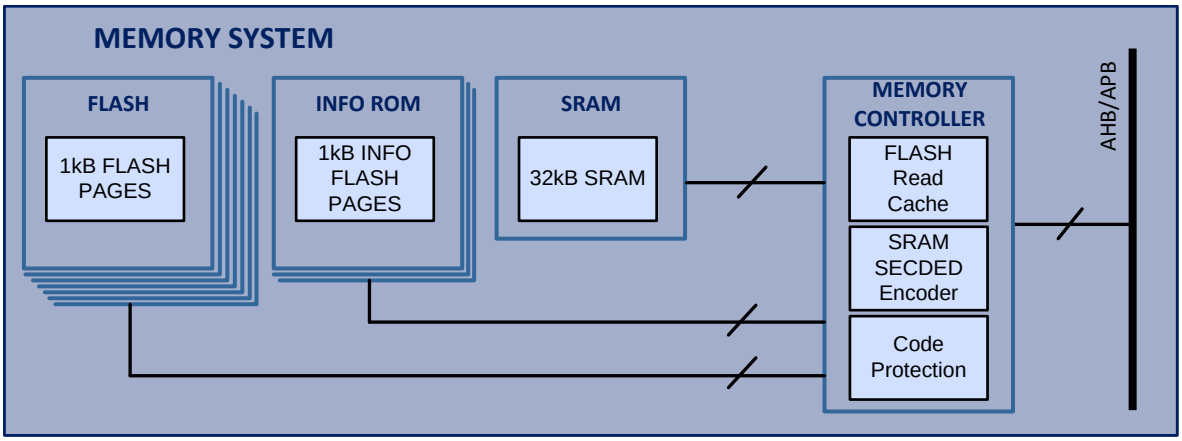
15 MEMORY SYSTEM

15.1 Features

- 128kB Embedded FLASH
  - 30,000 program/erase cycles
  - 10 years data retention
  - FLASH look-ahead buffer for optimizing access
- 1kB INFO-1 Embedded FLASH
- 1kB INFO-2 Embedded FLASH
  - Device ID, Unique ID, trim and manufacturing data
- 1kB INFO-3 Embedded FLASH
  - User data storage, configuration or parameter storage
  - Data or code
- 32kB SRAM
  - 150MHz access for code or data
  - SECDED for read/write operations
- User-configurable code protection

15.2 Memory System Block Diagram

Figure 15-1 Memory System



15.3 Functional Description

The PAC55XX has multiple banks of embedded FLASH memory, SRAM memory as well as peripheral control registers that are program-accessible in a flat memory map.

15.4 Program FLASH

The PAC55XX Memory Controller provides access to 128 1kB pages of main program FLASH for a total of 128kB of FLASH through the system AHB bus. Each page may be individually erased or written while the MCU is executing instructions from SRAM.

The PAC55XX Memory Controller provides a FLASH read buffer that optimizes access from the MCU to the FLASH memory. This look ahead buffer monitors the program execution and fetches instructions from FLASH before they are needed to optimize access to this memory.

15.5 INFO FLASH

The PAC55XX Memory Controller provides access to the INFO-1, INFO-2 and INFO-3 FLASH memories, which are each a single 1kB page for a total of 3kB of memory.

INFO-1 and INFO-2 are read-only memories that contains device-specific information such as the device ID, a unique ID, trimming and calibration data that may be used by programs executing on the PAC55XX.

INFO-3 is available to the user for data or program storage.

15.6 SRAM

The PAC55XX Memory Controller provides access to the 32kB SRAM for non-persistent data storage. The SRAM memory supports word (4B), half-word (2B) and byte addresses.

The PAC55XX Memory Controller can read or write data from RAM up to 150MHz. This can be a benefit for time-critical applications. This memory can also be used for program execution when modifying the contents of FLASH, INFO-1 or INFO-2 FLASH.

The PAC55XX Memory Controller also has an SECDED encoder, capable of detecting and correcting single-bit errors, and detecting double-bit errors. The user may read the status of the encoder, to see if a single-bit error has occurred. The user may also enable an interrupt upon detection of single-bit errors. Dual-bit errors can be configured to generate an interrupt in the PAC55XX.[6]

For more information on the PAC55XX Memory Controller, see the PAC55XX Family User Guide.

15.7 Code Protection

The PAC55XX allows user configurable code protection, to secure code from being read from the device.

There are four levels of code protection available as shown in the table below.

[6] Note that when writing half-word or single bytes to SRAM, the memory controller must perform a read-modify write to memory to perform the SECDED calculation. These operations will take more than one clock cycle to perform for this reason.

Table 15-1 Code Protection Level Description

LEVEL	NAME	FEATURES
0	UNLOCKED	• No restrictions
1	RW PROTECTION	• SWD/JTAG enabled • Programmable protection of up to 128 regions of FLASH • User-specified Read or Write protection per region
2	SWD DISABLED	• SWD/JTAG disabled • Programmable protection of up to 128 regions of FLASH • User-specified Read or Write protection per region
3	SWD/JTAG PERMANENTLY DISABLED	• SWD/JTAG disabled • Programmable protection of up to 128 regions of FLASH • User-specified Read or Write protection per region • No recovery

15.8 Electrical Characteristics

Table 15-2 Memory System Electrical Characteristics

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Embedded FLASH						
$t_{READ;FLASH}$	FLASH read time		40			ns
$t_{WRITE;FLASH}$	FLASH write time		30			µs
$t_{PERASE;FLASH}$	FLASH page erase time			2		ms
$t_{MERASE;FLASH}$	FLASH full erase time			10		ms
$N_{PERASE;FLASH}$	FLASH program/erase cycles		30k			cycles
$t_{DR;FLASH}$	FLASH data retention		10			years
SRAM						
$t_{ACC;SRAM}$	SRAM access time	HCLK = 150MHz; Word (32-bits), aligned	6.67			ns
		HCLK = 150MHz; Half-word (16-bits), byte (8-bits), aligned	6.67			ns

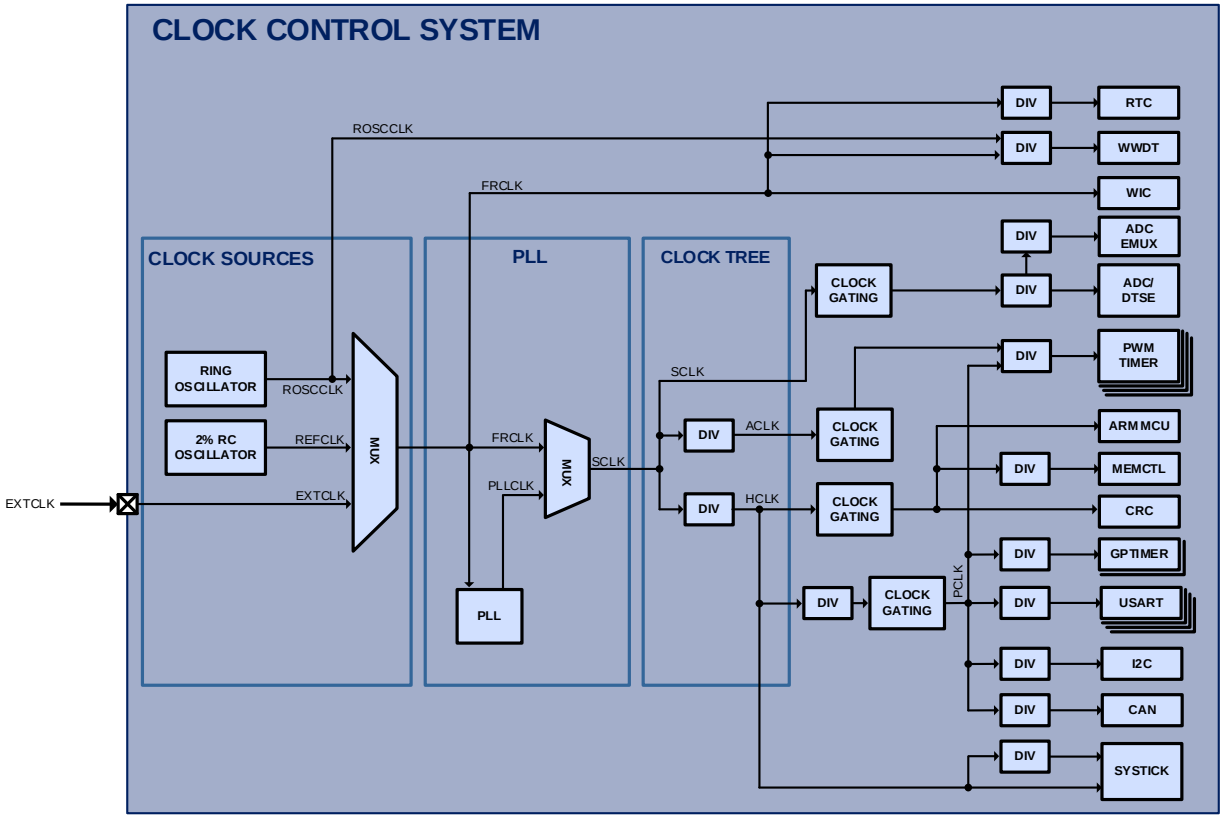
16 SYSTEM AND CLOCK CONTROL

16.1 Features

- 20MHz Ring Oscillator
- High accuracy 1.25% trimmed 4MHz RC oscillator
- External Clock Input for External Clocks up to 20MHz
- PLL with 1MHz to 50MHz input, 62.5MHz to 300MHz output
- Clock dividers for all system clocks
- Clock gating for power conservation during low-power operation

16.2 Block Diagram

Figure 16-1 Clock Control System



16.3 Clock Sources

16.3.1 Ring Oscillator

The Ring Oscillator (ROSC) is an integrated 20MHz clock oscillator that is the default system clock and is available by default when the PAC55XX comes out of reset. The output of the ROSC is the ***ROSCCLK*** clock. The ***ROSCLK*** may be selected as the ***FRCLK*** clock and may supply the WWDT, for applications that need an independent clock source or need to continue to be clocked when the system is in a low-power mode.

The ROSC may be disabled by the user by a configuration register.

16.3.2 Reference Clock

The Reference Clock (***REFCLK***) is an integrated 1.25% trimmed 4MHz RC clock. This clock is suitable for many applications. This clock may be selected as the ***FRCLK*** and can be used as the input to the PLL and is used to derive the clock for the MMPM.

16.3.3 External Clock Input

The External Clock Input (EXTCLK) is a clock input available through the digital peripheral MUX, and allows the drive the clock system by a 50% duty cycle clock of up to 20MHz. This clock may be selected as FRCLK and can be used as the input the PLL (as long as the accuracy is better than +/- 2%).

16.4 PLL

The PAC55XX contains a Phase Lock Loop (PLL) that can generate very high clock frequencies up to 300MHz for the peripherals and timers in the device. The input to the PLL is the ***FRCLK*** and must be from the ***EXTCLK*** or ***REFCLK*** clock sources

The input to the PLL must be between 1MHz – 50MHz and the output can be configured to be from 62.5MHz to 300MHz. The user can configure the PLL to generate the desired clock output based on a set of configuration registers in the CCS. The output of the PLL is the ***PLLCLK*** clock. The user may configure a MUX to generate the SCLK clock from ***PLLCLK*** or from ***FRCLK***.

In addition to configuring the PLL output frequency, the PLL may be enabled, disabled and bypassed through a set of configuration registers in the CCS.

16.5 Clock Tree

The following are the system clocks available in the clock tree. See the section below to see which clocks are available for each of the digital peripherals in the system.

16.5.1 FRCLK

The free-running clock (***FRCLK***) is generated from one of the four clock sources (***ROSCCLK***, ***EXTCLK*** or ***REFCLK***). This clock may be used by the WWDT and the RTC, for configurations that turn off all other system clocks during low power operation.

The ***FRCLK*** or ***PLLCLK*** is selected via a MUX and the output becomes ***SCLK***.

16.5.2 SCLK

The System Clock (***SCLK***) generates two system clocks: ***ACLK*** and ***HCLK***. Each of these system clocks has their own 3b clock divider and is described below.

16.5.3 PCLK

The Peripheral Clock (***PCLK***) is used by most of the digital peripherals in the PAC55XX. This clock has a 3b clock divider and also has clock gating support, which allows this clock output to be disabled before the system is put into the Arm® Cortex®-M4's deep sleep mode to conserve energy.

As shown above, most of the peripherals that use ***PCLK*** also have their own clock dividers so that this clock can be further divided down to meet the application's needs.

16.5.4 ACLK

The Auxiliary Clock (***ACLK***) may be optionally used by the PWM timer block in the PAC55XX in order to generate a very fast clock for PWM output to generate the best possible accuracy and edge generation.

This clock has a 3b clock divider and also has clock gating support, which disables this clock output when the system is put into the Arm® Cortex®-M4's deep sleep mode to conserve energy.

As shown above, the ***ACLK*** is an optional input for just the PWM timer block in the PAC55XX.

16.5.5 HCLK

The AHB Clock (***HCLK***) is used by the Arm® Cortex®-M4 MCU and Memory Controller peripheral. This clock has a 3b divider and also has clock gating support, which allows this clock output to be disabled before the system is put into the Arm® Cortex®-M4's deep sleep mode to conserve energy.

HCLK supplies PCLK with its clock source.

16.6 Electrical Characteristics

Table 16-1 CCS Electrical Characteristics

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Clock Tree (FRCLK, FCLK, PCLK, ACLK, HCLK)						
f_{FRCLK}	Free-running clock frequency				25	MHz
f_{SCLK}	System clock frequency				300	MHz
f_{PCLK}	Peripheral clock frequency	After divider			150	MHz
f_{ACLK}	Auxiliary clock frequency	After divider			300	MHz
f_{HCLK}	High-speed clock frequency	After divider			150	MHz
Internal Oscillators						
$f_{ROSCCLK}$	Ring oscillator frequency			20		MHz
$f_{TRIM;REFCLK}$	Trimmed RC oscillator frequency	T_A = 25°C	3.96	4	4.05	MHz
		T_A = -40°C to 125°C	3.92	4	4.08	MHz
$f_{JITTER;REFCLK}$	Trimmed RC oscillator clock jitter	T_A = -40°C to 85°C		0.5		%
External Clock Input (EXTCLK)						
f_{EXTCLK}	External Clock Input Frequency				20	MHz
	External Clock Input Duty Cycle		40		60	%
$V_{IH;EXTCLK}$	External Clock Input high-level input voltage		2.1			V
$V_{IL;EXTCLK}$	External Clock Input low-level input voltage				0.825	V
PLL						
$f_{IN;PLL}$	PLL input frequency range		1		50	MHz
$f_{OUT;PLL}$	PLL output frequency range		62.5		300	MHz
$t_{SETTLE;PLL}$	PLL setting time	T_A = 25°C, PLL settled			15	µs
		T_A = 25°C, **PLLLOCK** = 1		200	500	µs
$t_{JITTER;PLL}$	PLL period jitter	RMS		25		ps
		Peak to peak			100	ps
	PLL duty cycle		40	50	60	%

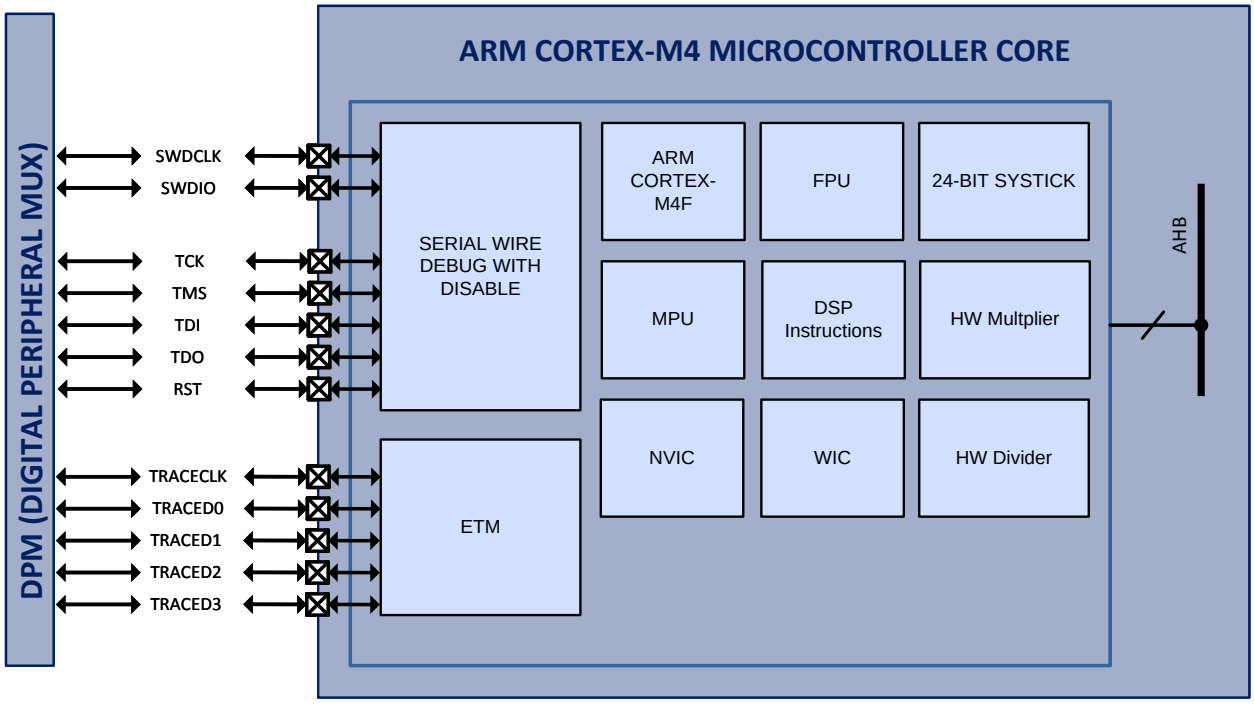
17 ARM® CORTEX®-M4F MCU CORE

17.1 Features

- Arm® Cortex®-M4F core
- SWD or JTAG Debug
- SWD/JTAG code security
- Embedded Trace Module (ETM) for instruction tracing
- Memory Protection Unit (MPU)
- Nested Vectored Interrupt Controller (NVIC) with 29 user interrupts and 8 levels of priority
- Floating Point Unit (FPU)
- Wakeup Interrupt Controller (WIC)
- 24-bit SysTick Count-down Timer
- Hardware Multiply and Divide Instructions

17.2 Block Diagram

Figure 17-1 Arm® Cortex®-M4F Microcontroller Core



17.3 Functional Description

The Arm® Cortex®-M4F microcontroller core is configured for little endian operation and includes hardware support for multiplication and division, DSP instructions as well as an IEEE754 single-precision Floating Point Unit (FPU).

The MCU also contains an 8-region Memory Protection Unit (MPU), as well as a Nested Vector Interrupt Controller (NVIC) that supports 29 user interrupts with 8 levels of priority. There is a 24-bit SysTick count-down timer.

The Arm® Cortex®-M4F supports sleep and deep sleep modes for low power operation. In sleep mode, the Arm® Cortex®-M4F is disabled. In deep sleep mode, the MCU as well as many peripherals are disabled. The Wakeup Interrupt Controller (WIC) can wake up the MCU when in deep sleep mode by using any GPIO interrupt, the Real-Time Clock (RTC) or Windowed Watchdog Timer (WWDT). The PAC55XX also supports clock gating to reduce power during deep sleep operation.

The debugger supports 4 breakpoint and 2 watch-point unit comparators using the SWD or JTAG protocols. The debug serial interfaces may be disabled to prevent memory access to the firmware during customer production.

For more information on the detailed operation of the Microcontroller Core in the PAC55XX, see the PAC55XX Family User Guide.

17.4 Application Typical Current Consumption

The MCU clock configuration and peripheral configuration have a large influence on the amount of load that the power supplies in the PAC55XX will have.

The table below shows a number of popular configurations and what the typical power consumption will be on the VSYS and VCORE power supplies in the PAC55XX.

Table 17-1 PAC55XX Application Typical Current Consumption

CLOCK CONFIGURATION	MCU PERIPHERALS	MCU STATE	I_{VSYS}	I_{VCORE}	I_{VCC33}
CLKREF = 4MHz PLL Disabled ACLK=HCLK=PCLK=SCLK=MCLK = 16MHz ROSCCLK Enabled FRCLK MUX = ROSCCLK	All peripherals disabled	Halted	9.5mA	2.3mA	n/a
CLKREF = 4MHz PLLCLK = 30MHz ACLK=HCLK=PCLK=SCLK= 16MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF	All peripherals disabled	Halted	10.5mA	3.5mA	n/a
CLKREF = 4MHz PLLCLK = 150MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF	All peripherals disabled	Halted	20mA	13.5mA	n/a
CLKREF = 4MHz PLLCLK = 300MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF	All peripherals disabled	Halted	22mA	15mA	n/a
CLKREF = 4MHz PLLCLK = 300MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF ADCCLK = 40MHz	ADC enabled (repeated conversions)	Halted	36mA	16mA	13.5mA
CLKREF = 4MHz PLLCLK = 300MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF	All peripherals disabled	CPU Executes instructions from FLASH	8.5mA	2.2mA	n/a
CLKREF = 4MHz PLLCLK = 300MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF	Timer A enabled; TAPWM[7:0] enabled; Fs = 100kHz; 50% duty cycle	Halted	22mA	15mA	n/a

17.5 Electrical Characteristics

Table 17-2 MCU and Clock Control System Electrical Characteristics

(T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{HCLK}	Microcontroller Clock				150	MHz
$I_{Q;VCORE}$	V_{CORE} quiescent current	Arm® Cortex®-M4F Sleep/Deep Sleep Modes			2	mA
		PAC5523 Hibernate Mode			0	mA
$I_{Q;VSYS}$	V_{SYS} quiescent current	Arm® Cortex®-M4F Sleep/Deep Sleep Modes			8	mA
		PAC5523 Hibernate Mode			15	µA
$I_{Q;VCCIO}$	VCCIO quiescent current	Arm® Cortex®-M4F Sleep/Deep Sleep Modes			0.15	mA
		PAC5523 Hibernate Mode			0	mA
$I_{Q;VCC33}$	VCC33 quiescent current	Arm® Cortex®-M4F Sleep/Deep Sleep Modes			0.4	mA
		PAC5523 Hibernate Mode			0	mA

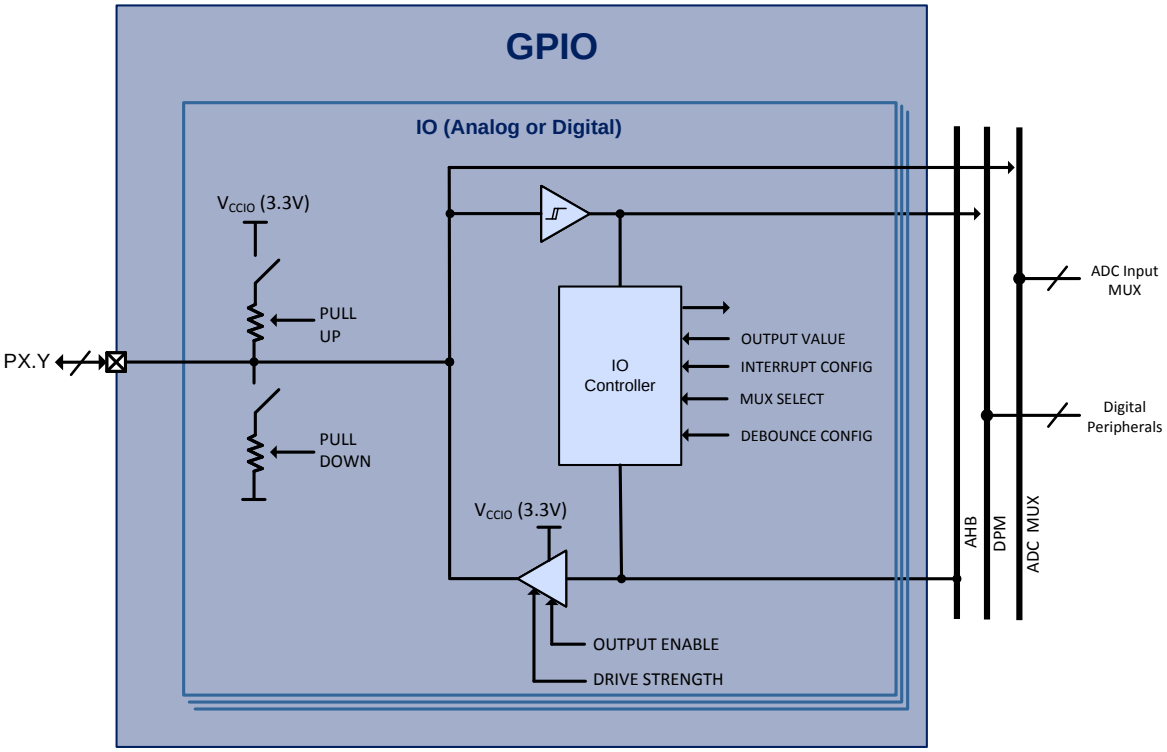
18 IO CONTROLLER

18.1 Features

- 3.3V Input/Output, 4.6V input tolerant
- Push-Pull Output, Open-Drain Output or High-Impedance Input for each IO
- Configurable Pull-up and Pull-down for each IO (60k)
- Configurable Drive Strength for each IO (up to 24mA)
- Analog Input for some IOs
- Edge-sensitive or level-sensitive interrupts
- Rising edge, falling edge or both edge interrupts
- Peripheral MUX allowing up to 8 peripheral selections for each IO
- Configurable De-bouncing Circuit for each IO

18.2 Block Diagram

Figure 18-1 IO Controller Block Diagram



18.3 Functional Description

The PAC55XX IO cells can be used for digital input/output and analog input for the ADC. All IOs are supplied by the V_{CCIO} (3.3V) power supply.

Each IO can be configured for digital push-pull output, open-drain output or high-impedance input. Each IO also has a configurable 60k weak pull-up or weak pull-down that can be enabled.

NOTE: Configuring both pull-up and pull-down at the same time may cause device damage and should be avoided.

Each IO has a configurable de-bouncing filter that can be enabled or disabled, to help filter out noise.

All IO have interrupt capability. Each pin can be configured for either level or edge sensitive interrupts, and can select between rising edge, falling edge and both edges for interrupts. Each pin has a separate interrupt enable and interrupt flag.

Some of the IO on the PAC5523 can be configured as an analog input to the ADC.

18.4 GPIO Current Injection

Under normal operation, there should not be current injected into the GPIOs on the device due to the GPIO voltage below ground or above the GPIO supply (VCCIO). Current will be injected into the GPIO when the GPIO pin voltage is less than -0.3V or when greater than GPIO supply + 0.3V.

In order provide a robust solution when this situation occurs, the PAC52XX family of products allows a small amount of injected current into the GPIO pins, to avoid excessive leakage or device damage.

For information on the GPIO current injection thresholds, see the absolute maximum parameters for this device.

Sustained operation with the GPIO pin voltage greater than the GPIO supply or when the GPIO pin voltage is less than -0.3V may result in reduced lifetime of the device. GPIO current injection should only be a temporary condition.

18.5 Peripheral MUX

The following table shows the available pin MUX options for this device. Note that if the pin is configured for analog input, the peripheral MUX is bypassed.

Table 18-1 PAC5556 Peripheral Pin MUX

PIN	Peripheral MUX Selection								ADC CH
	S0	S1	S2	S3	S4	S5	S6	S7	
PF4/ADC4	GPIOF4	TCPWM4	TDPWM4		TCIDX	USDSCLK	TRACED3	EMUXC	ADC4
PF3	GPIOF3	TCPWM3	TDPWM3	TDO	FRCLK	USBMISO	TRACECLK	TRACED2	
PF2	GPIOF2	TCPWM2	TDPWM2	TDI	TBPHB	USBMOSI	TRACED0	TRACED1	
PF1	GPIOF1	TCPWM1	TDPWM1	TMS/SWDIO	TBPHA	USBSS	TRACED1	TRACED0	
PF0	GPIOF0	TCPWM0	TDPWM0	TCK/SWDCL	TBIDX	USBSCLK	TRACED2	TRACECLK	
PE0	GPIOE0	TCPWM4	TDPWM0	TAIDX	TBIDX	USCCLK	I2CSCL	EMUXC	
PE1	GPIOE1	TCPWM5	TDPWM1	TAPHA	TBPHA	USCSS	I2CSDA	EMUXD	
PE2	GPIOE2	TCPWM6	TDPWM2	TAPHB	TBPHB	USCMOSI	CANRXD	EXTCLK	
PE3	GPIOE3	TCPWM7	TDPWM3	FRCLK		USCMISO	CANTXD		
PE4	GPIOE4	TCPWM4	TDPWM4	TDQEPIDX	USBSCLK	USDMOSI	I2CSCL		
PE5	GPIOE5	TCPWM5	TDPWM5	TDQEPPHA	USBSS	USDMISO	I2CSDA		
PE6	GPIOE6	TCPWM6	TDPWM6	TDQEPPHB	USBMOSI	USDSCLK	CANRXD		
PE7	GPIOE7	TCPWM7	TDPWM7		USBMISO	USDSS	CANTXD		
PF7/ADC7	GPIOF7	TCPWM7	TDPWM7			USDMISO	CANTXD	I2CSDA	ADC7
PF6/ADC6	GPIOF6	TCPWM6	TDPWM6		TCPHB	USDMOSI	CANRXD	I2CSCL	ADC6
PF5/ADC5	GPIOF5	TCPWM5	TDPWM5		TCPHA	USDSS		EMUXD	ADC5

18.6 Electrical Characteristics

Table 18-2 IO Controller Electrical Characteristics

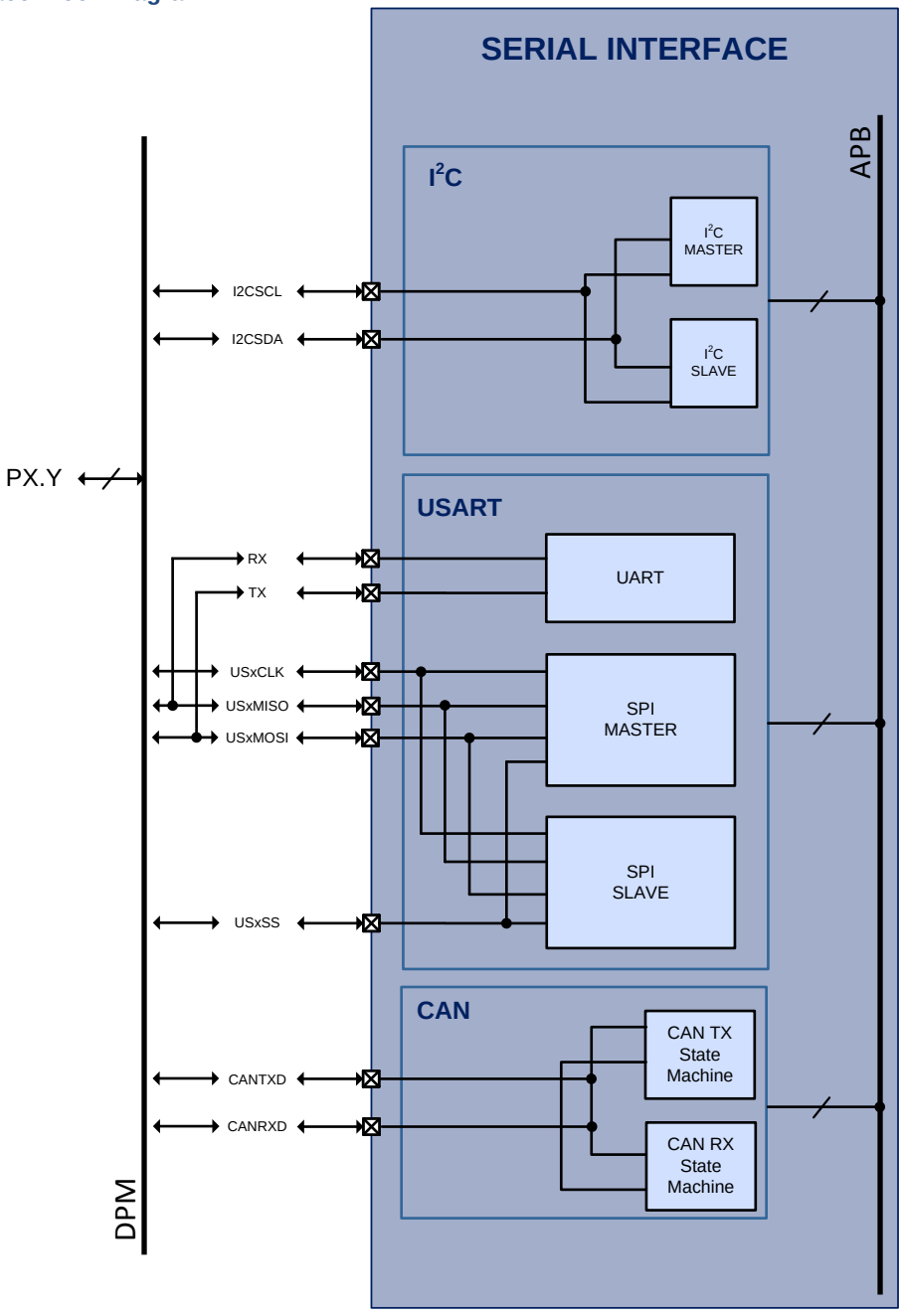
(V_{CCIO} = 3.3V, V_{SYS} = 5V, V_{CORE} = 1.2V, and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage			2.1			V
V_{IL}	Low-level input voltage					0.825	V
I_{OL}	Low-level output sink current (Limited by I_{VSYS} and I_{VCCIO})	V_{OL} = 0.4V	DS = 6mA	6			mA
			DS = 8mA	8			
			DS = 11mA	11			
			DS = 14mA	14			
			DS = 17mA	17			
			DS = 20mA	20			
			DS = 22mA	22			
			DS = 25mA	25			
I_{OH}	High-level output source current (Limited by I_{VSYS} and I_{VCCIO})	V_{OH} = 2.4V	DS = 6mA			-6	mA
			DS = 8mA			-8	
			DS = 11mA			-11	
			DS = 14mA			-14	
			DS = 17mA			-17	
			DS = 20mA			-20	
			DS = 22mA			-22	
			DS = 25mA			-25	
I_{IL}	Input leakage current			-2		0.95	µA
R_{PU}	Weak pull-up resistance	When pull-up enabled		45	60	100	kΩ
R_{PD}	Weak pull-down resistance	When pull-down enabled		45	60	115	kΩ
$I_{INJ;GPIO}$	GPIO pin current injection	V_{GPIO} < -0.3V or V_{GPIO} > VCCIO + 0.3V		-15		15	mA
$\Sigma I_{INJ;GPIO}$	Sum of all GPIO pin current injection	V_{GPIO} < -0.3V or V_{GPIO} > VCCIO + 0.3V		-40		40	mA

19 SERIAL INTERFACE

19.1 Block Diagram

Figure 19-1 Serial Interface Block Diagram



19.2 Functional Description

The PAC55XX has three types of serial interfaces: I²C, USART and CAN. The PAC55XX has one I²C controller, one CAN controller and up to 3 USARTs.

19.3 I²C Controller

The PAC55XX contains one I²C controller. This is a configurable APB peripheral and the clock input is PCLK. This peripheral has an input clock divider that can be used to generate various master clock frequencies. The I²C controller can support various modes of operation:

- I²C master operation
  - Standard (100kHz), full-speed (400kHz), fast (1MHz) or high-speed modes (3.4MHz)
  - Single and multi-master
  - Synchronization (multi-master)
  - Arbitration (multi-master)
  - 7-bit or 10-bit slave addressing
- I²C slave operation
  - Standard (100kHz), full-speed (400kHz), fast (1MHz) or high-speed modes (3.4MHz)
  - Clock stretching
  - 7-bit or 10-bit slave addressing

The I²C peripheral may operate either by polling, or can be configured to be interrupt driven for both receive and transmit operations.

19.4 USART

The PAC55XX contains up to 3 Universal Synchronous Receive Transmit (USART) peripherals. Each USART is a configurable APB bus client and input clock is PCLK. These peripherals have a configurable clock divider that can be used to produce various frequencies for the UART or SPI master peripheral.

The number of these peripherals depends on the peripheral MUX configuration. See the IO Controller section on information on how to configure the peripheral MUX with the USART peripheral.

The USART peripheral supports two main modes: SPI mode and UART mode.

19.4.1 USART SPI Mode

- Master or slave mode operation
- 8-bit, 16-bit or 32-bit word transfers
- Configurable clock polarity (active high or active low)
- Configurable data phase (setup/sample or sample/setup)
- Interrupts and status flags for RX and TX operations
- Support for up to 25MHz SPI clock

19.4.2 USART UART Mode

- 8-bit data
- Programmable data bit rate
- Maximum baud rate of 1Mbaud
- RX and TX FIFOs
- Configurable stop bits (1 or 2)
- Configurable parity: even, odd, none
  - Mark/space support for 9-bit addressing protocols
- Interrupt and status flags for RX and TX operations

19.5 CAN

The PAC55XX contains one Controller Area Network (CAN) peripheral. The CAN peripheral is a configurable APB bus client and input clock is PCLK. This peripheral has a configurable clock divider that can be used to produce various frequencies for the CAN peripheral.

- CAN 2.0B support
- 1Mb/s data rate
- 64-byte receive FIFO
- 16-byte transmit buffer
- Standard and extended frame support
- Arbitration
- Overload frame generated on FIFO overflow
- Normal and Listen Only modes supported
- Interrupt and status flags for RX and TX operations

19.6 Dynamic Characteristics

Table 19-1 Serial Interface Dynamic Characteristics

(V_{CCIO} = 3.3V, V_{SYS} = 5V, V_{CORE} = 1.2V, and T_A = -40°C to 125°C unless otherwise specified.)

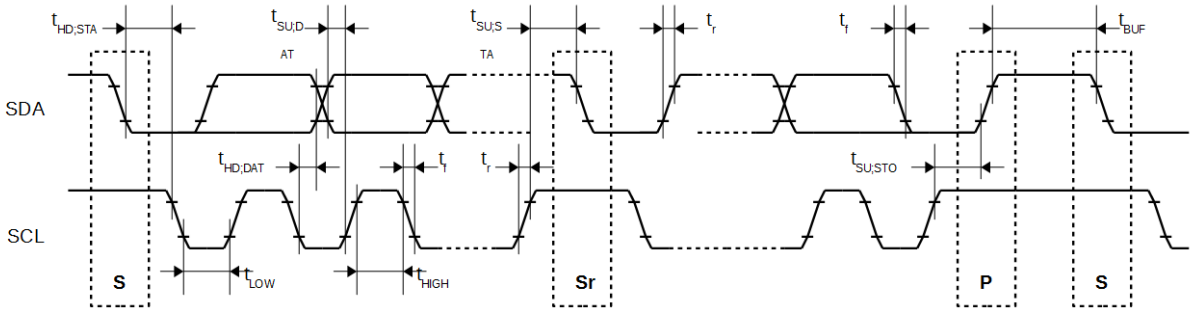
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I²C						
f_{I2CCLK}	I²C input clock frequency	Standard mode (100kHz)	2.8			MHz
		Full-speed mode (400kHz)	2.8			MHz
		Fast mode (1MHz)	6.14			MHz
		High-speed mode (3.4MHz)	20.88			MHz
USART (UART mode)						
$f_{UARTCLK}$	USART input clock frequency				f_{PCLK}/16	MHz
$f_{UARTBAUD}$	UART baud rate	$f_{USARTCLK}$ = 7.1825MHz			1	Mbps
USART (SPI mode)						
f_{SPICLK}	USART input clock frequency	Master mode			50	MHz
		Slave mode			50	MHz
$f_{USARTSPICLK}$	USART SPI clock frequency	Master mode			25	MHz
		Slave mode			25	MHz
CAN						
f_{CANCLK}	CAN input clock frequency				50	MHz
f_{CANTX}	CAN transmit clock frequency				1	Mbps
f_{CANRX}	CAN receive clock frequency				1	Mbps

Table 19-2 I²C Dynamic Characteristics

(V_{CCIO} = 3.3V, V_{SYS} = 5V, V_{CORE} = 1.2V, and T_A = -40°C to 125°C unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode	0		100	kHz
		Full-speed mode	0		400	kHz
		Fast mode	0		1	MHz
t_{LOW}	SCL clock low	Standard mode	4.7			µs
		Full-speed mode	1.3			µs
		Fast mode	0.5			µs
t_{HIGH}	SCL clock high	Standard mode	4.0			µs
		Full-speed mode	0.6			µs
		Fast mode	0.26			µs
$t_{HD;STA}$	Hold time for a repeated START condition	Standard mode	4.0			µs
		Full-speed mode	0.6			µs
		Fast mode	0.26			µs
$t_{SU;STA}$	Set-up time for a repeated START condition	Standard mode	4.7			µs
		Full-speed mode	0.6			µs
		Fast mode	0.26			µs
$t_{HD;DAT}$	Data hold time	Standard mode	0		3.45	µs
		Full-speed mode	0		0.9	µs
		Fast mode	0			µs
$t_{SU;DAT}$	Data setup time	Standard mode	250			ns
		Full-speed mode	100			ns
		Fast mode	50			ns
$t_{SU;STO}$	Set-up time for STOP condition	Standard mode	4.0			µs
		Full-speed mode	0.6			µs
		Fast mode	0.26			µs
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
		Full-speed mode	1.3			µs
		Fast mode	0.5			µs
t_r	Rise time for SDA and SCL	Standard mode			1000	ns
		Full-speed mode	20		300	ns
		Fast mode			120	ns
t_f	Fall time for SDA and SCL	Standard mode			300	ns
		Full-speed mode			300	ns
		Fast mode			120	ns
C_b	Capacitive load for each bus line	Standard mode, full-speed mode			400	pF
		Fast mode			550	pF

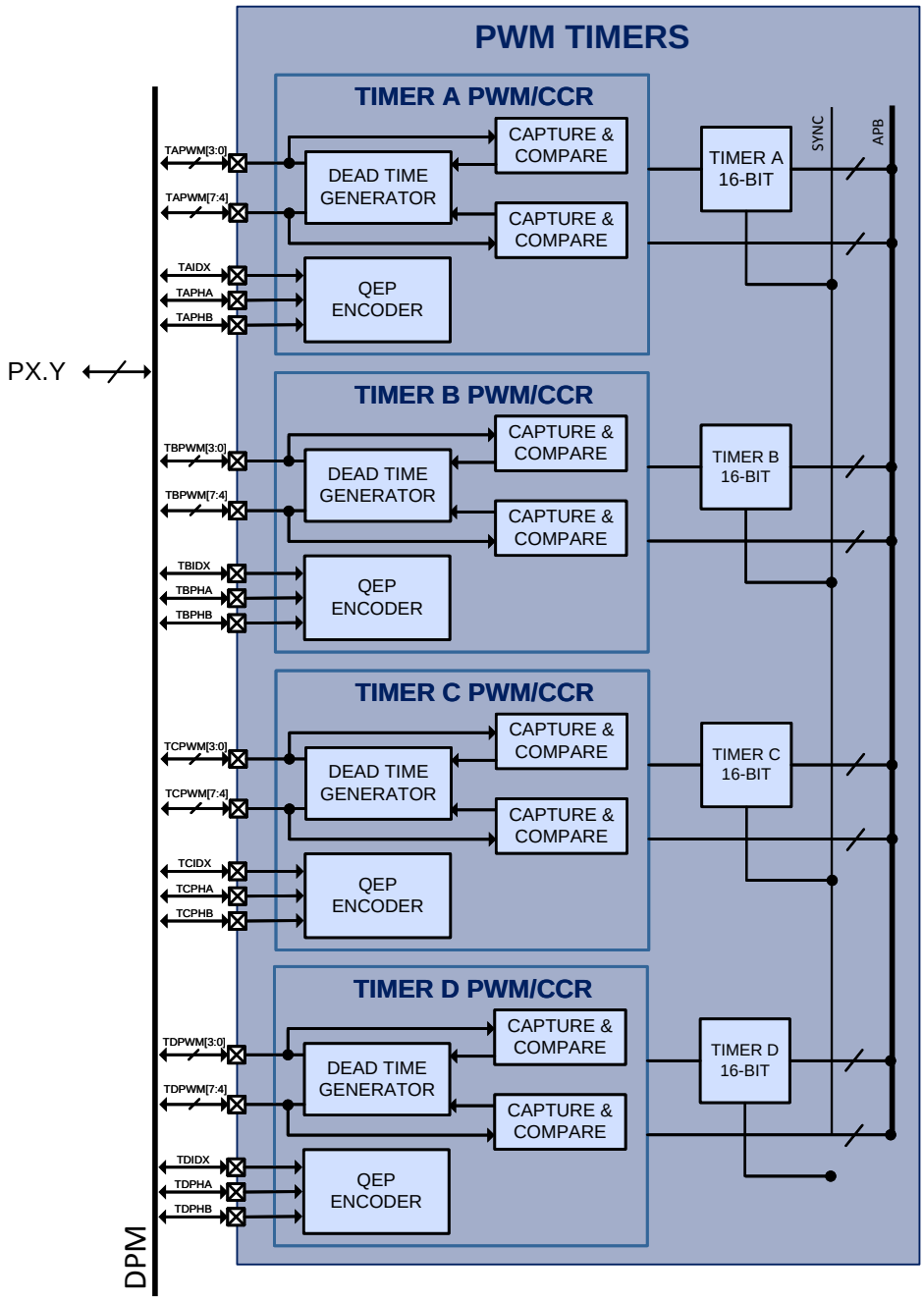
Figure 19-2 I²C Timing Diagram



20 PWM TIMERS

20.1 Block Diagram

Figure 20-1 PWM Timers Block Diagram



20.2 Timer Features

- Configurable input clock source: PCLK or ACLK
- Up to 300MHz input clock
- 3-bit Input clock divider
- Timer counting modes
  - up, up/down and asymmetric
- Timer latch modes
  - Latch when counter = 0
  - Latch when counter = period
  - Latch when CCR value written
  - Latch all CCR values at same time
- Base timer interrupts
- Single shot or auto-reload

20.2.1 CCR/PWM Timer

- PWM output or capture input
- CCR interrupt enable
- CCR interrupt skips
- SW force CCR interrupt
- CCR interrupt type
  - Rising, falling or both
- CCR compare latch modes
  - Latch when counter = 0
  - Latch when counter = period
  - Latch immediate
- CCR capture latch modes
  - Latch on rising edge
  - Latch on falling edge
  - Latch on both rising and falling edges
- Invert CCR output
- CCR phase delay for phase shifted drive topologies
- ADC trigger outputs
  - PWM rising edge or falling edge

20.2.2 Dead-time Generators (DTG)

- DTG enabled
- 12-bit rising edge delay
- 12-bit falling edge delay

20.2.3 QEP Decoder

- QEP encoder enabled
- Direction status
- Configurable Interrupts:
  - Phase A rising edge
  - Phase B rising edge
  - Index event
  - Counter wrap
- 4 different counting modes for best resolution, range and speed performance

21 GENERAL PURPOSE TIMERS

21.1 Block Diagram

Figure 21-1 SOC Bus Watchdog and Wake-up Timer

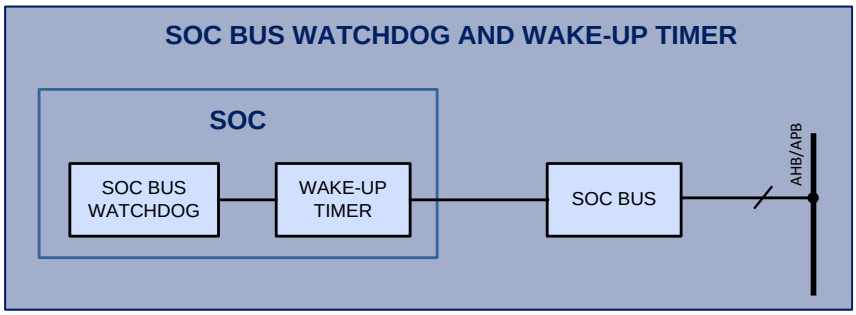
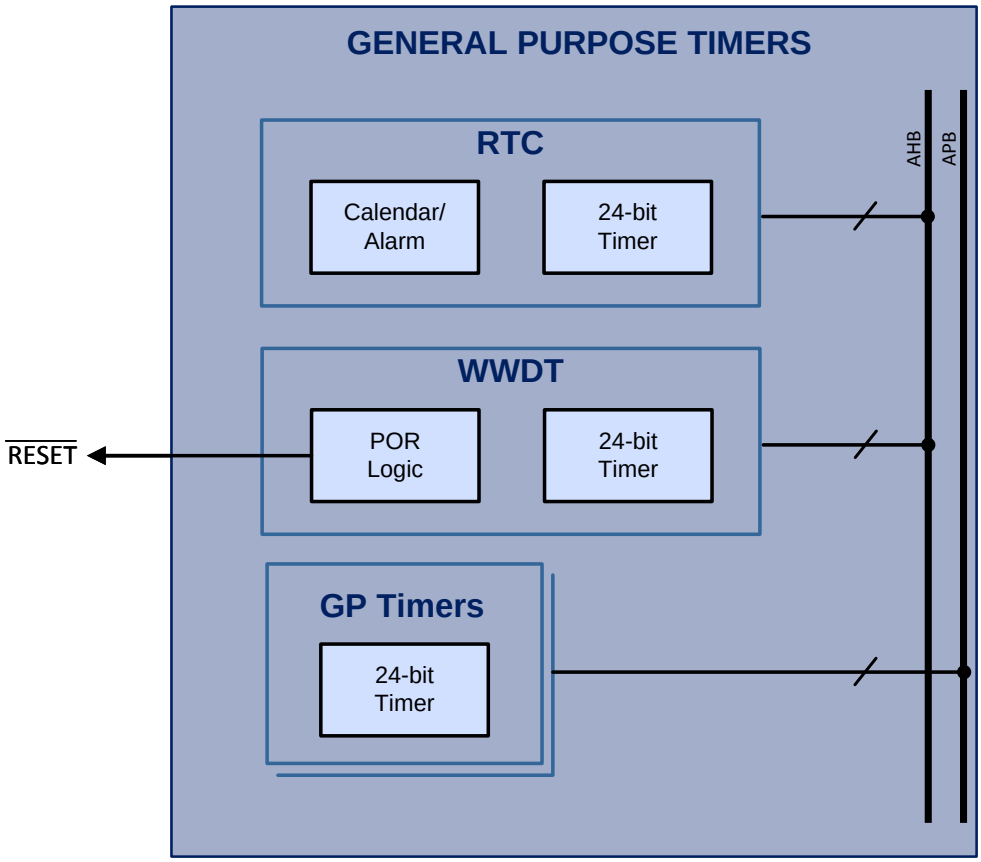


Figure 21-2 General Purpose Timers



21.2 Functional Description

21.2.1 SOC Bus Watchdog Timer

The SOC Bus Watchdog Timer is used to monitor internal SOC Bus communication. It will trigger a device reset if there is no SOC Bus communication to the AFE for 4s or 8s.

21.2.2 Wake-up Timer

The wake-up timer can be used for very low power hibernate and sleep modes to wake up the micro controller periodically. It can be configured to be 125ms, 250ms, 500ms, 1s, 2s, 4, or 8s.

21.2.3 Real-time Clock with Calendar (RTC)

The 24-bit real-time clock with calendar (RTC) is an AHB bus client and may also be used to measure long time periods and periodic wake up from sleep mode.

The RTC uses FRCLK as its clock source and has a divider that can be configured up to a /65536 input clock divider. In order to count accurately, the input clock divider must be configured to generate a 1MHz clock to the RTC.

The RTC counts the time (seconds, minutes, hours, days) since enabled. It also allows the user to set a calendar date to set an alarm function that can be configured to generate an interrupt to the NVIC when it counts to that value.

21.2.4 Windowed Watchdog Timer (WWDT)

The 24-bit windowed watchdog timer (WWDT) is an AHB bus client and can be used for long time period measurements or periodic wake up from sleep mode. Its primary use is to reset the system via a POR if it is not reset at a certain periodic interval.

The WWDT can be configured to use FRCLK or ROSCCLK as its clock source and has a divider that be configured up to a /65536 input clock divider.

The WWDT can be configured to allow only a small window when it is valid to reset the timer, to maximize application security and catch any stray code operating on the MCU.

The WWDT may be configured to enable an interrupt for the MCU, and the timer can be disabled when unused to save energy for low power operations.

21.2.5 GP Timer (GPT)

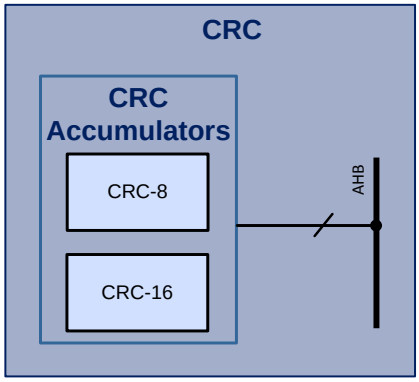
The PAC55XX contains two General Purpose (GP) Timers.

These timers are 24-bit timers and are both APB bus clients. These count-down timers use PCLK as their input clock and have a configurable divider of up to /32768. Each of the GPT can be configured to interrupt the MCU when they count down to 0.

22 CRC

22.1 Block Diagram

Figure 22-1 CRC Block Diagram



22.2 Functional Description

The CRC peripheral can perform CRC calculation on data through registers from the MCU to accelerate the calculation or validation of a CRC for communications protocols or data integrity checks.

The CRC peripheral allows the calculation of both CRC-8 and CRC-16 on data. The CRC peripheral also allows the user to specify a seed value, select the data input to be 8b or 32b and to reflect the final output for firmware efficiency.

The CRC peripheral is an AHB slave and has the following features:

- Polynomial selection via configuration register:
  - CCITT CRC-16 (0x1021)
  - IBM/ANSI CRC-16 (0x8005)
  - Dallas/Maxim CRC-8 (0x31)
- Input data width: 8b, 32b
- Reflect input
- Reflect output
- Specify seed value

23 THERMAL CHARACTERISTICS

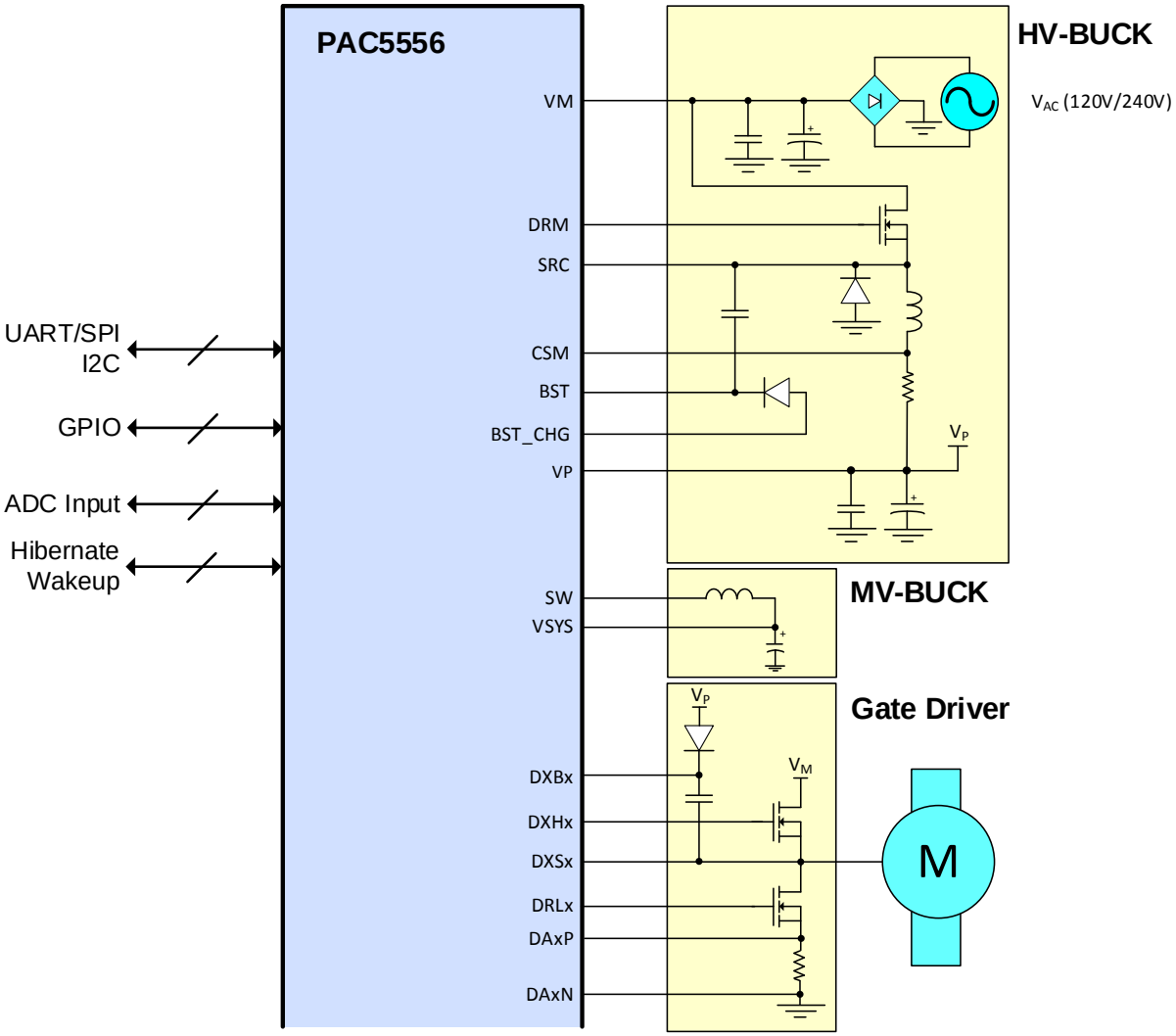
Table 23-1 Thermal Characteristics

PARAMETER	VALUE	UNIT
Operating ambient temperature range	-40 to 125	°C
Operating junction temperature range	-40 to 150	°C
Storage temperature range	-55 to 150	°C
Lead temperature (Soldering, 10 seconds)	300	°C
Junction-to-case thermal resistance (θ_{JC})	2.897	°C/W
Junction-to-ambient thermal resistance (θ_{JA})	23.36	°C/W

24 APPLICATION EXAMPLES

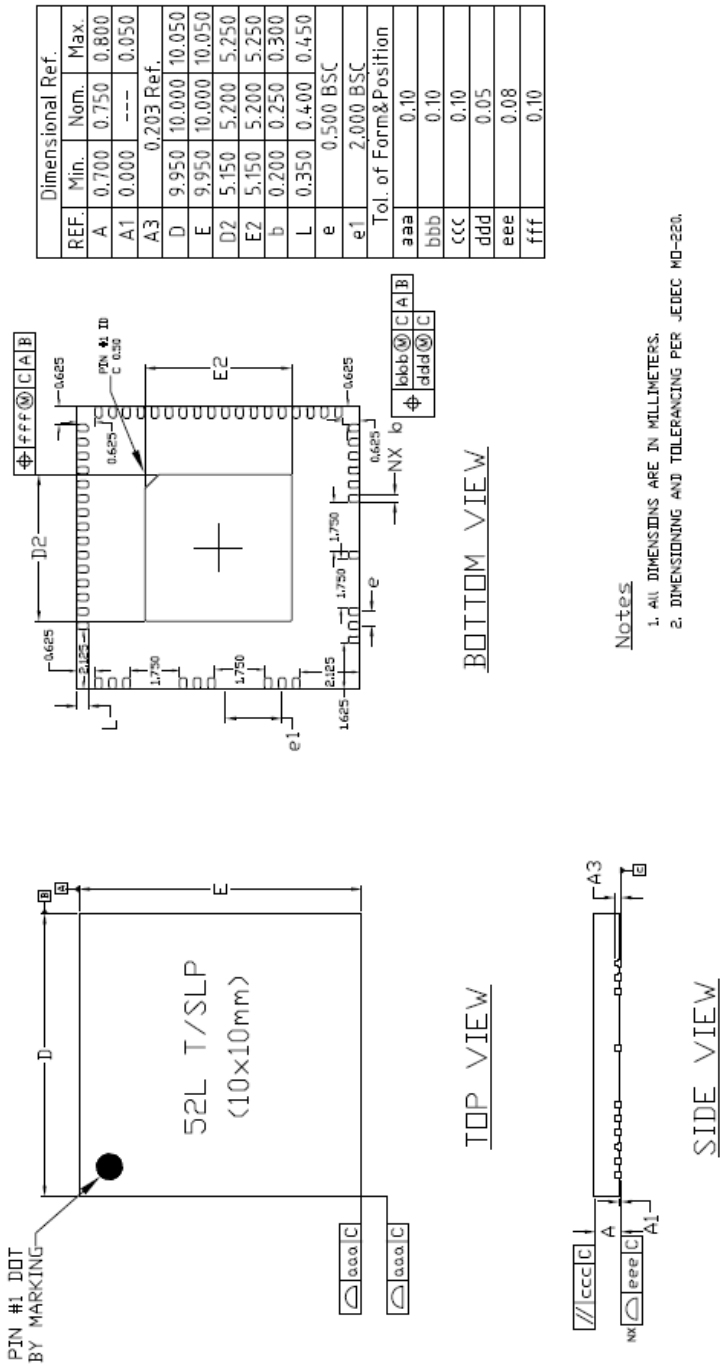
The following simplified diagram shows an example of a 3-phase BLDC or PMSM motor application for FOC or BEMF control.

Figure 24-1 BLDC/PMSM Motor Application Example



25 PACKAGE OUTLINE AND DIMENSIONS

Figure 25-1 QFN1010-52 Package Outline



Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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