19-Output DB1900Z Low-Power Derivative with 85ohm Terminations

9ZXL1950

DATASHEET

General Description

The 9ZXL1950 is a DB1900Z derivative buffer utilizing Low-Power HCSL (LP-HCSL) outputs to increase edge rates on long traces, reduce board space, and reduce power consumption more than 50% from the original 9ZX21901.It is pin-compatible to the 9ZXL1930 and fully integrates the output terminations. It is suitable for PCI-Express Gen1/2/3 or QPI/UPI applications, and uses a fixed external feedback to maintain low drift for demanding QPI/UPI applications.

Recommended Application

Buffer for Romley, Grantley and Purley Servers

Output Features

19 LP-HCSL output pairs w/integrated terminations (Zo = 85Ω)

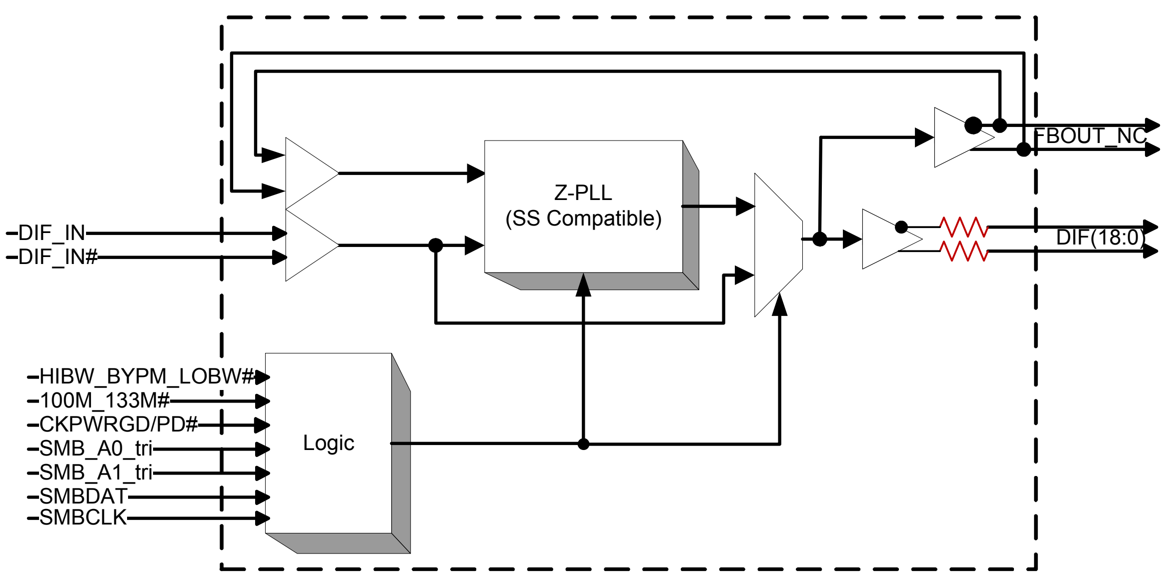
Key Specifications

- Cycle-to-cycle jitter: <50ps
- Output-to-output skew: <50ps
- Input-to-output delay variation: <50ps
- Phase jitter: PCIe Gen3 <1ps rms
- Phase jitter: QPI/UPI 9.6GB/s <0.2ps rms

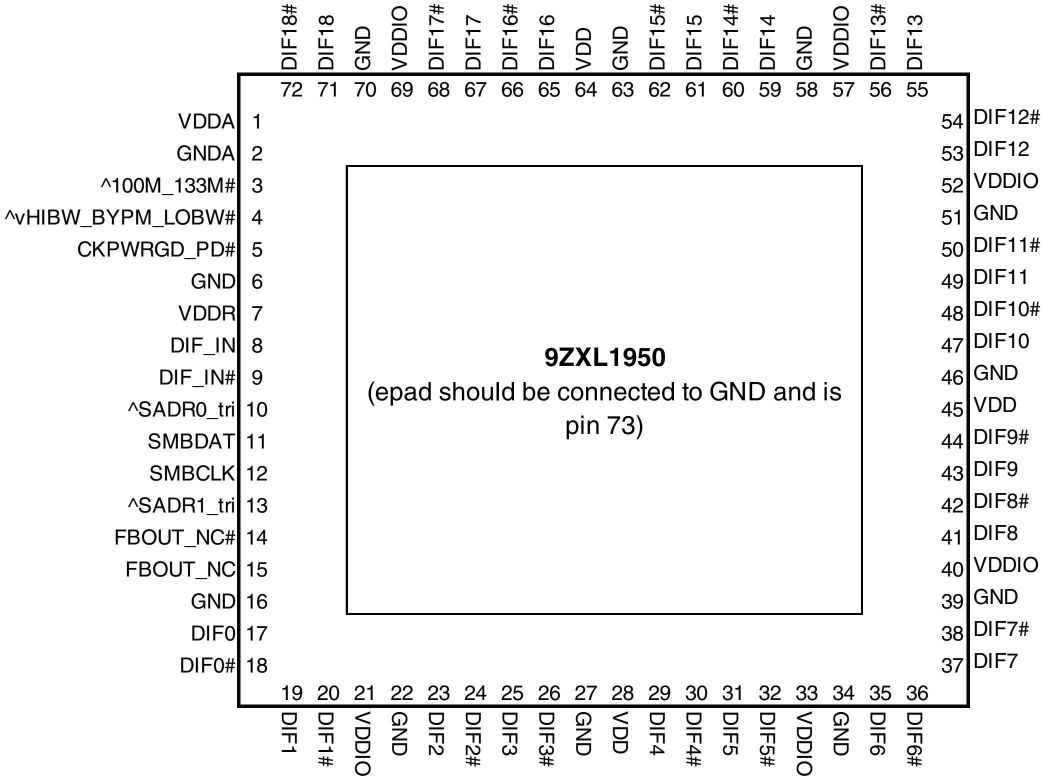
Features/Benefits

- LP-HCSL outputs; up to 90% IO power reduction, better signal integrity over long traces
- Direct connect to 85Ω transmission lines; eliminates 76 termination resistors, saves 130mm^2 area
- Pin compatible to the 9ZXL1930; easy upgrade to reduced board space
- 72-pin VFQFPN package; smallest 19-output Z-buffer
- Fixed feedback path; ~0ps input-to-output delay
- 9 Selectable SMBus addresses; multiple devices can share same SMBus segment
- Separate VDDIO for outputs; allows maximum power savings
- PLL or bypass mode; PLL can dejitter incoming clock
- 100MHz & 133.33MHz PLL mode; legacy QPI support
- Selectable PLL BW; minimizes jitter peaking in downstream PLL's
- Spread spectrum compatible; tracks spreading input clock for EMI reduction
- SMBus Interface; unused outputs can be disabled

Block Diagram



Pin Configuration



Note: Pins with ^ prefix have internal 120K pullup
Pins with v prefix have internal 120K pulldowm
Pins with ^v prefix have internal 120K pullup/pulldown (biased to VDD/2)

Power Management Table

Inputs		Control Bits	Outputs		PLL State
CKPWRGD_PD#	DIF_IN/ DIF_IN#	SMBus EN bit	DIFx/ DIFx#	FBOUT_NC/ FB_OUT_NC#	
0	X	X	Low/Low	Low/Low	OFF
1	Running	0	Low/Low	Running	ON
		1	Running	Running	ON

Power Connections

Pin Number			Description
VDD	VDDIO	GND	
1		2	Analog PLL
7		6	Analog Input
28, 45, 64	21, 33, 40, 52, 57, 69	16, 22, 27, 34, 39, 46, 51, 58, 63, 70, 73	DIF clocks

Functionality at Power-up (PLL mode)

100M_133M#	DIF_IN (MHz)	DIFx (MHz)
1	100.00	DIF_IN
0	133.33	DIF_IN

PLL Operating Mode

HiBW_BypM_LoBW#	Byte0, bit (7:6)
Low (PLL Low BW)	00
Mid (Bypass)	01
High (PLL High BW)	11

NOTE: PLL is off in Bypass mode

Tri-level Input Thresholds

Level	Voltage
Low	<0.8V
Mid	1.2<Vin<1.8V
High	Vin > 2.2V

Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDA	PWR	Power for the PLL core.
2	GNDA	GND	Ground pin for the PLL core.
3	^100M_133M#	IN	3.3V Input to select operating frequency. This pin has an internal pull-up resistor. See Functionality Table for Definition
4	^vHIBW_BYPM_LOBW#	LATCHED IN	Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details.
5	CKPWRGD_PD#	IN	3.3V Input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode.
6	GND	GND	Ground pin.
7	VDDR	PWR	3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately.
8	DIF_IN	IN	HCSL True input
9	DIF_IN#	IN	HCSL Complementary Input
10	^SADR0_tri	IN	SMBus address bit. This is a tri-level input that works in conjunction with the SADR1 to decode 1 of 9 SMBus Addresses. It has an internal 120Kohm pull up resistor.
11	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
12	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
13	^SADR1_tri	IN	SMBus address bit. This is a tri-level input that works in conjunction with the SADR0 to decode 1 of 9 SMBus Addresses. It has an internal 120Kohm pull up resistor.
14	FBOUT_NC#	OUT	Complementary half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay.
15	FBOUT_NC	OUT	True half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay.
16	GND	GND	Ground pin.
17	DIF0	OUT	Differential true clock output
18	DIF0#	OUT	Differential Complementary clock output
19	DIF1	OUT	Differential true clock output
20	DIF1#	OUT	Differential Complementary clock output
21	VDDIO	PWR	Power supply for differential outputs
22	GND	GND	Ground pin.
23	DIF2	OUT	Differential true clock output
24	DIF2#	OUT	Differential Complementary clock output
25	DIF3	OUT	Differential true clock output
26	DIF3#	OUT	Differential Complementary clock output
27	GND	GND	Ground pin.
28	VDD	PWR	Power supply, nominal 3.3V
29	DIF4	OUT	Differential true clock output
30	DIF4#	OUT	Differential Complementary clock output
31	DIF5	OUT	Differential true clock output
32	DIF5#	OUT	Differential Complementary clock output
33	VDDIO	PWR	Power supply for differential outputs
34	GND	GND	Ground pin.
35	DIF6	OUT	Differential true clock output
36	DIF6#	OUT	Differential Complementary clock output

Pin Descriptions (cont.)

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
37	DIF7	OUT	Differential true clock output
38	DIF7#	OUT	Differential Complementary clock output
39	GND	GND	Ground pin.
40	VDDIO	PWR	Power supply for differential outputs
41	DIF8	OUT	Differential true clock output
42	DIF8#	OUT	Differential Complementary clock output
43	DIF9	OUT	Differential true clock output
44	DIF9#	OUT	Differential Complementary clock output
45	VDD	PWR	Power supply, nominal 3.3V
46	GND	GND	Ground pin.
47	DIF10	OUT	Differential true clock output
48	DIF10#	OUT	Differential Complementary clock output
49	DIF11	OUT	Differential true clock output
50	DIF11#	OUT	Differential Complementary clock output
51	GND	GND	Ground pin.
52	VDDIO	PWR	Power supply for differential outputs
53	DIF12	OUT	Differential true clock output
54	DIF12#	OUT	Differential Complementary clock output
55	DIF13	OUT	Differential true clock output
56	DIF13#	OUT	Differential Complementary clock output
57	VDDIO	PWR	Power supply for differential outputs
58	GND	GND	Ground pin.
59	DIF14	OUT	Differential true clock output
60	DIF14#	OUT	Differential Complementary clock output
61	DIF15	OUT	Differential true clock output
62	DIF15#	OUT	Differential Complementary clock output
63	GND	GND	Ground pin.
64	VDD	PWR	Power supply, nominal 3.3V
65	DIF16	OUT	Differential true clock output
66	DIF16#	OUT	Differential Complementary clock output
67	DIF17	OUT	Differential true clock output
68	DIF17#	OUT	Differential Complementary clock output
69	VDDIO	PWR	Power supply for differential outputs
70	GND	GND	Ground pin.
71	DIF18	OUT	Differential true clock output
72	DIF18#	OUT	Differential Complementary clock output
73	epad	GND	Connect EPAD to ground.

Electrical Characteristics–Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Core Supply Voltage	VDDA, R				4.6	V	1,2
3.3V Logic Supply Voltage	VDD				4.6	V	1,2
I/O Supply Voltage	VDDIO				4.6	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5V	V	1
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			5.5V	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics–DIF_IN Clock Input Parameters

TA = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Crossover Voltage - DIF_IN	V_{CROSS}	Cross Over Voltage	150		900	mV	1
Input Swing - DIF_IN	V_{SWING}	Differential value	300			mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	
Input Duty Cycle	d_{tin}	Measurement from differential wavefrom	45		55	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential Measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2]Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics–Current Consumption

TA = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	I_{DDVDD}	All outputs 100MHz, C_L = 2pF; Zo = 85Ω		20	35	mA	
	$I_{DDVDDA/R}$	All outputs 100MHz, C_L = 2pF; Zo = 85Ω		15	20	mA	
	$I_{DDVDDIO}$	All outputs 100MHz, C_L = 2pF; Zo = 85Ω		142	185	mA	
Powerdown Current	$I_{DDVDDPD}$	All differential pairs low-low		2.2	6	mA	
	$I_{DDVDDA/RPD}$	All differential pairs low-low		4.5	9	mA	
	$I_{DDVDDIOPD}$	All differential pairs low-low		0.1	1	mA	

Electrical Characteristics–Input/Supply/Common Output Parameters

TA = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Ambient Operating Temperature	T_{COM}	Commmercial range	0	35	70	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	2		V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	GND - 0.3		0.8	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	
Input Frequency	F_{ibyp}	V_{DD} = 3.3 V, Bypass mode	33		150	MHz	2
	F_{ipll}	V_{DD} = 3.3 V, 100MHz PLL mode	90	100.00	110	MHz	2
	F_{ipll}	V_{DD} = 3.3 V, 133.33MHz PLL mode	120	133.33	147	MHz	2
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs	1.5		2.7	pF	1,4
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.65	1	ms	2
Input SS Modulation Frequency	f_{MODIN}	Allowable Frequency (Triangular Modulation)	30	31.5	33	kHz	
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion		25	300	us	1,3
Tfall	t_F	Fall time of control inputs			5	ns	1,2
Trise	t_R	Rise time of control inputs			5	ns	1,2
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	
Nominal Bus Voltage	V_{DDSMB}	3V to 5V +/- 10%	2.7		5.5	V	
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{SMB}	SMBus operating frequency	100			kHz	5

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Control input must be monotonic from 20% to 80% of input swing.

[3]Time from deassertion until outputs are >200 mV

[4]DIF_IN input

[5]The differential input clock must be running for the SMBus to be active

Electrical Characteristics–DIF 0.7V Low Power Differential Outputs

TA = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	Trf	Scope averaging on	1.5	2.7	4	V/ns	1, 2, 3
Slew rate matching	ΔTrf	Slew rate matching.		8.8	20	%	1, 2, 4
Voltage High	VHigh	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	787	850	mV	
Voltage Low	VLow		-150	33	150		
Max Voltage	Vmax	Single ended signal using absolute value. Includes 300mV of over/undershoot. (Scope		845	1150	mV	
Min Voltage	Vmin		-300	9			
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	471	550	mV	1, 5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		14	140	mV	1, 6

[1]Guaranteed by design and characterization, not 100% tested in production. C_L = 2pF with Zo = 85Ω differential trace impedance.

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

Clock Periods–Differential Outputs with Spread Spectrum Disabled

SSC OFF	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns	1,2,3
	133.33	7.44925		7.49925	7.50000	7.50075		7.55075	ns	1,2,4

Clock Periods–Differential Outputs with Spread Spectrum Enabled

SSC ON	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2,3
	133.00	7.44930	7.49930	7.51805	7.51880	7.51955	7.53830	7.58830	ns	1,2,4

Notes:

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ/CK410B+ accuracy requirements (+/-100ppm). The 9ZXL1950 itself does not contribute to ppm error.

[3] Driven by SRC output of main clock, 100 MHz PLL Mode or Bypass mode

[4] Driven by CPU output of main clock, 133 MHz PLL Mode or Bypass mode

Electrical Characteristics–Skew and Differential Jitter Parameters

TA = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
CLK_IN, DIF[x:0]	t_{SPO_PLL}	Input-to-Output Skew in PLL mode nominal value @ 35°C, 3.3V, 100MHz	-150	-117	-50	ps	1,2,4,5,8
CLK_IN, DIF[x:0]	t_{PD_BYP}	Input-to-Output Skew in Bypass mode nominal value @ 35°C, 3.3V	2.5	3.6	4.5	ns	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DSPO_PLL}	Input-to-Output Skew Varation in PLL mode across voltage and temperature	-50	0	50	ps	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DSPO_BYP}	Input-to-Output Skew Varation in Bypass mode across temperature for a given voltage	-250	0	250	ps	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DTE}	Random Differential Tracking error beween two 9ZX devices in Hi BW Mode		1	5	ps (rms)	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DSSTE}	Random Differential Spread Spectrum Tracking error beween two 9ZX devices in Hi BW Mode		5	75	ps	1,2,3,5,8
DIF[x:0]	t_{SKEW_ALL}	Output-to-Output Skew across all outputs (Common to Bypass and PLL mode). 100MHz		37	50	ps	1,2,3,8
PLL Jitter Peaking	$j_{peak-hibw}$	LOBW#_BYPASS_HIBW = 1	0	1.8	2.5	dB	7,8
PLL Jitter Peaking	$j_{peak-lobw}$	LOBW#_BYPASS_HIBW = 0	0	0.7	2	dB	7,8
PLL Bandwidth	pll_{HIBW}	LOBW#_BYPASS_HIBW = 1	2	3.3	4	MHz	8,9
PLL Bandwidth	pll_{LOBW}	LOBW#_BYPASS_HIBW = 0	0.7	1.2	1.4	MHz	8,9
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45	50	55	%	1
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode @100MHz	0	0.7	1.5	%	1,10
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	PLL mode		12	50	ps	1,11
		Additive Jitter in Bypass Mode		0	10	ps	1,11

Notes for preceding table:

[1] Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

[2] Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.

[3] All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.

[4] This parameter is deterministic for a given device

[5] Measured with scope averaging on to find mean value.

[6.] t is the period of the input clock

[7] Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.

[8.] Guaranteed by design and characterization, not 100% tested in production.

[9] Measured at 3 db down or half power point.

[10] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[11] Measured from differential waveform

Electrical Characteristics–Phase Jitter Parameters

TA = T_{COM}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, VDDIO = 1.05 to 3.3V +/-5%. See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG1}$	PCIe Gen 1		34	86	ps (p-p)	1,2,3
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		1.2	3	ps (rms)	1,2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		2.1	3.1	ps (rms)	1,2
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.5	1	ps (rms)	1,2,4
	t_{jphQPI_SMI}	QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.2	0.5	ps (rms)	1,5
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)		0.1	0.3	ps (rms)	1,5
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)		0.1	0.2	ps (rms)	1,5
Additive Phase Jitter, Bypass mode	$t_{jphPCIeG1}$	PCIe Gen 1		0.1	10	ps (p-p)	1,2,3
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.1	0.3	ps (rms)	1,2,6
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		0.1	0.7	ps (rms)	1,2,6
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.0	0.3	ps (rms)	1,2,4,6
	t_{jphQPI_SMI}	QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.0	0.3	ps (rms)	1,5,6
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)		0.0	0.1	ps (rms)	1,5,6
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)		0.0	0.1	ps (rms)	1,5,6

[1] Applies to all outputs.

[2] See http://www.pcisig.com for complete specs

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] Subject to final ratification by PCI SIG.

[5] Calculated from Intel-supplied Clock Jitter Tool v 1.6.4

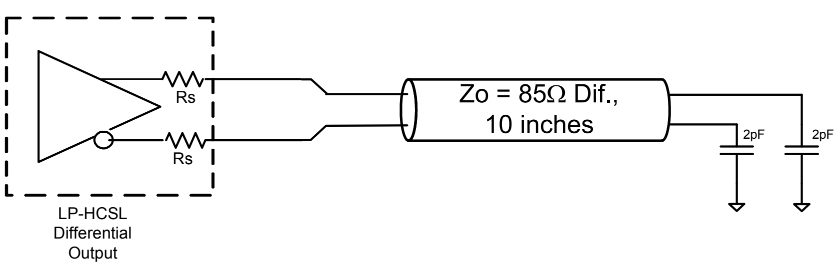
[6] For RMS figures, additive jitter is calculated by solving the following equation: (Additive jitter)^2 = (total jittter)^2 - (input jitter)^2

Test Loads

Differential Output Terminations

DIF Zo (Ω)	Rs (Ω)
85	Internal
100	7.5 (External)

9ZXL Differential Test Loads



General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

9ZXL1950 SMBus Addressing

SADR(1:0)_tri	SMBus Address (Rd/Wrt bit = 0)
00	D8
0M	DA
01	DE
M0	C2
MM	C4
M1	C6
10	CA
1M	CC
11	CE

SMBusTable: PLL Mode, and Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	4	PLL Mode 1	PLL Operating Mode Rd back 1	**R**	See PLL Operating Mode		Latch
Bit 6	4	PLL Mode 0	PLL Operating Mode Rd back 0	**R**	Readback Table		Latch
Bit 5	72/71	DIF_18_En	Output Control	RW	Low/Low	Enable	1
Bit 4	68/67	DIF_17_En	Output Control	RW	Low/Low	Enable	1
Bit 3	66/65	DIF_16_En	Output Control	RW	Low/Low	Enable	1
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0	3	100M_133M#	Frequency Select Readback	**R**	133MHz	100MHz	Latch

SMBusTable: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	38/37	DIF_7_En	Output Control	RW	Low/Low	Enable	1
Bit 6	35/36	DIF_6_En	Output Control	RW			1
Bit 5	31/32	DIF_5_En	Output Control	RW			1
Bit 4	29/30	DIF_4_En	Output Control	RW			1
Bit 3	25/26	DIF_3_En	Output Control	RW			1
Bit 2	23/24	DIF_2_En	Output Control	RW			1
Bit 1	19/20	DIF_1_En	Output Control	RW			1
Bit 0	17/18	DIF_0_En	Output Control	RW			1

SMBusTable: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	62/61	DIF_15_En	Output Control	RW	Low/Low	Enable	1
Bit 6	60/59	DIF_14_En	Output Control	RW			1
Bit 5	56/55	DIF_13_En	Output Control	RW			1
Bit 4	54/53	DIF_12_En	Output Control	RW			1
Bit 3	50/49	DIF_11_En	Output Control	RW			1
Bit 2	48/47	DIF_10_En	Output Control	RW			1
Bit 1	44/43	DIF_9_En	Output Control	RW			1
Bit 0	42/41	DIF_8_En	Output Control	RW			1

SMBusTable: PLL SW Override Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		PLL_SW_EN	Enable S/W control of PLL BW	RW	HW Latch	SMBus Control	0
Bit 2		PLL Mode 1	PLL Operating Mode 1	RW	See PLL Operating Mode		1
Bit 1		PLL Mode 0	PLL Operating Mode 1	RW	Readback Table		1
Bit 0		Reserved					0

Note: Setting bit 3 to '1' allows the user to overide the Latch value from pin 4 via use of bits 2 and 1. Use the values from the PLL Operating Mode Readback Table. Note that Byte 0, Bits 7:6 will keep the value originally latched on pin 4. A warm reset of the system will have to accomplished if the user changes these bits.

SMBusTable: Reserved Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

SMBusTable: Vendor & Revision ID Register

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	REVISION ID	R	A rev = 0000 B rev = 0001 etc.		X
Bit 6	-	RID2		R			X
Bit 5	-	RID1		R			X
Bit 4	-	RID0		R			X
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBusTable: DEVICE ID

Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	Device ID 7 (MSB)		R	1950 is 195 Decimal or C3 Hex 1550 is 155 Decimal or 9B Hex		1
Bit 6	-	Device ID 6		R			1
Bit 5	-	Device ID 5		R			0
Bit 4	-	Device ID 4		R			0
Bit 3	-	Device ID 3		R			0
Bit 2	-	Device ID 2		R			0
Bit 1	-	Device ID 1		R			1
Bit 0	-	Device ID 0		R			1

SMBusTable: Byte Count Register

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4	-	BC4	Writing to this register configures how many bytes will be read back.	RW	Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default.		0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			0
Bit 1	-	BC1		RW			0
Bit 0	-	BC0		RW			0

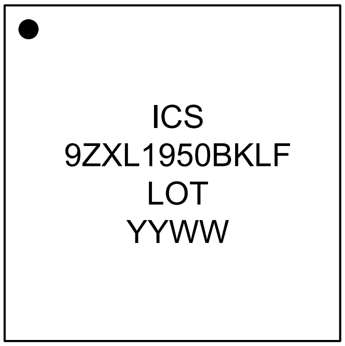
SMBusTable: Reserved Register

Byte 8	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

Alternate Terminations

The 9ZXL1950 can be terminated to other logic families. See “AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs” for details.

Marking Diagram

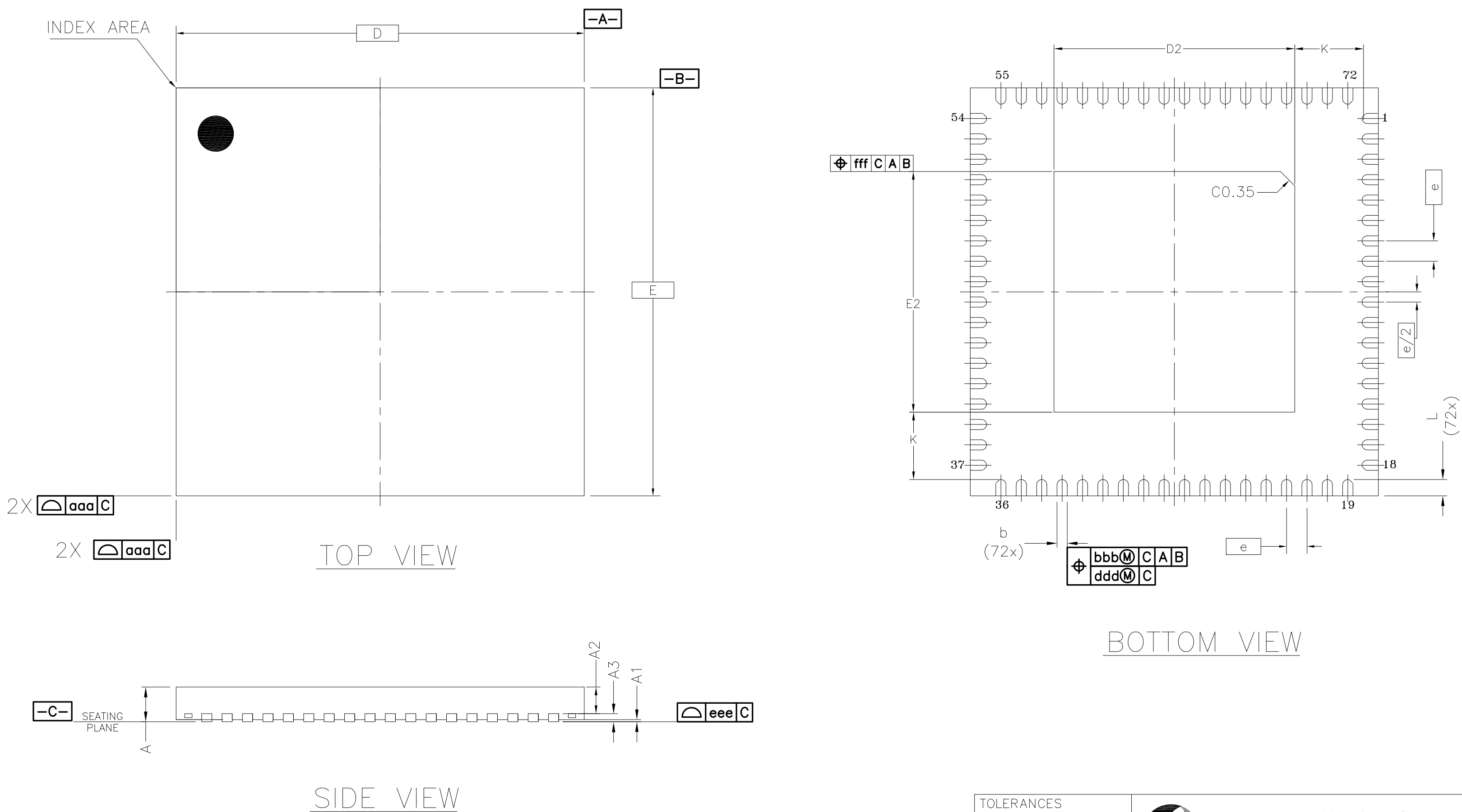


Notes:

1. “LOT” denotes the lot number.
2. “YYWW” is the last two digits of the year and week that the part was assembled.
3. “LF” denotes RoHS compliant package.
4. Bottom marking: country of origin if not USA.

Package Outline and Dimensions (NLG72)

DATE CREATED	REV	DESCRIPTION	AUTHOR
		REVISIONS	
2/2/16	00	INITIAL RELEASE.	JH
1/11/17	01	CORRECT eee TOLERANCE.	JH
5/8/17	02	CHANGE PACKAGE CODE QFN to VFQFPN	JH
		NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE	



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M−1994
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. INDEX AREA (PIN1 IDENTIFIER)

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR X± XX± XXX±	IDT™ www.IDT.com 6024 Silver Creek Valley Road San Jose, CA 95138 PHONE: (408) 284−8200 FAX: (408) 284−8591
	TITLE NL/NLG72 PACKAGE OUTLINE 10.0 x 10.0 mm BODY, EPAD 5.9mm SQ. 0.50 mm Pitch VFQFPN (SAWN)
	SIZE C | DRAWING No. PSC−4208−01 | REV 02
	DO NOT SCALE DRAWING | SHEET 1 OF 3

Package Outline and Dimensions (NLG72), cont.

DATE CREATED	REV	DESCRIPTION	AUTHOR
		REVISIONS	
2/2/16	00	INITIAL RELEASE.	JH
1/11/17	01	CORRECT eee TOLERANCE.	JH
5/8/17	02	CHANGE PACKAGE CODE QFN to VFQFPN	JH

NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
D2	5.80	5.90	6.00
E2	5.80	5.90	6.00
A2	0.00	0.65	1.00
L	0.30	0.40	0.50
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	0.20 ref.		
b	0.18	0.25	0.30
e	0.50 BSC		
D	10.00 BSC		
E	10.00 BSC		
K	1.65 ref.		
TOLERANCES			
aaa	0.15		
bbb	0.10		
ccc	0.05		
eee	0.08		
fff	0.10		

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
X±
XX±
XXX±

IDT™ www.IDT.com

6024 Silver Creek Valley Road
San Jose, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591

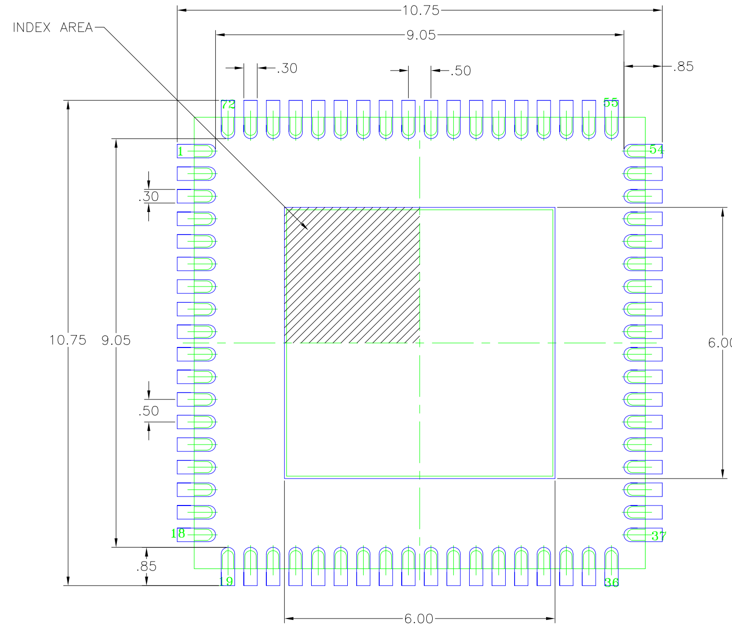
TITLE NL/NLG72 PACKAGE OUTLINE
10.0 x 10.0 mm BODY, EPAD 5.9mm SQ.
0.50 mm Pitch VFQFPN (SAWN)

SIZE	DRAWING No.	REV
C	PSC-4208-01	02

DO NOT SCALE DRAWING | SHEET 2 OF 3

Package Outline and Dimensions (NLG72), cont.

DATE CREATED	REV	REVISIONS DESCRIPTION	AUTHOR
2/2/16	00	INITIAL RELEASE.	JH
1/11/17	01	CORRECT eee TOLERANCE.	JH
5/8/17	02	CHANGE PACKAGE CODE QFN to VFQFPN	JH
		NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE	



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC–7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR X± XX± XXX±	IDT™ www.IDT.com 6024 Silver Creek Valley Road San Jose, CA 95138 PHONE: (408) 284–8200 FAX: (408) 284–8591
	TITLE NL/NLG72 PACKAGE OUTLINE 10.0 x 10.0 mm BODY, EPAD 5.9mm SQ. 0.50 mm Pitch VFQFPN (SAWN)
	SIZE C — DRAWING No. PSC–4208–01 — REV 02
	DO NOT SCALE DRAWING — SHEET 3 OF 3

Ordering Information

Part / Order Number	Shipping Package	Package	Temperature
9ZXL1950BKLF	Trays	72-pin VFQFPN	0 to +70°C
9ZXL1950BKLFT	Tape and Reel	72-pin VFQFPN	0 to +70°C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

"B" is the device revision designator (will not correlate with the datasheet revision).

Revision History

Rev.	Issuer	Issue Date	Description	Page #
A	RDW	3/11/2014	Moved to final.	
B	RDW	3/7/2015	1. Cleaned up output pin names to be DIFxx instead of DIF_xx 2. Updated electrical tables to new format 3. Updated ordering info to B rev along with Rev ID. 4. Updated termination schemes for driving LVDS. 5. Minor cleanup/reformatting of DS, including front page text.	Various
C	RDW	6/16/2015	Added landing pattern from POD	17
D	RDW	7/30/2015	1. Tightened O2O spec from 75 to 50ps 2. Added epad (pin 73) to power connections table 3. Updated pin 73 pin name from "GND" to "epad" 4. Clarified SMBus operating frequency by removing the word "Maximum" and updated the symbol from fMINSMB to fSMB 5. Tightened duty cycle distortion and additive cycle to cycle jitter specs 6. Updated Rs from 7 to 7.5 ohms in Test Loads Table 7. Replaced LVDS termination info with reference to AN891.	1,8 2 4 6 8 9 13
E	RDW	11/20/2015	1. Updated QPI references to QPI/UPI 2. Updated DIF_IN table to match PCI SIG specification, no silicon change	1,5
F	RDW	5/11/2017	Updated package outline drawings to latest version.	14-16

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