

### FEATURES

Interfaces to multiple serial and parallel precision converter evaluation boards

Supports high-speed LVDS interface

32MB SDRAM

4MB SRAM

USB 2.0 connection to PC

User reprogrammable Altera Cyclone FPGA

Provides 8 separate power supplies

Connects directly to Blackfin Ez-Kit

### APPLICATIONS

Evaluating Precision Converters

Creation of demonstration systems

Prototyping of end-user systems

### GENERAL DESCRIPTION

The CED1 board is part of a next generation platform from Analog Devices Inc., intended for use in evaluation, demonstration and development of systems using Analog Devices precision converters. It provides the necessary communications between the converter and the PC, programming or controlling the device, transmitting or receiving data over a USB link.

### PACKAGE CONTENTS

- CED Board
- USB A to Mini-B cable
- 7 Volt 15W Power Supply

### FUNCTIONAL BLOCK DIAGRAM

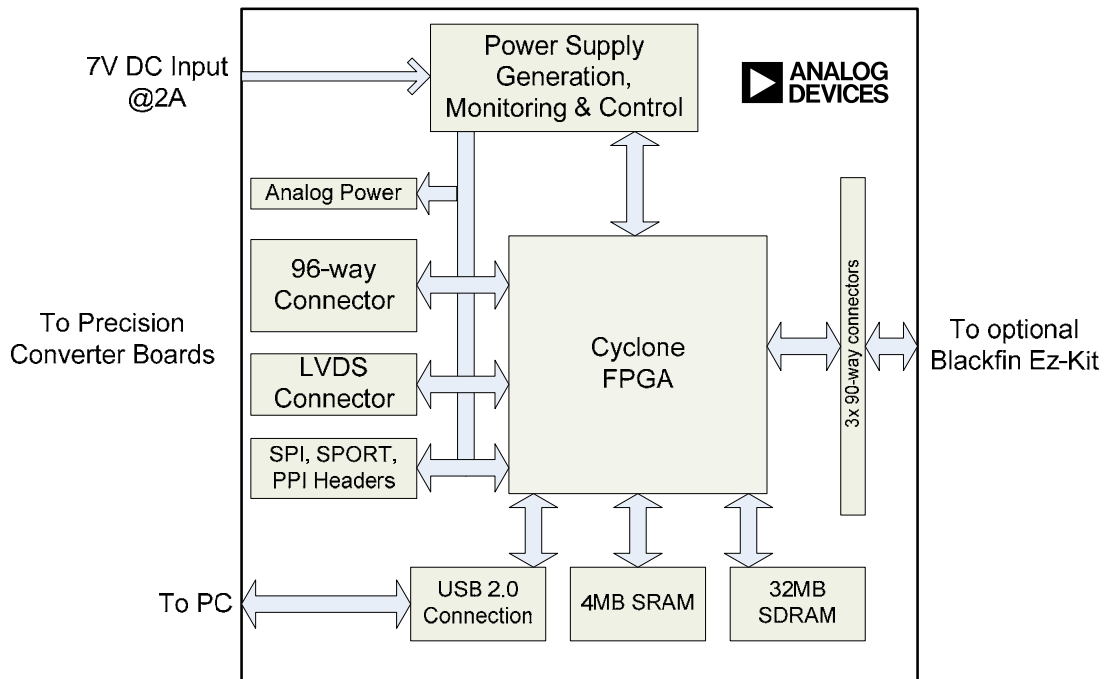


Figure 1.

#### Rev. PrA

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**REVISION HISTORY**

**7/07—Revision 0: Initial Revision**

## GENERAL DESCRIPTION

The Converter Evaluation and Development board is intended to assist system designers evaluate and prototype systems utilizing precision converter components from Analog Devices. It provides a means to read and write data, control and program devices from a PC via a high-speed USB 2.0 connection.

Due to its design, the CED1 can handle interfacing to multiple devices simultaneously for users who may wish to prototype their system utilizing proven hardware components from Analog Devices.

The reconfigurable FPGA-based architecture of the board allows the FPGA to be reprogrammed at any time via the USB connection. This allows the user to develop and run their own code to accomplish their desired task.

The many interfacing options accommodate connection to a wide range of precision converter evaluation boards in different form factors. Three standard 0.1-inch pitch headers are available, supporting SPI, SPORT and parallel functionality. A 96-way connector provides links to multiple

interfaces and power supplies simultaneously. LVDS is supported through a dedicated connector designed for data pairs with individual grounds.

For developments that require a processor as well as an FPGA, the CED1 board provides the means to connect directly to a Blackfin EZ-Kit. Three 90-way connectors present on the board mate directly with the Blackfin Ez-Kit allowing the development of very powerful systems and demonstrations.

To help minimize the amount of external equipment needed to run a system successfully, the CED board provides eight separate power supplies made available for external connection. The details of these supplies and their current ratings are contained in the Power Supply section of this document.

The CED board requires a single 7V, 15W supply which ships with the board. The user may also connect a bench-top supply providing it can source a minimum current of 2A.

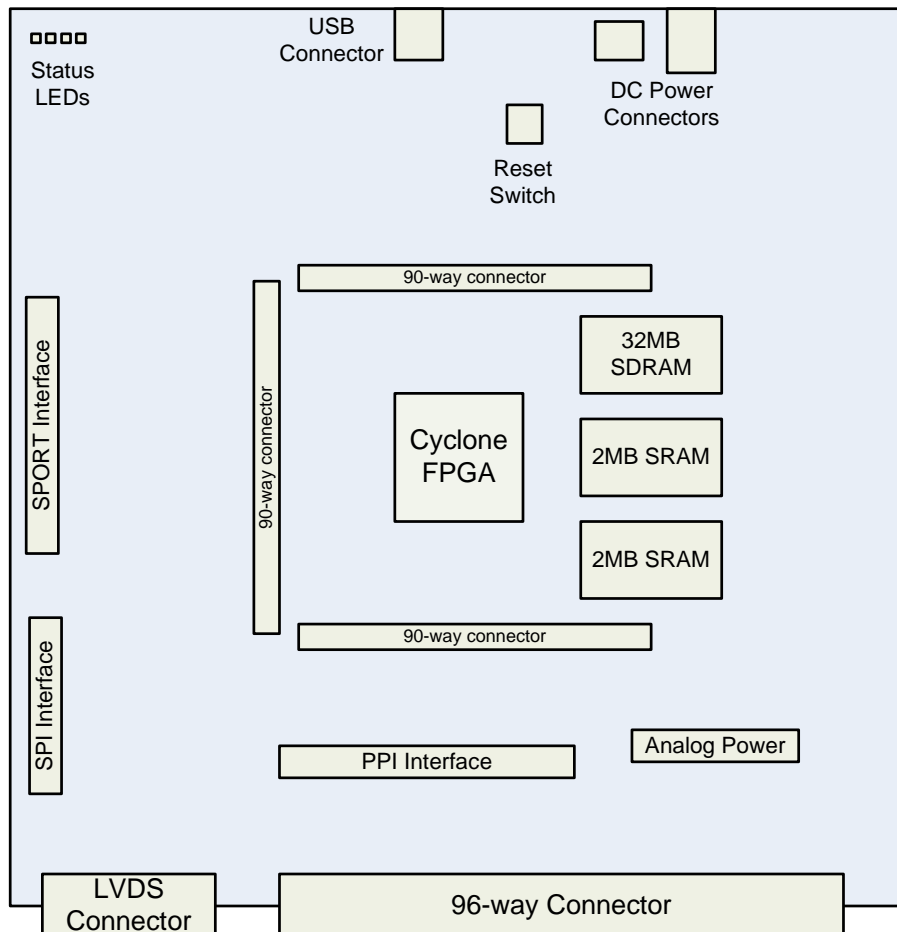


Figure 2. Major Component Locations

## CONNECTORS

Many connectors are provided on the CED board to facilitate design and attachment of a range of different form factor converter boards. Due to the number of connections available on the FPGA, certain signals on different connectors are shared and replicated across different connectors.

All signals have been named to assist the user in identifying the shared signals and to which group they belong. SPI signals begin with SPI\_xxx, SPORT signals begin with SPORT\_xxx and parallel/PPI signals begin with PAR\_xxx/PPI\_xxx. More details of these signals are given in the relevant connector sections.

### J5 – LVDS CONNECTOR

If connecting the CED1 to a high-speed LVDS converter evaluation board, this connector should be used. The connector provides for four differential receive and four differential transmit data pairs in addition to separate differential receive

and transmit clocks. Control of any high-speed device is normally achieved over an interface separate to the data. For this purpose, the SPI and some parallel control signals are also routed over this connector. With the inclusion of three power supplies, this connector provides the flexibility to interface to many LVDS converters. Details of the pin-out of this connector are given in Table 1.

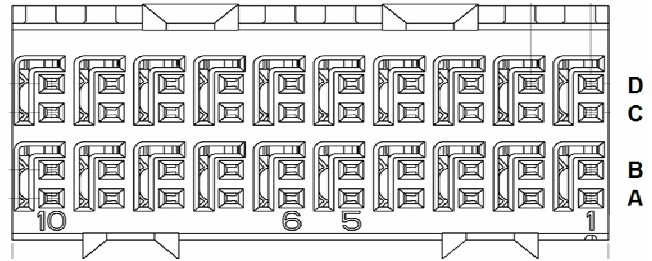


Figure 3. LVDS Connector pin locations

Table 1. LVDS Connector pin out

| Pin Num    | Pin Name                     | Description   |
|------------|------------------------------|---|
| 1A, 1B     | +VarA                        | Variable voltage analog power supply. See power supply section for more details.  |
| 1C, 1D     | CLKOUT+/-                    | Differential Clock Output   |
| 2A         | $\overline{\text{PAR\_CS0}}$ | Parallel Chip Select 0  |
| 2B         | $\overline{\text{PAR\_RD}}$  | Parallel Read Strobe  |
| C2-9, D2-7 | Dx+/-                        | Differential Data Receive or Transmit Pair. By default the CED board is configured for 4 receive pairs (D0-3) and 4 transmit pairs (D4-7). These can be reconfigured by changing the termination resistors on the CED board. See schematics for more details. |
| A3-6       | SPI_SELx                     | SPI Peripheral Chip Select  |
| B3         | $\overline{\text{PAR\_WR}}$  | Parallel Write Strobe   |
| B4         | SPI_MISO                     | SPI Master In, Slave Out Data line  |
| B5         | SPI_MOSI                     | SPI Master Out, Slave In Data line  |
| B6         | SPI_CLK                      | SPI Clock   |
| A7         | TMR0/PPI_FS2                 | Timer 0 or Frame Sync 2 for PPI usage   |
| B7         | GPIO3/TMR1/PPI_FS1           | General Purpose I/O, Timer 1 or Frame Sync 2 for PPI usage  |
| A8         | RXINT/GPIO2/PPI_FS3          | Receive Interrupt, General Purpose I/O or Frame Sync 3 for PPI usage  |
| B8         | GPIO4/PAR_A0                 | General Purpose I/O or parallel address LSB   |
| A9, B9     | +3.3VD_Edge                  | +3.3V Digital power supply  |
| A10, B10   | +VarD                        | Variable voltage digital power supply. See power supply section for more details.   |
| C10, D10   | CLKIN+/-                     | Differential Clock Input pair   |

**J1 – MINI USB ‘B’ CONNECTOR**

This is used to connect the CED1 to the PC for control and data transfer

**J2 – 2-PIN SCREW TERMINAL POWER CONNECTOR**

This connector is used when powering the CED board with a lab supply. Care must be taken to ensure the external supply is connected with the correct polarity.

**J4 – DC POWER CONNECTOR**

When using the CED1 with the supplied power supply, the DC plug should be connected here. The polarity for this connector is centre positive.

**J6 – FPGA JTAG CONNECTOR**

This can be used with Altera SignalTap Logic Analyzer and appropriate hardware to assist with FPGA development and debug.

**J8, 9, 10 – 3× 90-WAY BLACKFIN EZ-KIT CONNECTORS**

These three connectors bring across most of the peripheral signals from the Blackfin Ez-Kit directly into the FPGA where

they can be used directly or rerouted to the other connectors. Additional processor or microcontroller boards could be designed and connected here if the user wished to add a processor to the design. See the Blackfin Ez-Kit manual for details of these connectors.

**J3 – 96-WAY DIN41612 CONNECTOR**

This connector has traditionally appeared on most precision ADC evaluation boards. It contains SPI, SPORT and Parallel signals as well as programmable digital and 5 separate analog power supplies. Pin out for this connector is shown in Table 2.

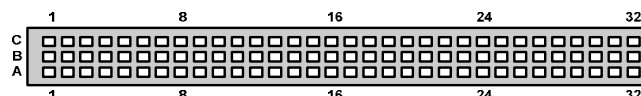


Figure 4. 96-way connector pin locations

Table 2. 96-way connector pin-out

| Pin Num    | Pin Name                          | Description   |
|------------|-----------------------------------|---|
| A1         | SPORT_DT1PRI/<br>SPI_MOSI/PAR_D16 | Sport1 Data Transmit Primary. SPI Master Out, Slave In data line. Parallel Data bit 16. |
| B1         | GPIO3/TMR1/<br>PPI_FS1            | General Purpose I/O bit 3. Timer 1. Parallel Peripheral Interface Frame Sync 1.         |
| C1         | SPORT_DR1PRI/<br>SPI_MISO/PAR_D19 | Sport 1 Data Receive Primary. SPI Master In, Slave Out data line. Parallel Data bit 19. |
| A2         | SPORT_TFS1/<br>SPI_SEL0/PAR_D17   | Sport 1 Transmit Frame Sync. SPI Peripheral Chip Select 0. Parallel Data bit 17.        |
| B2         | PAR_D0                            | Parallel Data bit 0 (LSb)   |
| C2         | SPORT_RFS1/<br>SPI_SEL1/PAR_D20   | Sport 1 Receive Frame Sync. SPI Peripheral Chip Select 1. Parallel Data bit 20.         |
| A3         | SPORT_TSCLK1/<br>SPI_CLK/PAR_D18  | Sport 1 Transmit Serial Clock. SPI Clock. Parallel Data bit 18.                         |
| B3         | PAR_D1                            | Parallel Data bit 1.  |
| C3         | SPORT_RSCLK1/<br>SPI_CLK/PAR_D21  | Sport 1 Receive Clock. SPI Clock. Parallel Data bit 21.                                 |
| A4, B4, C4 | DGND                              | Digital Ground  |
| A5         | SPORT_DT0PRI/<br>SPI_SEL7         | Sport 0 Data Transmit Primary. SPI Peripheral Chip Select 7                             |
| B5         | PAR_D2                            | Parallel Data bit 2   |

|                      |                                 |  |
|----------------------|---------------------------------|--|
| <b>C5</b>            | SPORT_DR0PRI/<br>SPI_SEL4       | Sport 0 Data Receive Primary. SPI Peripheral Chip Select 4                               |
| <b>A6</b>            | SPORT_TFS0/<br>SPI_SEL6         | Sport 0 Transmit Frame Sync. SPI Peripheral Chip Select 6                                |
| <b>B6</b>            | PAR_D3                          | Parallel Data bit 3  |
| <b>C6</b>            | SPORT_RFS0/<br>SPI_SEL3         | Sport 0 Receive Frame Sync. SPI Peripheral Chip Select 3                                 |
| <b>A7</b>            | SPORT_TSCLK0/<br>SPI_SEL5       | Sport 0 Transmit Serial Clock. SPI Peripheral Chip Select 5                              |
| <b>B7</b>            | PAR_D4                          | Parallel Data bit 4  |
| <b>C7</b>            | SPORT_RSCLK0/<br>SPI_SEL2       | SPORT 0 Receive Serial Clock. SPI Peripheral Chip Select 2                               |
| <b>A8, B8, C8</b>    | +VarD (DV <sub>DD</sub> )       | Variable Digital Power Supply. See Power Supply section for further details.             |
| <b>A9</b>            | PAR_RD                          | Parallel Read Strobe   |
| <b>B9</b>            | PAR_D5                          | Parallel Data bit 5  |
| <b>C9</b>            | PAR_WR                          | Parallel Write Strobe  |
| <b>A10</b>           | PAR_D22/PAR_A7                  | Parallel Data bit 22. Parallel Address bit 7 (MSb)                                       |
| <b>B10</b>           | PAR_D6                          | Parallel Data bit 5  |
| <b>C10</b>           | PAR_CS0                         | Parallel Chip Select 0   |
| <b>A11</b>           | SPORT_DT0SEC/<br>PAR_CS1/PAR_A5 | Sport 0 Data Transmit Secondary. Parallel Chip Select 1. Parallel Address bit 5          |
| <b>B11</b>           | PAR_D7                          | Parallel Data bit 7  |
| <b>C11</b>           | GPIO6/PAR_D23/<br>PAR_A6        | General Purpose I/O bit 6. Parallel Data bit 23. Parallel Address bit 6                  |
| <b>A12, B12, C12</b> | DGND                            | Digital Ground   |
| <b>A13</b>           | TWI_SDA/PAR_CS3/<br>PAR_A3      | Two Wire Interface Serial Data. Parallel Chip Select 3. Parallel Address bit 3           |
| <b>B13</b>           | PAR_D8                          | Parallel Data bit 8  |
| <b>C13</b>           | SPORT_DR0SEC/<br>PAR_CS2/PAR_A4 | Sport 0 Data Receive Secondary. Parallel Chip Select 2. Parallel Address bit 4           |
| <b>A14</b>           | GPIO5/PAR_A1                    | General Purpose I/O bit 5. Parallel Address bit 1  |
| <b>B14</b>           | PAR_D9                          | Parallel Data bit 9  |
| <b>C14</b>           | TWI_SCL/GPIO7/<br>PAR_A2        | Two Wire Interface Serial Clock. General Purpose I/O bit 7 (MSb). Parallel Address bit 2 |
| <b>A15</b>           | GPIO0                           | General Purpose I/O bit 0 (LSb)  |
| <b>B15</b>           | PAR_D10                         | Parallel Data bit 10   |
| <b>C15</b>           | GPIO4/PAR_A0                    | General Purpose I/O bit 4. Parallel Address bit 0 (LSb)                                  |
| <b>A16, B16, C16</b> | DGND                            | Digital Ground   |

|                               |                          |   |
|-------------------------------|--------------------------|---|
| <b>A17</b>                    | TMR0/PPI_FS2             | Timer 0. Parallel Peripheral Interface Frame Sync 2   |
| <b>B17</b>                    | PAR_D11                  | Parallel Data bit 11  |
| <b>C17</b>                    | RXINT/GPIO2/<br>PPI_FS3  | Receive Data Interrupt. General Purpose I/O bit 2. Parallel Peripheral Interface Frame Sync 3 |
| <b>A18</b>                    | PAR_D12                  | Parallel Data bit 12  |
| <b>B18</b>                    | PAR_D13                  | Parallel Data bit 13  |
| <b>C18</b>                    | PAR_D14                  | Parallel Data bit 14  |
| <b>A19</b>                    | CLKOUT                   | Clock Output  |
| <b>B19</b>                    | GPIO1                    | General Purpose I/O bit 1   |
| <b>C19</b>                    | PAR_D15                  | Parallel Data bit 15  |
| <b>A20, B20, C20</b>          | DGND                     | Digital Ground  |
| <b>A21-26, B21-26, C21-26</b> | AGND                     | Analog Ground   |
| <b>A27, C27</b>               | +VarA                    | Variable Analog Power Supply. See Power Supply section for further details.                   |
| <b>B27</b>                    | AGND                     | Analog Ground   |
| <b>A28</b>                    | N/C                      | No Connect. Do not use this pin.  |
| <b>B28</b>                    | AGND                     | Analog Ground   |
| <b>C28</b>                    | N/C                      | No Connect. Do not use this pin.  |
| <b>A29, B29, C29</b>          | AGND                     | Analog Ground   |
| <b>A30</b>                    | -12VA                    | -12V Analog Power Supply. See Power Supply section for further details.                       |
| <b>B30</b>                    | AGND                     | Analog Ground   |
| <b>C30</b>                    | +12VA                    | +12V Analog Power Supply. See Power Supply section for further details.                       |
| <b>A31, B31, C31</b>          | -5VA (AV <sub>SS</sub> ) | -5V Analog Power Supply. See Power Supply section for further details.                        |
| <b>A32, B32, C32</b>          | +5VA (AV <sub>DD</sub> ) | +5V Analog Power Supply. See Power Supply section for further details.                        |

**J7 – ANALOG POWER CONNECTOR**

If any analog power supplies are required on boards connected to the CED1 via any connector other than the J3 (96-way), they can be taken from this pin header. Pin-out details of this connector are given in Table 3. Further details of the power supplies are given in the following section.



Figure 5. Analog Power Connector Pin Locations

**Table 3. Analog Power Connector pin-out**

| Pin No  | Function   | Description  |
|---------|------------|--|
| 1       | +12VA_Edge | +12V Analog Supply   |
| 2       | -12VA_Edge | -12V Analog Supply   |
| 3, 6, 8 | AGND       | Analog Ground  |
| 4       | +5VA_Edge  | +5V Analog Supply  |
| 5       | -5VA_Edge  | -5V Analog Supply  |
| 7       | +VarA      | Variable Voltage Analog Supply. See Power Supply Section for more details. |

**J12 – SPORT INTERFACE**

This standard two row, 0.1-inch connector can be used to connect any daughter board that utilizes the SPORT interface. This connector also contains all the SPI and Two Wire Interface (TWI) signals as well as 5V, 3.3V and the +7V CED board supply. See Table 4 for details. The pin-out of this connector is compatible with the Blackfin Stamp and Ez-Kit SPORT connector. More information on the pin names is given in the section detailing the 96-way connector.

**Table 4. SPORT Connector Pin out**

|                     |    |    |                       |
|---------------------|----|----|-----------------------|
| +5VD_Edge           | 1  | 2  | +7V                   |
| DGND                | 3  | 4  | N/C (Keying Pin)      |
| RESET               | 5  | 6  | SPORT_TSClk0/SPI_SEL5 |
| SPORT_RFS0/SPI_SEL3 | 7  | 8  | SPORT_DR0PRI/SPI_SEL4 |
| DGND                | 9  | 10 | SPORT_DR0SEC          |
| SPORT_TFS0/SPI_SEL6 | 11 | 12 | SPORT_DT0SEC          |
| +3.3VD_Edge         | 13 | 14 | SPORT_DT0PRI/SPI_SEL7 |
| +3.3VD_Edge         | 15 | 16 | SPORT_RSCLk0/SPI_SEL2 |
| SPI_SS              | 17 | 18 | SPI_MOSI              |
| SPI_SEL1            | 19 | 20 | SPI_MISO              |
| SPI_SEL2            | 21 | 22 | SPI_CLK               |
| SPI_SEL3            | 23 | 24 | TWI_SDA               |
| SPI_SEL4            | 25 | 26 | TWI_SCK               |
| SPI_SEL5            | 27 | 28 | RXINT/GPIO2/PPI_FS3   |
| SPI_SEL6            | 29 | 30 | GPIO3/TMR1/PPI_FS1    |
| SPI_SEL7            | 31 | 32 | TMR0/PPI_FS2          |
| DGND                | 33 | 34 | DGND                  |



### J13 – SPI INTERFACE

Using the SPI connector instead of the SPORT should only be considered when the user is satisfied that the device being connected is completely compatible with the SPI specification. This implies that only 8- or 16-bit active low framing is required. See Table 5 for pin-out details of this connector. This connector is compatible with the SPI connector on the Blackfin Stamp and Ez-Kits. More information on the pin names is given in the section detailing the 96-way connector.

**Table 5. SPI Connector Pin out**

|                  |    |    |             |
|------------------|----|----|-------------|
| +5VD_Edge        | 1  | 2  | +3.3VD_Edge |
| +5VD_Edge        | 3  | 4  | +3.3VD_Edge |
| SPI_MOSI         | 5  | 6  | SPI_MISO    |
| RESET            | 7  | 8  | SPI_CLK     |
| SPI_SEL1         | 9  | 10 | SPI_SS      |
| SPI_SEL3         | 11 | 12 | SPI_SEL2    |
| SPI_SEL5         | 13 | 14 | SPI_SEL4    |
| SPI_SEL7         | 15 | 16 | SPI_SEL6    |
| N/C (Keying Pin) | 17 | 18 | DGND        |
| +7V              | 19 | 20 | DGND        |

### J14 – PPI INTERFACE

This connector is intended to allow attachment of daughter boards designed to connect to the PPI Connector on the Blackfin Stamp and Ez-Kit. However, with the signals provided, it should be possible to connect to most parallel interface devices needing up to 16 data bits and multiple control signals.

The inclusion of the SPI signals on this connector allows for separate data and configuration interfaces if required. See Table 6 for details of this connector. More information on the pin names is given in the section detailing the 96-way connector.

**Table 6. PPI Connector Pin out**

|                     |    |    |                  |
|---------------------|----|----|------------------|
| +5VD_Edge           | 1  | 2  | +7V              |
| +5VD_Edge           | 3  | 4  | N/C (Keying Pin) |
| +3.3VD_Edge         | 5  | 6  | CLKOUTP_EXT      |
| +3.3VD_Edge         | 7  | 8  | PAR_D0           |
| PAR_D1              | 9  | 10 | PAR_D2           |
| PAR_D3              | 11 | 12 | PAR_D4           |
| PAR_D5              | 13 | 14 | PAR_D6           |
| PAR_D7              | 15 | 16 | PAR_D8           |
| PAR_D9              | 17 | 18 | PAR_D10          |
| PAR_D11             | 19 | 20 | PAR_D12          |
| PAR_D13             | 21 | 22 | PAR_D14          |
| PAR_D15             | 23 | 24 | SPI_SEL3         |
| SPI_SEL2            | 25 | 26 | SPI_SEL1         |
| SPI_SS              | 27 | 28 | RESET            |
| RxInt/GPIO2/PPI_FS3 | 29 | 30 | SPI_MOSI         |
| GPIO3/TMR1/PPI_FS1  | 31 | 32 | SPI_MISO         |
| TMR0/PPI_FS2        | 33 | 34 | SPI_CLK          |
| DGND                | 35 | 36 | TWI_SDA          |
| DGND                | 37 | 38 | TWI_SCK          |
| DGND                | 39 | 40 | DGND             |

### CONNECTOR PART NUMBERS

**Table 7. Connector Part Numbers**

| Ref. Des. | Description                              | Manufacturer       | Part Number      | Mating Connector          |
|-----------|--|--------------------|------------------|---------------------------|
| J1        | USB Mini-B connector                     | Molex              | 565790576        | Standard Mini-B USB Cable |
| J2        | 2-pin screw terminal                     | Camden Electronics | CTB5000/2        | Cables inserted directly  |
| J3        | 96-Way 90° DIN41612 socket               | Harting            | 0973 296 6801    | 0903 196 6921             |
| J4        | DC Barrel connector, 2mm centre          | Kycon              | KLDX-SMT2-0202-A | Cliff - DCPPI (FC68147)   |
| J5        | LVDS connector                           | Tyco Electronics   | 1469028-1        | 1469169-1                 |
| J6        | 10-Pin, 2 row standard 0.1" pitch header | Harwin             | M20-8760542      | M20-7830546               |
| J8-10     | 90-way Micro-strip Terminal              | Samtec             | TFC-145-X2-FD-A  | SFC-145-T2-FD-A           |
| J12       | 34-Pin, 2 row standard 0.1" pitch header | Harwin             | M20-8761742      | M20-7831746               |
| J13       | 20-Pin, 2 row standard 0.1" pitch header | Harwin             | M20-8761042      | M20-7831046               |
| J14       | 40-Pin, 2 row standard 0.1" pitch header | Harwin             | M20-8762042      | M20-7832046               |

**POWER SUPPLIES**

The CED board provides multiple power supplies that are made available for use with connected boards. A single 7V supply is required for the CED board and this is used to power the board itself and the supplies for boards connected to it. A resettable 2A fuse limits the current that can be drawn from the supply thus limiting the power consumption of the CED and any attached boards.

On it's own without any converter boards attached, the idle current of the CED is approximately 220 mA. When accessing SRAM for example, the current drawn by the CED board itself can increase significantly. Users designing boards to operate with the CED that wish to use the supplies provided must bear in mind the total available power when calculating their power requirements.

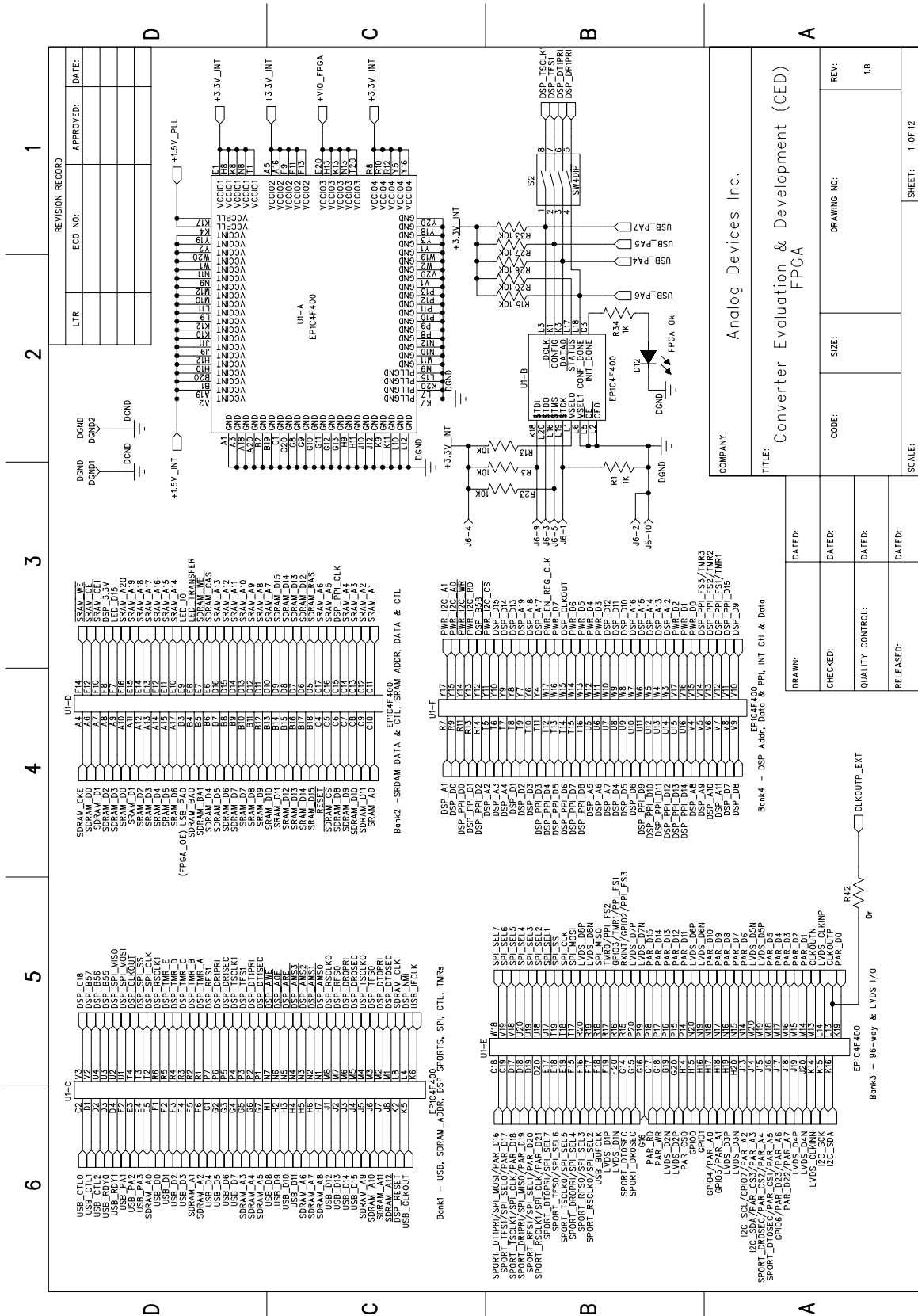
While the supplies generated on the CED are kept as clean as possible, designers of boards connected to the CED must ensure that all devices and supplies are adequately decoupled. This will prevent noise being fed back onto the power supplies of the CED. Excessive noise introduced on to the power supplies may cause the CED or attached boards to malfunction.

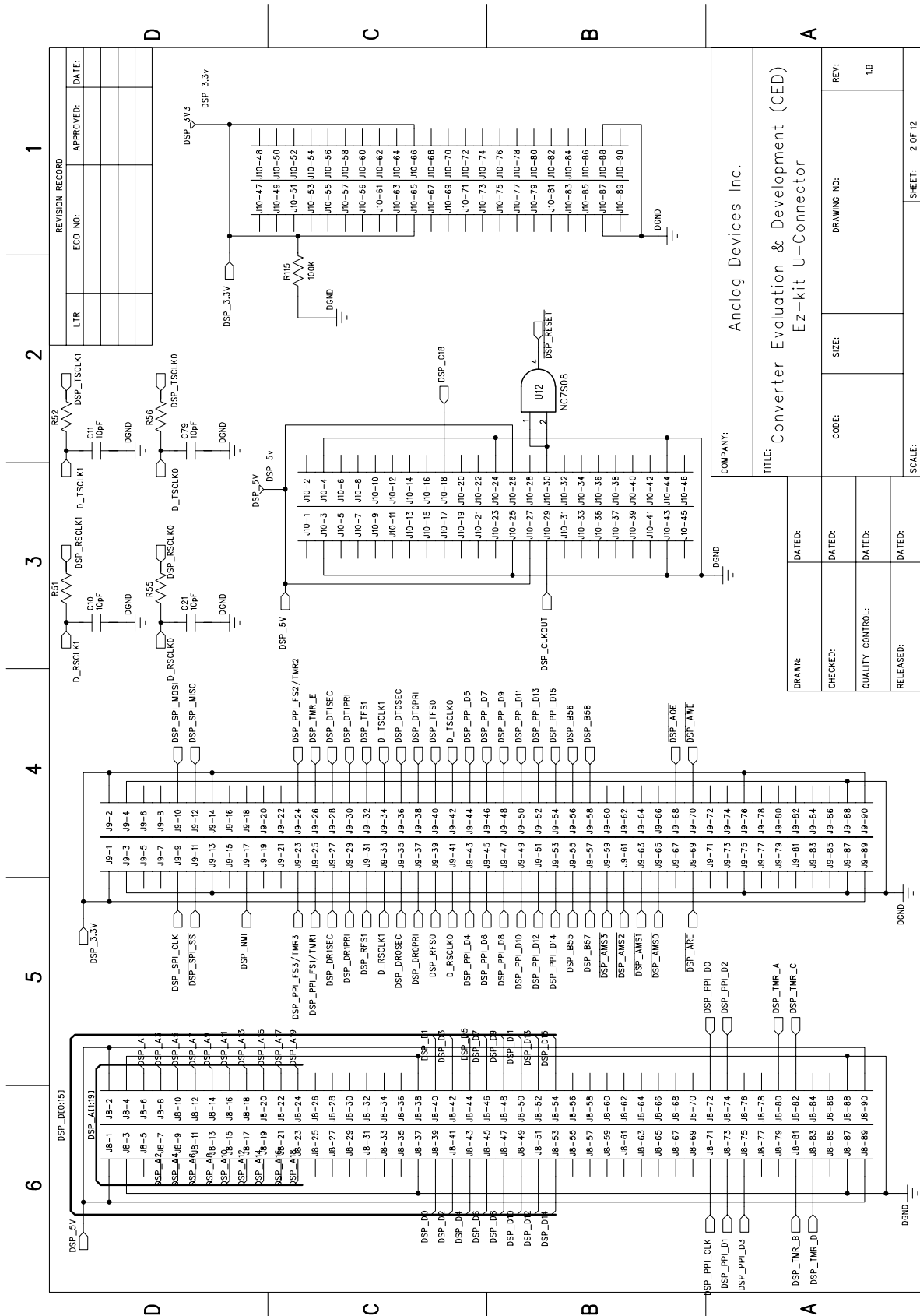
The voltage and current ratings of the supplies listed in Table 8 are defined to be absolute maximum limits. While fuses and thermal overload protection have been provided in the power supply circuitry, attempting to draw more current from a particular supply or exceeding the total power available from a combination of supplies may cause damage to the CED board.

**Table 8. Power Supplies**

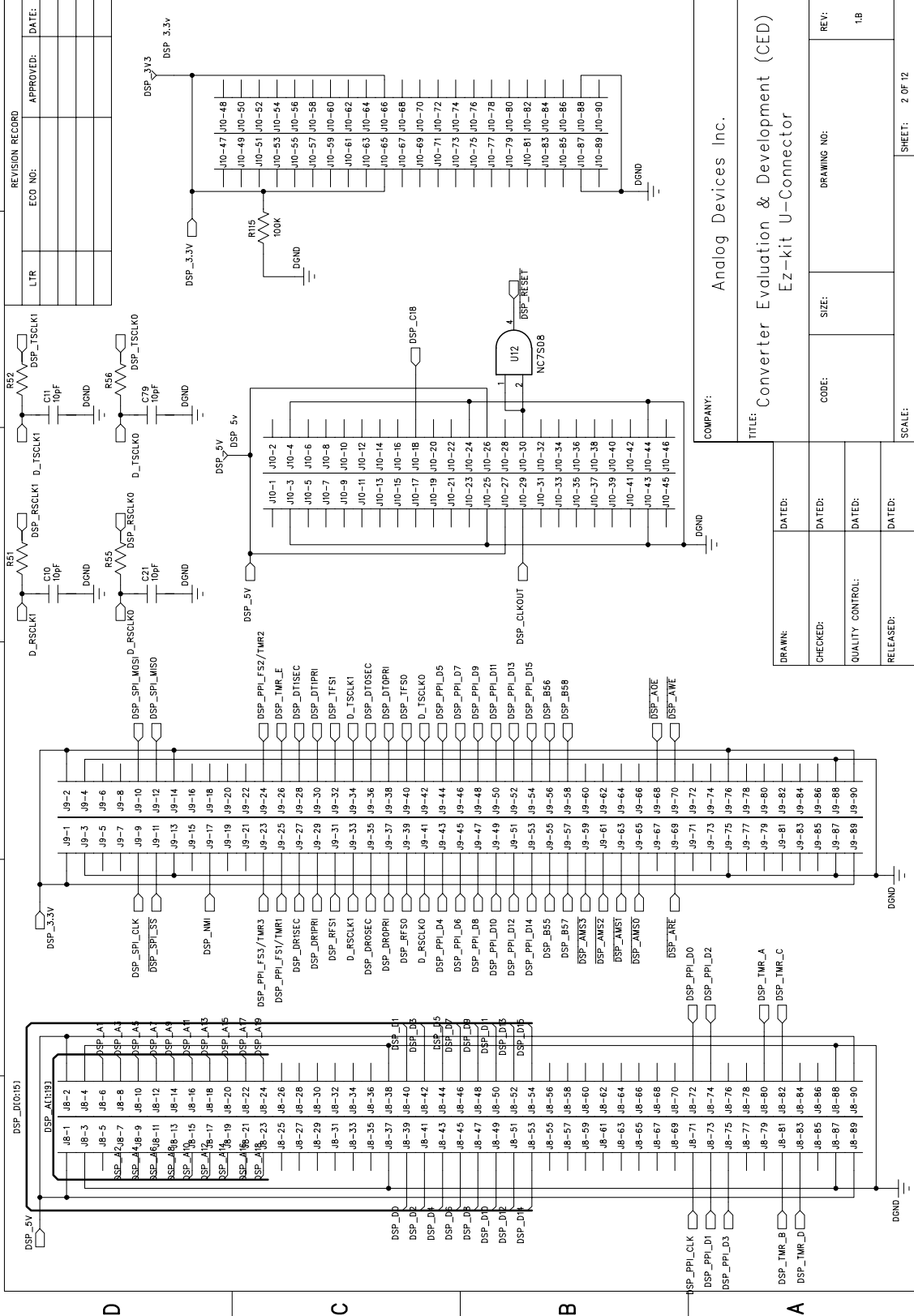
| <b>Name</b> | <b>Voltage</b> | <b>Max. Current</b> | <b>Test Conditions / Comments</b>   |
|-------------|----------------|---------------------|---|
| +VarA       | +1.5V to +5.5V | 300mA               | Regulation may suffer at lower voltages.  |
| -12VA       | -12V ±5%       | 100mA               | Fuse limited at 100mA.  |
| +12VA       | +12V ±5%       | 100mA               | Fuse limited at 100mA.  |
| -5VA        | -5V ±5%        | 100mA               | Fuse limited at 100mA.  |
| +5VA        | +5V ±5%        | 500mA               | Regulator rated for 500mA but thermally limited.  |
| +5VD        | +5V ±5%        | 500mA               | Regulator rated for 500mA but thermally limited.  |
| +3.3VD      | +3.3V ±5%      | 300mA               | Thermally limited.  |
| +VarD       | +1.5V to +5.5V | 300mA               | Regulation may suffer at lower voltages.  |
| +7V         | +7V ±5%        | 2A                  | Total current that can be drawn through board including all other supplies. Fuse limited. |

SCHEMATICS



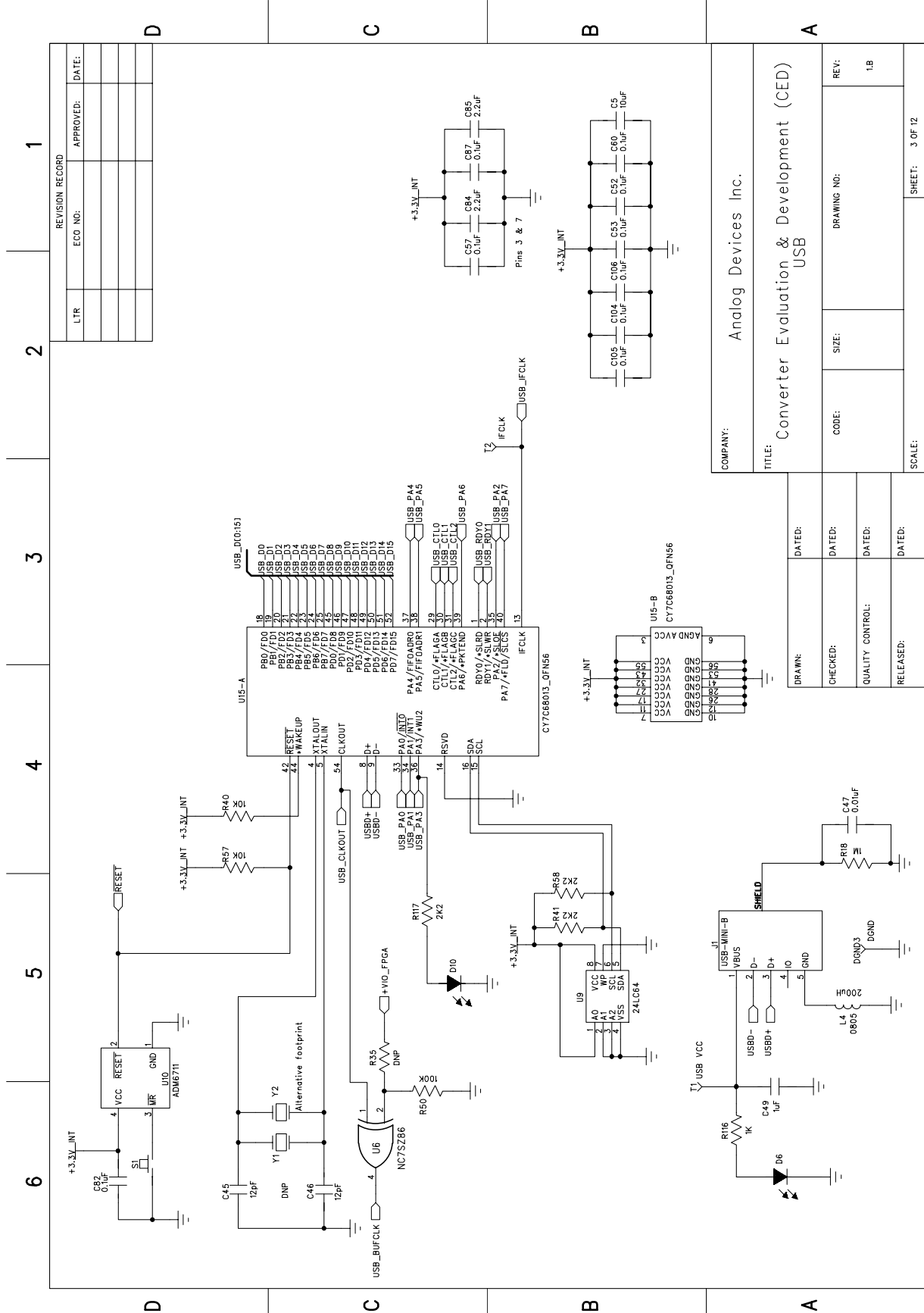


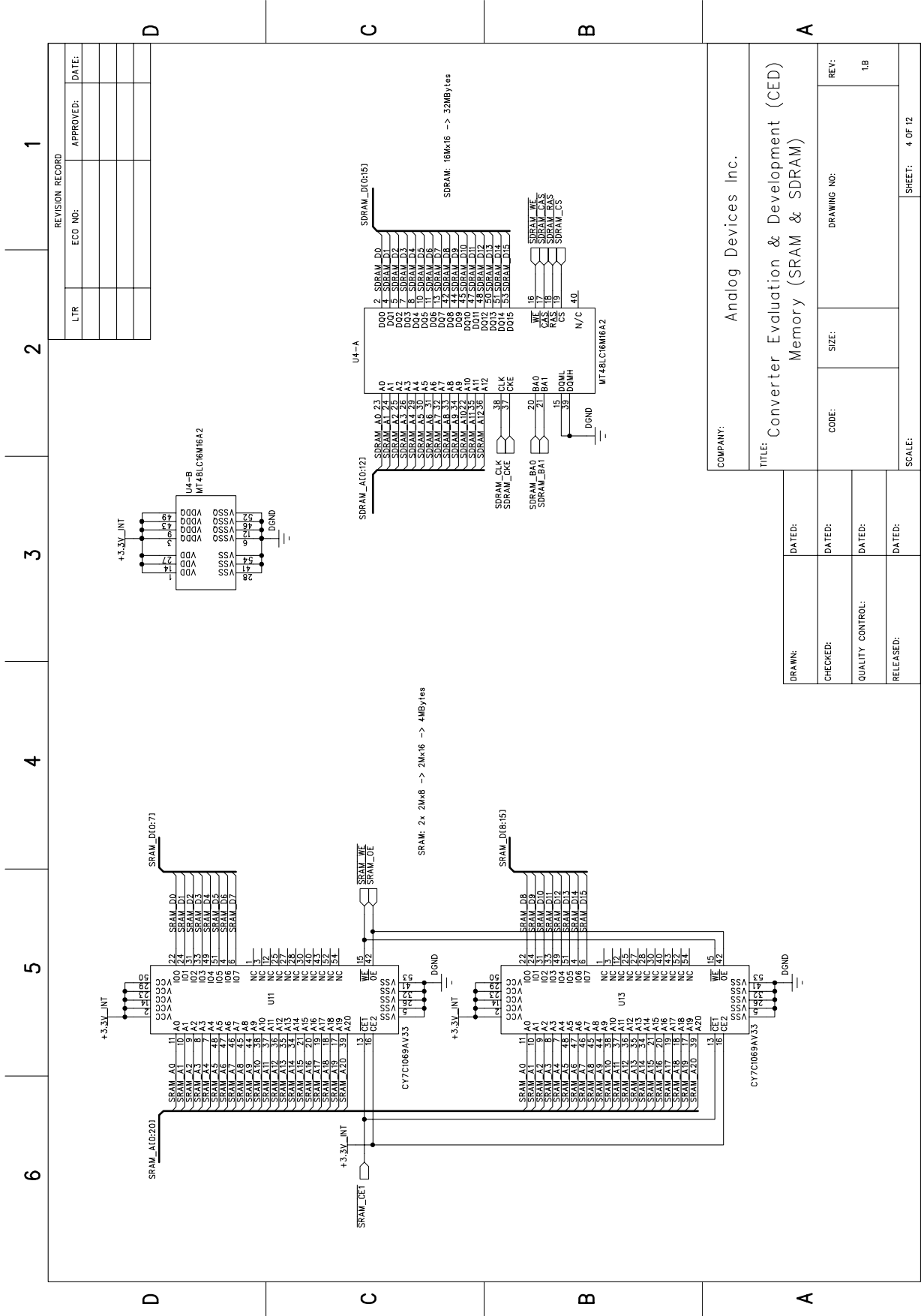
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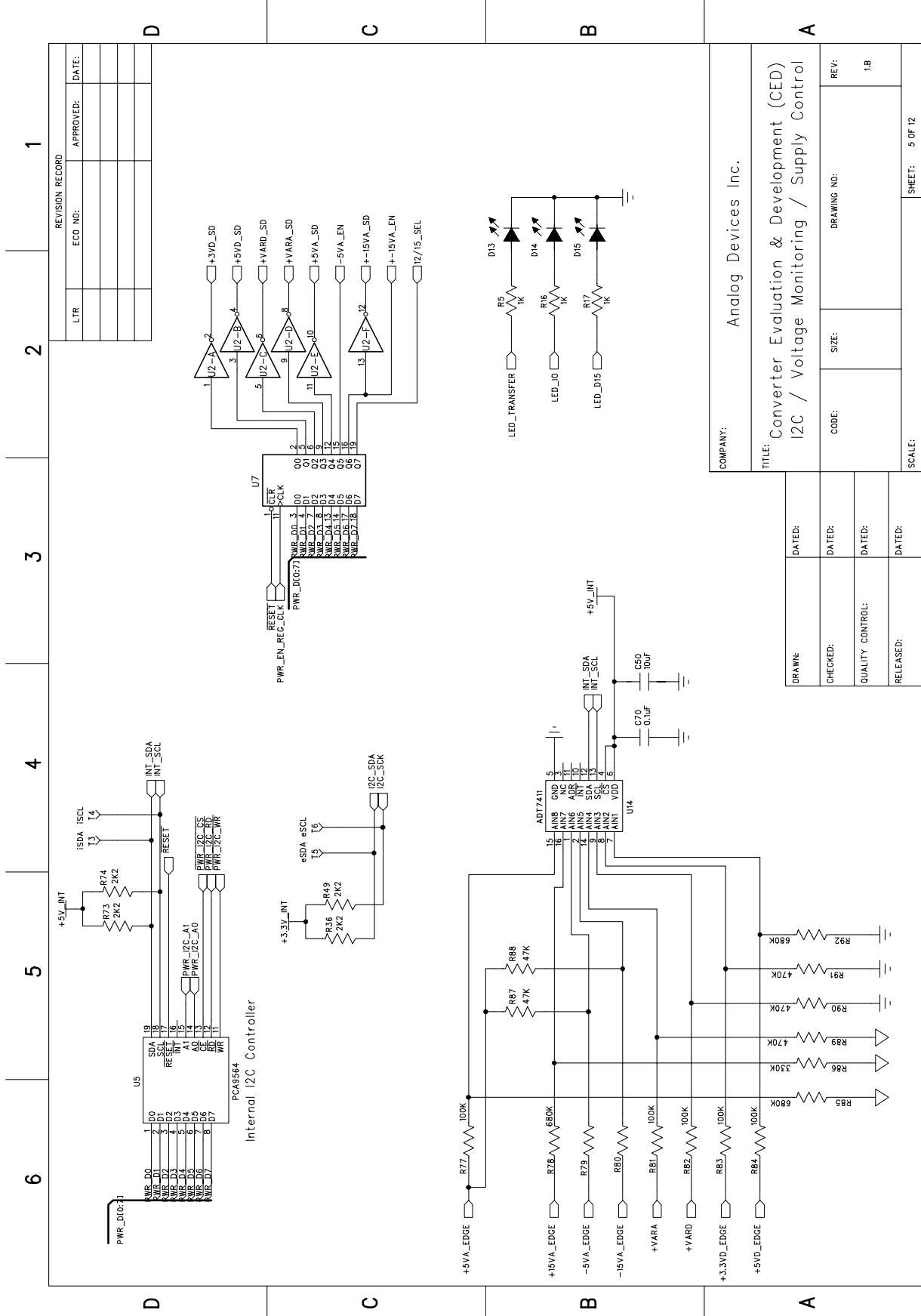
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| DRAWN:           |       | COMPANY:    | ANALOG DEVICES INC.                      |
| CHECKED:         | DATE: | TITLE:      | Converter Evaluation & Development (CED) |
| QUALITY CONTROL: | DATE: | DRAWING NO: |  |
| RELEASED:        | DATE: | SCALE:      |  |
|                  |       | REV:        | 1.B                                      |
|                  |       | SHEET:      | 2 OF 12                                  |





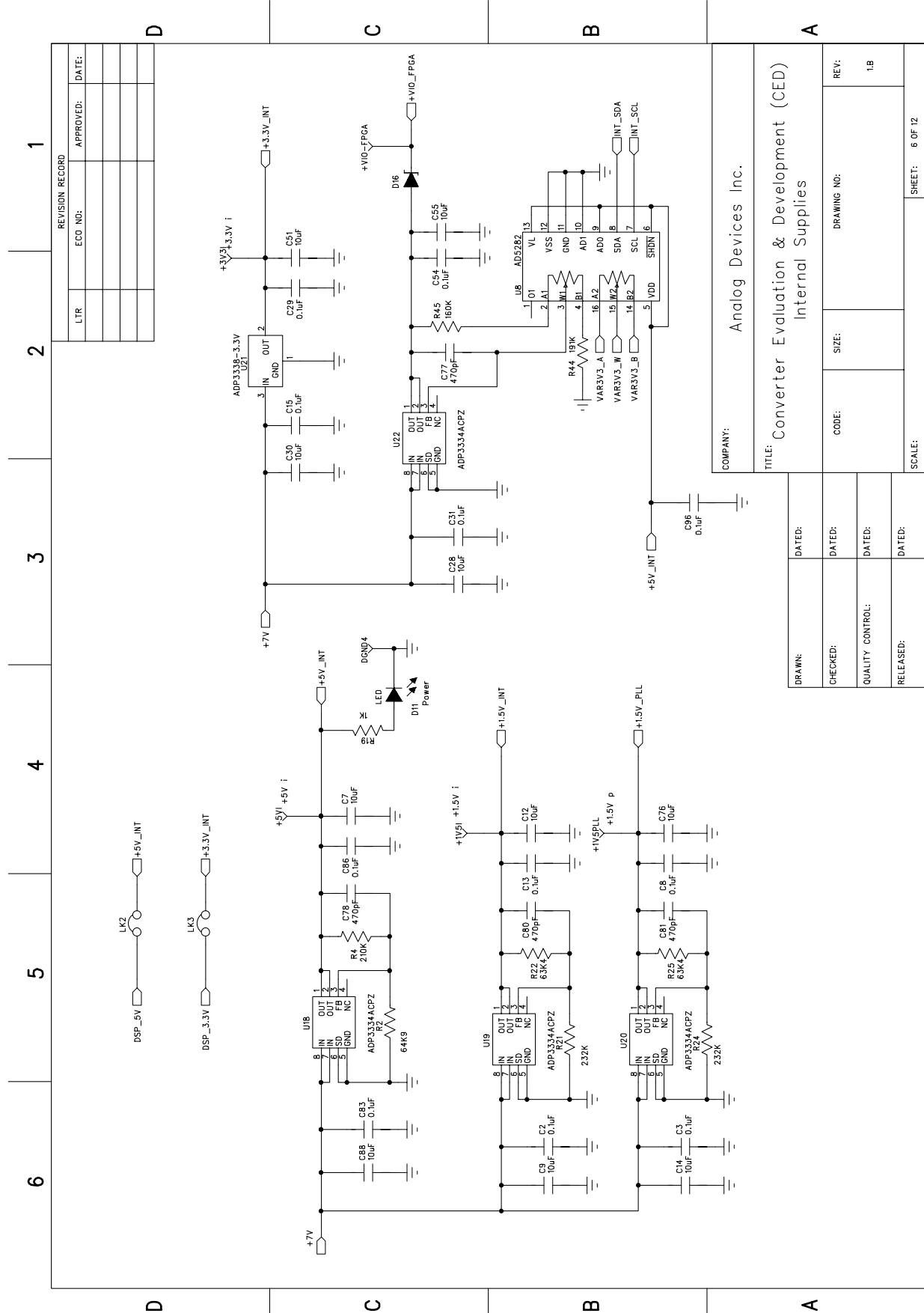
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|---|--------|---------------------|----------------|
| COMPANY:  |        | Analog Devices Inc. |                |
| TITLE: Converter Evaluation & Development (CED) Memory (SRAM & SDRAM) |        |                     |                |
| DRAWN:  | DATED: | CODE:               | SIZE:          |
| CHECKED:  | DATED: | DRAWING NO:         | REV:           |
| QUALITY CONTROL:  | DATED: |                     | 1.8            |
| RELEASED:   | DATED: | SCALE:              | SHEET: 4 OF 12 |



| REVISION RECORD |         |                 |
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| LTR             | ECO NO. | APPROVED: DATE: |
|                 |         |                 |
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|  |                |
|--|----------------|
| COMPANY: Analog Devices Inc.   |                |
| TITLE: Converter Evaluation & Development (CED)<br>I2C / Voltage Monitoring / Supply Control |                |
| CODE:  | DRAWING NO:    |
| SIZE:  | REV: 1.1B      |
| SCALE:   | SHEET: 5 OF 12 |

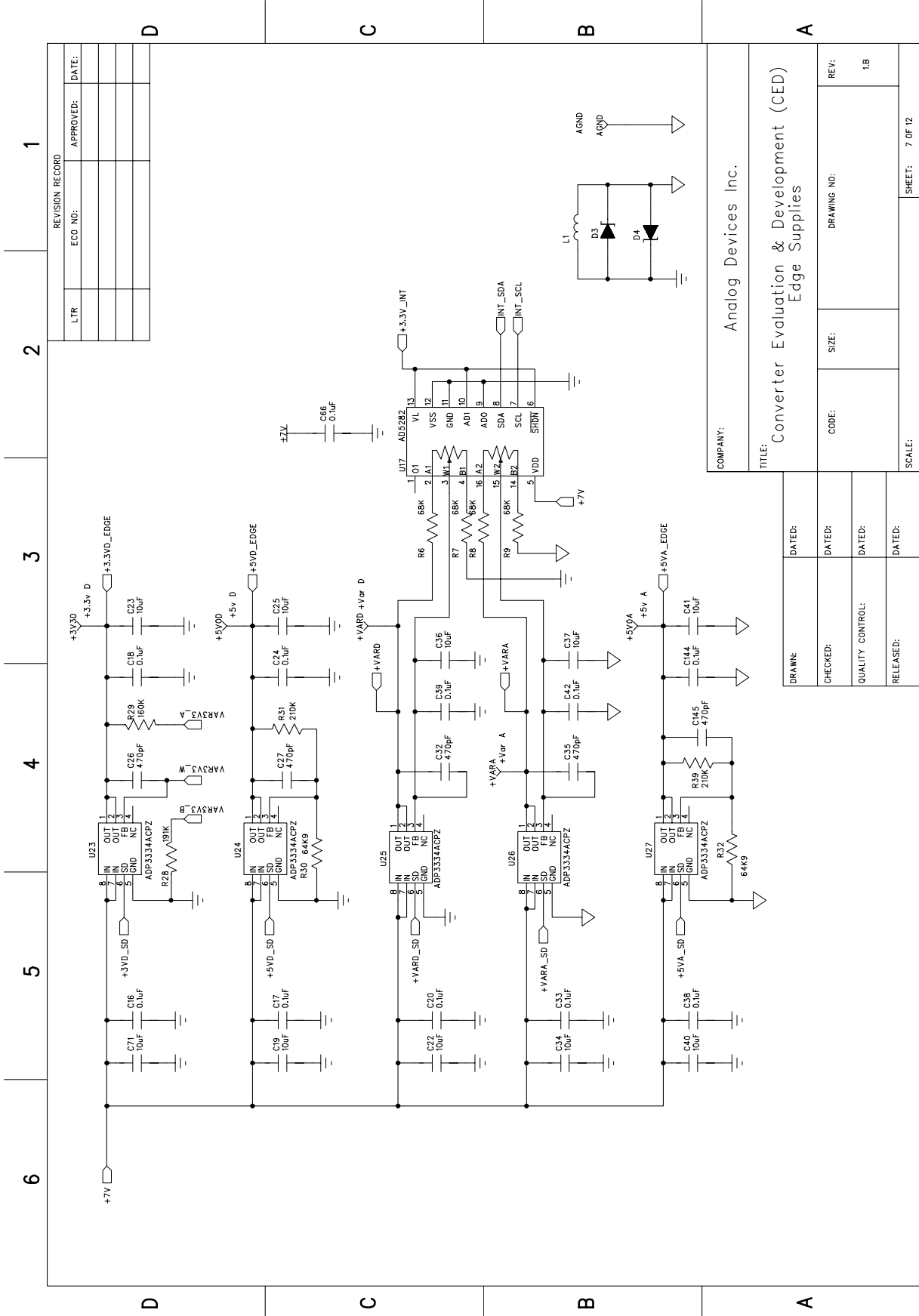
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| CHECKED:         | DATE: |
| QUALITY CONTROL: | DATE: |
| RELEASED:        | DATE: |



| REVISION RECORD |                 |
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| LTR             | APPROVED: DATE: |
| ECCO NO:        |                 |
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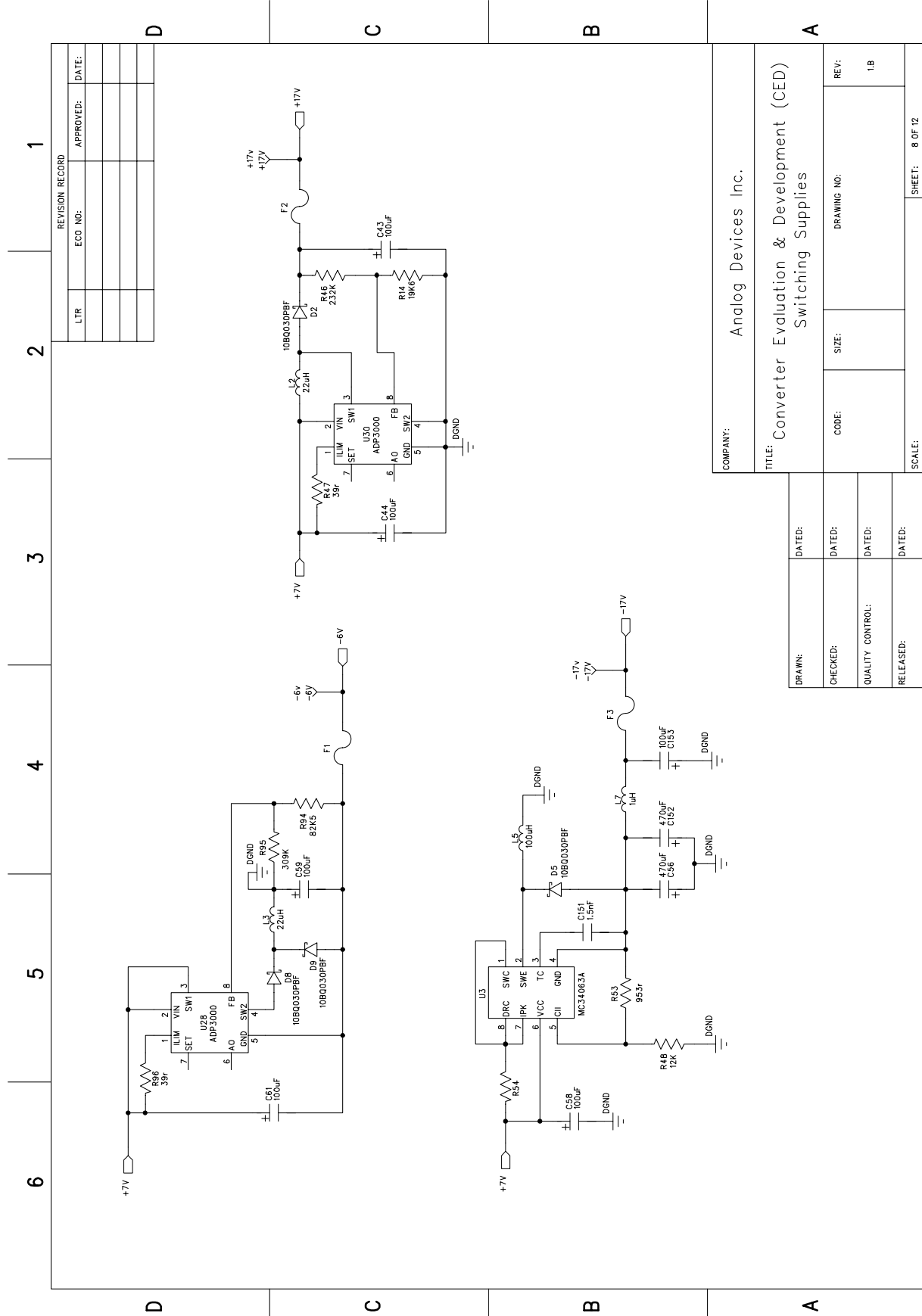
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| COMPANY: Analog Devices Inc.                                      |                |
| TITLE: Converter Evaluation & Development (CED) Internal Supplies |                |
| DRAWN:  | DATED:         |
| CHECKED:  | DATED:         |
| QUALITY CONTROL:  | DATED:         |
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| DRAWING NO:   | REV: 1B        |
| SCALE:  | SHEET: 6 OF 12 |

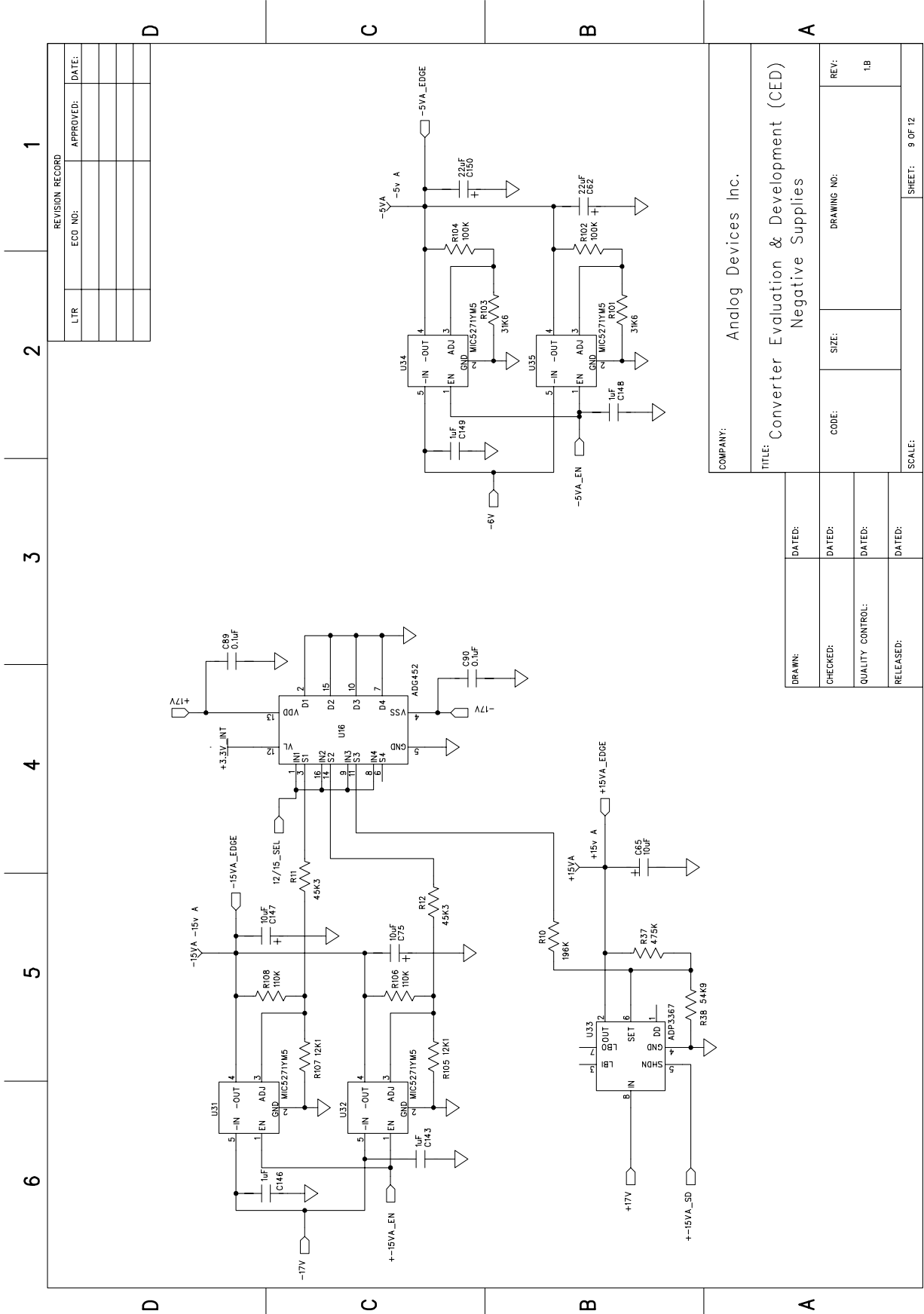




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| LTR             | ECO NO. | APPROVED: DATE: |
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|---|----------------|
| COMPANY: Analog Devices Inc.                                  |                |
| TITLE: Converter Evaluation & Development (CED) Edge Supplies |                |
| DRAWN:  | DATED:         |
| CHECKED:  | DATED:         |
| QUALITY CONTROL:  | DATED:         |
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| SCALE:  | SHEET: 7 OF 12 |

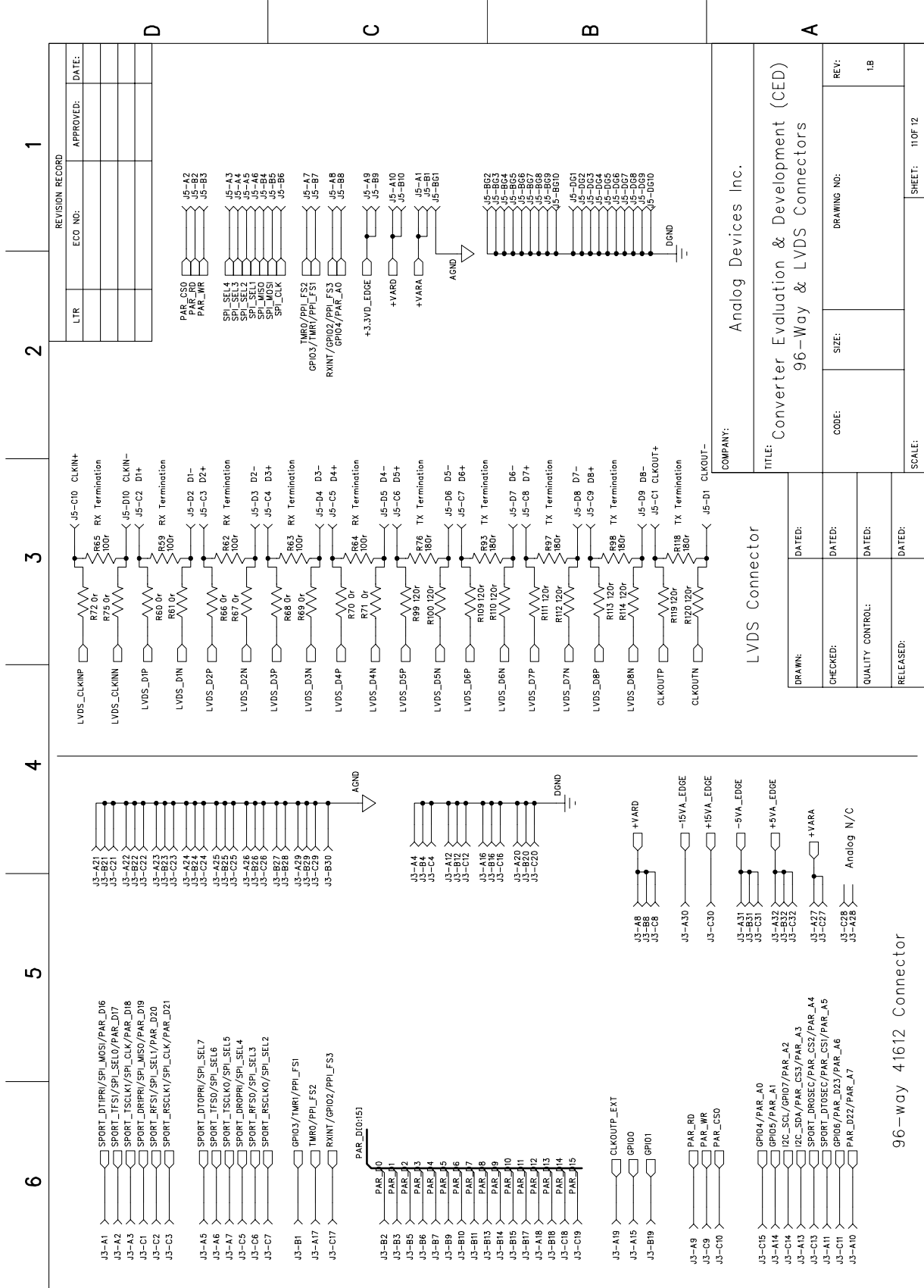




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|   |                |
|---|----------------|
| COMPANY: Analog Devices Inc.                                      |                |
| TITLE: Converter Evaluation & Development (CED) Negative Supplies |                |
| DRAWN:  | DATED:         |
| CHECKED:  | DATED:         |
| QUALITY CONTROL:  | DATED:         |
| RELEASED:   | DATED:         |
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| DRAWING NO:   | REV: 1B        |
| SCALE:  | SHEET: 9 OF 12 |





REVISION RECORD

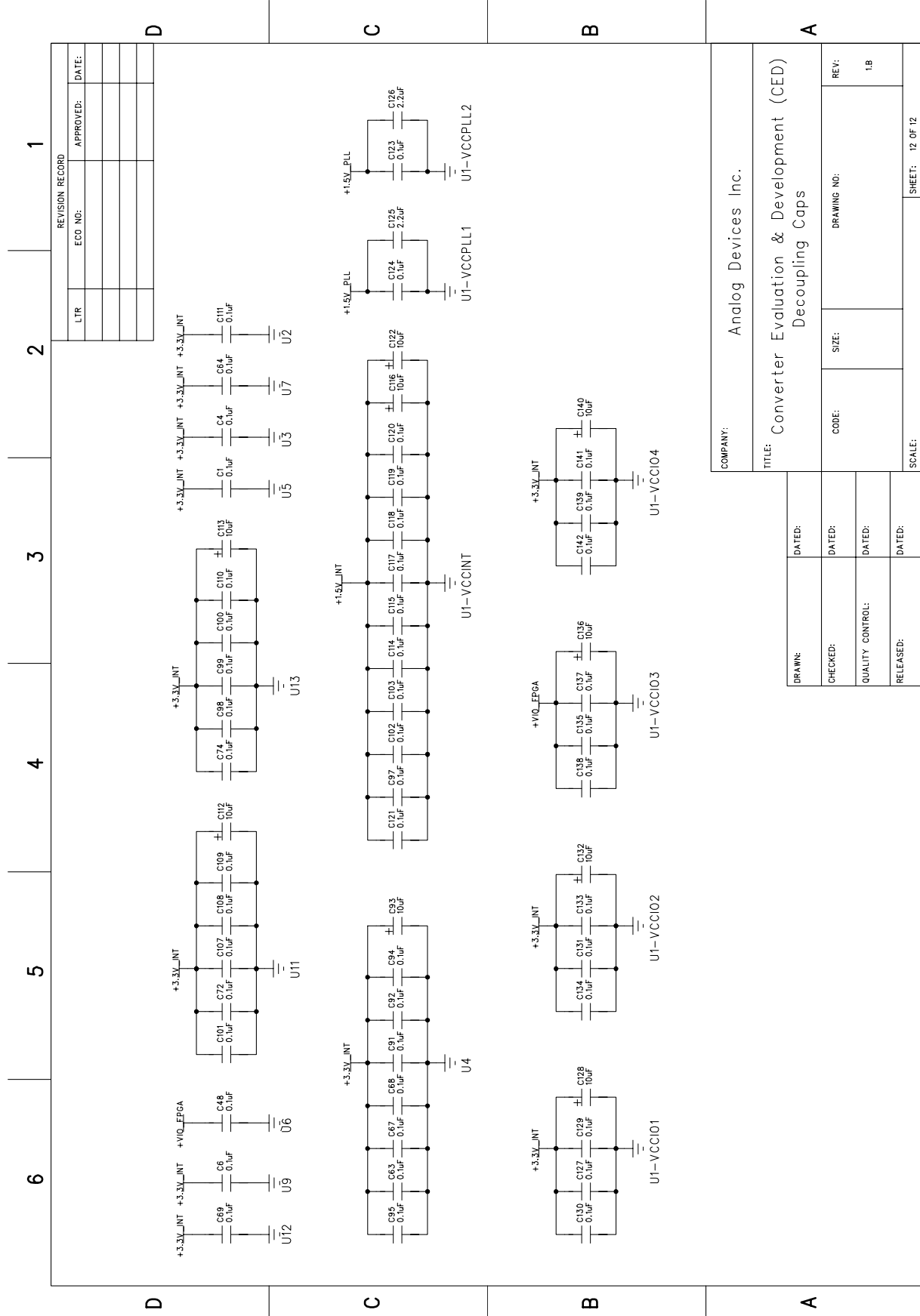
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|-----|---------|-----------|-------|
|     |         |           |       |

COMPANY: Analog Devices Inc.

TITLE: Converter Evaluation & Development (CED)  
96-Way & LVDS Connectors

|                  |       |       |       |             |      |
|------------------|-------|-------|-------|-------------|------|
| DRAWN:           | DATE: | CODE: | SIZE: | DRAWING NO: | REV: |
| CHECKED:         | DATE: |       |       |             | 1.B  |
| QUALITY CONTROL: | DATE: |       |       |             |      |
| RELEASED:        | DATE: |       |       |             |      |

SCALE: SHEET: 11 OF 12





Ordering Information

**ORDERING GUIDE**

| <b>Model</b>            | <b>Description</b>                         |
|-------------------------|--|
| EVAL-CED1Z <sup>1</sup> | Converter Evaluation and Development Board |

<sup>1</sup> Z = RoHS Compliant Part.

**ESD CAUTION**



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.