

FEATURES

- 16-element FIFO for event recording**
- 10 configurable I/Os allowing functions such as**
 - Key pad decoding for a matrix of up to 5 × 5**
 - 11 GPIOs (5 × 6) with ADP5585ACxZ-01-R7 models**
- Key press/release interrupts**
- GPIO functions**
- GPI with selectable interrupt level**
- 100 kΩ or 300 kΩ pull-up resistors**
- 300 kΩ pull-down resistors**
- GPO with push-pull or open-drain**
- Programmable logic block**
- PWM generator**
 - Internal PWM generation**
 - External PWM with internal PWM AND function**
- Reset generators**
- I²C interface with fast mode plus (Fm+) support of up to 1 MHz**
- Open-drain interrupt output**
- 16-ball WLCSP, 1.59 mm × 1.59 mm**
- 16-lead LFCSP, 3 mm × 3 mm**

APPLICATIONS

- Keypad entries and input/output expansion capabilities**
- Smart phones, remote controls, and cameras**
- Healthcare, industrial, and instrumentation**

GENERAL DESCRIPTION

The ADP5585 is a 10 input/output port expander with a built in keypad matrix decoder, programmable logic, reset generator, and PWM generator. Input/output expander ICs are used in portable devices (phones, remote controls, and cameras) and nonportable applications (healthcare, industrial, and instrumentation). I/O expanders can be used to increase the number of I/Os available to a processor or to reduce the number of I/Os required through interface connectors for front panel designs.

The ADP5585 handles all key scanning and decoding and can flag the main processor via an interrupt line that new key events have occurred. GPI changes and logic changes can also be tracked

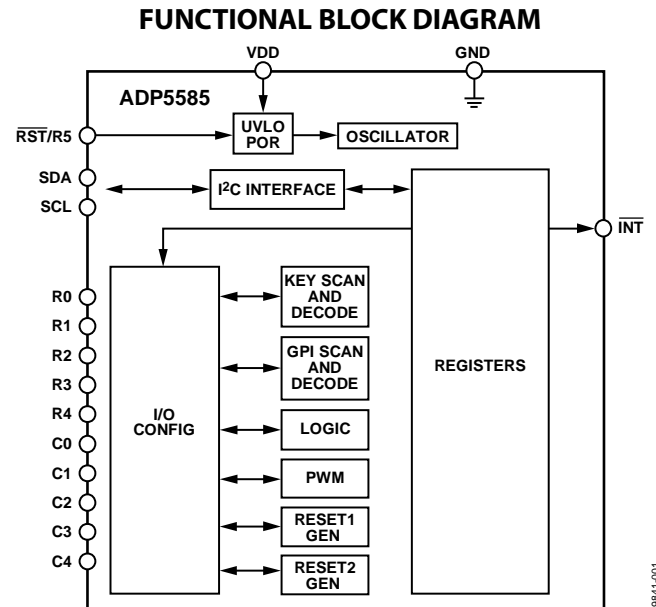


Figure 1.

as events via the FIFO, eliminating the need to monitor different registers for event changes. The ADP5585 is equipped with a FIFO to store up to 16 events. Events can be read back by the processor via an I²C-compatible interface.

The ADP5585 frees up the main processor from having to monitor the keypad, thereby reducing power consumption and/or increasing processor bandwidth for performing other functions.

The programmable logic functions allow common logic requirements to be integrated as part of the GPIO expander, thus saving board area and cost.

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REVISION HISTORY

1/13—Rev. B to Rev. C

| | |
|--|----|
| Changes to Detailed Register Description Section | 19 |
| Changes to Table 31 and Table 32 | 24 |
| Changes to Table 33, Table 34, and Table 35 | 25 |
| Changes to Table 37 | 26 |
| Changes to Table 39 | 27 |
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7/12—Rev. A to Rev B

| | |
|----------------------------------|----|
| Changes to Table 5 | 8 |
| Updated Outline Dimensions | 36 |
| Changes to Ordering Guide | 37 |

10/11—Rev. Sp0 to Rev. A

| | |
|--|-----------|
| Added 16-Lead LFCSP_WQ Package | Universal |
| Changes to Features Section | 1 |
| Added Figure 4; Renumbered Sequentially | 6 |
| Changes to Table 4 | 6 |
| Changes to Device Enable Section and Table 5 | 8 |
| Change to General Section | 11 |
| Changes to Logic Blocks Section | 12 |
| Changes to PWM Block Section | 13 |
| Changes to Interrupts Section | 14 |
| Changes to Register Interface Section | 15 |
| Changes to Figure 27 | 35 |
| Updated Outline Dimensions | 36 |
| Changes to Ordering Guide | 38 |

5/11—Revision Sp0: Initial Version

SPECIFICATIONS

VDD = 1.8 V to 3.3 V, T_A = T_J = -40°C to +85°C, unless otherwise noted¹.

Table 1.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|--|----------------------|---|---------|------|---------|------|
| SUPPLY VOLTAGE | | | | | | |
| VDD Input Voltage Range | VDD | | 1.65 | | 3.6 | V |
| Undervoltage Lockout Threshold | UVLO _{VDD} | UVLO active, VDD falling | 1.2 | 1.3 | | V |
| | | UVLO inactive, VDD rising | | 1.4 | 1.6 | V |
| SUPPLY CURRENT | | | | | | |
| Standby Current | I _{STBY} | VDD = 1.65 V | | 1 | 4 | μA |
| | | VDD = 3.3 V | | 1 | 10 | μA |
| Operating Current (One Key Press) | I _{SCAN1} | Scan = 10 ms, CORE_FREQ = 50 kHz, scan active, 300 kΩ pull-up, VDD = 1.65 V | | 30 | 40 | μA |
| | I _{SCAN2} | Scan = 10 ms, CORE_FREQ = 50 kHz, scan active, 100 kΩ pull-up, VDD = 1.65 V | | 35 | 45 | μA |
| | I _{SCAN3} | Scan = 10 ms, CORE_FREQ = 50 kHz, scan active, 300 kΩ pull-up, VDD = 3.3 V | | 75 | 85 | μA |
| | I _{SCAN4} | Scan = 10 ms, CORE_FREQ = 50 kHz, scan active, 100 kΩ pull-up, VDD = 3.3 V | | 80 | 90 | μA |
| PULL-UP, PULL-DOWN RESISTANCE | | | | | | |
| Pull-Up | | | | | | |
| Option 1 | | | 50 | 100 | 150 | kΩ |
| Option 2 | | | 150 | 300 | 450 | kΩ |
| Pull-Down | | | 150 | 300 | 450 | kΩ |
| INPUT LOGIC LEVEL (RST, SCL, SDA, R0, R1, R2, R3, R4, R5, C0, C1, C2, C3, C4) | | | | | | |
| Input Voltage | | | | | | |
| Logic Low | V _{IL} | | | | 0.3 VDD | V |
| Logic High | V _{IH} | | 0.7 VDD | | | V |
| Input Leakage Current (Per Pin) | V _{I-Leak} | | | 0.1 | 1 | μA |
| PUSH-PULL OUTPUT LOGIC LEVEL (R0, R1, R2, R3, R4, R5, C0, C1, C2, C3, C4) | | | | | | |
| Output Voltage | | | | | | |
| Logic Low | V _{OL1} | Sink current = 10 mA, maximum of five GPIOs active simultaneously | | | 0.4 | V |
| | V _{OL2} | Sink current = 10 mA, all GPIOs active simultaneously | | | 0.5 | V |
| Logic High | V _{OH} | Source current = 5 mA | 0.7 VDD | | | V |
| Logic High Leakage Current (Per Pin) | V _{OH-Leak} | | | 0.1 | 1 | μA |
| OPEN-DRAIN OUTPUT LOGIC LEVEL (INT, SDA) | | | | | | |
| Output Voltage | | | | | | |
| Logic Low | | | | | | |
| INT | V _{OL3} | I _{SINK} = 10 mA | | | 0.4 | V |
| SDA | V _{OL4} | I _{SINK} = 20 mA | | | 0.4 | V |
| Logic High Leakage Current (Per Pin) | V _{OH-Leak} | | | 0.1 | 1 | μA |
| Logic Propagation Delay | | | | 125 | 300 | ns |
| FF Hold Time ² | | | | 0 | | ns |
| FF Setup Time ² | | | | 175 | | ns |
| GPIO Debounce ² | | | | | 70 | μs |
| Internal Oscillator Frequency ³ | OSC _{FREQ} | | 900 | 1000 | 1100 | kHz |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|-----------------------------|--------------------------|------|-----|------|------|
| I²C TIMING SPECIFICATIONS | | | | | | |
| Delay from UVLO/Reset Inactive to I ² C Access | | | | | 60 | μs |
| SCL Clock Frequency | f _{SCL} | | 0 | | 1000 | kHz |
| SCL High Time | t _{HIGH} | | 0.26 | | | μs |
| SCL Low Time | t _{LOW} | | 0.5 | | | μs |
| Data Setup Time | t _{SU; DAT} | | 50 | | | ns |
| Data Hold Time | t _{HD; DAT} | | 0 | | | μs |
| Setup Time for Repeated Start | t _{SU; STA} | | 0.26 | | | μs |
| Hold Time for Start/Repeated Start | t _{HD; STA} | | 0.26 | | | μs |
| Bus Free Time for Stop and Start Condition | t _{BUF} | | 0.5 | | | μs |
| Setup Time for Stop Condition | t _{SU; STO} | | 0.26 | | | μs |
| Data Valid Time | t _{VD; DAT} | | | | 0.45 | μs |
| Data Valid Acknowledge | t _{VD; ACK} | | | | 0.45 | μs |
| Rise Time for SCL and SDA | t _R | | | | 120 | ns |
| Fall Time for SCL and SDA | t _F | | | | 120 | ns |
| Pulse Width of Suppressed Spike | t _{SP} | | 0 | | 50 | ns |
| Capacitive Load for Each Bus Line | C _B ⁴ | | | | 550 | pF |

¹ All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC). Typical values are at T_A = 25°C, VDD = 1.8 V.
² Guaranteed by design.
³ All timers are referenced from the base oscillator and have the same ±10% accuracy.
⁴ C_B is the total capacitance of one bus line in picofarads.

TIMING DIAGRAM

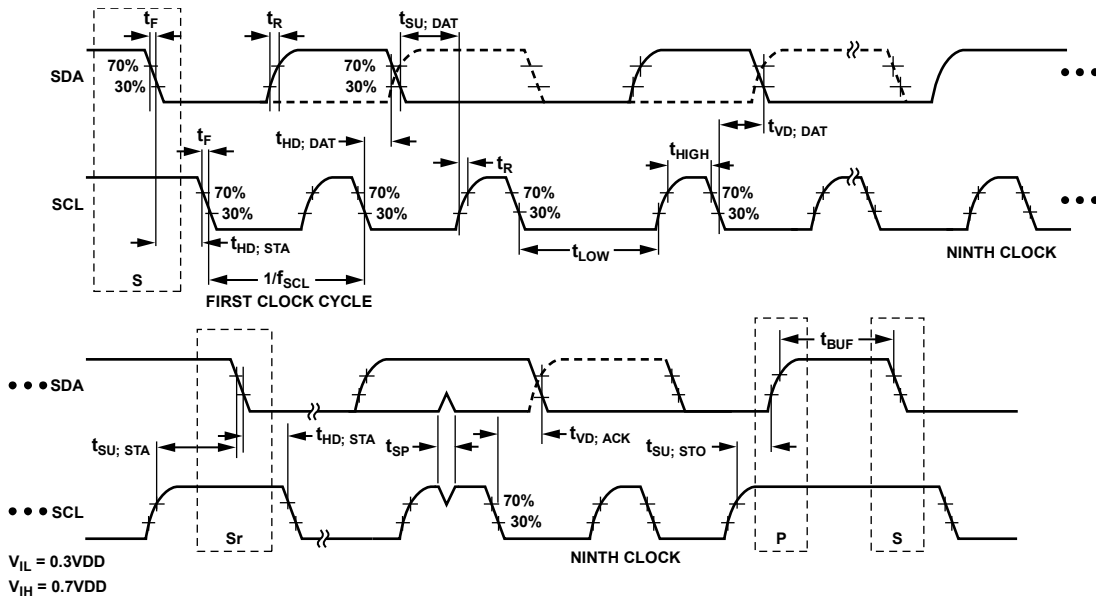


Figure 2. I²C Interface Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter | Rating |
|---|-----------------------------|
| VDD to GND | −0.3 V to +4 V |
| SCL, SDA, $\overline{\text{RST}}$, $\overline{\text{INT}}$, R0, R1, R2, R3, R4, C0, C1, C2, C3, C4 to GND | −0.3 V to (VDD + 0.3 V) |
| Temperature Range | |
| Operating (Ambient) | −40°C to +85°C ¹ |
| Operating (Junction) | −40°C to +125°C |
| Storage | −65°C to +150°C |

¹ In applications where high power dissipation and poor thermal resistance are present, the maximum ambient temperature may need to be derated. Maximum ambient temperature ($T_{A(MAX)}$) is dependent on the maximum operating junction temperature ($T_{J(MAXOP)} = 125^{\circ}\text{C}$), the maximum power dissipation of the device ($P_{D(MAX)}$), and the junction-to-ambient thermal resistance of the device/package in the application (θ_{JA}), using the following equation: $T_{A(MAX)} = T_{J(MAXOP)} - (\theta_{JA} \times P_{D(MAX)})$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to GND.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a printed circuit board (PCB) for surface-mount packages.

Table 3.

| Thermal Resistance | θ_{JA} | Unit |
|---------------------------|---------------|------|
| 16-Ball WLCSP | 62 | °C/W |
| Maximum Power Dissipation | 70 | mW |
| 16-Lead LFCSP | 67.154 | °C/W |
| Maximum Power Dissipation | 70 | mW |

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

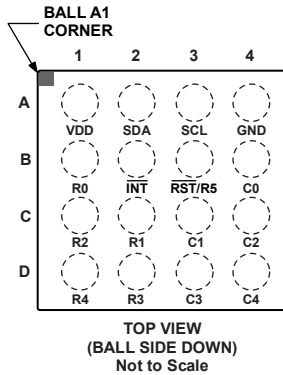
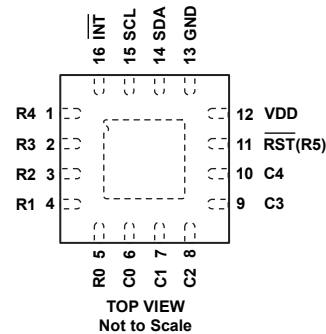


Figure 3. WLCSP Pin Configuration



NOTES
1. THE EXPOSED PAD IS NOT CONNECTED. IT IS RECOMMENDED TO CONNECT THE EXPOSED PAD TO GROUND FOR THERMAL DISSIPATION.

Figure 4. LFCSP Pin Configuration

Table 4. Pin Function Descriptions

| Pin No. | | Mnemonic | Description |
|---------|-------|----------|---|
| WLCSP | LFCSP | | |
| D1 | 1 | R4 | GPIO 5 (GPIO Alternate Function: RESET1). This pin functions as Row 4 when used as a keypad. |
| D2 | 2 | R3 | GPIO 4 (GPIO Alternate Function: Logic Block Input LC, PWM_OUT). This pin functions as Row 3 when used as a keypad. |
| C1 | 3 | R2 | GPIO 3 (GPIO Alternate Function: Logic Block Input LB). This pin functions as Row 2 when used as a keypad. |
| C2 | 4 | R1 | GPIO 2 (GPIO Alternate Function: Logic Block Input LA). This pin functions as Row 1 when used as a keypad. |
| B1 | 5 | R0 | GPIO 1 (GPIO Alternate Function: Logic Block Output LY). This pin functions as Row 0 when used as a keypad. |
| B4 | 6 | C0 | GPIO 7. This pin functions as Column 0 when used as a keypad. |
| C3 | 7 | C1 | GPIO 8. This pin functions as Column 1 when used as a keypad. |
| C4 | 8 | C2 | GPIO 9. This pin functions as Column 2 when used as a keypad. |
| D3 | 9 | C3 | GPIO 10 (GPIO Alternate Function: PWM_IN). This pin functions as Column 3 when used as a keypad. |
| D4 | 10 | C4 | GPIO 11 (GPIO Alternate Function: RESET2). This pin functions as Column 4 when used as a keypad. |
| B3 | 11 | RST/R5 | Input Reset Signal. To expand the keypad matrix, select the ADP5585ACBZ-01-R7 or the ADP5585ACPZ-01-R7 device model for this pin to function as GPIO 6/Row 5. |
| A1 | 12 | VDD | Supply Voltage Input. |
| A4 | 13 | GND | Ground. |
| A2 | 14 | SDA | I ² C Data Input/Output. |
| A3 | 15 | SCL | I ² C Clock Input. |
| B2 | 16 | INT | Open-Drain Interrupt Output. |
| | EP | EP | Exposed Pad. The exposed pad is not connected. It is recommended to connect the exposed pad to ground for thermal dissipation. |

THEORY OF OPERATION

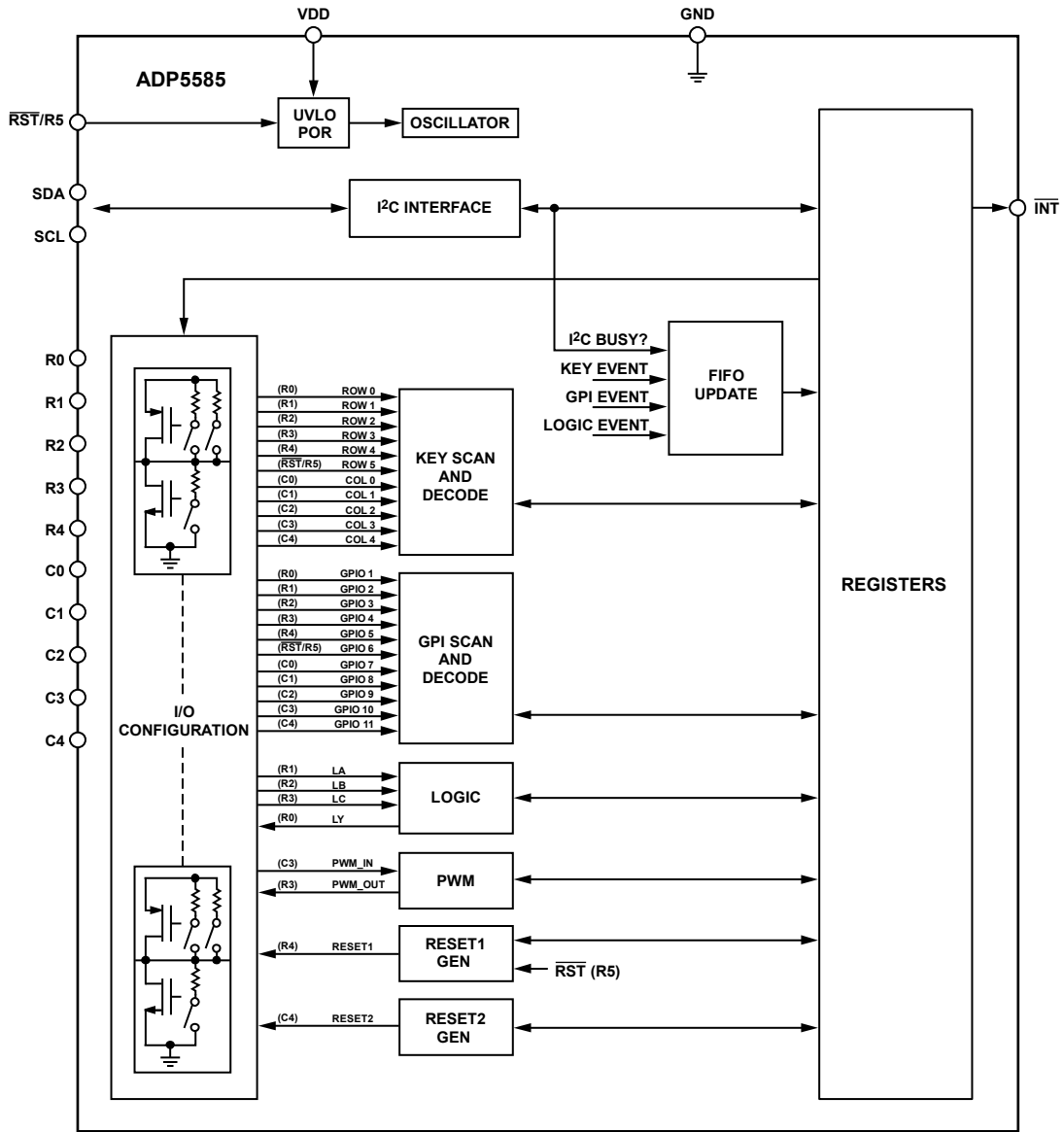


Figure 5. Internal Block Diagram

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DEVICE ENABLE

When sufficient voltage is applied to VDD and the $\overline{\text{RST}}$ pin is driven with a logic high level, the ADP5585 starts up in standby mode with all settings at default. The user can configure the device via the I²C interface. When the $\overline{\text{RST}}$ pin is low, the ADP5585 enters a reset state and all settings return to default. The $\overline{\text{RST}}$ pin features a debounce filter.

If using the ADP5585ACBZ-01-R7 or ADP5585ACPZ-01-R7 device model, the $\overline{\text{RST}}$ pin acts as an extra row pin. Without a reset pin, the only method to reset the device is by bringing VDD below the UVLO threshold.

DEVICE OVERVIEW

The ADP5585 contains 10 multiconfigurably input/output pins. Each pin can be programmed to enable the device to carry out its various functions, as follows:

- Keypad matrix decoding (five-column by five-row matrix maximum).
- General-purpose I/O expansion (up to 10 inputs/outputs).
- PWM generation.
- Logic function building blocks (up to three inputs and one output).
- Two reset generators.

All 10 input/output pins have an I/O structure as shown in Figure 6.

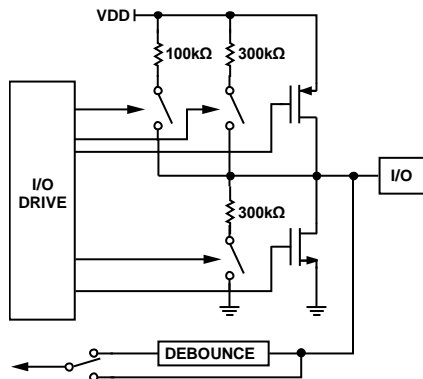


Figure 6. I/O Structure

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Each I/O can be pulled up with a 100 kΩ or 300 kΩ resistor or pulled down with a 300 kΩ resistor. For logic output drive, each I/O has a 5 mA PMOS source and a 10 mA NMOS sink for a push-pull type output. For open-drain output situations, the 5 mA PMOS source is not enabled. For logic input applications, each I/O can be sampled directly or, alternatively, sampled through a debounce filter.

The I/O structure shown in Figure 6 allows for all GPI and GPO functions, as well as PWM and clock divide functions. For key matrix scan and decode, the scanning circuit uses the 100 kΩ or 300 kΩ resistor for pulling up keypad row pins and the 10 mA NMOS sinks for grounding keypad column pins (see the Key Scan Control section for details about key decoding).

Configuration of the device is carried out by programming an array of internal registers via the I²C interface. Feedback of device status and pending interrupts can be flagged to an external processor by using the INT pin.

The ADP5585 is offered with three feature sets. Table 5 lists the options that are available for each model of the ADP5585.

Table 5. Matrix Options by Device Model

| Model | Description |
|-------------------|---|
| ADP5585ACBZ-00-R7 | GPIO pull up (default option) 5-row × 5-column matrix |
| ADP5585ACBZ-01-R7 | Row 5 added to GPIOs 6-row × 5-column matrix |
| ADP5585ACBZ-02-R7 | No pull-up resistors to special function pins ¹ 5-row × 5-column matrix |
| ADP5585ACBZ-04-R7 | Pull-down resistors to all GPIO pins on start-up 5-row × 5-column matrix |
| ADP5585ACPZ-00-R7 | GPIO pull up (default option) 5-row × 5-column matrix |
| ADP5585ACPZ-01-R7 | Row 5 added to GPIOs 6-row × 5-column matrix |
| ADP5585ACPZ-03-R7 | Alternate I ² C address (0x30) 5-row × 5-column matrix |

¹ Special function pins are defined as R0, R3, R4, and C4. See Table 4 for details.

FUNCTIONAL DESCRIPTION

EVENT FIFO

Before going into detail on the various ADP5585 blocks, it is important to understand the function of the event FIFO. The ADP5585 features an event FIFO that can record as many as 16 events. By default, the FIFO primarily records key events, such as key press and key release. However, it is possible to configure the general-purpose input (GPI) and logic activity to generate event information on the FIFO as well. An event count, EC[4:0], is composed of five bits and works in tandem with the FIFO so that the user knows how much of the FIFO must be read back at any given time.

The FIFO is composed of 16 eight-bit sections that the user accesses by reading the FIFO_x registers. The actual FIFO is not in user accessible registers until a read occurs. The FIFO can be thought of as a “first in first out” buffer that is used to fill Register 0x03 to Register 0x12.

The event FIFO is made up of 16 eight-bit registers. In each register, Bits[6:0] hold the event identifier, and Bit 7 holds the event state. With seven bits, 127 different events can be identified. See Table 11 for event decoding.

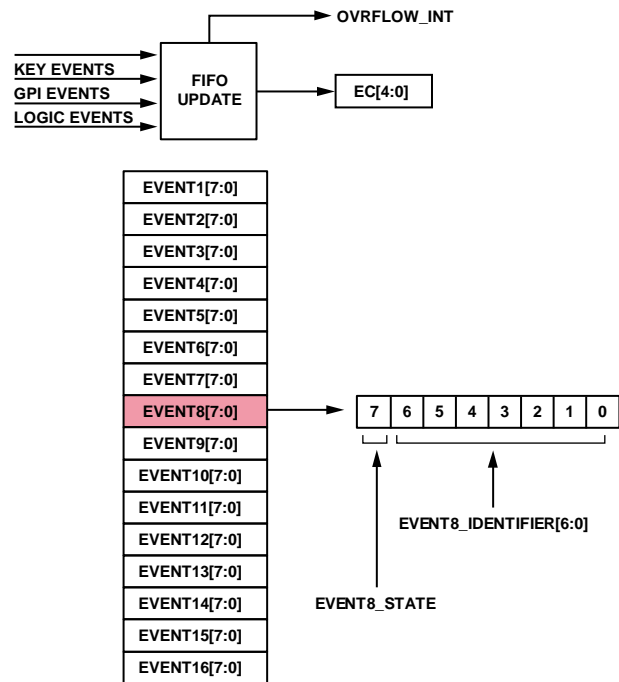


Figure 7. Breakdown of Eventx[7:0] Bits

When events are available on the FIFO, the user should first read back the event count, EC[4:0], to determine how many events must be read back. Events can be read from the top of the FIFO only. When an event is read back, all remaining events in the FIFO are shifted up one location, and the EC[4:0] count is decremented.

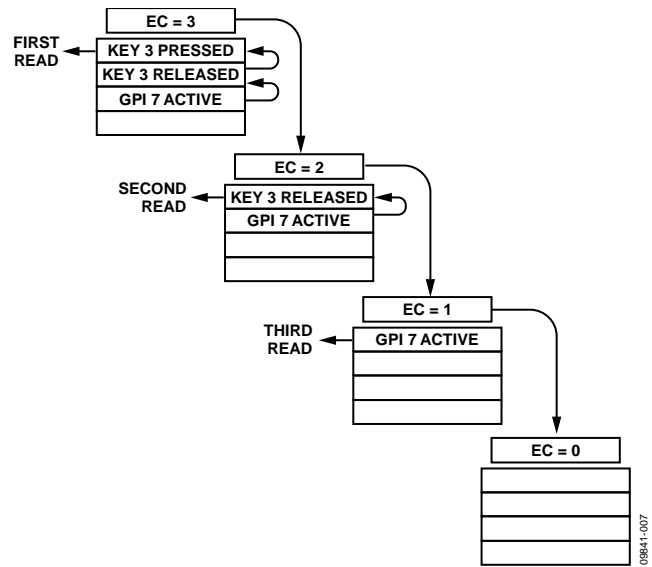


Figure 8. FIFO Operation

The FIFO registers (0x03 to 0x12) always point to the top of the FIFO (that is, the location of EVENT1[7:0]). If the user tries to read back from any location in a FIFO, data is always obtained from the top of that FIFO. This ensures that events can only be read back in the order in which they occurred, thus ensuring the integrity of the FIFO system.

As stated above, some of the onboard functions of ADP5585 can be programmed to generate events on the FIFO. A FIFO update control block manages updates to the FIFO. If an I²C transaction is accessing any of the FIFO address locations, updates are paused until the I²C transaction has completed.

A FIFO overflow event occurs when more than 16 events are generated prior to an external processor reading a FIFO and clearing it.

If an overflow condition occurs, the overflow status bit is set. An interrupt is generated if overflow interrupt is enabled, signaling to the processor that more than 16 events have occurred.

KEY SCAN CONTROL

General

The 10 input/output pins can be configured to decode a keypad matrix up to a maximum size of 25 switches (5 × 5 matrix). Smaller matrices can also be configured, freeing up the unused row and column pins for other I/O functions.

The R0 through R4 I/O pins comprise the rows of the keypad matrix. The C0 through C4 I/O pins comprise the columns of the keypad matrix. Pins used as rows are pulled up via the internal 300 kΩ (or 100 kΩ) resistors. Pins used as columns are driven low via the internal NMOS current sink.

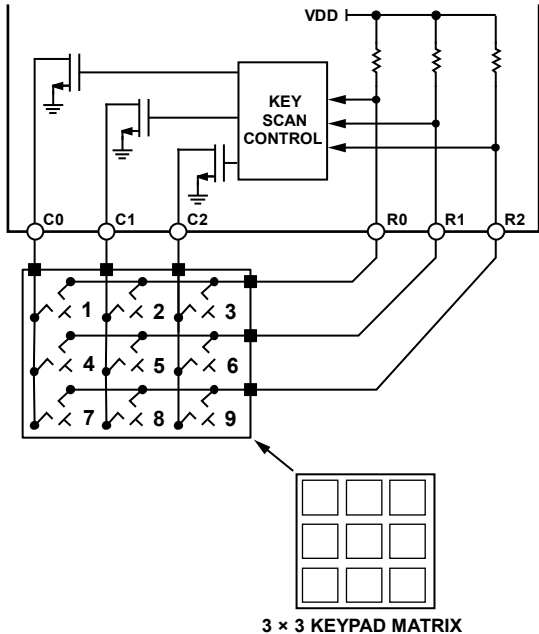


Figure 9. Simplified Key Scan Block

Figure 9 shows a simplified representation of the key scan block using three row and three column pins connected to a small 3 × 3, nine-switch keypad matrix. When the key scanner is idle, the row pins are pulled high and the column pins are driven low. The key scanner operates by checking the row pins to see if they are low.

If Switch 6 in the matrix is pressed, R1 connects to C2. The key scan circuit senses that one of the row pins has been pulled low, and a key scan cycle begins. Key scanning involves driving all column pins high, then driving each column pin, one at a time,

low and sensing whether a row pin is low or not. All row/column pairs are scanned; therefore, if multiple keys are pressed, they are detected.

To prevent glitches or narrow press times being registered as a valid key press, the key scanner requires the key be pressed for two scan cycles. The key scanner has a wait time between each scan cycle; therefore, the key must be pressed and held for at least this wait time to register as being pressed. If the key is continuously pressed, the key scanner continues to scan, wait, scan, wait, and so forth.

If Switch 6 is released, the connection between R1 and C2 breaks, and R1 is pulled up high. The key scanner requires that the key be released for two scan cycles because the release of a key is not necessarily in sync with the key scanner, it may take up to two full wait/scan cycles for a key to register as released. When the key is registered as released, and no other keys are pressed, the key scanner returns to idle mode.

For the remainder of this document, the press/release status of a key is represented as simply a logic signal in the figures. A logic high level represents the key status as pressed, and a logic low represents released. This eliminates the need to draw individual row/column signals when describing key events.

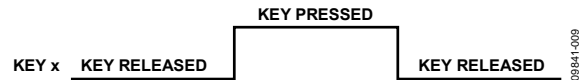


Figure 10. Logic Low: Released, Logic High: Pressed

Figure 11 shows a detailed representation of the key scan block and its associated control and status signals. When all row and column pins are used, a matrix of 25 unique keys can be scanned.

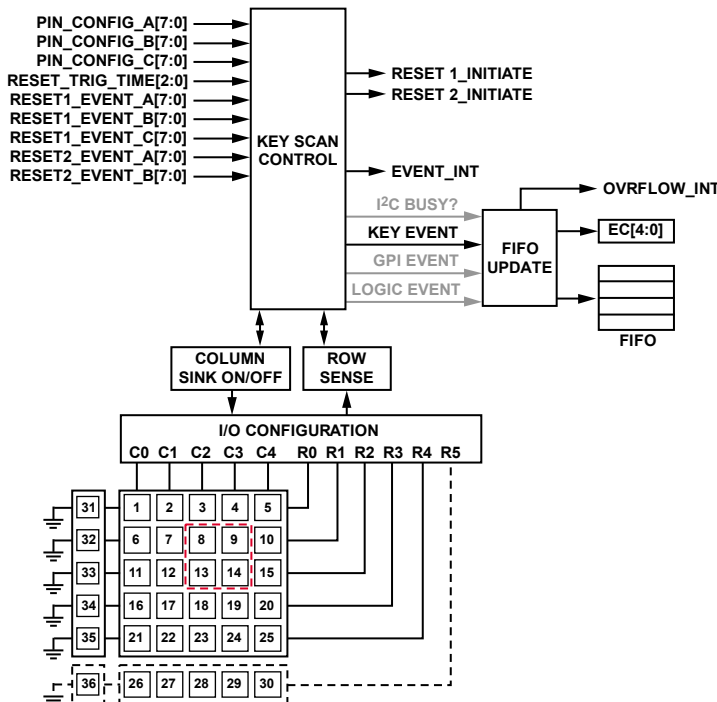


Figure 11. Detailed Key Scan Block

Use Registers PIN_CONFIG_A[7:0] and PIN_CONFIG_B[7:0] to configure I/Os for keypad decoding. The number label on each key switch represents the event identifier that is recorded if that switch was pressed. If all row/column pins are configured, it is possible to observe all 25 key identifiers on the FIFO. A larger 6 × 5 matrix can be configured by using the ADP5585ACBZ-01-R7 or the ADP5585ACPZ-01-R7.

If a smaller 2 × 2 matrix is configured, for example, by using the C2 and C3 column pins and the R1 and R2 row pins, only the four event identifiers (8, 9, 13, and 14) can possibly be observed on the FIFO, as shown in Figure 11.

By default, ADP5585 records key presses and releases on the FIFO. Figure 12 illustrates what happens when a single key is pressed and released. Initially, the key scanner is idle. When Key 3 is pressed, the scanner begins scanning through all configured row/column pairs. After the scan wait time, the scanner again scans through all configured row/column pairs and detects that Key 3 has remained pressed, which sets the EVENT_INT interrupt. The event counter, EC[4:0], is incremented to 1, EVENT1_IDENTIFIER[6:0] of the FIFO is updated with its event identifier set to 3, and its EVENT1_STATE bit is set to 1, indicating a press.

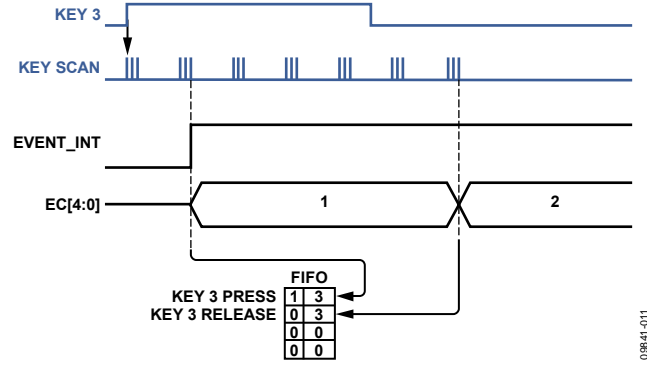


Figure 12. Press and Release Event

The key scanner continues the scan/wait cycles while the key remains pressed. If the scanner detects that the key has been released for two consecutive scan cycles, the event counter, EC[4:0], is incremented to 2, and EVENT2_IDENTIFIER[6:0] of the FIFO is updated with its event identifier set to 3. Its EVENT2_STATE bit is set to 0, indicating a release. The key scanner returns to idle mode because no other keys are pressed.

The EVENT_INT interrupt can be triggered by both press and release key events. As shown in Figure 14, if Key 3 is pressed, EVENT_INT is asserted, EC[4:0] is updated, and the FIFO is updated. During the time that the key remains pressed, it is possible for the FIFO to be read, the event counter decremented to 0, and EVENT_INT cleared. When the key is finally released, EVENT_INT is asserted, the event counter is incremented, and the FIFO is updated with the release event information.

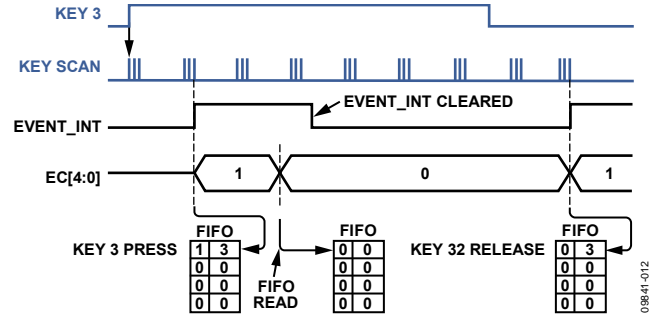


Figure 13. Asserting the EVENT_INT Interrupt Key Pad Extension

As shown in Figure 11, the keypad can be extended if each row is connected directly to ground by a switch. If the switch placed between R0 and ground is pressed, the entire row is grounded. When the key scanner completes scanning, it normally detects Key 1 to Key 5 as being pressed; however, this unique condition is decoded by the ADP5585, and Key Event 31 is assigned to it. Up to eight more key event assignments are possible, allowing the keypad size to extend up to 30. However, if one of the extended keys is pressed, none of the keys on that row is detectable. Activation of a ground key causes all other keys sharing that row to be undetectable.

Ghosting

Ghosting is an occurrence where, given certain key press combinations on a keypad matrix, a false positive reading of an additional key is detected. Ghosting is created when three or more keys are pressed simultaneously on multiple rows or columns (see Figure 14). Key combinations that form a right angle on the keypad matrix can cause ghosting.

The solution to ghosting is to select a keypad matrix layout that takes into account three key combinations that are most likely to be pressed together. Multiple keys pressed across one row or across one column do not cause ghosting. Staggering keys so that they do not share a column also avoids ghosting. The most common practice is to place keys that are likely to be pressed together in the same row or column. Some examples of keys that are likely to be pressed together are as follows:

- The navigation keys in combination with Select.
- The navigation keys in combination with the space bar.
- The reset combination keys, such as CTRL + ALT + DEL.

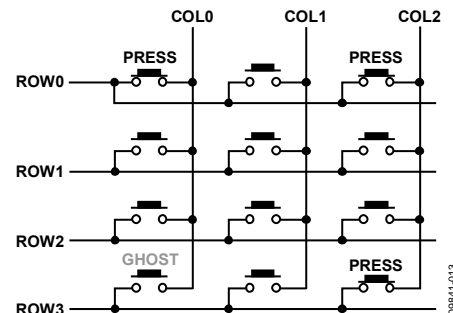


Figure 14. COL0: ROW3 is a Ghost Key Due to a Short Among ROW0, COL0, COL2, and ROW3 During Key Press

GPI INPUT

Each of the 10 input/output lines can be configured as a general-purpose logic input line. Figure 15 shows a detailed representation of the GPI scan and detect block and its associated control and status signals.

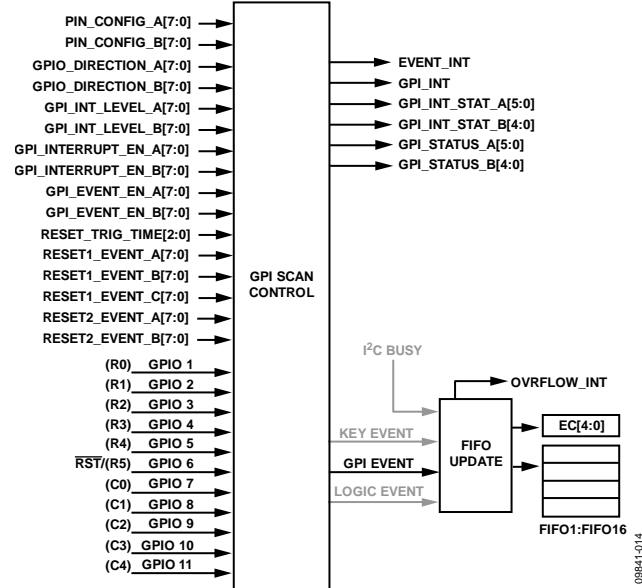


Figure 15. GPI Scan and Detect Block

The current input state of each GPI can be read back using the GPI_STATUS_x registers. Each GPI can be programmed to generate an interrupt via the GPI_INTERRUPT_EN_x registers. The interrupt status is stored in the GPI_INT_STAT_x registers. GPI interrupts can be programmed to trigger on the positive or negative edge by configuring the GPI_INT_LEVEL_x registers. If any of the GPI interrupts is triggered, the master GPI_INT interrupt is also triggered. Figure 16 shows a single GPI and how it affects its corresponding status and interrupt status bits.

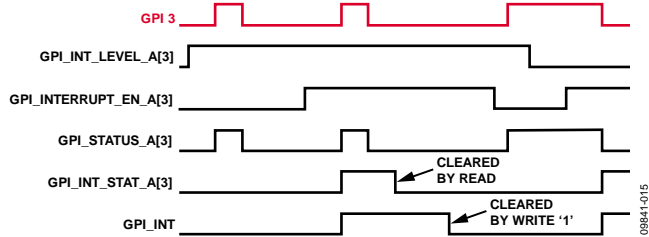


Figure 16. Single GPI Example

GPIs can be programmed to generate FIFO events via the GPI_EVENT_EN_x registers. GPIs in this mode do not generate GPI_INT interrupts and instead generate EVENT_INT interrupts. Figure 17 shows several GPI lines and their effects on the FIFO and event count, EC[4:0].

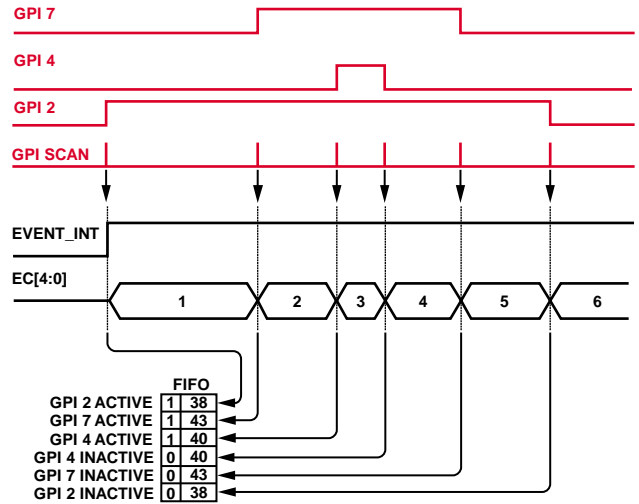


Figure 17. Multiple GPI Example

The GPI scanner is idle until it detects a level transition. It scans the GPI inputs and updates accordingly. It then returns to idle immediately, it does not scan/wait, like the key scanner. As such, the GPI scanner can detect narrow pulses once they get past the 50 µs input debounce filter.

GPO OUTPUT

Each of the 10 input/output lines can be configured as a general-purpose output (GPO) line. Figure 6 shows a detailed diagram of the I/O structure. See the Detailed Register Descriptions section for GPO configuration and usage.

LOGIC BLOCKS

Several of the ADP5585 input/output lines can be used as inputs and outputs for implementing some common logic functions.

The R1, R2, and R3 input/output pins can be used as inputs, and the R0 input/output pin can be used as an output for the logic block.

The outputs from the logic blocks can be configured to generate interrupts. They can also be configured to generate events on the FIFO.

Figure 19 shows a detailed diagram of the internal make-up of the logic block, illustrating the possible logic functions that can be implemented.

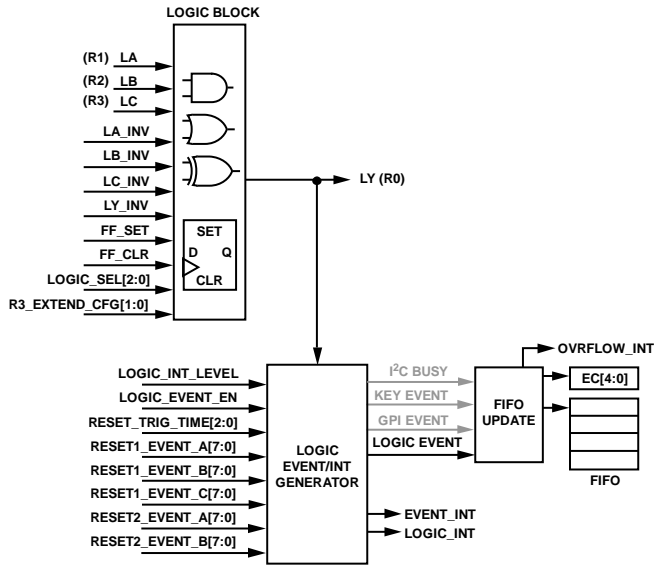


Figure 18. Logic Block Overview

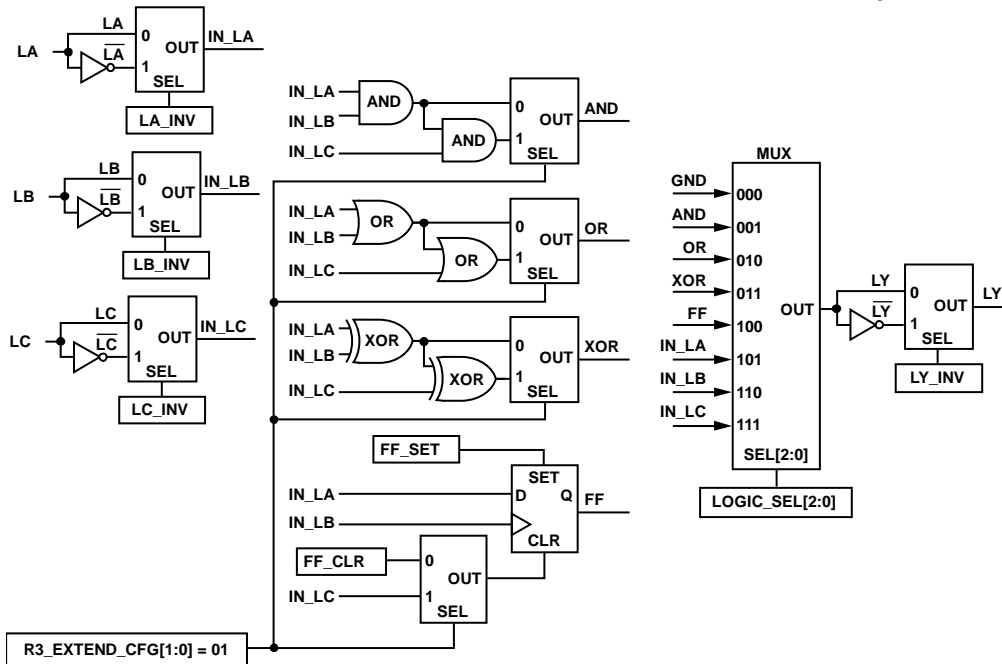


Figure 19. Logic Block

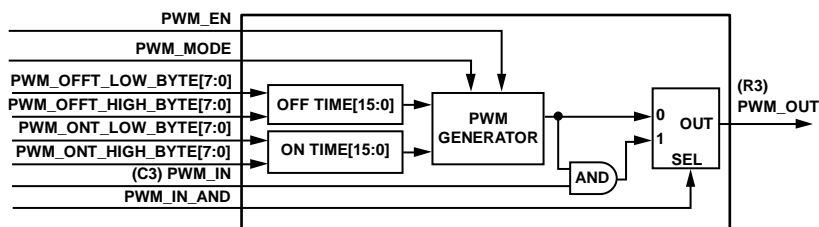


Figure 20. PWM Block Diagram

PWM BLOCK

The ADP5585 features a PWM generator whose output can be configured to drive out on the R3 I/O pin. PWM on/off times are programmed via four 8-bit registers (see Figure 20). Each bit of the on or off time represents 1 μ s. The highest frequency obtainable from the PWM is performed by setting the least significant bit of both the on and off time bit patterns, resulting in a 500 kHz signal with a 50% duty cycle.

The PWM block provides support for continuous PWM mode as well as a one-shot mode (see Table 59). Additionally, an external signal can be ANDed with the internal PWM signal. This option can be selected by writing a 1 to PWM_IN_AND (PWM_CFG[2]). The input to the external AND is the C3 I/O pin. C3 should be set to GPI. Note that the debounce for C3 results in a delay of the AND'ing, and can be turned on or off using Register 0x21.

Newly programmed values are not latched until the final byte, PWM_ONT_HIGH_BYTE (Register 0x32, Bits[7:0]), is written.

RESET BLOCKS

ADP5585 features two reset blocks that can generate reset conditions if certain events are detected simultaneously. Up to three reset trigger events can be programmed for RESET1. Up to two reset trigger events can be programmed for RESET2. The event scan control blocks monitor whether these events are present for the duration of RESET_TRIG_TIME[2:0] (Register 0x2E, Bits[4:2]). If they are, reset-initiate signals are sent to the reset generator blocks. The generated reset signal pulse width is programmable.

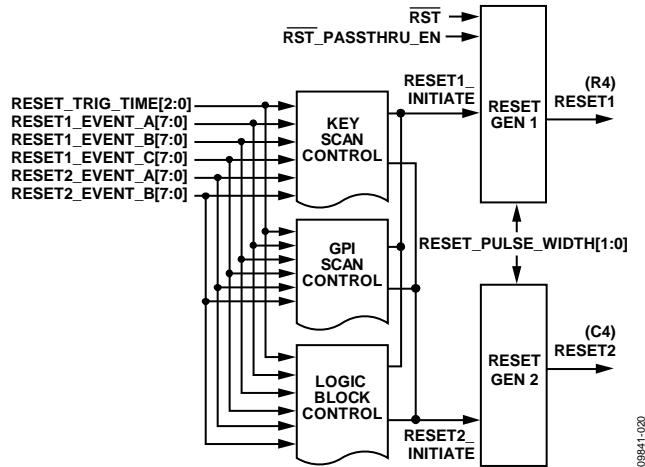


Figure 21. Reset Blocks

The Reset 1 signal uses the R4 I/O pin as its output. A pass through mode allows the main RST pin to be output on the R4 pin also. The Reset 2 signal uses the C4 I/O pin as its output.

The reset generation signals are useful in situations where the system processor has locked up and the system is unresponsive to input events. The user can press one of the reset event combinations and initiate a system wide reset. This alleviates the need for removing the battery from the system and doing a hard reset.

It is not recommended to use the immediate trigger time (see Table 54) because this setting may cause false triggering.

Interrupts

The $\overline{\text{INT}}$ pin can be asserted low if any of the internal interrupt sources is active. The user can select which internal interrupts interact with the external interrupt pin in Register 0x3C (refer to Table 68). Register 0x3B allows the user to choose whether the external interrupt pin remains asserted, or deasserts for 50 μs , then reasserts, in the case that there are multiple internal interrupts asserted and one is cleared (refer to Table 67).

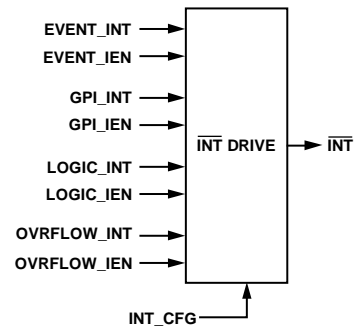


Figure 22. Asserting $\overline{\text{INT}}$ Low

REGISTER INTERFACE

Register access to the ADP5585 is acquired via its I²C-compatible serial interface. The interface can support clock frequencies of up to 1 MHz. If the user is accessing the FIFO or key event counter (KEC), FIFO/KEC updates are paused. If the clock frequency is very low, events may not be recorded in a timely manner. FIFO or KEC updates can happen up to 23 μs after an interrupt is asserted because of the number of I²C cycles required to perform an I²C read or write. This delay should not present an issue to the user.

Figure 23 shows a typical write sequence for programming an internal register. The cycle begins with a start condition, followed by the hard coded 7-bit device address, which for the ADP5585 is 0x34, followed by the R/W bit set to 0 for a write cycle. The ADP5585 acknowledges the address byte by pulling the data line low. The address of the register to which data is to be written is sent next. The ADP5585 acknowledges the register pointer byte by pulling the data line low. The data byte to be written is sent next. The ADP5585 acknowledges the data byte by pulling the data line low. A stop condition completes the sequence.

Figure 24 shows a typical multibyte write sequence for programming internal registers. The cycle begins with a start condition followed by the 7-bit device address (0x34 for all models except the ADP5585ACPZ-03-R7, 0x30 for the ADP5585ACPZ-03-R7 only), followed by the R/W bit set to 0 for a write cycle. The ADP5585 acknowledges the address byte by pulling the data

line low. The address of the register to which data is to be written is sent next. The ADP5585 acknowledges the register pointer byte by pulling the data line low. The data byte to be written is sent next. The ADP5585 acknowledges the data byte by pulling the data line low. The pointer address is then incremented to write the next data byte, until it finishes writing the n data byte. The ADP5585 pulls the data line low after every byte, and a stop condition completes the sequence.

Figure 25 shows a typical byte read sequence for reading internal registers. The cycle begins with a start condition followed by the 7-bit device address (0x34 for all models except the ADP5585ACPZ-03-R7, 0x30 for the ADP5585ACPZ-03-R7 only), followed by the R/W bit set to 0 for a write cycle. The ADP5585 acknowledges the address byte by pulling the data line low. The address of the register from which data is to be read is sent next. The ADP5585 acknowledges the register pointer byte by pulling the data line low. A start condition is repeated, followed by the 7-bit device address (0x34 for all models except the ADP5585ACPZ-03-R7, 0x30 for the ADP5585ACPZ-03-R7 only), followed by the R/W bit set to 1 for a read cycle. The ADP5585 acknowledges the address byte by pulling the data line low. The 8-bit data is then read. The host pulls the data line high (no acknowledge), and a stop condition completes the sequence.



Figure 23. I²C Single Byte Write Sequence

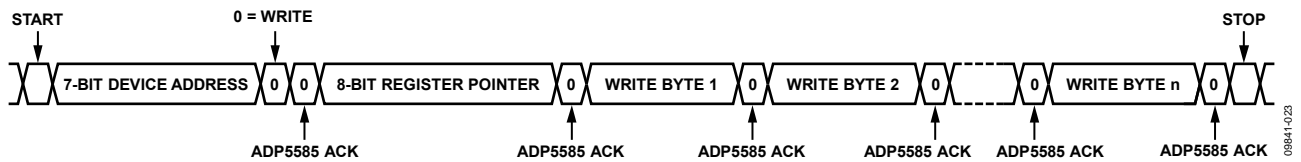


Figure 24. I²C Multibyte Write Sequence

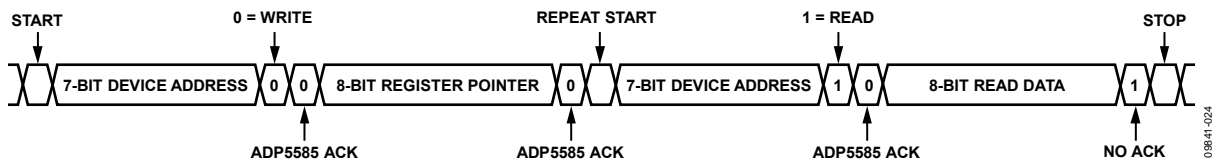


Figure 25. I²C Single Byte Read Sequence

Figure 26 shows a typical multibyte read sequence for reading internal registers. The cycle begins with a start condition, followed by the 7-bit device address (0x34 for all models except the ADP5585ACPZ-03-R7, 0x30 for the ADP5585ACPZ-03-R7 only), followed by the R/W bit set to 0 for a write cycle. The ADP5585 acknowledges the address byte by pulling the data line low. The address of the register from which data is to be read is sent next. The ADP5585 acknowledges the register pointer byte by pulling the data line low. A start condition is repeated, followed by the 7-bit device address (0x34 for all models except the

ADP5585ACPZ-03-R7, 0x30 for the ADP5585ACPZ-03-R7 only), followed by the R/W bit set to 1 for a read cycle. The ADP5585 acknowledges the address byte by pulling the data line low. The 8-bit data is then read. The address pointer is then incremented to read the next data byte, and the host continues to pull the data line low for each byte (master acknowledge) until the n data byte is read. The host pulls the data line high (no acknowledge) after the last byte is read, and a stop condition completes the sequence.

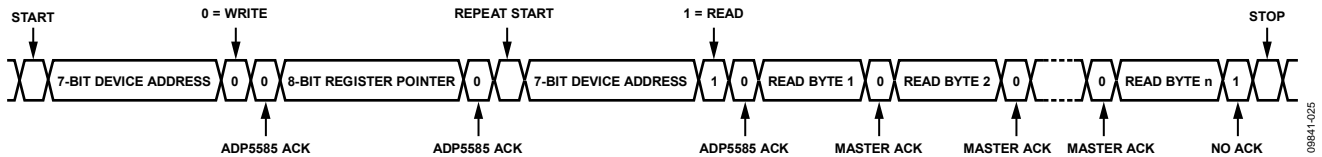


Figure 26. I²C Multibyte Read Sequence

09841-025

REGISTER MAP

Table 6.

| Reg Add | Reg Name | R/W ¹ | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|--------------------|------------------|---------------|-------------------------|-----------------|------------------|------------------|-----------------|-----------------|-----------------|
| 0x00 | ID | R | MAN_ID | | | | REV_ID | | | |
| 0x01 | INT_STATUS | R/W | Reserved | | | LOGIC_INT | Reserved | OVRFLOW_INT | GPI_INT | EVENT_INT |
| 0x02 | Status | R | Reserved | LOGIC_STAT | Reserved | EC[4:0] | | | | |
| 0x03 | FIFO_1 | R | EVENT1_STATE | EVENT1_IDENTIFIER[6:0] | | | | | | |
| 0x04 | FIFO_2 | R | EVENT2_STATE | EVENT2_IDENTIFIER[6:0] | | | | | | |
| 0x05 | FIFO_3 | R | EVENT3_STATE | EVENT3_IDENTIFIER[6:0] | | | | | | |
| 0x06 | FIFO_4 | R | EVENT4_STATE | EVENT4_IDENTIFIER[6:0] | | | | | | |
| 0x07 | FIFO_5 | R | EVENT5_STATE | EVENT5_IDENTIFIER[6:0] | | | | | | |
| 0x08 | FIFO_6 | R | EVENT6_STATE | EVENT6_IDENTIFIER[6:0] | | | | | | |
| 0x09 | FIFO_7 | R | EVENT7_STATE | EVENT7_IDENTIFIER[6:0] | | | | | | |
| 0x0A | FIFO_8 | R | EVENT8_STATE | EVENT8_IDENTIFIER[6:0] | | | | | | |
| 0x0B | FIFO_9 | R | EVENT9_STATE | EVENT9_IDENTIFIER[6:0] | | | | | | |
| 0x0C | FIFO_10 | R | EVENT10_STATE | EVENT10_IDENTIFIER[6:0] | | | | | | |
| 0x0D | FIFO_11 | R | EVENT11_STATE | EVENT11_IDENTIFIER[6:0] | | | | | | |
| 0x0E | FIFO_12 | R | EVENT12_STATE | EVENT12_IDENTIFIER[6:0] | | | | | | |
| 0x0F | FIFO_13 | R | EVENT13_STATE | EVENT13_IDENTIFIER[6:0] | | | | | | |
| 0x10 | FIFO_14 | R | EVENT14_STATE | EVENT14_IDENTIFIER[6:0] | | | | | | |
| 0x11 | FIFO_15 | R | EVENT15_STATE | EVENT15_IDENTIFIER[6:0] | | | | | | |
| 0x12 | FIFO_16 | R | EVENT16_STATE | EVENT16_IDENTIFIER[6:0] | | | | | | |
| 0x13 | GPI_INT_STAT_A | R | Reserved | | GPI_6_INT | GPI_5_INT | GPI_4_INT | GPI_3_INT | GPI_2_INT | GPI_1_INT |
| 0x14 | GPI_INT_STAT_B | R | Reserved | | | GPI_11_INT | GPI_10_INT | GPI_9_INT | GPI_8_INT | GPI_7_INT |
| 0x15 | GPI_STATUS_A | R | Reserved | | GPI_6_STAT | GPI_5_STAT | GPI_4_STAT | GPI_3_STAT | GPI_2_STAT | GPI_1_STAT |
| 0x16 | GPI_STATUS_B | R | Reserved | | | GPI_11_STAT | GPI_10_STAT | GPI_9_STAT | GPI_8_STAT | GPI_7_STAT |
| 0x17 | R_PULL_CONFIG_A | R/W | R3_PULL_CFG | | R2_PULL_CFG | | R1_PULL_CFG | | R0_PULL_CFG | |
| 0x18 | R_PULL_CONFIG_B | R/W | Reserved | | | | R5_PULL_CFG | | R4_PULL_CFG | |
| 0x19 | R_PULL_CONFIG_C | R/W | C3_PULL_CFG | | C2_PULL_CFG | | C1_PULL_CFG | | C0_PULL_CFG | |
| 0x1A | R_PULL_CONFIG_D | R/W | Reserved | | | | | | C4_PULL_CFG | |
| 0x1B | GPI_INT_LEVEL_A | R/W | Reserved | | GPI_6_INT_LEVEL | GPI_5_INT_LEVEL | GPI_4_INT_LEVEL | GPI_3_INT_LEVEL | GPI_2_INT_LEVEL | GPI_1_INT_LEVEL |
| 0x1C | GPI_INT_LEVEL_B | R/W | Reserved | | | GPI_11_INT_LEVEL | GPI_10_INT_LEVEL | GPI_9_INT_LEVEL | GPI_8_INT_LEVEL | GPI_7_INT_LEVEL |
| 0x1D | GPI_EVENT_EN_A | R/W | Reserved | | GPI_6_EVENT_EN | GPI_5_EVENT_EN | GPI_4_EVENT_EN | GPI_3_EVENT_EN | GPI_2_EVENT_EN | GPI_1_EVENT_EN |
| 0x1E | GPI_EVENT_EN_B | R/W | Reserved | | | GPI_11_EVENT_EN | GPI_10_EVENT_EN | GPI_9_EVENT_EN | GPI_8_EVENT_EN | GPI_7_EVENT_EN |
| 0x1F | GPI_INTERRUPT_EN_A | R/W | Reserved | | GPI_6_INT_EN | GPI_5_INT_EN | GPI_4_INT_EN | GPI_3_INT_EN | GPI_2_INT_EN | GPI_1_INT_EN |
| 0x20 | GPI_INTERRUPT_EN_B | R/W | Reserved | | | GPI_11_INT_EN | GPI_10_INT_EN | GPI_9_INT_EN | GPI_8_INT_EN | GPI_7_INT_EN |
| 0x21 | DEBOUNCE_DIS_A | R/W | Reserved | | GPI_6_DEB_DIS | GPI_5_DEB_DIS | GPI_4_DEB_DIS | GPI_3_DEB_DIS | GPI_2_DEB_DIS | GPI_1_DEB_DIS |
| 0x22 | DEBOUNCE_DIS_B | R/W | Reserved | | | GPI_11_DEB_DIS | GPI_10_DEB_DIS | GPI_9_DEB_DIS | GPI_8_DEB_DIS | GPI_7_DEB_DIS |
| 0x23 | GPO_DATA_OUT_A | R/W | Reserved | | GPO_6_DATA | GPO_5_DATA | GPO_4_DATA | GPO_3_DATA | GPO_2_DATA | GPO_1_DATA |
| 0x24 | GPO_DATA_OUT_B | R/W | Reserved | | | GPO_11_DATA | GPO_10_DATA | GPO_9_DATA | GPO_8_DATA | GPO_7_DATA |
| 0x25 | GPO_OUT_MODE_A | R/W | Reserved | | GPO_6_OUT_MODE | GPO_5_OUT_MODE | GPO_4_OUT_MODE | GPO_3_OUT_MODE | GPO_2_OUT_MODE | GPO_1_OUT_MODE |

| Reg Add | Reg Name | R/W ¹ | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
|---------|--------------------|------------------|-------------------------|----------------------|------------------|----------------------|--------------------|----------------|------------------------|-----------------|--|
| 0x26 | GPO_OUT_MODE_B | R/W | Reserved | | | GPO_11_OUT_MODE | GPO_10_OUT_MODE | GPO_9_OUT_MODE | GPO_8_OUT_MODE | GPO_7_OUT_MODE | |
| 0x27 | GPIO_DIRECTION_A | R/W | Reserved | | GPIO_6_DIR | GPIO_5_DIR | GPIO_4_DIR | GPIO_3_DIR | GPIO_2_DIR | GPIO_1_DIR | |
| 0x28 | GPIO_DIRECTION_B | R/W | Reserved | | | GPO_11_DIR | GPO_10_DIR | GPO_9_DIR | GPO_8_DIR | GPO_7_DIR | |
| 0x29 | RESET1_EVENT_A | R/W | RESET1_EVENT_A_LEVEL | RESET1_EVENT_A [6:0] | | | | | | | |
| 0x2A | RESET1_EVENT_B | R/W | RESET1_EVENT_B_LEVEL | RESET1_EVENT_B [6:0] | | | | | | | |
| 0x2B | RESET1_EVENT_C | R/W | RESET1_EVENT_C_LEVEL | RESET1_EVENT_C [6:0] | | | | | | | |
| 0x2C | RESET2_EVENT_A | R/W | RESET2_EVENT_A_LEVEL | RESET2_EVENT_A [6:0] | | | | | | | |
| 0x2D | RESET2_EVENT_B | R/W | RESET2_EVENT_B_LEVEL | RESET2_EVENT_B [6:0] | | | | | | | |
| 0x2E | RESET2_CFG | R/W | RESET2_POL | RESET1_POL | RST_PASS_THRU_EN | RESET_TRIG_TIME[2:0] | | | RESET_PULSE_WIDTH[1:0] | | |
| 0x2F | PWM_OFFT_LOW | R/W | PWM_OFFT_LOW_BYTE[7:0] | | | | | | | | |
| 0x30 | PWM_OFFT_HIGH | R/W | PWM_OFFT_HIGH_BYTE[7:0] | | | | | | | | |
| 0x31 | PWM_ONT_LOW | R/W | PWM_ONT_LOW_BYTE[7:0] | | | | | | | | |
| 0x32 | PWM_ONT_HIGH | R/W | PWM_ONT_HIGH_BYTE[7:0] | | | | | | | | |
| 0x33 | PWM_CFG | R/W | Reserved | | | | | PWM_IN_AND | PWM_MODE | PWM_EN | |
| 0x34 | LOGIC_CFG | R/W | Reserved | LY_INV | LC_INV | LB_INV | LA_INV | LOGIC_SEL[2:0] | | | |
| 0x35 | LOGIC_FF_CFG | R/W | Reserved | | | | | | FF_SET | FF_CLR | |
| 0x36 | LOGIC_INT_EVENT_EN | R/W | Reserved | | | | | LY_DBNC_DIS | LOGIC_EVENT_EN | LOGIC_INT_LEVEL | |
| 0x37 | POLL_TIME_CFG | R/W | Reserved | | | | | | KEY_POLL_TIME[1:0] | | |
| 0x38 | PIN_CONFIG_A | R/W | Reserved | | R5_CONFIG | R4_CONFIG | R3_CONFIG | R2_CONFIG | R1_CONFIG | R0_CONFIG | |
| 0x39 | PIN_CONFIG_B | R/W | Reserved | | | C4_CONFIG | C3_CONFIG | C2_CONFIG | C1_CONFIG | C0_CONFIG | |
| 0x3A | PIN_CONFIG_C | R/W | PULL_SELECT | C4_EXTEND_CFG | R4_EXTEND_CFG | Reserved | R3_EXTEND_CFG[1:0] | | Reserved | R0_EXTEND_CFG | |
| 0x3B | GENERAL_CFG | R/W | OSC_EN | CORE_FREQ[1:0] | | Reserved | | | INT_CFG | RST_CFG | |
| 0x3C | INT_EN | R/W | Reserved | | | LOGIC_IEN | Reserved | OVRFLOW_IEN | GPI_IEN | EVENT_IEN | |

¹ R means read, W means write, and R/W means read/write.

DETAILED REGISTER DESCRIPTIONS

Note that N/A throughout this section means not applicable.

Note: All register default to 0000 0000 unless otherwise specified.

ID Register 0x00

Table 7. ID Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|----------|-----------|---------------------------------|
| 7 to 4 | MAN_ID | Read only | Manufacturer ID, default = 0010 |
| 3 to 0 | REV_ID | Read only | Rev ID |

INT_STATUS Register 0x01

Table 8. INT_STATUS Bit Descriptions

| Bit(s) | Bit Name | Access | Description ¹ |
|--------|--------------|------------|--|
| 7 to 5 | N/A | | Reserved. |
| 4 | LOGIC_INT | Read/write | 0 = no interrupt. 1 = interrupt due to a general logic condition. |
| 3 | N/A | | Reserved. |
| 2 | OVERFLOW_INT | Read/write | 0 = no interrupt. 1 = interrupt due to an overflow condition. |
| 1 | GPI_INT | Read/write | This bit is not set by a GPI that has been configured to update the FIFO and event count. This bit cannot be cleared until all GPI_x_INT bits are cleared. 0 = no interrupt. 1 = interrupt due to a general GPI condition. |
| 0 | EVENT_INT | Read/write | 0 = no interrupt. 1 = interrupt due to key event (press/release), GPI event (GPI programmed for FIFO updates), or logic event (programmed for FIFO updates). |

¹ Interrupt bits are cleared by writing a 1 to the flag; writing a 0 or reading the flag has no effect.

Status Register 0x02

Table 9. Status Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|------------|-----------|---|
| 7 | N/A | | Reserved. |
| 6 | LOGIC_STAT | Read only | 0 = output from logic block (LY) is low. 1 = output from logic block (LY) is high. |
| 5 | N/A | | Reserved. |
| 4 to 0 | EC[4:0] | Read only | Event count value. Indicates how many events are currently stored on the FIFO. |

FIFO_1 Register 0x03

Table 10. FIFO_1 Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|------------------------|-----------|--|
| 7 | EVENT1_STATE | Read only | This bit represents the state of the event that is recorded in the EVENT1_IDENTIFIER[6:0] bit. For key events from Event 1 to Event 36, use the following settings: 1 = key is pressed. 0 = key is released. For GPI and logic events from Event 37 to Event 48, use the following settings: 1 = GPI/logic is active. 0 = GPI/logic is inactive. Active and inactive states for Event 37 to Event 48 are programmable. |
| 6 to 0 | EVENT1_IDENTIFIER[6:0] | Read only | Contains the event identifier for the pin. Refer to Table 11. |

Table 11. Event Decoding

| Event No. | Meaning | Event No. | Meaning | Event No. | Meaning | Event No. | Meaning |
|-----------|------------------|-----------|------------------|-----------|---------|-----------|---------|
| 0 | No event | 32 | Key 32 (R1, GND) | 64 | Unused | 96 | Unused |
| 1 | Key 1 (R0, C0) | 33 | Key 33 (R2, GND) | 65 | Unused | 97 | Unused |
| 2 | Key 2 (R0, C1) | 34 | Key 34 (R3, GND) | 66 | Unused | 98 | Unused |
| 3 | Key 3 (R0, C2) | 35 | Key 35 (R4, GND) | 67 | Unused | 99 | Unused |
| 4 | Key 4 (R0, C3) | 36 | Key 36 (R5, GND) | 68 | Unused | 100 | Unused |
| 5 | Key 5 (R0, C4) | 37 | GPI 1 (R0) | 69 | Unused | 101 | Unused |
| 6 | Key 6 (R1, C0) | 38 | GPI 2 (R1) | 70 | Unused | 102 | Unused |
| 7 | Key 7 (R1, C1) | 39 | GPI 3 (R2) | 71 | Unused | 103 | Unused |
| 8 | Key 8 (R1, C2) | 40 | GPI 4 (R3) | 72 | Unused | 104 | Unused |
| 9 | Key 9 (R1, C3) | 41 | GPI 5 (R4) | 73 | Unused | 105 | Unused |
| 10 | Key 10 (R1, C4) | 42 | GPI 6 (R5) | 74 | Unused | 106 | Unused |
| 11 | Key 11 (R2, C0) | 43 | GPI 7 (C0) | 75 | Unused | 107 | Unused |
| 12 | Key 12 (R2, C1) | 44 | GPI 8 (C1) | 76 | Unused | 108 | Unused |
| 13 | Key 13 (R2, C2) | 45 | GPI 9 (C2) | 77 | Unused | 109 | Unused |
| 14 | Key 14 (R2, C3) | 46 | GPI 10 (C3) | 78 | Unused | 110 | Unused |
| 15 | Key 15 (R2, C4) | 47 | GPI 11 (C4) | 79 | Unused | 111 | Unused |
| 16 | Key 16 (R3, C0) | 48 | Logic | 80 | Unused | 112 | Unused |
| 17 | Key 17 (R3, C1) | 49 | Unused | 81 | Unused | 113 | Unused |
| 18 | Key 18 (R3, C2) | 50 | Unused | 82 | Unused | 114 | Unused |
| 19 | Key 19 (R3, C3) | 51 | Unused | 83 | Unused | 115 | Unused |
| 20 | Key 20 (R3, C4) | 52 | Unused | 84 | Unused | 116 | Unused |
| 21 | Key 21 (R4, C0) | 53 | Unused | 85 | Unused | 117 | Unused |
| 22 | Key 22 (R4, C1) | 54 | Unused | 86 | Unused | 118 | Unused |
| 23 | Key 23 (R4, C2) | 55 | Unused | 87 | Unused | 119 | Unused |
| 24 | Key 24 (R4, C3) | 56 | Unused | 88 | Unused | 120 | Unused |
| 25 | Key 25 (R4, C4) | 57 | Unused | 89 | Unused | 121 | Unused |
| 26 | Key 26 (R5, C0) | 58 | Unused | 90 | Unused | 122 | Unused |
| 27 | Key 27 (R5, C1) | 59 | Unused | 91 | Unused | 123 | Unused |
| 28 | Key 28 (R5, C2) | 60 | Unused | 92 | Unused | 124 | Unused |
| 29 | Key 29 (R5, C3) | 61 | Unused | 93 | Unused | 125 | Unused |
| 30 | Key 30 (R5, C4) | 62 | Unused | 94 | Unused | 126 | Unused |
| 31 | Key 31 (R0, GND) | 63 | Unused | 95 | Unused | 127 | Unused |

FIFO_2 Register 0x04

Table 12. FIFO_2 Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|------------------------|-----------|--------------------|
| 7 | EVENT2_STATE | Read only | Refer to Table 10. |
| 6 to 0 | EVENT2_IDENTIFIER[6:0] | Read only | Refer to Table 10. |

FIFO_3 Register 0x05

Table 13. FIFO_3 Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|------------------------|-----------|--------------------|
| 7 | EVENT3_STATE | Read only | Refer to Table 10. |
| 6 to 0 | EVENT3_IDENTIFIER[6:0] | Read only | Refer to Table 10. |

FIFO_4 Register 0x06

Table 14. FIFO_4 Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|------------------------|-----------|--------------------|
| 7 | EVENT4_STATE | Read only | Refer to Table 10. |
| 6 to 0 | EVENT4_IDENTIFIER[6:0] | Read only | Refer to Table 10. |

FIFO_5 Register 0x07

Table 15. FIFO_5 Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|------------------------|-----------|--------------------|
| 7 | EVENT5_STATE | Read only | Refer to Table 10. |
| 6 to 0 | EVENT5_IDENTIFIER[6:0] | Read only | Refer to Table 10. |

FIFO_6 Register 0x08

Table 16. FIFO_6 Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|------------------------|-----------|--------------------|
| 7 | EVENT6_STATE | Read only | Refer to Table 10. |
| 6 to 0 | EVENT6_IDENTIFIER[6:0] | Read only | Refer to Table 10. |

FIFO_7 Register 0x09

Table 17. FIFO_7 Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|------------------------|-----------|--------------------|
| 7 | EVENT7_STATE | Read only | Refer to Table 10. |
| 6 to 0 | EVENT7_IDENTIFIER[6:0] | Read only | Refer to Table 10. |

FIFO_8 Register 0x0A

Table 18. FIFO_8 Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|------------------------|-----------|--------------------|
| 7 | EVENT8_STATE | Read only | Refer to Table 10. |
| 6 to 0 | EVENT8_IDENTIFIER[6:0] | Read only | Refer to Table 10. |

FIFO_9 Register 0x0B

Table 19. FIFO_9 Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|------------------------|-----------|--------------------|
| 7 | EVENT9_STATE | Read only | Refer to Table 10. |
| 6 to 0 | EVENT9_IDENTIFIER[6:0] | Read only | Refer to Table 10. |

FIFO_10 Register 0x0C

Table 20. FIFO_10 Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-------------------------|-----------|--------------------|
| 7 | EVENT10_STATE | Read only | Refer to Table 10. |
| 6 to 0 | EVENT10_IDENTIFIER[6:0] | Read only | Refer to Table 10. |

FIFO_11 Register 0x0D

Table 21. FIFO_11 Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-------------------------|-----------|--------------------|
| 7 | EVENT11_STATE | Read only | Refer to Table 10. |
| 6 to 0 | EVENT11_IDENTIFIER[6:0] | Read only | Refer to Table 10. |

FIFO_12 Register 0x0E

Table 22. FIFO_12 Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-------------------------|-----------|--------------------|
| 7 | EVENT12_STATE | Read only | Refer to Table 10. |
| 6 to 0 | EVENT12_IDENTIFIER[6:0] | Read only | Refer to Table 10. |

FIFO_13 Register 0x0F

Table 23. FIFO_13 Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-------------------------|-----------|--------------------|
| 7 | EVENT13_STATE | Read only | Refer to Table 10. |
| 6 to 0 | EVENT13_IDENTIFIER[6:0] | Read only | Refer to Table 10. |

FIFO_14 Register 0x10

Table 24. FIFO_14 Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-------------------------|-----------|--------------------|
| 7 | EVENT14_STATE | Read only | Refer to Table 10. |
| 6 to 0 | EVENT14_IDENTIFIER[6:0] | Read only | Refer to Table 10. |

FIFO_15 Register 0x11

Table 25. FIFO_15 Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-------------------------|-----------|--------------------|
| 7 | EVENT15_STATE | Read only | Refer to Table 10. |
| 6 to 0 | EVENT15_IDENTIFIER[6:0] | Read only | Refer to Table 10. |

FIFO_16 Register 0x12

Table 26. FIFO_16 Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-------------------------|-----------|--------------------|
| 7 | EVENT16_STATE | Read only | Refer to Table 10. |
| 6 to 0 | EVENT16_IDENTIFIER[6:0] | Read only | Refer to Table 10. |

GPI_INT_STAT_A Register 0x13

Table 27. GPI_INT_STAT_A Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-----------|-----------|---|
| 7 to 6 | N/A | | Reserved. |
| 5 | GPI_6_INT | Read only | 0 = no interrupt 1 = interrupt due to GPI_6 (R5 pin). Cleared on read. |
| 4 | GPI_5_INT | Read only | 0 = no interrupt 1 = interrupt due to GPI_5 (R4 pin). Cleared on read. |
| 3 | GPI_4_INT | Read only | 0 = no interrupt 1 = interrupt due to GPI_4 (R3 pin). Cleared on read. |
| 2 | GPI_3_INT | Read only | 0 = no interrupt 1 = interrupt due to GPI_3 (R2 pin). Cleared on read. |
| 1 | GPI_2_INT | Read only | 0 = no interrupt 1 = interrupt due to GPI_2 (R1 pin). Cleared on read. |
| 0 | GPI_1_INT | Read only | 0 = no interrupt 1 = interrupt due to GPI_1 (R0 pin). Cleared on read. |

GPI_INT_STAT_B Register 0x14

Table 28. GPI_INT_STAT_B Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|------------|-----------|---|
| 7 to 5 | N/A | | Reserved. |
| 4 | GPI_11_INT | Read only | 0 = no interrupt. 1 = interrupt due to GPI_11 (C4 pin). Cleared on read. |
| 3 | GPI_10_INT | Read only | 0 = no interrupt. 1 = interrupt due to GPI_10 (C3 pin). Cleared on read. |

| Bit(s) | Bit Name | Access | Description |
|--------|-----------|-----------|--|
| 2 | GPI_9_INT | Read only | 0 = no interrupt. 1 = interrupt due to GPI_9 (C2 pin). Cleared on read. |
| 1 | GPI_8_INT | Read only | 0 = no interrupt. 1 = interrupt due to GPI_8 (C1 pin). Cleared on read. |
| 0 | GPI_7_INT | Read only | 0 = no interrupt. 1 = interrupt due to GPI_7 (C0 pin). Cleared on read. |

GPI_STATUS_A Register 0x15

Table 29. GPI_STATUS_A Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|------------|-----------|---|
| 7 to 6 | N/A | | Reserved. |
| 5 | GPI_6_STAT | Read only | 0 = GPI_6 (R5 pin) is low. 1 = GPI_6 (R5 pin) is high. |
| 4 | GPI_5_STAT | Read only | 0 = GPI_5 (R4 pin) is low. 1 = GPI_5 (R4 pin) is high. |
| 3 | GPI_4_STAT | Read only | 0 = GPI_4 (R3 pin) is low. 1 = GPI_4 (R3 pin) is high. |
| 2 | GPI_3_STAT | Read only | 0 = GPI_3 (R2 pin) is low. 1 = GPI_3 (R2 pin) is high. |
| 1 | GPI_2_STAT | Read only | 0 = GPI_2 (R1 pin) is low. 1 = GPI_2 (R1 pin) is high. |
| 0 | GPI_1_STAT | Read only | 0 = GPI_1 (R0 pin) is low. 1 = GPI_1 (R0 pin) is high. |

GPI_STATUS_B Register 0x16

Table 30. Register 0x16, GPI_STATUS_B Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-------------|-----------|---|
| 7 to 5 | N/A | | Reserved. |
| 4 | GPI_11_STAT | Read only | 0 = GPI_11 (C4 pin) is low. 1 = GPI_11 (C4 pin) is high. |
| 3 | GPI_10_STAT | Read only | 0 = GPI_10 (C3 pin) is low. 1 = GPI_10 (C3 pin) is high. |
| 2 | GPI_9_STAT | Read only | 0 = GPI_9 (C2 pin) is low. 1 = GPI_9 (C2 pin) is high. |
| 1 | GPI_8_STAT | Read only | 0 = GPI_8 (C1 pin) is low. 1 = GPI_8 (C1 pin) is high. |
| 0 | GPI_7_STAT | Read only | 0 = GPI_7 (C0 pin) is low. 1 = GPI_7 (C0 pin) is high. |

RPULL_CONFIG_A Register 0x17**Table 31. RPULL_CONFIG_A Bit Descriptions**

| Bit(s) | Bit Name | Access | Description |
|--------|-------------|------------|---|
| 7 to 6 | R3_PULL_CFG | Read/write | 00 = enable 300 k Ω pull-up resistor. 01 = enable 300 k Ω pull-down resistor. 10 = enable 100 k Ω pull-up resistor. 11 = disable all pull-up/pull-down resistors. |
| 5 to 4 | R2_PULL_CFG | Read/write | 00 = enable 300 k Ω pull-up resistor. 01 = enable 300 k Ω pull-down resistor. 10 = enable 100 k Ω pull-up resistor. 11 = disable all pull-up/pull-down resistors. |
| 3 to 2 | R1_PULL_CFG | Read/write | 00 = enable 300 k Ω pull-up resistor. 01 = enable 300 k Ω pull-down resistor. 10 = enable 100 k Ω pull-up resistor. 11 = disable all pull-up/pull-down resistors. |
| 1 to 0 | R0_PULL_CFG | Read/write | 00 = enable 300 k Ω pull-up resistor. 01 = enable 300 k Ω pull-down resistor. 10 = enable 100 k Ω pull-up resistor. 11 = disable all pull-up/pull-down resistors. |

ADP5585AC_Z-00-R7, ADP5585AC_Z-01-R7, ADP5585ACPZ-03-R7 Default = 0000 0000

ADP5585ACBZ-02-R7 Default = 1100 0011

ADP5585ACBZ-04-R7 Default = 0101 0101

RPULL_CONFIG_B Register 0x18**Table 32. RPULL_CONFIG_B Bit Descriptions**

| Bit(s) | Bit Name | Access | Description |
|--------|-------------|------------|--|
| 7 to 4 | N/A | | Reserved. |
| 3 to 2 | R5_PULL_CFG | Read/write | (Reserved except for ADP5585ACBZ-01-R7 options) 00 = enable 300 k Ω pull-up resistor. 01 = enable 300 k Ω pull-down resistor. 10 = enable 100 k Ω pull-up resistor. 11 = disable all pull-up/pull-down resistors. |
| 1 to 0 | R4_PULL_CFG | Read/write | 00 = enable 300 k Ω pull-up resistor. 01 = enable 300 k Ω pull-down resistor. 10 = enable 100 k Ω pull-up resistor. 11 = disable all pull-up/pull-down resistors. |

ADP5585AC_Z-00-R7, ADP5585AC_Z-01-R7, ADP5585ACPZ-03-R7 Default = 0000 0000

ADP5585ACBZ-02-R7 Default = 0000 0011

ADP5585ACBZ-04-R7 Default = 0000 0101

RPULL_CONFIG_C Register 0x19

Table 33. RPULL_CONFIG_C Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-------------|------------|---|
| 7 to 6 | C3_PULL_CFG | Read/write | 00 = enable 300 kΩ pull-up resistor. 01 = enable 300 kΩ pull-down resistor. 10 = enable 100 kΩ pull-up resistor. 11 = disable all pull-up/pull-down resistors. |
| 5 to 4 | C2_PULL_CFG | Read/write | 00 = enable 300 kΩ pull-up resistor. 01 = enable 300 kΩ pull-down resistor. 10 = enable 100 kΩ pull-up resistor. 11 = disable all pull-up/pull-down resistors. |
| 3 to 2 | C1_PULL_CFG | Read/write | 00 = enable 300 kΩ pull-up resistor. 01 = enable 300 kΩ pull-down resistor. 10 = enable 100 kΩ pull-up resistor. 11 = disable all pull-up/pull-down resistors. |
| 1 to 0 | C0_PULL_CFG | Read/write | 00 = enable 300 kΩ pull-up resistor. 01 = enable 300 kΩ pull-down resistor. 10 = enable 100 kΩ pull-up resistor. 11 = disable all pull-up/pull-down resistors. |

ADP5585AC_Z-00-R7, ADP5585AC_Z-01-R7, ADP5585ACBZ-02-R7, ADP5585ACPZ-03-R7 Default = 0000 0000

ADP5585ACBZ-04-R7 Default = 0101 0101

RPULL_CONFIG_D Register 0x1A

Table 34. RPULL_CONFIG_D Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-------------|------------|---|
| 7 to 2 | N/A | | Reserved. |
| 1 to 0 | C4_PULL_CFG | Read/write | 00 = enable 300 kΩ pull-up resistor. 01 = enable 300 kΩ pull-down resistor. 10 = enable 100 kΩ pull-up resistor. 11 = disable all pull-up/pull-down resistors. |

ADP5585AC_Z-00-R7, ADP5585AC_Z-01-R7, ADP5585ACPZ-03-R7 Default = 0000 0000

ADP5585ACBZ-02-R7 Default = 0000 0011

ADP5585ACBZ-04-R7 Default = 0000 0001

GPI_INT_LEVEL_A Register 0x1B

Table 35. GPI_INT_LEVEL_A Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-----------------|------------|---|
| 7 to 6 | N/A | | Reserved. |
| 5 | GPI_6_INT_LEVEL | Read/write | (Reserved except for ADP5585AC_Z-01-R7 options) 0 = GPI_6 interrupt is active low (GPI_6_INT sets whenever R5 is low). 1 = GPI_6 interrupt is active high (GPI_6_INT sets whenever R5 is high). |
| 4 | GPI_5_INT_LEVEL | Read/write | 0 = GPI_5 interrupt is active low (GPI_5_INT sets whenever R4 is low). 1 = GPI_5 interrupt is active high (GPI_5_INT sets whenever R4 is high). |
| 3 | GPI_4_INT_LEVEL | Read/write | 0 = GPI_4 interrupt is active low (GPI_4_INT sets whenever R3 is low). 1 = GPI_4 interrupt is active high (GPI_4_INT sets whenever R3 is high). |
| 2 | GPI_3_INT_LEVEL | Read/write | 0 = GPI_3 interrupt is active low (GPI_3_INT sets whenever R2 is low). 1 = GPI_3 interrupt is active high (GPI_3_INT sets whenever R2 is high). |
| 1 | GPI_2_INT_LEVEL | Read/write | 0 = GPI_2 interrupt is active low (GPI_2_INT sets whenever R1 is low). 1 = GPI_2 interrupt is active high (GPI_2_INT sets whenever R1 is high). |
| 0 | GPI_1_INT_LEVEL | Read/write | 0 = GPI_1 interrupt is active low (GPI_1_INT sets whenever R0 is low). 1 = GPI_1 interrupt is active high (GPI_1_INT sets whenever R0 is high). |

GPI_INT_LEVEL_B Register 0x1C

Table 36. Register 0x1C, GPI_INT_LEVEL_B Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|------------------|------------|--|
| 7 to 5 | N/A | | Reserved. |
| 4 | GPI_11_INT_LEVEL | Read/write | 0 = GPI_11 interrupt is active low (GPI_11_INT sets whenever R10 is low). 1 = GPI_11 interrupt is active high (GPI_11_INT sets whenever R10 is high). |
| 3 | GPI_10_INT_LEVEL | Read/write | 0 = GPI_10 interrupt is active low (GPI_10_INT sets whenever R9 is low). 1 = GPI_10 interrupt is active high (GPI_10_INT sets whenever R9 is high). |
| 2 | GPI_9_INT_LEVEL | Read/write | 0 = GPI_9 interrupt is active low (GPI_9_INT sets whenever R8 is low). 1 = GPI_9 interrupt is active high (GPI_9_INT sets whenever R8 is high). |
| 1 | GPI_8_INT_LEVEL | Read/write | 0 = GPI_8 interrupt is active low (GPI_8_INT sets whenever R7 is low). 1 = GPI_8 interrupt is active high (GPI_8_INT sets whenever R7 is high). |
| 0 | GPI_7_INT_LEVEL | Read/write | 0 = GPI_7 interrupt is active low (GPI_7_INT sets whenever R6 is low). 1 = GPI_7 interrupt is active high (GPI_7_INT sets whenever R6 is high). |

GPI_EVENT_EN_A Register 0x1D

Table 37. GPI_EVENT_EN_A Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|----------------|------------|---|
| 7 to 6 | N/A | | Reserved. |
| 5 | GPI_6_EVENT_EN | Read/write | (Reserved except for ADP5585AC_Z-01-R7 options) 0 = disable GPI events from GPI 6. 1 = allow GPI 6 activity to generate events on the FIFO ¹ . |
| 4 | GPI_5_EVENT_EN | Read/write | 0 = disable GPI events from GPI 5. 1 = allow GPI 5 activity to generate events on the FIFO ¹ . |
| 3 | GPI_4_EVENT_EN | Read/write | 0 = disable GPI events from GPI 4. 1 = allow GPI 4 activity to generate events on the FIFO ¹ . |
| 2 | GPI_3_EVENT_EN | Read/write | 0 = disable GPI events from GPI 3. 1 = allow GPI 3 activity to generate events on the FIFO ¹ . |
| 1 | GPI_2_EVENT_EN | Read/write | 0 = disable GPI events from GPI 2. 1 = allow GPI 2 activity to generate events on the FIFO ¹ . |
| 0 | GPI_1_EVENT_EN | Read/write | 0 = disable GPI events from GPI 1. 1 = allow GPI 1 activity to generate events on the FIFO ¹ . |

¹ GPIs in this mode are considered FIFO events and can be used for unlock purposes. GPI activity in this mode causes EVENT_INT interrupts. GPIs in this mode do not generate GPI_INT interrupts.

GPI_EVENT_EN_B Register 0x1E

Table 38. GPI_EVENT_EN_B Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-----------------|------------|--|
| 7 to 5 | N/A | | Reserved. |
| 4 | GPI_11_EVENT_EN | Read/write | 0 = disable GPI events from GPI 11. 1 = allow GPI 11 activity to generate events on the FIFO ¹ . |
| 3 | GPI_10_EVENT_EN | Read/write | 0 = disable GPI events from GPI 10. 1 = allow GPI 10 activity to generate events on the FIFO ¹ . |
| 2 | GPI_9_EVENT_EN | Read/write | 0 = disable GPI events from GPI 9. 1 = allow GPI 9 activity to generate events on the FIFO ¹ . |
| 1 | GPI_8_EVENT_EN | Read/write | 0 = disable GPI events from GPI 8. 1 = allow GPI 8 activity to generate events on the FIFO ¹ . |
| 0 | GPI_7_EVENT_EN | Read/write | 0 = disable GPI events from GPI 7. 1 = allow GPI 7 activity to generate events on the FIFO ¹ . |

¹ GPIs in this mode are considered FIFO events and can be used for unlock purposes. GPI activity in this mode cause EVENT_INT interrupts. GPIs in this mode do not generate GPI_INT interrupts.

GPI_EVENT_INTERRUPT_EN_A Register 0x1F**Table 39. GPI_INTERRUPT_EN_A Bit Descriptions**

| Bit(s) | Bit Name | Access | Description |
|--------|--------------|------------|--|
| 7 to 6 | N/A | | Reserved. |
| 5 | GPI_6_INT_EN | Read/write | (Reserved except for ADP5585AC_Z-01-R7 options) 0 = GPI_6_INT is disabled. 1 = GPI_6_INT enabled. Asserts the GPI_INT bit (Register 0x01, Bit 1) if GPI_6_INT is set and the GPI 6 interrupt condition is met. |
| 4 | GPI_5_INT_EN | Read/write | 0 = GPI_5_INT is disabled. 1 = GPI_5_INT enabled. Asserts the GPI_INT bit (Register 0x01, Bit 1) if GPI_5_INT is set and the GPI 5 interrupt condition is met. |
| 3 | GPI_4_INT_EN | Read/write | 0 = GPI_4_INT is disabled. 1 = GPI_4_INT enabled. Asserts the GPI_INT bit (Register 0x01, Bit 1) if GPI_4_INT is set and the GPI 4 interrupt condition is met. |
| 2 | GPI_3_INT_EN | Read/write | 0 = GPI_3_INT is disabled. 1 = GPI_3_INT enabled. Asserts the GPI_INT bit (Register 0x01, Bit 1) if GPI_3_INT is set and the GPI 3 interrupt condition is met. |
| 1 | GPI_2_INT_EN | Read/write | 0 = GPI_2_INT is disabled. 1 = GPI_2_INT enabled. Asserts the GPI_INT bit (Register 0x01, Bit 1) if GPI_2_INT is set and the GPI 2 interrupt condition is met. |
| 0 | GPI_1_INT_EN | Read/write | 0 = GPI_1_INT is disabled. 1 = GPI_1_INT enabled. Asserts the GPI_INT bit (Register 0x01, Bit 1) if GPI_1_INT is set and the GPI 1 interrupt condition is met. |

GPI_EVENT_INTERRUPT_EN_B Register 0x20**Table 40. GPI_INTERRUPT_EN_B Bit Descriptions**

| Bit(s) | Bit Name | Access | Description |
|--------|---------------|------------|---|
| 7 to 5 | N/A | | Reserved. |
| 4 | GPI_11_INT_EN | Read/write | 0 = GPI_11_INT is disabled. 1 = GPI_11_INT enabled. Asserts the GPI_INT bit (Register 0x01, Bit 1) if GPI_11_INT is set and the GPI 11 interrupt condition is met. |
| 3 | GPI_10_INT_EN | Read/write | 0 = GPI_10_INT is disabled. 1 = GPI_10_INT enabled. Asserts the GPI_INT bit (Register 0x01, Bit 1) if GPI_10_INT is set and the GPI 10 interrupt condition is met. |
| 2 | GPI_9_INT_EN | Read/write | 0 = GPI_9_INT is disabled. 1 = GPI_9_INT enabled. Asserts the GPI_INT bit (Register 0x01, Bit 1) if GPI_9_INT is set and the GPI 9 interrupt condition is met. |
| 1 | GPI_8_INT_EN | Read/write | 0 = GPI_8_INT is disabled. 1 = GPI_8_INT enabled. Asserts the GPI_INT bit (Register 0x01, Bit 1) if GPI_8_INT is set and the GPI 8 interrupt condition is met. |
| 0 | GPI_7_INT_EN | Read/write | 0 = GPI_7_INT is disabled. 1 = GPI_7_INT enabled. Asserts the GPI_INT bit (Register 0x01, Bit 1) if GPI_7_INT is set and the GPI 7 interrupt condition is met. |

DEBOUNCE_DIS_A Register 0x21**Table 41. DEBOUNCE_DIS_A Bit Descriptions**

| Bit(s) | Bit Name | Access | Description |
|--------|---------------|------------|--|
| 7 to 6 | N/A | | Reserved. |
| 5 | GPI_6_DEB_DIS | Read/write | (Reserved except for ADP5585AC_Z-01-R7 options) 0 = debounce enabled on GPI 6. 1 = debounce disabled on GPI 6. |
| 4 | GPI_5_DEB_DIS | Read/write | 0 = debounce enabled on GPI 5. 1 = debounce disabled on GPI 5. |
| 3 | GPI_4_DEB_DIS | Read/write | 0 = debounce enabled on GPI 4. 1 = debounce disabled on GPI 4. |
| 2 | GPI_3_DEB_DIS | Read/write | 0 = debounce enabled on GPI 3. 1 = debounce disabled on GPI 3. |
| 1 | GPI_2_DEB_DIS | Read/write | 0 = debounce enabled on GPI 2. 1 = debounce disabled on GPI 2. |
| 0 | GPI_1_DEB_DIS | Read/write | 0 = debounce enabled on GPI 1. 1 = debounce disabled on GPI 1. |

DEBOUNCE_DIS_B Register 0x22**Table 42. DEBOUNCE_DIS_B Bit Descriptions**

| Bit(s) | Bit Name | Access | Description |
|--------|----------------|------------|---|
| 7 to 5 | N/A | | Reserved. |
| 4 | GPI_11_DEB_DIS | Read/write | 0 = debounce enabled on GPI 11. 1 = debounce disabled on GPI 11. |
| 3 | GPI_10_DEB_DIS | Read/write | 0 = debounce enabled on GPI 10. 1 = debounce disabled on GPI 10. |
| 2 | GPI_9_DEB_DIS | Read/write | 0 = debounce enabled on GPI 9. 1 = debounce disabled on GPI 9. |
| 1 | GPI_8_DEB_DIS | Read/write | 0 = debounce enabled on GPI 8. 1 = debounce disabled on GPI 8. |
| 0 | GPI_7_DEB_DIS | Read/write | 0 = debounce enabled on GPI 7. 1 = debounce disabled on GPI 7. |

GPO_DATA_OUT_A Register 0x23**Table 43. GPO_DATA_OUT_A Bit Descriptions**

| Bit(s) | Bit Name | Access | Description |
|--------|------------|------------|--|
| 7 to 6 | N/A | | Reserved. |
| 5 | GPO_6_DATA | Read/write | (Reserved except for ADP5585AC_Z-01-R7 options) 0 = sets output low. 1 = sets output high. |
| 4 | GPO_5_DATA | Read/write | 0 = sets output low. 1 = sets output high. |
| 3 | GPO_4_DATA | Read/write | 0 = sets output low. 1 = sets output high. |
| 2 | GPO_3_DATA | Read/write | 0 = sets output low. 1 = sets output high. |
| 1 | GPO_2_DATA | Read/write | 0 = sets output low. 1 = sets output high. |
| 0 | GPO_1_DATA | Read/write | 0 = sets output low. 1 = sets output high. |

GPO_DATA_OUT_B Register 0x24**Table 44. GPO_DATA_OUT_B Bit Descriptions**

| Bit(s) | Bit Name | Access | Description |
|--------|-------------|------------|---|
| 7 to 5 | N/A | | Reserved. |
| 4 | GPO_11_DATA | Read/write | 0 = sets output low. 1 = sets output high. |
| 3 | GPO_10_DATA | Read/write | 0 = sets output low. 1 = sets output high. |
| 2 | GPO_9_DATA | Read/write | 0 = sets output low. 1 = sets output high. |
| 1 | GPO_8_DATA | Read/write | 0 = sets output low. 1 = sets output high. |
| 0 | GPO_7_DATA | Read/write | 0 = sets output low. 1 = sets output high. |

GPO_OUT_MODE_A Register 0x25**Table 45. Register 0x25, GPO_OUT_MODE_A Bit Descriptions**

| Bit(s) | Bit Name | Access | Description |
|--------|----------------|------------|--|
| 7 to 6 | N/A | | Reserved. |
| 5 | GPO_6_OUT_MODE | Read/write | (Reserved except for ADP5585AC_Z-01-R7 options) 0 = push/pull. 1 = open drain. |
| 4 | GPO_5_OUT_MODE | Read/write | 0 = push/pull. 1 = open drain. |
| 3 | GPO_4_OUT_MODE | Read/write | 0 = push/pull. 1 = open drain. |
| 2 | GPO_3_OUT_MODE | Read/write | 0 = push/pull. 1 = open drain. |
| 1 | GPO_2_OUT_MODE | Read/write | 0 = push/pull. 1 = open drain. |
| 0 | GPO_1_OUT_MODE | Read/write | 0 = push/pull. 1 = open drain. |

GPO_OUT_MODE_B Register 0x26**Table 46. Register 0x26, GPO_OUT_MODE_B Bit Descriptions**

| Bit(s) | Bit Name | Access | Description |
|--------|-----------------|------------|-----------------------------------|
| 7 to 5 | N/A | | Reserved. |
| 4 | GPO_11_OUT_MODE | Read/write | 0 = push/pull. 1 = open drain. |
| 3 | GPO_10_OUT_MODE | Read/write | 0 = push/pull. 1 = open drain. |
| 2 | GPO_9_OUT_MODE | Read/write | 0 = push/pull. 1 = open drain. |
| 1 | GPO_8_OUT_MODE | Read/write | 0 = push/pull. 1 = open drain. |
| 0 | GPO_7_OUT_MODE | Read/write | 0 = push/pull. 1 = open drain. |

GPIO_DIRECTION_A Register 0x27

Table 47. GPIO_DIRECTION_A Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|------------|------------|--|
| 7 to 6 | N/A | | Reserved. |
| 5 | GPIO_6_DIR | Read/write | (Reserved except for ADP5585AC_Z-01-R7 options) 0 = GPIO 6 is an input. 1 = GPIO 6 is an output. |
| 4 | GPIO_5_DIR | Read/write | 0 = GPIO 5 is an input. 1 = GPIO 5 is an output. |
| 3 | GPIO_4_DIR | Read/write | 0 = GPIO 4 is an input. 1 = GPIO 4 is an output. |
| 2 | GPIO_3_DIR | Read/write | 0 = GPIO 3 is an input. 1 = GPIO 3 is an output. |
| 1 | GPIO_2_DIR | Read/write | 0 = GPIO 2 is an input. 1 = GPIO 2 is an output. |
| 0 | GPIO_1_DIR | Read/write | 0 = GPIO 1 is an input. 1 = GPIO 1 is an output. |

GPIO_DIRECTION_B Register 0x28

Table 48. Register 0x28, GPIO_DIRECTION_B Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-------------|------------|---|
| 7 to 5 | N/A | | Reserved. |
| 4 | GPIO_11_DIR | Read/write | 0 = GPIO 11 is an input. 1 = GPIO 11 is an output. |
| 3 | GPIO_10_DIR | Read/write | 0 = GPIO 10 is an input. 1 = GPIO 10 is an output. |
| 2 | GPIO_9_DIR | Read/write | 0 = GPIO 9 is an input. 1 = GPIO 9 is an output. |
| 1 | GPIO_8_DIR | Read/write | 0 = GPIO 8 is an input. 1 = GPIO 8 is an output. |
| 0 | GPIO_7_DIR | Read/write | 0 = GPIO 7 is an input. 1 = GPIO 7 is an output. |

RESET1_EVENT_A Register 0x29

Table 49. RESET1_EVENT_A Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|----------------------|------------|---|
| 7 | RESET1_EVENT_A_LEVEL | Read/write | Defines which level the first reset event should be to generate the RESET1 signal. For key events, use the following settings: 0 = not applicable; releases not used for reset generation. 1 = press is used as reset event. For GPIOs and logic outputs configured for FIFO updates, use the following settings: 0 = inactive event used as reset condition. 1 = active event used as reset condition. |
| 6 to 0 | RESET1_EVENT_A[6:0] | Read/write | Defines an event that can be used to generate the RESET1 signal. Up to three events can be defined for generating the RESET1 signal, using RESET1_EVENT_A[6:0], RESET1_EVENT_B[6:0], and RESET1_EVENT_C[6:0]. If one of the registers is 0, that register is not used for reset generation. All reset events must be detected at the same time to trigger the reset. |

RESET1_EVENT_B Register 0x2A

Table 50. RESET1_EVENT_B Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|----------------------|------------|--|
| 7 | RESET1_EVENT_B_LEVEL | Read/write | Defines which level the second reset event should be to generate the RESET1 signal. Refer to Table 49. |
| 6 to 0 | RESET1_EVENT_B[6:0] | Read/write | Defines an event that can be used to generate the RESET1 signal. Refer to Table 11. |

RESET1_EVENT_C Register 0x2B

Table 51. RESET1_EVENT_C Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|----------------------|------------|--|
| 7 | RESET1_EVENT_C_LEVEL | Read/write | Defines which level the second reset event should be to generate the RESET1 signal. Refer to Table 49. |
| 6 to 0 | RESET1_EVENT_C[6:0] | Read/write | Defines an event that can be used to generate the RESET1 signal. Refer to Table 11. |

RESET2_EVENT_A Register 0x2C

Table 52. RESET2_EVENT_A Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|----------------------|------------|---|
| 7 | RESET2_EVENT_A_LEVEL | Read/write | Defines which level the first reset event should be to generate the RESET2 signal. For key events, use the following settings: 0 = not applicable; releases not used for reset generation. 1 = press is used as reset event. For GPIOs and logic outputs configured for FIFO updates, use the following settings: 0 = inactive event used as reset condition. 1 = active event used as reset condition. |
| 6 to 0 | RESET2_EVENT_A[6:0] | Read/write | Defines an event that can be used to generate the RESET2 signal. Up to two events can be defined for generating the RESET2 signal, using RESET2_EVENT_A[6:0], and RESET2_EVENT_B[6:0]. If one of the registers is 0, that register is not used for reset generation. All reset events must be detected at the same time to trigger the reset. |

RESET2_EVENT_B Register 0x2D

Table 53. RESET2_EVENT_B Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|----------------------|------------|--|
| 7 | RESET2_EVENT_B_LEVEL | Read/write | Defines which level the second reset event should be to generate the RESET2 signal. Refer to Table 52. |
| 6 to 0 | RESET2_EVENT_B[6:0] | Read/write | Defines an event that can be used to generate the RESET2 signal. Refer to Table 11. |

RESET_CFG Register 0x2E

Table 54. RESET_CFG Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-----------------|------------|---|
| 7 | RESET2_POL | Read/write | Sets the polarity of RESET2. 0 = RESET2 is active low. 1 = RESET2 is active high. |
| 6 | RESET1_POL | Read/write | Sets the polarity of RESET1. 0 = RESET1 is active low. 1 = RESET1 is active high. |
| 5 | RST_PASSTHRU_EN | Read/write | Allows the RST pin to override (OR with) the RESET1 signal. This function not applicable to RESET2. |

| Bit(s) | Bit Name | Access | Description |
|--------|------------------------|------------|---|
| 4 to 2 | RESET_TRIG_TIME[2:0] | Read/write | Defines the length of time that the reset events must be active before a reset signal is generated. All events must be active at the same time for the same duration. RESET_TRIG_TIME[2:0] is common to both RESET1 and RESET2. 000 = immediate. 001 = 1.0 sec. 010 = 1.5 sec. 011 = 2.0 sec. 100 = 2.5 sec. 101 = 3.0 sec. 110 = 3.5 sec. 111 = 4.0 sec. |
| 1 to 0 | RESET_PULSE_WIDTH[1:0] | Read/write | Defines the pulse width of the reset signals. RESET_PULSE_WIDTH[1:0] is common to both RESET1 and RESET2. 00 = 500 μ s. 01 = 1 ms. 10 = 2 ms. 11 = 10 ms. |

PWM_OFFT_LOW Register 0x2F

Table 55. Register 0x2F, PWM_OFFT_LOW Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|------------------------|------------|-----------------------------------|
| 7 to 0 | PWM_OFFT_LOW_BYTE[7:0] | Read/write | Lower eight bits of PWM off time. |

PWM_OFFT_HIGH Register 0x30

Table 56. PWM_OFFT_HIGH Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-------------------------|------------|-----------------------------------|
| 7 to 0 | PWM_OFFT_HIGH_BYTE[7:0] | Read/write | Upper eight bits of PWM off time. |

PWM_ONT_LOW Register 0x31

Table 57. PWM_ONT_LOW Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-----------------------|------------|----------------------------------|
| 7 to 0 | PWM_ONT_LOW_BYTE[7:0] | Read/write | Lower eight bits of PWM on time. |

PWM_ONT_HIGH Register 0x32

Table 58. PWM_ONT_HIGH Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|------------------------|------------|--|
| 7 to 0 | PWM_ONT_HIGH_BYTE[7:0] | Read/write | Upper eight bits of PWM on time. Note that updated PWM times are not latched until this byte is written to. PWM count times are referenced from the internal oscillator. The fastest oscillator setting is 500 kHz (2 μ s increments). Therefore, the maximum period is $2 \mu\text{s} \times 2^{16} = 131 \text{ ms}$ This gives PWM frequencies from 500 kHz down to 7.6 Hz. |

PWM_CFG Register 0x33

Table 59. PWM_CFG Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|------------|------------|--|
| 7 to 3 | N/A | | Reserved. |
| 2 | PWM_IN_AND | | 0 = no external AND'ing. 1 = PWM signal AND'ed with an externally supplied PWM signal (C3). |
| 1 | PWM_MODE | Read/write | Defines PWM mode. 0 = continuous. 1 = executes one PWM period, then sets PWM_EN to 0. |
| 0 | PWM_EN | Read/write | Enable PWM generator. |

LOGIC_CFG Register 0x34

Table 60. LOGIC_CFG Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|----------------|------------|---|
| 7 | N/A | | Reserved. |
| 6 | LY_INV | Read/write | 0 = LY output not inverted before passing into logic block. 1 = inverts output LY from the logic block. |
| 5 | LC_INV | Read/write | 0 = LC input not inverted before passing into the logic block. 1 = inverts input LC before passing it into the logic block. |
| 4 | LB_INV | R/W | 0 = LB input not inverted before passing into the logic block. 1 = inverts input LB before passing it into the logic block. |
| 3 | LA_INV | R/W | 0 = LA input not inverted before passing into the logic block. 1 = inverts input LA before passing it into the logic block. |
| 2 to 0 | LOGIC_SEL[2:0] | R/W | Configures the digital mux for the logic block. Refer to Figure 19. 000 = off/disable. 001 = AND. 010 = OR. 011 = XOR. 100 = FF. 101 = IN_LA. 110 = IN_LB. 111 = IN_LC. |

LOGIC_FF_CFG Register 0x35

Table 61. LOGIC_FF_CFG Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|----------|------------|--|
| 7 to 2 | N/A | Read/write | Reserved. |
| 1 | FF_SET | Read/write | 0 = FF not set in the logic block. Refer to Figure 19. 1 = set FF in the logic block. |
| 0 | FF_CLR | Read/write | 0 = FF not cleared in the logic block. Refer to Figure 19. 1 = clear FF in the logic block. |

LOGIC_INT_EVENT_EN Register 0x36

Table 62. LOGIC_INT_EVENT_EN Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-----------------|------------|---|
| 7 to 3 | N/A | | Reserved. |
| 2 | LY_DBNC_DIS | Read/write | 0 = output of the logic block is debounced before entering the event/interrupt block. 1 = output of the logic block is not debounced before entering the event/interrupt block. Use with caution because glitches may generate interrupts prematurely. |
| 1 | LOGIC_EVENT_EN | Read/write | 0 = LY cannot generate interrupt. 1 = allow LY activity to generate events on the FIFO. |
| 0 | LOGIC_INT_LEVEL | Read/write | Configure the logic level of LY that generates an interrupt. 0 = LY is active low. 1 = LY is active high. |

POLL_TIME_CFG Register 0x37

Table 63. Register 0x37, POLL_TIME_CFG Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|--------------------|------------|---|
| 7 to 2 | N/A | | Reserved. |
| 1 to 0 | KEY_POLL_TIME[1:0] | Read/write | Configure time between consecutive scan cycles. 00 = 10 ms. 01 = 20 ms. 10 = 30 ms. 11 = 40 ms. |

PIN_CONFIG_A Register 0x38

Table 64. PIN_CONFIG_A Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-----------|------------|---|
| 7 to 6 | N/A | | Reserved. |
| 5 | R5_CONFIG | Read/write | Reserved except for ADP5585AC_Z-01-R7 options) 0 = GPIO 6. 1 = Row 5. |
| 4 | R4_CONFIG | Read/write | 0 = GPIO 5 (see R4_EXTEND_CFG in Table 66 for alternate configuration, RESET1). 1 = Row 4 |
| 3 | R3_CONFIG | Read/write | 0 = GPIO 4 (see R3_EXTEND_CFG[1:0] in Table 66 for alternate configuration, LC/PWM_OUT). 1 = Row 3 |
| 2 | R2_CONFIG | Read/write | 0 = GPIO 3 1 = Row 2 |
| 1 | R1_CONFIG | Read/write | 0 = GPIO 2 1 = Row 1 |
| 0 | R0_CONFIG | Read/write | 0 = GPIO 1/LY (see R0_EXTEND_CFG in Table 66 for alternate configuration, LY). 1 = Row 0 |

PIN_CONFIG_B Register 0x39

Table 65. PIN_CONFIG_B Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-----------|------------|---|
| 7 to 5 | N/A | | Reserved. |
| 4 | C4_CONFIG | Read/write | 0 = GPIO 11 (see C4_EXTEND_CFG in Table 66 for alternate configuration, RESET2). 1 = Column 4. |
| 3 | C3_CONFIG | Read/write | 0 = GPIO 10. 1 = Column 3. |
| 2 | C2_CONFIG | Read/write | 0 = GPIO 9. 1 = Column 2. |
| 1 | C1_CONFIG | Read/write | 0 = GPIO 8. 1 = Column 1. |
| 0 | C0_CONFIG | Read/write | 0 = GPIO 7. 1 = Column 0. |

PIN_CONFIG_C Register 0x3A

Table 66. PIN_CONFIG_D Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|---------------|------------|--|
| 7 | PULL_SELECT | Read/write | 0 = 300 kΩ resistor used for row pull-up during key scanning. 1 = 100 kΩ resistor used for row pull-up during key scanning. |
| 6 | C4_EXTEND_CFG | Read/write | 0 = C4 remains configured as GPIO 11. 1 = C4 reconfigured as RESET2 output. |

| Bit(s) | Bit Name | Access | Description |
|--------|--------------------|------------|--|
| 5 | R4_EXTEND_CFG | Read/write | 0 = R4 remains configured as GPIO 5. 1 = R4 reconfigured as RESET1 output. |
| 4 | N/A | | Reserved. |
| 3 to 2 | R3_EXTEND_CFG[1:0] | Read/write | 00 = R3 remains configured as GPIO 4. 01 = R3 reconfigured as LC input for the logic block. 10 = R3 reconfigured as PWM_OUT output from PWM block. 11 = unused. |
| 1 | N/A | | Reserved. |
| 0 | R0_EXTEND_CFG | Read/write | 0 = R0 remains configured as GPIO 1. 1 = R0 reconfigured as LY output from the logic block. |

GENERAL_CFG Register 0x3B

Table 67. GENERAL_CFG Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|--------------------------------------|------------|--|
| 7 | OSC_EN | Read/write | 0 = disable internal 1 MHz oscillator. 1 = enable internal 1 MHz oscillator. |
| 6 to 5 | OSC_FREQ[1:0] | Read/write | Sets the input clock frequency fed from the base 1 MHz oscillator to the digital core. Slower frequencies result in less quiescent current, but key and GPI scan times increase. 00 = 50 kHz. 01 = 100 kHz. 10 = 200 kHz. 11 = 500 kHz. |
| 4 to 2 | N/A | | Reserved. |
| 1 | $\overline{\text{INT}}_{\text{CFG}}$ | Read/write | Configure the behavior of the $\overline{\text{INT}}$ pin if the user tries to clear it while an interrupt is pending. 0 = $\overline{\text{INT}}$ pin remains asserted if an interrupt is pending. 1 = $\overline{\text{INT}}$ pin deasserts for 50 μs and reasserts if an interrupt is pending. |
| 0 | $\overline{\text{RST}}_{\text{CFG}}$ | R/W | Configure the response ADP5585 has to the $\overline{\text{RST}}$ pin. 0 = ADP5585 resets if $\overline{\text{RST}}$ is low. 1 = ADP5585 does not reset if $\overline{\text{RST}}$ is low. |

INT_EN Register 0x3C

Table 68. INT_EN Bit Descriptions

| Bit(s) | Bit Name | Access | Description |
|--------|-------------|------------|--|
| 7 to 5 | N/A | | Reserved. |
| 4 | LOGIC_IEN | Read/write | 0 = Logic 1 interrupt is disabled. 1 = assert the $\overline{\text{INT}}$ pin if LOGIC_INT is set. |
| 3 | N/A | | Reserved. |
| 2 | OVRFLOW_IEN | Read/write | 0 = overflow interrupt is disabled. 1 = assert the $\overline{\text{INT}}$ pin if OVRFLOW_INT is set. |
| 1 | GPI_IEN | Read/write | 0 = GPI interrupt is disabled. 1 = assert the $\overline{\text{INT}}$ pin if GPI_INT is set. |
| 0 | EVENT_IEN | Read/write | 0 = event interrupt is disabled. 1 = assert the $\overline{\text{INT}}$ pin if EVENT_INT is set. |

APPLICATIONS DIAGRAM

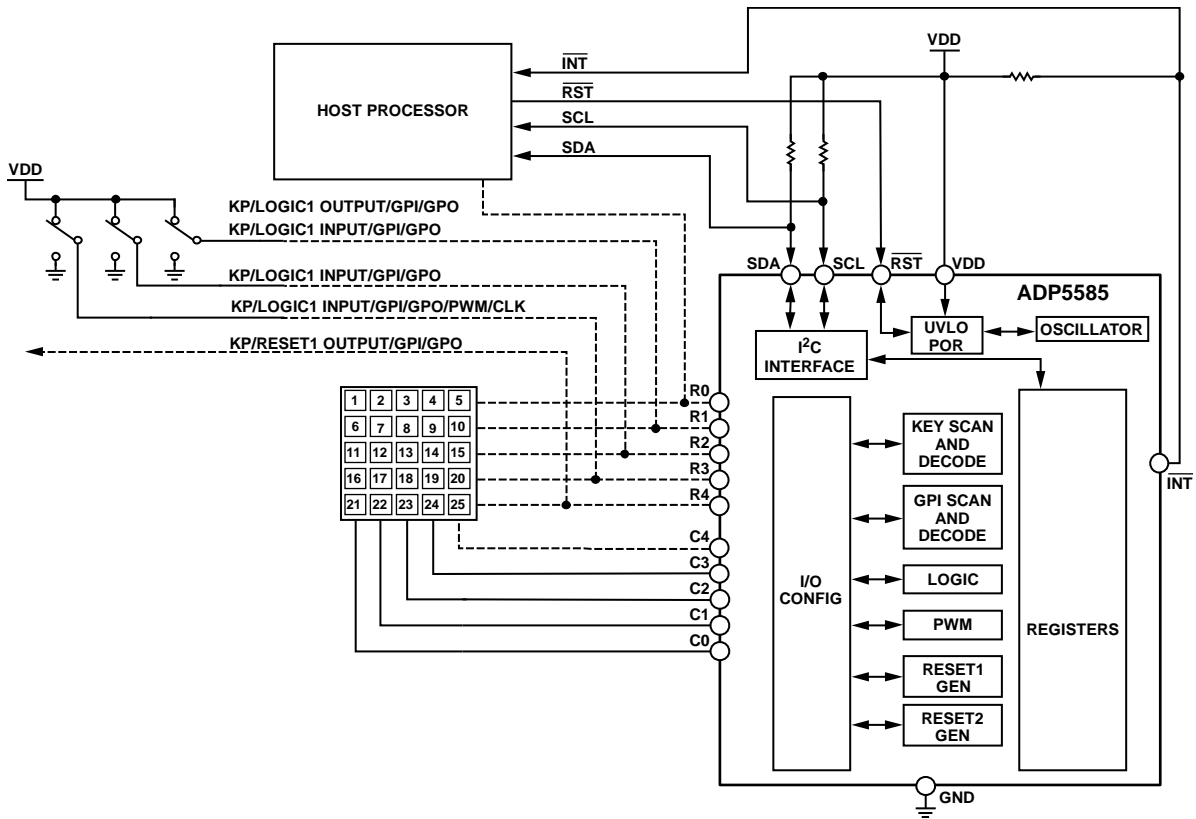


Figure 27. Typical Application Schematic

09841-026

OUTLINE DIMENSIONS

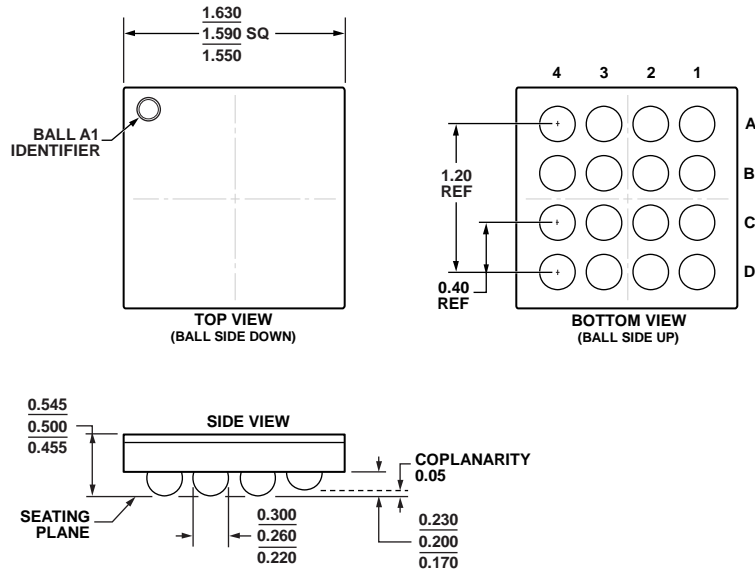
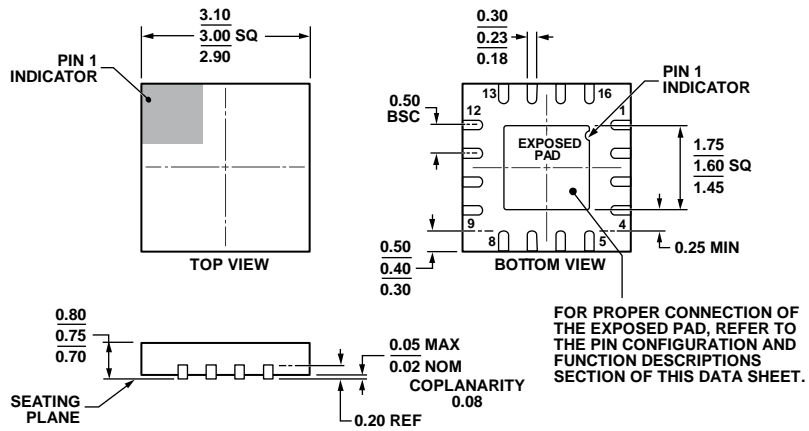


Figure 28. 16-Ball Wafer Level Chip Scale Package [WLCSP] (CB-16-10)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 29. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] 3 x 3 mm Body, Very Very Thin Quad (CP-16-22)

Dimensions shown in millimeters

10-23-2012-A

08-16-2010-E

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option | Branding |
|--------------------|-------------------|--|----------------|----------|
| ADP5585ACBZ-00-R7 | -40°C to +85°C | 16-Ball Wafer Level Chip Scale Package [WLCSP] | CB-16-10 | |
| ADP5585ACBZ-01-R7 | -40°C to +85°C | 16-Ball Wafer Level Chip Scale Package [WLCSP] | CB-16-10 | |
| ADP5585ACBZ-02-R7 | -40°C to +85°C | 16-Ball Wafer Level Chip Scale Package [WLCSP] | CB-16-10 | |
| ADP5585ACBZ-04-R7 | -40°C to +85°C | 16-Ball Wafer Level Chip Scale Package [WLCSP] | CB-16-10 | |
| ADP5585ACPZ-00-R7 | -40°C to +85°C | 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-16-22 | LJM |
| ADP5585ACPZ-01-R7 | -40°C to +85°C | 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-16-22 | LJN |
| ADP5585ACPZ-03-R7 | -40°C to +85°C | 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-16-22 | LJP |
| ADP5585CP-EVALZ | | LFCSP Evaluation Board | CP-16-22 | |

¹ Z = RoHS Compliant Part.

NOTES

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).