



**3.3V/5V 1GHz  
DIFFERENTIAL PECL/ECL  
RECEIVER/BUFFER**

**Precision Edge®  
SY89206/216V**

**FEATURES**

- $f_{MAX} > 1.0\text{GHz}$
- 3.3V and 5V power supply options
- 250ps propagation delay
- High bandwidth output transitions
- Internal 75kΩ input pull-down resistors
- SY89206V: 100k PECL/ECL compatible
- SY89216V: 10k PECL/ECL compatible
- Industrial temperature range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Available in an ultra-small 8-pin (2mm x 2mm) MLF™ package



**Precision Edge®**

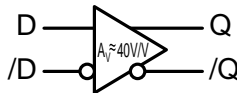
**DESCRIPTION**

The SY89206V and SY89216V are differential PECL/ECL receiver/buffers in a space-saving (2mm x 2mm) MLF™ package. The devices are functionally equivalent to the SY10/100EL16V, but feature a 70% smaller footprint.

The SY89206/216V provide a  $V_{BB}$  output for either single-ended use or as a DC bias for AC-coupling to the device. The  $V_{BB}$  pin should be used only as a bias for the SY89206/16V as its current sink/source capability is limited. Whenever used, the  $V_{BB}$  pin should be bypassed with a 0.01μF capacitor to  $V_{CC}$ .

Under open input conditions (pulled to  $V_{EE}$ ), internal input clamps will force the Q output LOW.

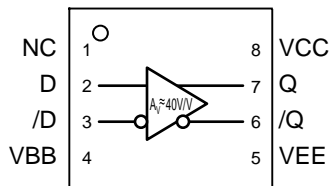
**BLOCK DIAGRAM**



**FUNCTIONAL CROSS REFERENCE**

Micrel Part Number	PECL/ECL	Functional Cross
SY89206V	100k	SY100EL16V
SY89216V	10k	SY10EL16V

**PACKAGE/ORDERING INFORMATION**



**8-Pin MLF™  
Ultra-Small Outline**

**Ordering Information<sup>(1)</sup>**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89206VMITR <sup>(2)</sup>	MLF-8	Industrial	206	Sn-Pb
SY89216VMITR <sup>(2)</sup>	MLF-8	Industrial	216	Sn-Pb
SY89206VMGTR <sup>(2)</sup>	MLF-8	Industrial	206 with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY89216VMGTR <sup>(2)</sup>	MLF-8	Industrial	216 with Pb-Free bar-line indicator	Pb-Free NiPdAu

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC electricals only.
2. Tape and Reel.

**PIN DESCRIPTION**

**SY89206V**

Pin Number	Pin Name	Type	Pin Function
2, 3	D, /D	100k ECL Input	Differential PECL/ECL Input: The signal inputs include internal 75kΩ pull-down resistors. If inputs are left open, Q output will default to LOW. See "Input Interface Applications" section for single-ended inputs.
7, 6	Q, /Q	100k ECL Output	Differential PECL/ECL Output: Q output defaults to LOW if D inputs left open. See "Output Interface Applications" section for recommendations on terminations.
8	VCC	Positive Power Supply	Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors.
5	VEE Exposed Pad	Negative Power Supply	Negative Power Supply: VEE and exposed pad must be tied to most negative supply. For PECL/LVPECL connect to ground.
4	VBB	Reference Voltage Output	Bias Voltage: V <sub>CC</sub> -1.3V. Used as reference voltage when AC coupling to the D, /D inputs. Max sink/source is ±0.5mA.
1	NC		No connection.

**SY89216V**

Pin Number	Pin Name	Type	Pin Function
2, 3	D, /D	10k ECL Input	Differential PECL/ECL Input: The signal inputs include internal 75kΩ pull-down resistors. If inputs are left open, Q output will default to LOW. See "Input Interface Applications" section for single-ended inputs.
7, 6	Q, /Q	10k ECL Output	Differential PECL/ECL Output: O output defaults to LOW if D inputs left open. See "Output Interface Applications" section for recommendations on terminations.
8	VCC	Positive Power Supply	Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors.
5	VEE Exposed Pad	Negative Power Supply	Negative Power Supply: VEE and exposed pad must be tied to most negative supply. For PECL/LVPECL connect to ground.
4	VBB	Reference Voltage Output	Bias Voltage: V <sub>CC</sub> -1.3V. Used as reference voltage when AC coupling to the D, /D inputs. Max sink/source is ±0.5mA.
1	NC		No connection.

**Absolute Maximum Ratings**(Note 1)

Power Supply Voltage ( $V_{CC}$ ) ..... -0.5V to 6.0V  
 ECL Input Voltage ( $V_{IN}$ ) ..... +0V to  $V_{CC} + 0.5V$   
 Voltage Applied to Output at HIGH State  
 ( $V_{OUT}$ ) ..... -0.5V to  $V_{CC}$   
 Current Applied to Output at LOW State  
 ( $I_{OUT}$ ) ..... Twice the Rated  $I_{OL}$  mA  
 Lead Temperature (soldering, 10 sec.) ..... 220°C  
 Storage Temperature ( $T_S$ ) ..... -65°C to +150°C

**Operating Ratings**(Note 2)

Power Supply Voltage  $|V_{CC} - V_{EE}|$  .. 3.3V ±10% or 5V ±10%  
 Ambient Temperature ( $T_A$ ) ..... -40°C to +85°C  
 Package Thermal Resistance **Note 3**  
 MLF™ ( $\theta_{JA}$ )  
 Still-Air ..... 93°C/W  
 500lfpm ..... 87°C/W  
 MLF™ ( $\psi_{JB}$ ), ..... 60°C/W

**DC ELECTRICAL CHARACTERISTICS**

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{EE}$	Power Supply	$ V_{CC} - V_{EE} $	3.0	3.3	3.6	V
		$ V_{CC} - V_{EE} $	4.5	5.0	5.5	V
$I_{EE}$	Power Supply Current	SY89206V		21	26	mA
		SY89216V		18	22	mA
$I_{IH}$	Input HIGH Current				150	μA
$V_{BB}$	Output Reference Voltage	SY89206V	-1.38		-1.26	V
		SY89216V	-1.43		-1.19	V

**SY89206V (100K ECL) DC ELECTRICAL CHARACTERISTICS**

$V_{CC} = +3.3V \pm 10\%$  or  $+5V \pm 10\%$  and  $V_{EE} = 0V$ ;  $V_{CC} = 0V$  and  $V_{EE} = -3.3V \pm 10\%$  or  $-5V \pm 10\%$ ;  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OH}$	Output HIGH Voltage	<b>Note 4, 5</b>	$V_{CC} - 1.085$	—	$V_{CC} - 0.880$	V
$V_{OL}$	Output LOW Voltage	<b>Note 4, 5</b>	$V_{CC} - 1.830$	—	$V_{CC} - 1.555$	V
$V_{IH}$	Input HIGH Voltage		$V_{CC} - 1.165$	—	$V_{CC} - 0.880$	V
$V_{IL}$	Input LOW Voltage		$V_{CC} - 1.810$	—	$V_{CC} - 1.475$	V
$V_{PP}$	Minimum Input Swing		150	—	—	mV
$I_{IH}$	Input HIGH Current		—	—	150	μA
$I_{IL}$	Input LOW Current		0.5	—	—	μA

**SY89216V (10K ECL) DC ELECTRICAL CHARACTERISTICS**

$V_{CC} = +3.3V \pm 10\%$  or  $+5V \pm 10\%$  and  $V_{EE} = 0V$ ;  $V_{CC} = 0V$  and  $V_{EE} = -3.3V \pm 10\%$  or  $-5V \pm 10\%$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$  unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OH}$	Output HIGH Voltage	<b>Note 4</b> , Input Card	$V_{CC}-1.080$	—	$V_{CC}-0.720$	V
$V_{OL}$	Output LOW Voltage	<b>Note 4</b> , Input Card	$V_{CC}-1.950$	—	$V_{CC}-1.595$	V
$V_{IH}$	Input HIGH Voltage		$V_{CC}-1.230$	—	$V_{CC}-0.720$	V
$V_{IL}$	Input LOW Voltage		$V_{CC}-1.950$	—	$V_{CC}-1.445$	V
$V_{PP}$	Minimum Input Swing		150	—	—	mV
$I_{IH}$	Input HIGH Current		—	—	150	$\mu A$
$I_{IL}$	Input LOW Current		0.5	—	—	$\mu A$

**AC ELECTRICAL CHARACTERISTICS**

$V_{CC} = +3.3V \pm 10\%$  or  $+5V \pm 10\%$  and  $V_{EE} = 0V$ ;  $V_{CC} = 0V$  and  $V_{EE} = -3.3V \pm 10\%$  or  $-5V \pm 10\%$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$  unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$f_{MAX}$	Maximum Frequency	$V_{OUT} \geq 400mV$	1.0			GHz
$t_{PLH}$	Propagation Delay	D (Differential)	125	280	375	ns
$t_{PHL}$		D (Single ended)	75	280	425	ns
$t_{SKEW}$	Duty Cycle Skew	<b>Note 6</b> , EL/6V no space – $40^\circ C$		5	20	ps
$V_{PP}$	Minimum Input Swing	<b>Note 7</b>	150			mV
$V_{CMR}$	Common Mode Range	<b>Note 8</b>	$V_{CC}-1.3$		$V_{CC}-0.4$	V
$t_r, t_f$	Output Rise/Fall Times (20% to 80%)		100	225	350	ps

**Note 1.** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

**Note 2.** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

**Note 3.** Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

**Note 4.** Output loaded with  $50\Omega$  to  $V_{CC}-2V$ .

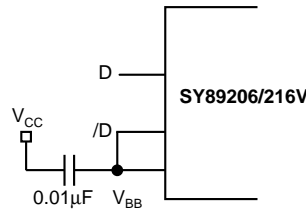
**Note 5.**  $V_{IN} = V_{IL}$  (min) or  $V_{IH}$  (max)

**Note 6.** Duty cycle skew is the difference between a  $t_{PLH}$  and  $t_{PHL}$  propagation delay through a device.

**Note 7.** Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of  $\approx 40V/V$ .

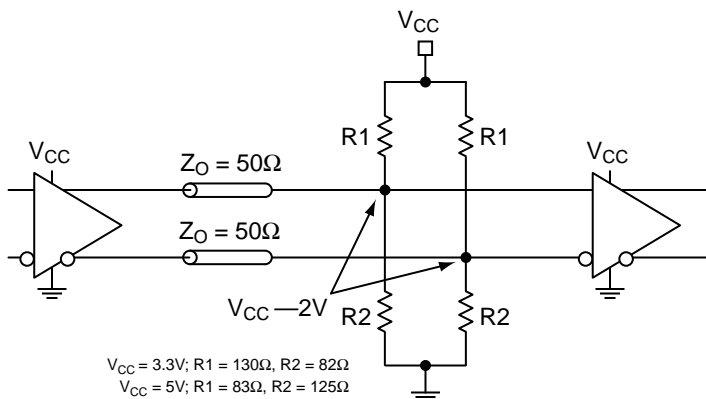
**Note 8.** The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PP}$  min. and 1V. The lower end of the CMR range varies 1:1 with  $V_{EE}$ . The numbers in the specification table assume a nominal  $V_{EE} = -3.3V$ . Note for PECL operation, the  $V_{CMR}$  (min) will be fixed at  $3.3V - |V_{CMR}(\text{min})|$ .

**INPUT INTERFACE APPLICATIONS**

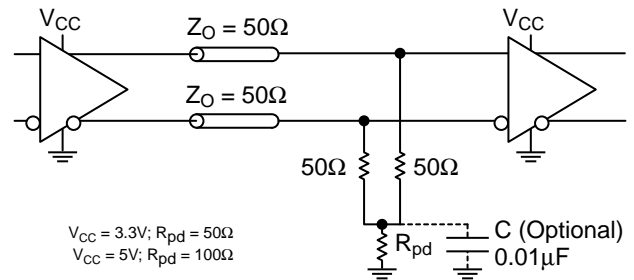


**Figure 1. Single-Ended LVPECL Input (Terminating Unused Input)**

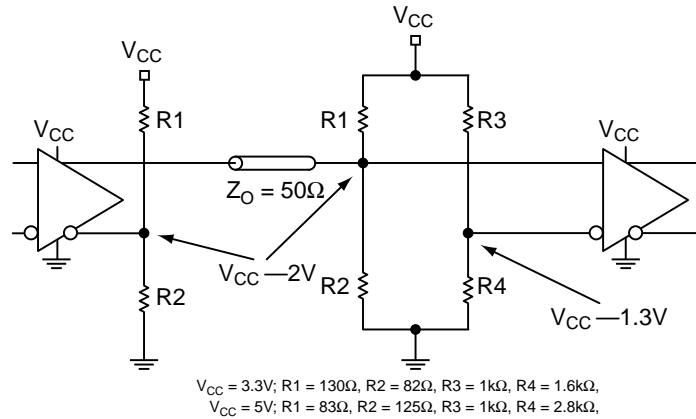
**OUTPUT INTERFACE APPLICATIONS**



**Figure 2a. Parallel Thevenin-Equivalent Termination**



**Figure 2b. Three Resistor "Y Termination"**

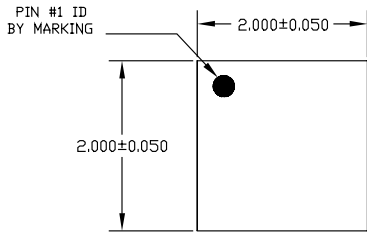


**Figure 2c. Terminating Unused I/O**

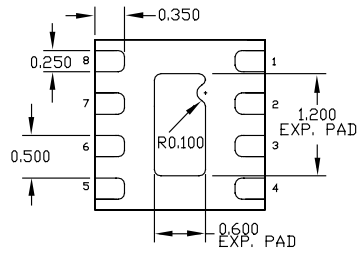
**RELATED PRODUCT AND SUPPORT DOCUMENTATION**

Part Number	Function	Data Sheet Link
SY89306/316V	3.3V/5V 2.5GHz PECL/ECL Differential Receiver/Buffer	<a href="http://www.micrel.com/product-info/products/sy89306-316v.shtml">www.micrel.com/product-info/products/sy89306-316v.shtml</a>
SY89223L	3.3V Dual Differential LVPECL-to-LVTTL Translator	<a href="http://www.micrel.com/product-info/products/sy89223l.shtml">www.micrel.com/product-info/products/sy89223l.shtml</a>
HBW Solutions	New Products and Applications	<a href="http://www.micrel.com/product-info/products/solutions.shtml">www.micrel.com/product-info/products/solutions.shtml</a>

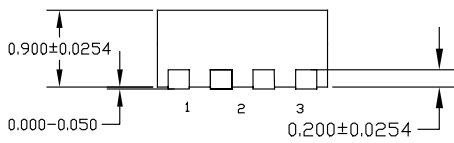
**8 LEAD ULTRA-SMALL EPAD-MicroLeadFrame™ (MLF-8)**



TOP VIEW

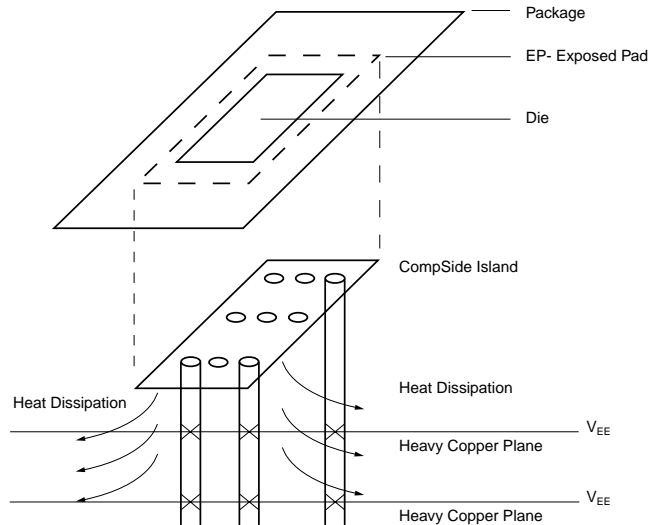


BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
  2. MAX. PACKAGE WARPAGE IS 0.05 mm.
  3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
  4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



**PCB Thermal Consideration for 8-Pin MLF™ Package**

**Package Notes:**

- Note 1.** Package meets level two qualification.
- Note 2.** All parts are dry-packed before shipment.
- Note 3.** Exposed pads must be soldered to the most negative supply plane, equivalent to  $V_{EE}$ , for proper thermal management.

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