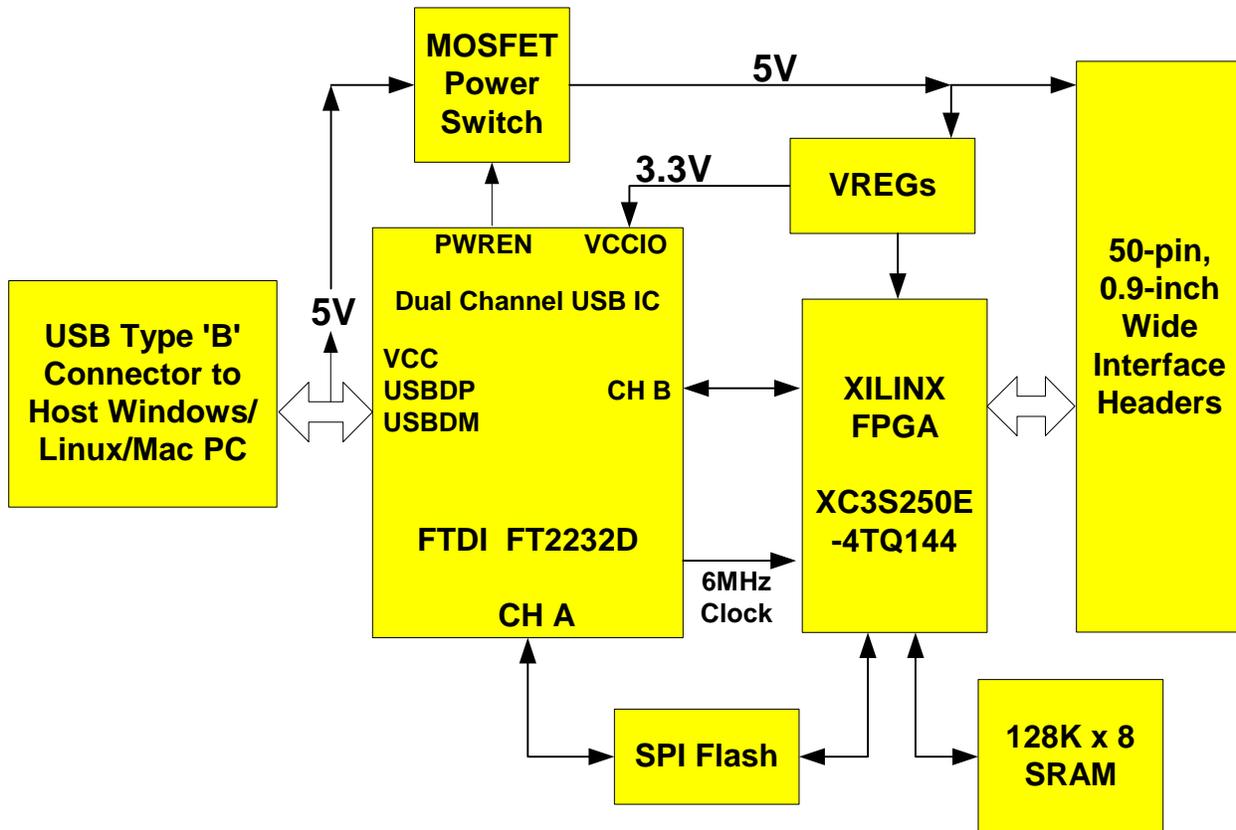




## USB - FPGA MODULE



### APPLICATIONS:

- Rapid Prototyping
- Educational Tool
- Industrial/Process Control

### FEATURES:

- Training Manual/Tutorial Available
- Built-In Configuration Loader—Writes Bit File Directly to SPI Flash via Full-Speed USB Interface
- 40 I/O Channels: 27 Input/Output; 13 Input Only
- Xilinx XC3S250E-4TQ144 FPGA
- On-Board 128K x 8, 70nS SRAM
- USB Port Powered
- USB 1.1 and 2.0 Compatible Interface
- Small Footprint: 2.8 x 1.-Inch PCB
- Standard 50-Pin, 0.9-Inch DIP Interface

## 1.0 INTRODUCTION

The DLP-FPGA Module is a low-cost, compact prototyping module that can be used for rapid proof of concept or for educational environments. The module is based on the Xilinx Spartan 3E and Future Technology Devices International's FT2232D Dual-Channel USB IC. Used by itself or with the optional 200-page training manual, the DLP-FPGA provides both the beginner as well as the experienced engineer with a rapid path to developing FPGA-based designs. When combined with the free WebPACK™ Tools from Xilinx, this module is more than sufficient for creating anything from basic logical functions to a highly complex system controller.

As a bonus feature, one channel of the dual-channel USB interface is used to load user bit files directly to the SPI Flash—no external programmer is required. This represents a savings of as much as \$200 in that no additional programming cable is required for configuring the FPGA. All that is needed to load bit files to the DLP-FPGA is a Windows software utility (free with purchase), a Windows PC and a USB cable. The module can also be programmed from within the Xilinx ISE tool environment using a Xilinx programming cable (purchased separately).

The DLP-FPGA is fully compatible with the free ISE™ WebPACK™ tools from Xilinx. ISE WebPACK offers the ideal development environment for FPGA designs with HDL synthesis and simulation, implementation, device fitting and JTAG programming.

The DLP-FPGA has on-board voltage regulators that generate all required power supply voltages from a single 5-volt source. Power for the module can be taken from either the host USB port or from a user-supplied, external 5-volt power supply.

Connection to user electronics is made via a 50-pin, 0.9-inch wide, industry-standard 0.025 square inch post DIP header. Other on-board features include a 128K x 8 static RAM IC for user projects, and both JTAG and SPI Flash interface ports for connection to Xilinx programming tools.

## 2.0 TRAINING MANUAL

A 200+ page training manual for the DLP-FPGA is also available. While this manual is designed to provide entry-level instruction for those new to designing with FPGAs, it is recommended for developers who have some experience with FPGA products and associated development tools. An ISE™ WebPACK™ Software installation DVD is included with the manual.

The manual is comprised of 5 Chapters and 4 Labs as outlined below:

**Chapter 1:** Installing the Xilinx ISE WebPACK tools and Understanding the Design Flow

**Chapter 2:** Lab 1: Implementing a Simple AND Gate: Create a New Project, Implement the Design, View the Synthesized Design, View the Placed and Routed Design

**Chapter 3:** Lab 2: Heartbeat: Understanding the Digital Clock Manager (DCM), Methods of Starting ISE Project Navigator, VHDL Module Structure, Utilizing Hierarchy, Adding the DCM Component, Adding the Heartbeat Component, Connecting the Components, Synthesizing the Design Using XST, Simulating the Design Using the ISE Simulator, Adding the User Constraint File, Implementing the Design, Download the Design to the FPGA

**Chapter 4:** Lab 3: Memory Test: Block Diagram, DCM Design, SRAM State Machine, Bi-Directional Buffers, Test Failed Indicator, User Constraint File, Synthesize the Memory Test Design, Simulate the Memory Test Design, Implementing the Design, Download the Design to the FPGA

**Chapter 5:** Lab 4: USB Loopback: Initial Design, USB State Machine Module, Language Template, Bi-Directional Buffers, Synthesize, Simulate, Pin Constraints, Implement, Download the Design to the FPGA

(The completed design files for each lab are available for download from the DLP Design website upon purchase of the DLP-FPGA and Lab Manual.)

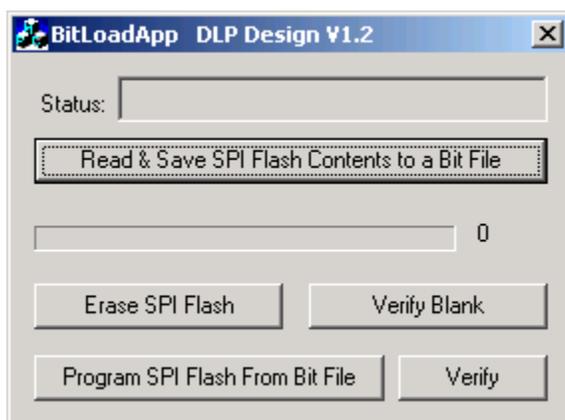
### 3.0 FPGA SPECIFICATIONS

The FPGA device used on the DLP-FPGA is the Xilinx Spartan 3E: XC3S250E-4TQ144.

- Part Number: XC3S250E
- System Gates: 250K
- Equivalent Logic Cells: 5,508
  
- CLB Array
  - Rows: 34
  - Columns: 26
  - Total CLB's: 612
  - Total Slices: 2,448
  
- Distributed RAM Bits: 38K
- Block RAM Bits: 216K
- Dedicated Multipliers: 12
- DCM's: 4

### 4.0 BITLOADAPP SOFTWARE

Windows software is provided for use with the DLP-FPGA that will load an FPGA configuration (.bit) file directly to the SPI Flash device via the USB interface. This app (shown below) will allow the user to erase the flash, verify the erasure and then program and verify the flash:



## 5.0 JTAG INTERFACE

The easiest way to load an FPGA configuration (bit file) to the FPGA is to run the BitLoadApp software, then select and program a file from the local hard drive directly to the SPI flash. Once written to the SPI flash, the configuration will load to the FPGA and execute. Alternatively, a traditional JTAG header location is provided on the DLP-FPGA giving the user access to the pins on the FPGA required by the development tools. (Refer to the schematic at the end of this datasheet for details.)

## 6.0 EEPROM SETUP / MPROG

The DLP-FPGA has a dual-channel USB interface to the host PC. Channel A is used exclusively to load an FPGA configuration (bit file) to the SPI flash. This configuration data is automatically transferred to the FPGA when power is applied to the module. Channel B is used for communication between the FPGA and host PC at run time. A 93C56B EEPROM connected to the USB interface IC is used to store the setup for the two channels. The parameters stored in the EEPROM include the Vendor ID (VID), Product ID (PID), Serial Number, Description String, driver selection (VCP or D2XX) and port type (UART serial or FIFO parallel).

As mentioned above, Channel A is used exclusively for loading the FPGA's configuration to the SPI flash, and Channel B is used for communication between the host PC and the DLP-FPGA. As such, the D2XX drivers and FIFO mode must be selected in the EEPROM for Channel A. Channel B must use the FIFO mode, but can use either the VCP or D2XX drivers. The VCP drivers make the DLP-FPGA appear as an RS232 port to the host app. The D2XX drivers provide faster throughput, but require working with a .lib or .dll library in the host app.

The operational modes and other EEPROM selections are written to the EEPROM using the MPROG utility. This utility and its manual are available for download from the bottom of the page at [www.dlpdesign.com](http://www.dlpdesign.com).

## 7.0 TEST BIT FILE

A test file is provided as a download from the DLP Design website that provides rudimentary access to the I/O features of the DLP-FPGA.

The following features are provided:

- Ping
- Read the High/Low State of the Input-Only Pins
- Drive I/O Pins High/Low or Read their High/Low State
- Simple Loopback on Channel B
- Simple Read/Write of Each Address in the SRAM

This bit file is available from the DLP-FPGA's download page.

## 8.0 USB DRIVERS

USB drivers for the following operating systems are available for download from the DLP Design website at <http://www.dlpdesign.com>:

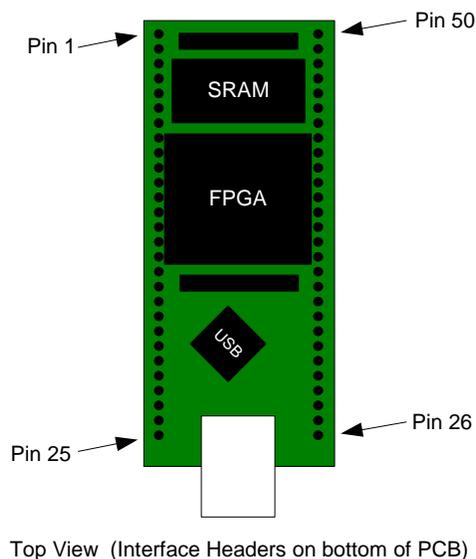
<b>Windows XP x64</b>	<b>Mac OSX</b>
<b>Windows Server 2003</b>	<b>Mac OS9</b>
<b>Windows 2000</b>	<b>Mac OS8</b>
<b>Windows 98, ME</b>	<b>Linux</b>

### Notes:

1. The bit file load utility only runs on the Windows platforms.
2. The bit file load utility requires the use of USB channel A, and channel A is dedicated to this function.
3. If you are using the dual-mode drivers from FTDI (CDM2.02.04) and wish to use the Virtual COM Port (VCP) drivers for Channel B communications, then it may be necessary to disable the D2XX drivers first via Device Manager. To do so, right click on the Channel B entry under USB Controllers that appears when the DLP-FPGA is connected, select Properties, select the Advanced tab, check the option for "Load VCP" and click OK. Once you unplug and then replug the DLP-FPGA, a COM port should appear in Device Manager under Ports (COM & LPT).

## 9.0 USING THE DLP-FPGA

Select a power source via Header Pins 23 and 24, and connect the DLP-FPGA to the PC to initiate the loading of USB drivers. The easiest way to do this is to connect Pins 23 and 24 to each other. This will result in operational power being taken from the host PC. Once the drivers are loaded, the DLP-FPGA is ready for use.

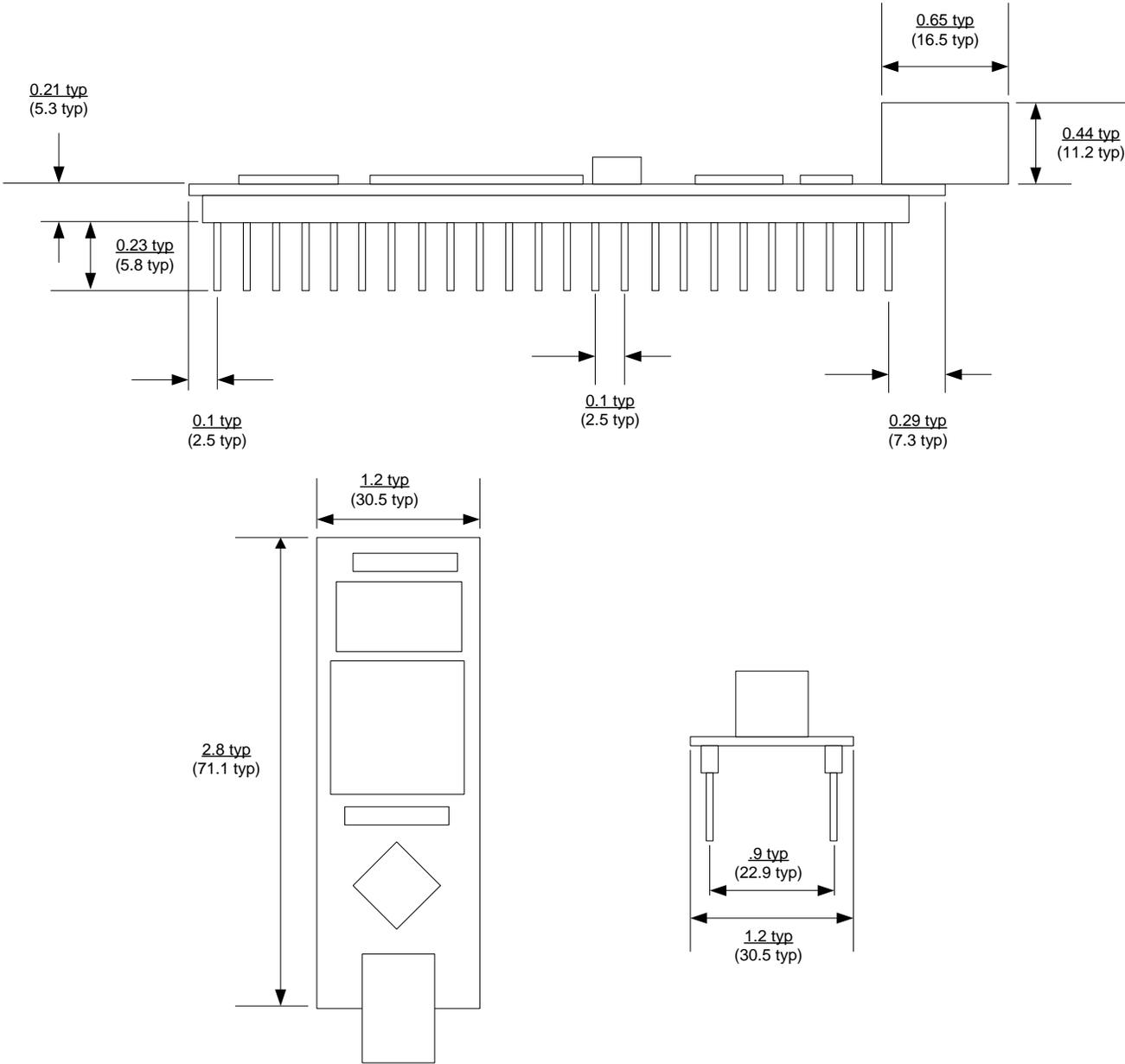


## TABLE 1

NN (dec)*	NN (hex)*	Name	FPGA Pin	JP2 Pin
0	0	user_io(0)	U5 Pin 58	JP2 Pin 2
1	1	user_io(1)	U5 Pin 59	JP2 Pin 4
2	2	user_io(2)	U5 Pin 93	JP2 Pin 5
3	3	user_io(3)	U5 Pin 94	JP2 Pin 6
4	4	user_io(4)	U5 Pin 96	JP2 Pin 7
5	5	user_io(5)	U5 Pin 97	JP2 Pin 8
6	6	user_io(6)	U5 Pin 103	JP2 Pin 9
7	7	user_io(7)	U5 Pin 104	JP2 Pin 10
8	8	user_io(8)	U5 Pin 105	JP2 Pin 12
9	9	user_io(9)	U5 Pin 106	JP2 Pin 13
10	A	user_io(10)	U5 Pin 112	JP2 Pin 14
11	B	user_io(11)	U5 Pin 113	JP2 Pin 15
12	C	user_io(12)	U5 Pin 116	JP2 Pin 16
13	D	user_io(13)	U5 Pin 117	JP2 Pin 17
14	E	user_in(14) [INPUT ONLY!]	U5 Pin 119	JP2 Pin 18
15	F	user_in(15) [INPUT ONLY!]	U5 Pin 120	JP2 Pin 19
16	10	user_io(16)	U5 Pin 122	JP2 Pin 20
17	11	user_io(17)	U5 Pin 123	JP2 Pin 21
18	12	user_io(18)	U5 Pin 124	JP2 Pin 22
19	13	user_io(19)	U5 Pin 125	JP2 Pin 27
20	14	user_io(20)	U5 Pin 126	JP2 Pin 29
21	15	user_io(21)	U5 Pin 130	JP2 Pin 30
22	16	user_io(22)	U5 Pin 131	JP2 Pin 31
23	17	user_io(23)	U5 Pin 132	JP2 Pin 32
24	18	user_io(24)	U5 Pin 134	JP2 Pin 33
25	19	user_io(25)	U5 Pin 135	JP2 Pin 34
26	1A	user_io(26)	U5 Pin 139	JP2 Pin 35
27	1B	user_io(27)	U5 Pin 140	JP2 Pin 36
28	1C	user_io(28)	U5 Pin 142	JP2 Pin 37
30	1E	user_in(0)	U5 Pin 10	JP2 Pin 49
31	1F	user_in(1)	U5 Pin 12	JP2 Pin 48
32	20	user_in(2)	U5 Pin 29	JP2 Pin 47
33	21	user_in(3)	U5 Pin 31	JP2 Pin 46
34	22	user_in(4)	U5 Pin 36	JP2 Pin 45
35	23	user_in(5)	U5 Pin 38	JP2 Pin 44
36	24	user_in(6)	U5 Pin 41	JP2 Pin 43
37	25	user_in(7)	U5 Pin 47	JP2 Pin 42
38	26	user_in(8)	U5 Pin 48	JP2 Pin 41
39	27	user_in(9)	U5 Pin 66	JP2 Pin 39
40	28	user_in(10)	U5 Pin 69	JP2 Pin 38
Read: 29, >40	Read:1D, >29	Returns Read Pin Error E4	n/a	n/a
Write: 14, 15, >30	Write: E, F, >1E	Returns Write Pin Error E2 for Pin Clear (low), or E3 for Pin Set (high)	n/a	n/a
		Ground		1,11,25,26,40,50
		FPGA_RESET	128	3
		5VIN – Module power source		23
		PORTVCC – Power from Host PC		24
		VCCSW – 5V power after host enumerates the USB port		28

\***Note:** This is the I/O number for use with the Test Bit File described in Section 7.

# 10.0 MECHANICAL DIMENSIONS IN INCHES (MM) (PRELIMINARY)



## 11.0 DISCLAIMER

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## 12.0 CONTACT INFORMATION

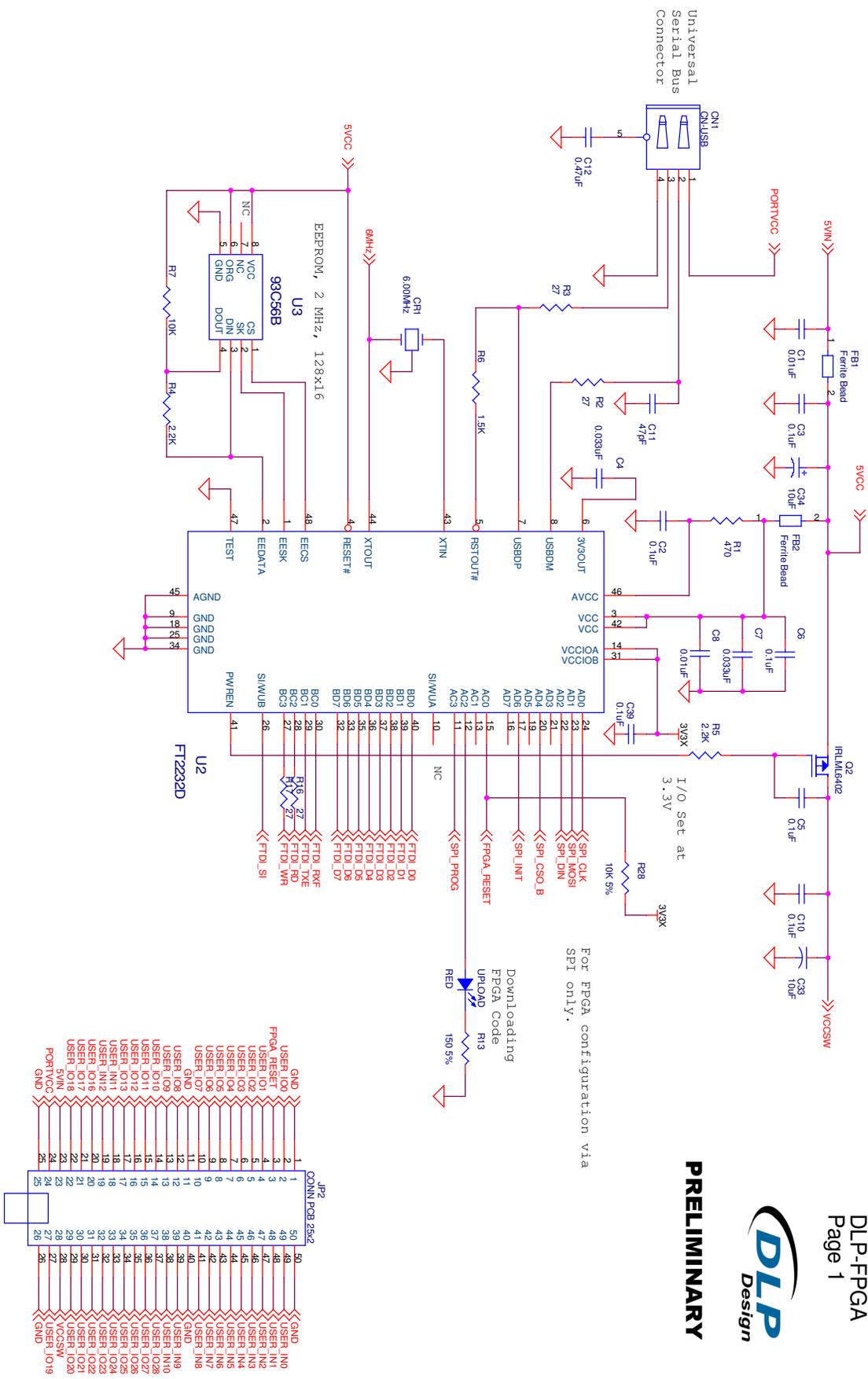
DLP Design, Inc.  
1605 Roma Lane  
Allen, TX 75013

Phone: 469-964-8027  
Fax: 415-901-4859

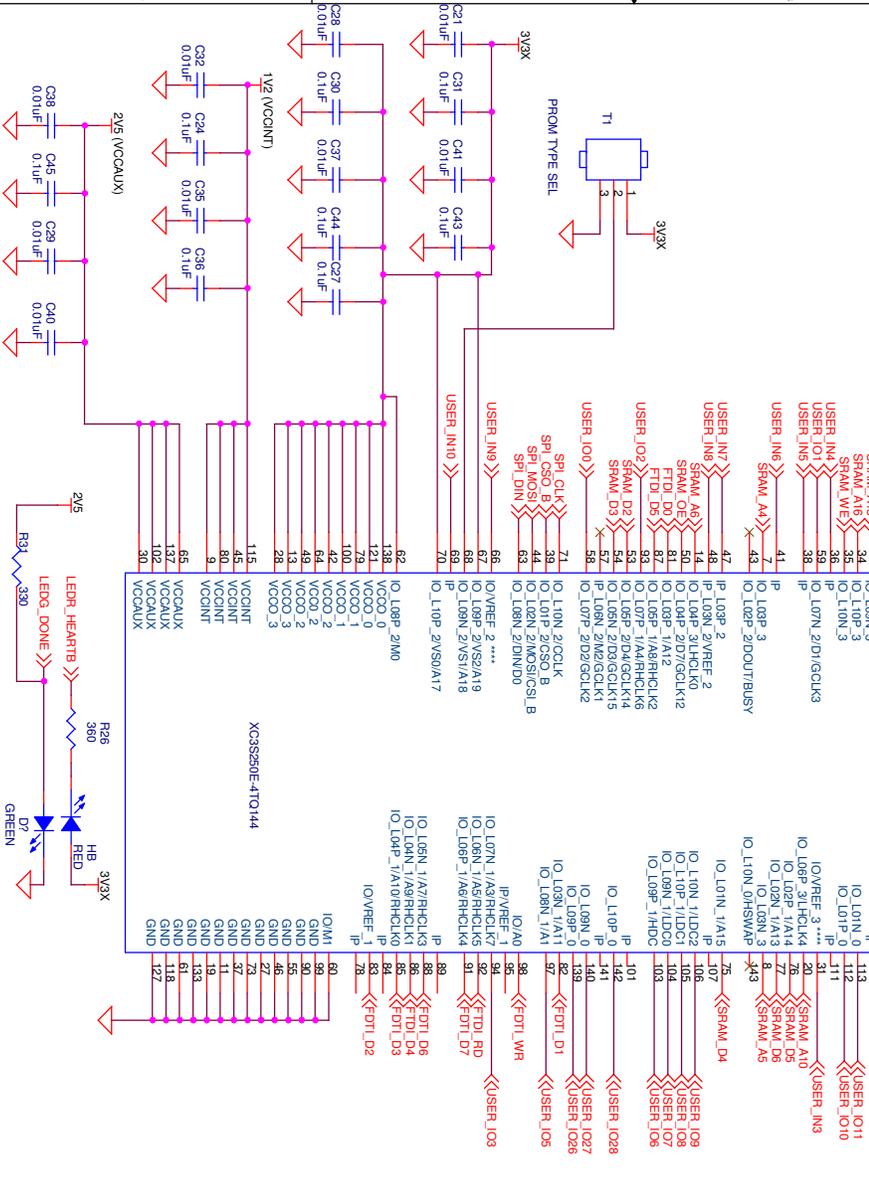
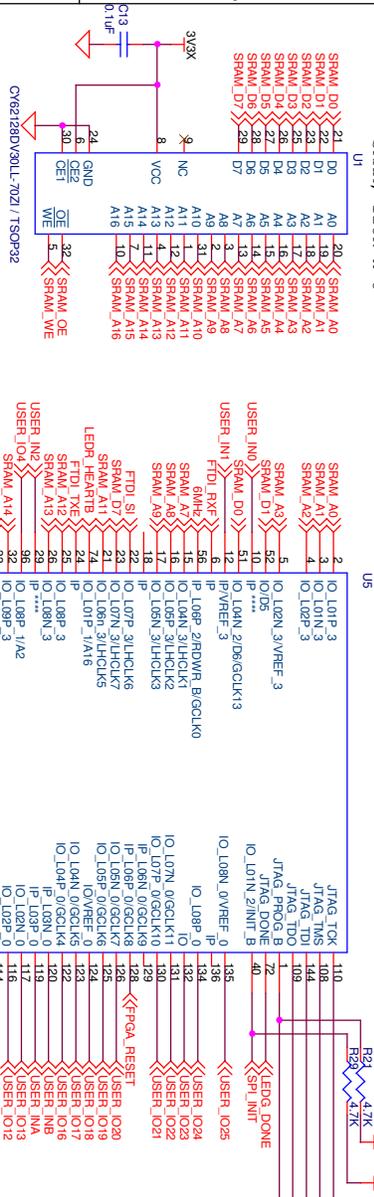
Email Sales: [sales@dlpdesign.com](mailto:sales@dlpdesign.com)  
Email Support: [support@dlpdesign.com](mailto:support@dlpdesign.com)  
Website URL: <http://www.dlpdesign.com>



**PRELIMINARY**

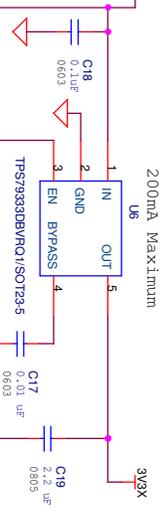


Pin	Signal	Pin	Signal
1	GND	27	FTDI_S1
2	USER_I00	28	FTDI_RXE
3	USER_I01	29	FTDI_TXE
4	USER_I02	30	FTDI_RXD
5	USER_I03	31	FTDI_TXD
6	USER_I04	32	FTDI_W#
7	USER_I05	33	FTDI_D0
8	USER_I06	34	FTDI_D1
9	USER_I07	35	FTDI_D2
10	USER_I08	36	FTDI_D3
11	USER_I09	37	FTDI_D4
12	USER_I10	38	FTDI_D5
13	USER_I11	39	FTDI_D6
14	USER_I12	40	FTDI_D7
15	USER_I13	41	FTDI_D8
16	USER_I14	42	FTDI_D9
17	USER_I15	43	FTDI_D10
18	USER_I16	44	FTDI_D11
19	USER_I17	45	FTDI_D12
20	USER_I18	46	FTDI_D13
21	USER_I19	47	FTDI_D14
22	USER_I20	48	FTDI_D15
23	USER_I21	49	FTDI_D16
24	USER_I22	50	FTDI_D17
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181	USER_I179		
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183	USER_I181		
184	USER_I182		
185	USER_I183		
186	USER_I184		
187	USER_I185		
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189	USER_I187		
190	USER_I188		
191	USER_I189		
192	USER_I190		
193	USER_I191		
194	USER_I192		
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199	USER_I197		
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248	USER_I246		
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269	USER_I267		
270	USER_I268		
271	USER_I269		
272	USER_I270		
273	USER_I271		
274	USER_I272		
275	USER_I273		
276	USER_I274		
277	USER_I275		
278	USER_I276		
279	USER_I277		
280	USER_I278		
281	USER_I279		
282	USER_I280		
283	USER_I281		
284	USER_I282		
285	USER_I283		
286	USER_I284		
287	USER_I285		
288	USER_I286		
289	USER_I287		
290	USER_I288		
291	USER_I289		
292	USER_I290		
293	USER_I291		
294	USER_I292		
295	USER_I293		
296	USER_I294		
297	USER_I295		
298	USER_I296		
299	USER_I297		
300	USER_I298		
301	USER_I299		
302	USER_I300		
303	USER_I301		
304	USER_I302		
305	USER_I303		
306	USER_I304		
307	USER_I305		
308	USER_I306		
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317	USER_I315		
318	USER_I316		
319	USER_I317		
320	USER_I318		
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322	USER_I320		
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326	USER_I324		
327	USER_I325		
328	USER_I326		
329	USER_I327		
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331	USER_I329		
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333	USER_I331		
334	USER_I332		
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338	USER_I336		
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367	USER_I365		
368	USER_I366		
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370	USER_I368		
371	USER_I369		
372	USER_I370		
373	USER_I371		
374	USER_I372		
375	USER_I373		
376	USER_I374		
377	USER_I375		
378	USER_I376		



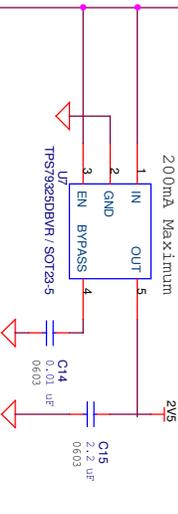
### 3.3V REGULATOR

200mA Maximum



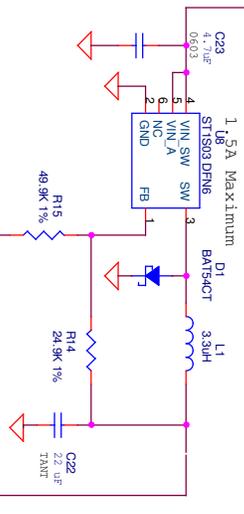
### 2.5V REGULATOR

200mA Maximum



### 1.2V REGULATOR

1.5A Maximum



### PRELIMINARY



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