POWER

DS750PED

750 Watts Distributed Power System

Data Sheet

Front-end Bulk Power
Total Output Power:
750 W continuous
Wide Input Voltage:
90 to 264 Vac

SPECIAL FEATURES

- 750 W output power
- High-power and short form factor
- 1U power supply
- High-density design: 16.4 W/in^3
- Active Power Factor Correction
- EN61000-3-2 Harmonic compliance
- Inrush current control
- 80plus Platinum efficiency
- N+1 or N+N Redundant
- Hot-pluggable
- Active current sharing
- Full Digital control
- PMBus Compliant
- Accurate input power reporting
- Compatible with Artesyn's Universal PMBus GUI
- Reverse airflow option
- Two-year Warranty

COMPLIANCE

- Conducted/Radiated EMI Class A Limits + 6 dB margin
- EN61000-4-11

SAFETY

- UL/cUL
- Demko +CB Report
- CE Mark
- CCC
- BSMI

Electrical Specifications

Input						
Input range:	90 - 264 Vac					
Frequency:	47 Hz to 63 Hz					
Efficiency:	94.0% peak					
Max Input current:	10.0 Arms @ 90 Vac					
Inrush current:	55 Apk					
Conducted EMI:	Class A with 6 dB margin					
Radiated EMI:	Class A with 6 dB margin					
Power factor:	>0.9 beginning at 20% load					
ITHD:	10%					
Leakage current:	1.75 mA					
Hold-up time:	10 ms at full load					
Output						
	Main DC Output			**Standby DC Output**		
	MIN	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
Nominal setting:	-0.20%	12	0.20%	-1%	12	1%
Total output regulation range:	11.4 V		12.6 V	11.4 V		12.6 V
Dynamic load regulation range:	11.4 V		12.6 V	11.4 V		12.6 V
Output ripple:			120 mVp-p			120 mVp-p
Output current:	0.5 A[1]		62.5 A	0.1 A		3.0 A
Current sharing:	Within ±5% of full load rating			N/A		
Capacitive loading:	2000 uF		40,000 uF	47 uF		680 uF
Start-up from AC to output:			2200 ms			1700 ms
Output rise time:	5 ms		50 ms	2 ms		60 ms

[1] Minimum current for transient load response testing only. Unit is designed to operate and be within output regulation range at zero load.

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EMBEDDED TECHNOLOGIES

Electrical Specifications

Protections

Main Output	MIN	NOM	MAX
Over-current protection[2]:	120%		150%
Over-voltage protection[1]:	13.5 V		15.0 V
Under-voltage protection:	10.5 V		11.0 V
Over-temperature protection:		Yes	
Fan fault protection:		Yes	
Standby Output			
Over-current protection[3]:	120%		150%
Over-voltage protection[3]:	13.5 V		15.0 V
Under-voltage protection:	10.0 V		11.0 V

[1] Latch mode
[2] Autorecovery if the overcurrent is less than 120% and last only for <500 ms
[3] Standby protection is auto-recovery

Ordering Information

Model Number	Nominal Main Output	Standby Output	Airflow Direction
DS750PED-3	12 V @ 62.5 A	12 V @ 3 A	Standard (forward)
DS750PED-3-001	12 V @ 62.5 A	12 V @ 3 A	Reverse

Control and Status Signals

Input Signals

PSON_L

Active LOW signal which enables/disables the main output. Pulling this signal LOW will turn-on the main output. Recommended pull-up resistor to 12 VSB is 8.2 k with a 3.0 k pull-down to ground. A 100 pF decoupling capacitor is also recommended.

		MIN	MAX
V_{IL}	Input logic level LOW		0.8 V
V_{IH}	Input logic level HIGH	2.0 V	5.0 V
I_{SOURCE}	Current that may be sourced by this pin		2 mA
I_{SINK}	Current that may be sunk by this pin at low state		0.5 mA

PSKILL_L

First break/last mate active LOW signal which enables/disables the main output. This signal will have to be pulled to ground at the system side with a 220 ohm resistor. A 100 pF decoupling capacitor is also recommended.

		MIN	MAX
V_{IL}	Input logic level LOW		0.8 V
V_{IH}	Input logic level HIGH	2.0 V	5.0 V
I_{SOURCE}	Current that may be sourced by this pin		2 mA
I_{SINK}	Current that may be sunk by this pin at low state		0.5 mA

Control and Status Signals

Output Signals

ACOK

Signal used to indicate the presence of AC input to the power supply. A logic level HIGH will indicate that the AC input to the power supply is within the operating range while a logic level LOW will indicate that AC has been lost.

This is an open collector/drain output. This pin is pulled high by a 1.0 kohm resistor connected to 3.3 V inside the power supply. It is recommended that this pin be connected to a 100 pF decoupling capacitor and pulled down by a 100 kohm resistor.

		MIN	MAX
V_{IL}	Input logic level LOW		0.6 V
V_{IH}	Input logic level HIGH	2.0 V	5.0 V
I_{SOURCE}	Current that may be sourced by this pin		3.3 mA
I_{SINK}	Current that may be sunk by this pin at low state		0.7 mA

PWR_GOOD/PWOK

Signal used to indicate that main output voltage is within regulation range. The PWR_GOOD signal will be driven HIGH when the output voltage is valid and will be driven LOW when the output falls below the under-voltage threshold.

This signal also gives an advance warning when there is an impending power loss due to loss of AC input or system shutdown request. More details in the Timing Section.

This is an open collector/drain output. This pin is pulled high by a 1.0 kohm resistor connected to 3.3 V inside the power supply. It is recommended that this pin be connected to a 100 pF decoupling capacitor and pulled down by a 10 kohm resistor.

		MIN	MAX
V_{IL}	Input logic level LOW		0.8 V
V_{IH}	Input logic level HIGH	2.0 V	5.0 V
I_{SOURCE}	Current that may be sourced by this pin		3.3 mA
I_{SINK}	Current that may be sunk by this pin at low state		0.7 mA

Output Signals

PS_PRESENT

Signal used to indicate to the system that a power supply is inserted in the power bay. This pin is shorted to the standby return in the power supply. Recommended pull-up resistor to 12 VSB is 8.2 k with a 3.0 k pull-down to ground. A 100 pF decoupling capacitor is also recommended.

PS_INTERRUPT_L

Active low signal used by the power supply to indicate to the system that a change in power supply status has occurred. This event can be triggered by faults such as OVP, OCP, OTP, and fan fault. This signal can be cleared by a CLEAR_FAULT command. Recommended pull-up resistor to 12 VSB is 8.2 k with a 3.0 k pull-down to ground. A 100 pF decoupling capacitor is also recommended.

		MIN	MAX
V_{IL}	Input logic level LOW		0.8 V
V_{IH}	Input logic level HIGH	2.0 V	5.0 V
I_{SOURCE}	Current that may be sourced by this pin		4 mA
I_{SINK}	Current that may be sunk by this pin at low state		4 mA

BUS Signals

ISHARE

Bus signal used by the power supply for active current sharing. All power supplies configured in the system for n+n sharing will refer to this bus voltage inorder to load share.

Voltage Range	The range of this signal for active sharing will be up to 8.0 V, which corresponds to the maximum output current.		
		MIN	MAX
I_{SHARE} Voltage	Vshare at 100% load, stand-alone unit	7.75	8.25
	Voltage at 50% load, stand-alone unit	3.85	4.15
	Voltage at 0% load, stand-alone unit	0	0.3
I_{SOURCE}	Current that may be sourced by this pin		160 mA

SCL, SDA

Clock and data signals defined as per I²C requirements. It is recommended that these pins be pulled-up to a 2.2 kohm resistor to 3.3 V and a 100 pF decoupling capacitor at the system side.

VL	Input logic level LOW		0.8 V
VH	Input logic level HIGH	2.0 V	5.0 V

Note: All signal noise levels are below 400 mVpk-pk from 0 - 100 MHz.

I²C Addressing Table: Not applicable. This power supply has a fixed I²C address. In order to support multiple addresses, the system will have to utilize a switcher or an I²C expander.

Electrical Specifications

LED Indicators

A single bi-color LED is used to indicate the power supply status.

	Status LED
No AC input to PSU	Off when stand-alone, blinking AMBER when in parallel
Main output ON	Solid GREEN
Standby mode or Power supply failure (OCP, OVP, OTP, FAN FAULT)	Blinking AMBER

Firmware Reporting And Monitoring

	Accuracy Range		
Output loading	5 to 20%	20 to 50%	50 to 100%
Input voltage	±5%		
Input current	±0.55 A fixed error	±4%	
Input power	±1.25 W at <125 W input	±1.25%	
Output voltage	±2%		
Output current	0.3 A fixed error	±2%	
Temperature	±5 °C on the operating range		
E_{IN}	±15% from 10% to 20% load	±5%	
Fan speed	Actual RPM ±250 RPM		

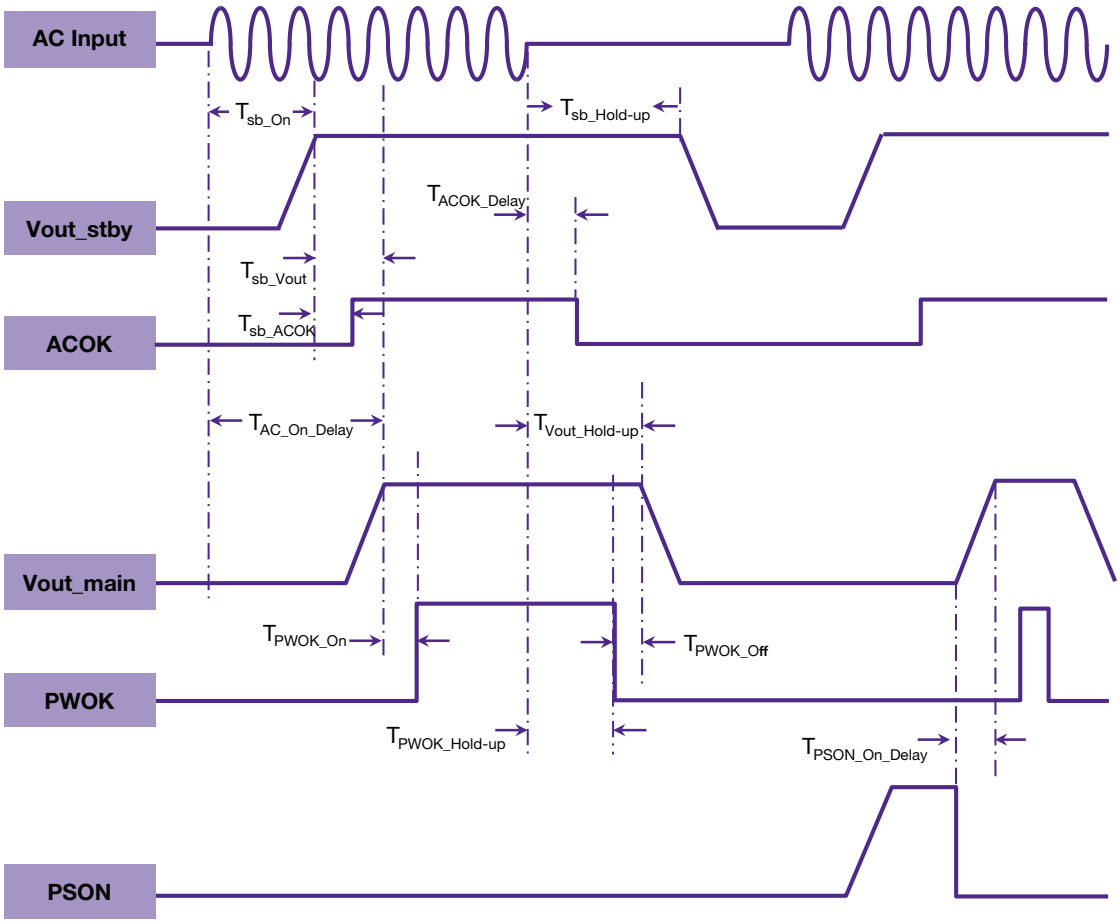
PMBus	YES
Remote ON/OFF	YES

Timing Specifications

	Description	Min	Max	Unit
T_{sb_On}	Delay from AC being applied to standby output being within regulation	20	1700	ms
T_{sb_ACOK}	Delay from standby output to ACOK assertion	*See note below*	20	ms
T_{sb_Vout}	Delay from standby output to main output voltage being within regulation		300	ms
$T_{AC\_On\_Delay}$	Delay from AC being applied to main output being within regulation		2200	ms
$T_{PWR\_GOOD\_On}$	Delay from output voltages within regulation limits to PWOK asserted	100	1000	ms
T_{ACOK_Delay}	Delay from loss of AC to assertion of ACOK		6	ms
$T_{PWR\_GOOD\_Hold\text{-}up}$	Delay from loss of AC to deassertion of PWOK	10		ms
$T_{Vout\_Hold\text{-}up}$	Delay from loss of AC to main output being within regulation	11		ms
$T_{sb\_Hold\text{-}up}$	Delay from loss of AC to standby output being within regulation	150		ms
$T_{PWR\_GOOD\_Off}$	Delay from deassertion of PWOK to output falling out of regulation	1		ms
$T_{PSON\_On\_Delay}$	Delay from PSON assertion to output being within regulation		350	ms
T_{PWOK_Low}	Duration of PWOK being in deasserted state during an ON/OFF cycle of PSU	N/A	N/A	

Note: $T_{vout\_hold\text{-}up}$: tested at 1A load on standby output
T_{sb_ACOK}: ACOK can assert earlier than the standby output

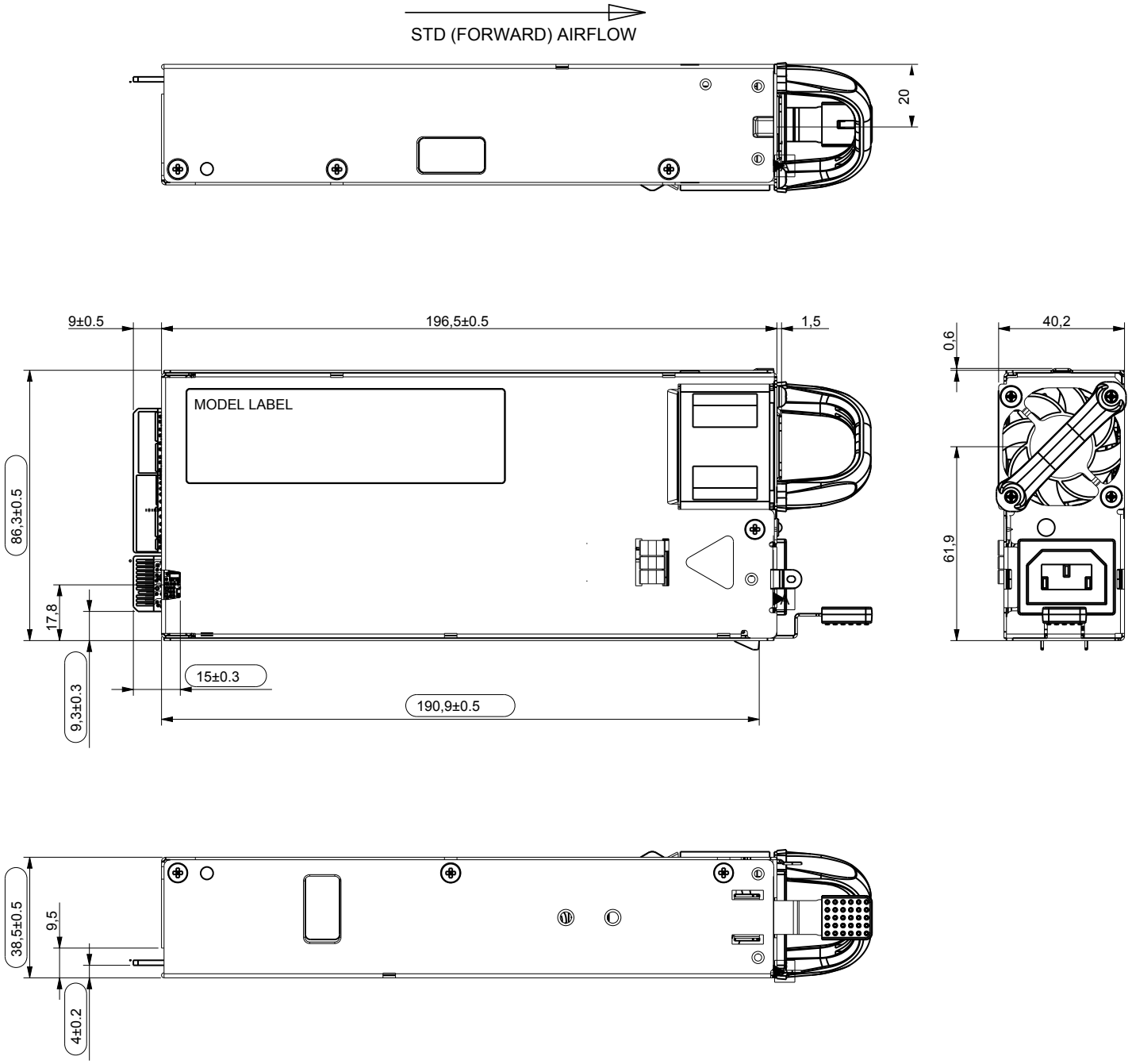
Timing Diagram



Environmental Specifications

Operating temperature:	0 to 50 °C, withstand operation up to 60 °C at full power without damage
Operating altitude:	up to 10,000 feet
Operating relative humidity:	20% to 80% non-condensing
Non-operating temperature:	-40 to +70 °C
Non-operating relative humidity:	10% to 95% non-condensing
Non-operating altitude:	up to 50,000 feet
Vibration and shock:	Standard operating/non-operating random shock and vibration
ROHS compliance:	Yes
MTBF:	200,000 hours per Telcordia Issue 2, Method 1, Case 3 at 25 °C ambient at full load.
Operating life:	Minimum of 5 years
Reliability:	All electronic component derating analysis and capacitor life calculation is done at maximum ambient, 80% of maximum rated load, nominal input line voltage.

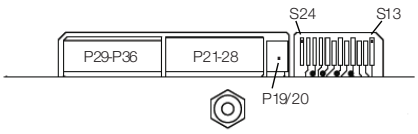
Mechanical Outline



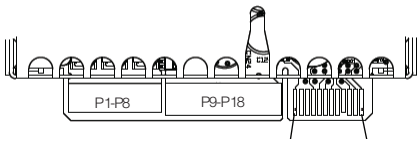
Connector Definitions

Output Connector Part Number	Card-edge
Mating Connector Part Number	FCI 10107844-002LF or equivalent

Power Supply Output Card Edge (Bottom Side)



Power Supply Output Card Edge (Top Side)



Output Connector Pin Configuration			
S1	PS PRESENT	S13	PS_ON_L
S2	Reserved	S14	PS_KILL_L
S3	Reserved	S15	Reserved
S4	Pwr_Good (PWOK)	S16	RETURN
S5	ACOK (AC Input Present)	S17	SDA
S6	RETURN	S18	RETURN
S7	ISHARE	S19	SCL
S8	RESERVE	S20	RETURN
S9	PS INTERRUPT_L	S21	REMOTE SENSE-
S10	RETURN	S22	RETURN
S11	Reserved	S23	REMOTE SENSE+
S12	Reserved	S24	RESERVE
P1-P8	Vo	P19-P20	VSB
P9-P18	RTN	P21-P28	RTN
		P29-P36	Vo

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