Multiple Output, High Precision, Dual-Tracking Reference

Data Sheet

AD588

FEATURES

Low drift: 1.5 ppm/°C
Low initial error: 1 mV
Pin programmable output
+10 V, +5 V, ±5 V tracking, −5 V, −10 V
Flexible output force and sense terminals
High impedance ground sense
16-lead SOIC package and 16-lead CERDIP
MIL-STD-883-compliant versions available

GENERAL DESCRIPTION

The AD588 represents a major advance in state-of-the-art monolithic voltage references. Low initial error and low temperature drift give the AD588 absolute accuracy performance previously not available in monolithic form. The AD588 uses a proprietary ion-implanted, buried Zener diode and laser-wafer drift trimming of high stability thin film resistors to provide outstanding performance.

The AD588 includes the basic reference cell and three additional amplifiers that provide pin programmable output ranges. The amplifiers are laser trimmed for low offset and low drift to maintain the accuracy of the reference. The amplifiers are configured to allow Kelvin connections to the load and/or boosters for driving long lines or high current loads, delivering the full accuracy of the AD588 where it is required in the application circuit.

The low initial error allows the AD588 to be used as a system reference in precision measurement applications requiring 12-bit absolute accuracy. In such systems, the AD588 can provide a known voltage for system calibration in software. The low drift also allows compensation for the drift of other components in a system. Manual system calibration and the cost of periodic recalibration can, therefore, be eliminated. Furthermore, the mechanical instability of a trimming potentiometer and the potential for improper calibration can be eliminated by using the AD588 in conjunction with auto calibration software.

The AD588 is available in seven versions. The AD588JQ and AD588KQ are packaged in a 16-lead CERDIP and are specified for 0°C to +70°C operation. The AD588AQ and AD588BQ are packaged in a 16-lead CERDIP, and the AD588ARWZ is packaged in a 16-lead SOIC, and they are specified for the −25°C to +85°C industrial temperature range. The ceramic AD588TE and AD588TQ grades are specified for the full military/aerospace temperature range.

FUNCTIONAL BLOCK DIAGRAM

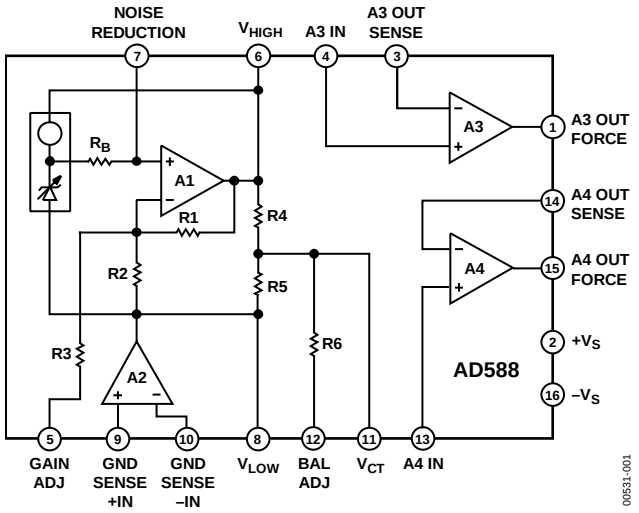

Figure 1.

PRODUCT HIGHLIGHTS

1. The AD588 offers 12-bit absolute accuracy without any user adjustments. Optional fine-trim connections are provided for applications requiring higher precision. The fine trimming does not alter the operating conditions of the Zener or the buffer amplifiers, and so does not increase the temperature drift.
2. Output noise of the AD588 is very low, typically 6 µV p-p. A pin is provided for additional noise filtering using an external capacitor.
3. A precision ±5 V tracking mode with Kelvin output connections is available with no external components. Tracking error is less than 1 mV, and a fine trim is available for applications requiring exact symmetry between the +5 V and −5 V outputs.
4. Pin strapping capability allows configuration of a wide variety of outputs: ±5 V, +5 V, +10 V, −5 V, and −10 V dual outputs or +5 V, −5 V, +10 V, and −10 V single outputs.

Rev. M **Document Feedback**
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REVISION HISTORY

11/15—Rev. L to Rev. M
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Deleted Figure 10c ... 7
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SPECIFICATIONS

Typical at 25°C, 10 V output, V_S = ±15 V, unless otherwise noted.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All minimum and maximum specifications are guaranteed, although only those shown in boldface are tested on all production units.

Table 1.

	AD588JQ/AD588AQ			AD588BQ/AD588KQ			AD588ARWZ			
Parameter[1]	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
OUTPUT VOLTAGE ERROR										
+10 V, −10 V Outputs			**±3**	**−1**		**+1**	**−5**		**+5**	mV
+5 V, −5 V Outputs			**±3**	**−1**		**+1**	**−5**		**+5**	mV
±5 V TRACKING MODE										
Symmetry Error			**±1.5**			**±0.75**			**±1.5**	mV
OUTPUT VOLTAGE DRIFT										
0°C to 70°C (J, K, B)		±2	**±3**			**±1.5**		±2	**±3**	ppm/°C
−25°C to +85°C (A, B)			**±3**			**±3**			**±3**	ppm/°C
GAIN ADJ AND BAL ADJ[2]										
Trim Range		±4			±4			±4		mV
Input Resistance		150			150			150		kΩ
LINE REGULATION										
T_{MIN} to T_{MAX}[3]			**±200**			**±200**			**±200**	µV/V
LOAD REGULATION										
T_{MIN} to T_{MAX}										
+10 V Output, 0 mA < I_{OUT} < 10 mA			**±50**			**±50**			**±50**	µV/mA
−10 V Output, −10 mA < I_{OUT} < 0 mA			**±50**			**±50**			**±50**	µV/mA
SUPPLY CURRENT										
T_{MIN} to T_{MAX}		6	**10**		6	**10**		6	**10**	mA
Power Dissipation		180	**300**		180	**300**		180	**300**	mW
OUTPUT NOISE (Any Output)										
0.1 Hz to 10 Hz		6			6			6		µV p-p
Spectral Density, 100 Hz		100			100			100		nV/√Hz
LONG-TERM STABILITY (at 25°C)		15			15			15		ppm/1000 hr
BUFFER AMPLIFIERS										
Offset Voltage		100			10			100		µV
Offset Voltage Drift		1			1			1		µV/°C
Bias Current		20			20			20		nA
Open-Loop Gain		110			110			110		dB
Output Current (A3, A4)	−10		+10	−10		+10	−10		+10	mA
Common-Mode Rejection (A3, A4)										
V_{CM} = 1 V p-p		100			100			100		dB
Short Circuit Current		50			50			50		mA
TEMPERATURE RANGE										
Specified Performance										
J, K Grades	0		70	0		70				°C
A, B Grades	−25		+85	−25		+85	−25		+85	°C

[1]Specifications tested using ±5 V configuration, unless otherwise indicated. See Figure 4 through Figure 6 for output configurations at +10 V, −10 V, +5 V, −5 V and ±5 V.
[2]Gain and balance adjustments guaranteed capable of trimming output voltage error and symmetry error to zero.
[3]For ±10 V output, ±V_S can be as low as ±12 V. See Table 3 for test conditions at various voltages.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
$+V_S$ to $-V_S$	36 V
Power Dissipation (25°C)	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 sec)	300°C
Package Thermal Resistance (θ_{JA}/θ_{JC})	90°C/25°C/W
Output Protection	All outputs safe if shorted to ground

Table 3. Test Conditions

Voltage	Conditions
+10 V Output	$-V_S = -15$ V, $+13.5$ V ≤ $+V_S$ ≤ $+18$ V
−10 V Output	-18 V ≤ $-V_S$ ≤ -13.5 V, $+V_S = +15$ V
±5 V Output	$+V_S = +18$ V, $-V_S = -18$ V
	$+V_S = +10.8$ V, $-V_S = -10.8$ V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

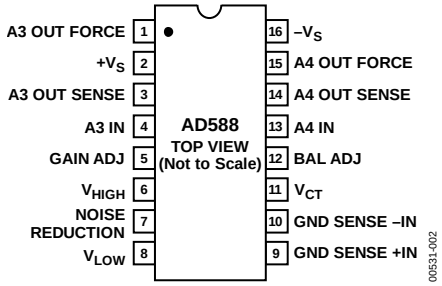


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A3 OUT FORCE	Output from Buffering Amplifier 3 with Kelvin Force. Connect to Pin 3.
2	$+V_S$	Positive Power Supply.
3	A3 OUT SENSE	Output from Buffering Amplifier 3 with Kelvin Sense. Connect to Pin 1.
4	A3 IN	Positive Input to Amplifier 3. Connect to V_{HIGH}, Pin 6.
5	GAIN ADJ	Reference Gain Adjustment for Calibration. See the Calibration section.
6	V_{HIGH}	Unbuffered Reference High Output.
7	NOISE REDUCTION	Noise Filtering Pin. Connect external 1 µF capacitor to ground to reduce the output noise (see the Noise Performance and Reduction section). Can be left open.
8	V_{LOW}	Unbuffered Reference Low Output.
9	GND SENSE +IN	Positive Input to the Ground Sense Amplifier.
10	GND SENSE −IN	Negative Input to the Ground Sense Amplifier.
11	V_{CT}	Center Tap Voltage used for Calibration. See the Calibration section.
12	BAL ADJ	Reference Centering Adjustment for Calibration. See the Calibration section.
13	A4 IN	Positive Input to Amplifier 4. Connect to V_{LOW}, Pin 8.
14	A4 OUT SENSE	Output of Buffering Amplifier 4 with Kelvin Sense. Connect to Pin 15.
15	A4 OUT FORCE	Output of Buffering Amplifier 4 with Kelvin Force. Connect to Pin 14.
16	$-V_S$	Negative Power Supply.

THEORY OF OPERATION

The AD588 consists of a buried Zener diode reference, amplifiers used to provide pin programmable output ranges, and associated thin-film resistors, as shown in Figure 3. The temperature compensation circuitry provides the device with a temperature coefficient of 1.5 ppm/°C or less.

Amplifier A1 performs several functions. A1 primarily acts to amplify the Zener voltage from 6.5 V to the required 10 V output. In addition, A1 provides for external adjustment of the 10 V output through Pin 5, GAIN ADJ. Using the bias compensation resistor between the Zener output and the noninverting input to A1, a capacitor can be added at the NOISE REDUCTION pin (Pin 7) to form a low-pass filter and reduce the noise contribution of the Zener to the circuit. Two matched 10 kΩ nominal thin-film resistors (R4 and R5) divide the 10 V output in half. Pin V_{CT} (Pin 11) provides access to the center of the voltage span and BAL ADJ (Pin 12) can be used for fine adjustment of this division.

Ground sensing for the circuit is provided by Amplifier A2. The noninverting input (Pin 9) senses the system ground, which is transferred to the point on the circuit where the inverting input (Pin 10) is connected. This can be Pin 6, Pin 8, or Pin 11. The output of A2 drives Pin 8 to the appropriate voltage. Thus, if Pin 10 is connected to Pin 8, the V_{LOW} pin is the same voltage as the system ground. Alternatively, if Pin 10 is connected to the V_{CT} pin, it is a ground; and Pin 6 and Pin 8 are +5 V and −5 V, respectively.

Amplifier A3 and Amplifier A4 are internally compensated and are used to buffer the voltages at Pin 6, Pin 8, and Pin 11, as well as to provide a full Kelvin output. Thus, the AD588 has a full Kelvin capability by providing the means to sense a system ground and provide forced and sensed outputs referenced to that ground.

Note that both positive and negative supplies are required for operation of the AD588.

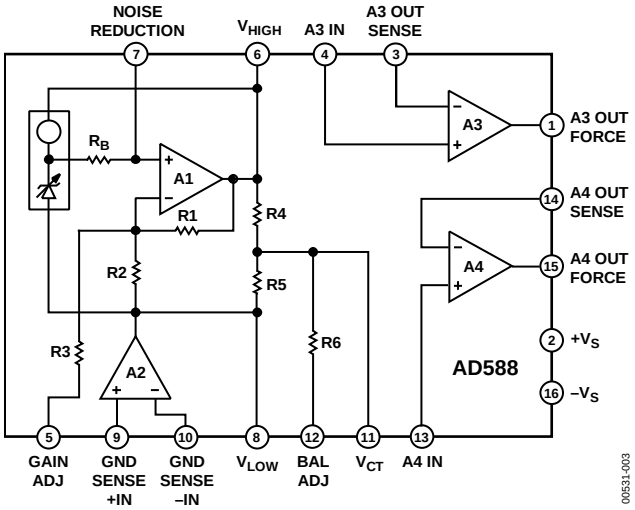


Figure 3. AD588 Functional Block Diagram

APPLICATIONS INFORMATION

The AD588 can be configured to provide +10 V and −10 V reference outputs, as shown in Figure 4 and Figure 6, respectively. It can also be used to provide +5 V, −5 V, or a 5 V tracking reference, as shown in Figure 5. Table 5 details the appropriate pin connections for each output range. In each case, Pin 9 is connected to system ground, and power is applied to Pin 2 and Pin 16.

The architecture of the AD588 provides ground sense and uncommitted output buffer amplifiers that offer the user a great deal of functional flexibility. The AD588 is specified and tested in the configurations shown in Figure 6. The user can choose to take advantage of the many other configuration options available with the AD588. However, performance in these configurations is not guaranteed to meet the extremely stringent data sheet specifications.

As indicated in Table 5, a +5 V buffered output can be provided using Amplifier A4 in the +10 V configuration (Figure 4). A −5 V buffered output can be provided using Amplifier A3 in the −10 V configuration (Figure 6). Specifications are not guaranteed for the +5 V or −5 V outputs in these configurations. Performance is similar to that specified for the +10 V or −10 V outputs.

As indicated in Table 5, unbuffered outputs are available at Pin 6, Pin 8, and Pin 11. Loading of these unbuffered outputs impairs circuit performance.

Amplifier A3 and Amplifier A4 can be used interchangeably. However, the AD588 is tested (and the specifications are guaranteed) with the amplifiers connected, as indicated in Figure 4 and Table 5. When either A3 or A4 is unused, its output force and sense pins should be connected or the input tied to ground.

Two outputs of the same voltage can be obtained by connecting both A3 and A4 to the appropriate unbuffered output on Pin 6, Pin 8, or Pin 11. Performance in these dual-output configurations typically meets data sheet specifications.

CALIBRATION

Generally, the AD588 meets the requirements of a precision system without additional adjustment. Initial output voltage error of 1 mV and output noise specs of 10 μV p-p allow for accuracies of 12 bits to 16 bits. However, in applications where an even greater level of accuracy is required, additional calibration may be called for. Provision for trimming has been made through the use of the GAIN ADJ and BAL ADJ pins (Pin 5 and Pin 12, respectively).

The AD588 provides a precision 10 V span with a center tap (V_{CT}) that is used with the buffer and ground sense amplifiers to achieve the voltage output configurations in Table 5. GAIN ADJ and BAL ADJ can be used in any of these configurations to trim the magnitude of the span voltage and the position of the center tap within the span. The gain adjust should be performed first. Although the trims are not interactive within the device, the gain trim moves the balance trim point as it changes the magnitude of the span.

Table 5. Pin Connections

		Unbuffered[1] Output on Pins						Buffered Output on Pins				
Range	Connect Pin 10 to Pin	−10 V	−5 V	0 V	+5 V	+10 V	Buffered Output Connections	−10 V	−5 V	0 V	+5 V	+10 V
+10 V	8			8	11	6	11 to 13, 14 to 15, 6 to 4, and 3 to 1				15	1
−5 V or +5 V	11		8	11	6		8 to 13, 14 to 15, 6 to 4, and 3 to 1		15		1	
−10 V	6	8	11	6			8 to 13, 14 to 15, 11 to 4, and 3 to 1	15	1			
+5 V	11				6		6 to 4 and 3 to 1				1	
−5 V	11		8				8 to 13 and 14 to 15		15			

[1] Unbuffered outputs should not be loaded.

Figure 5 shows gain and balance trims in a +5 V and −5 V tracking configuration. A 100 kΩ, 20-turn potentiometer is used for each trim. The potentiometer for gain trim is connected between Pin 6 (V_{HIGH}) and Pin 8 (V_{LOW}) with the wiper connected to Pin 5 (GAIN ADJ). The potentiometer is adjusted to produce exactly 10 V between Pin 1 and Pin 15, the amplifier outputs. The balance potentiometer, also connected between Pin 6 and Pin 8 with the wiper to Pin 12 (BAL ADJ), is then adjusted to center the span from +5 V to −5 V.

Trimming in other configurations works in exactly the same manner. When producing +10 V and +5 V, GAIN ADJ is used to trim +10 V and BAL ADJ is used to trim +5 V. In the −10 V and −5 V configuration, GAIN ADJ is again used to trim the magnitude of the span, −10 V, while BAL ADJ is used to trim the center tap, −5 V.

Trimming the AD588 introduces no additional errors over temperature, so precision potentiometers are not required. For single-output voltage ranges, or in cases when balance adjust is not required, Pin 12 should be connected to Pin 11. If gain adjust is not required, Pin 5 should be left floating.

In single output configurations, GAIN ADJ is used to trim outputs utilizing the full span (+10 V or −10 V), while BAL ADJ is used to trim outputs using half the span (+5 V or −5 V).

Input impedance on both the GAIN ADJ and BAL ADJ pins is approximately 150 kΩ. The GAIN ADJ trim network effectively attenuates the 10 V across the trim potentiometer by a factor of about 1500 to provide a trim range of −3.5 mV to +7.5 mV with a resolution of approximately 550 μV/turn (20-turn potentiometer). The BAL ADJ trim network attenuates the trim voltage by a factor of about 1400, providing a trim range of ±4.5 mV with resolution of 450 μV/turn.

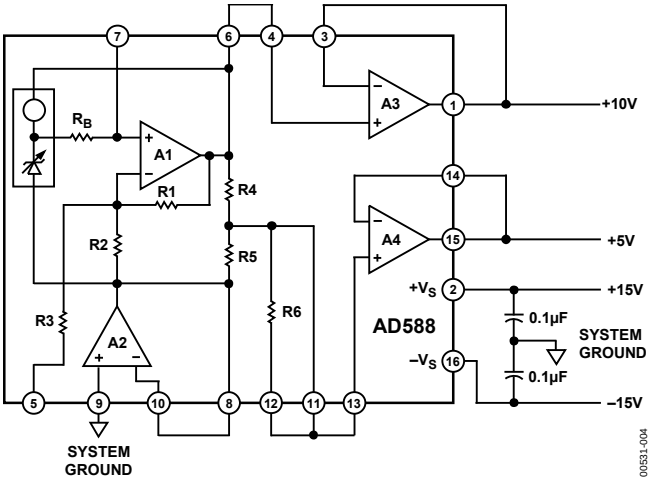


Figure 4. +10 V Output

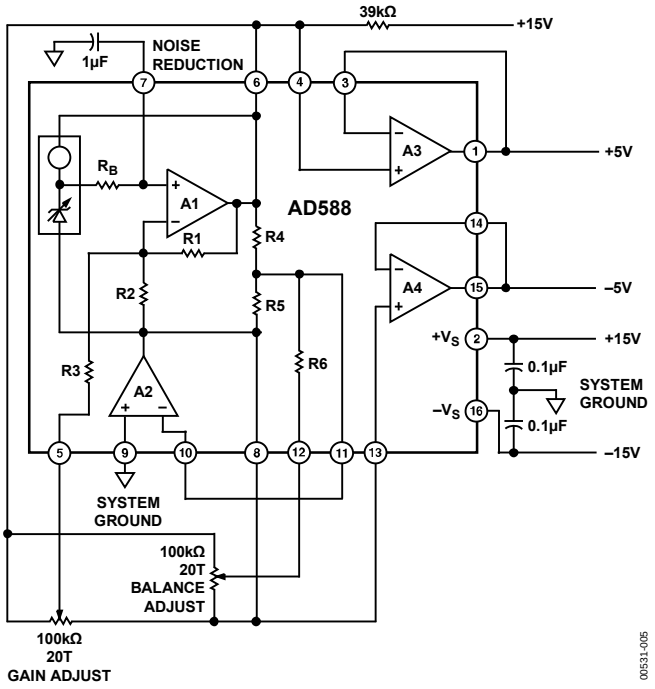


Figure 5. +5 V and −5 V Outputs

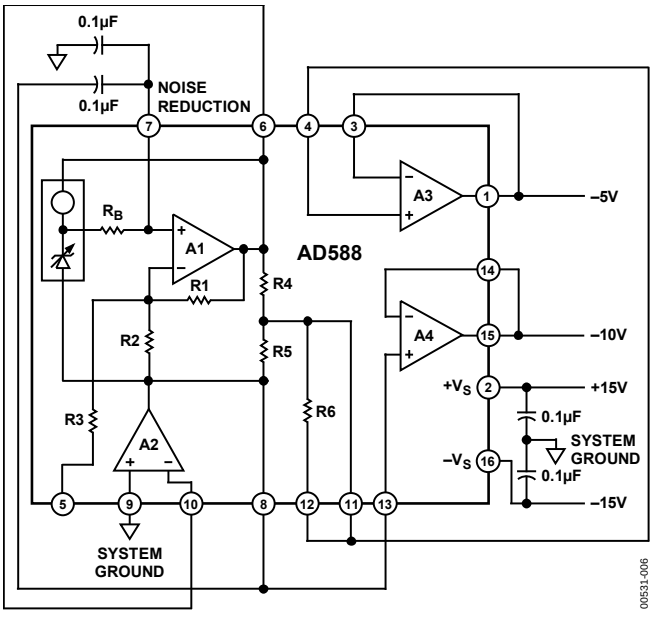


Figure 6. −10 V Output

NOISE PERFORMANCE AND REDUCTION

The noise generated by the AD588 is typically less than 6 µV p-p over the 0.1 Hz to 10 Hz band. Noise in a 1 MHz bandwidth is approximately 600 µV p-p. The dominant source of this noise is the buried Zener, which contributes approximately 100 nV/√Hz. In comparison, the op amp's contribution is negligible. Figure 7 shows the 0.1 Hz to 10 Hz noise of a typical AD588.

If further noise reduction is desired, an optional capacitor, C_N, can be added between the NOISE REDUCTION pin and ground, as shown in Figure 5.

This forms a low-pass filter with the 4 kΩ R_B on the output of the Zener cell. A 1 µF capacitor has a 3 dB point at 40 Hz and reduces the high frequency noise (to 1 MHz) to about 200 µV p-p. Figure 8 shows the 1 MHz noise of a typical AD588 both with and without a 1 µF capacitor.

Note that a second capacitor is needed in order to implement the noise reduction feature when using the AD588 in the −10 V mode (Figure 6). The noise reduction capacitor is limited to 0.1 µF maximum in this mode.

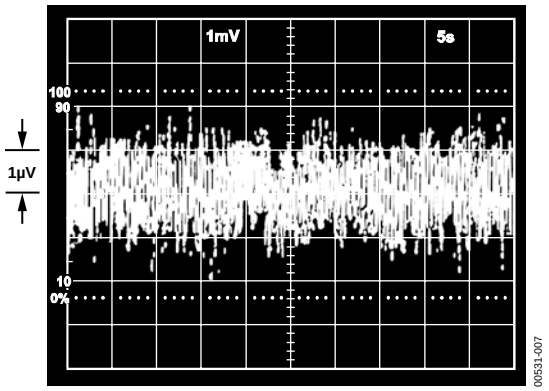


Figure 7. 0.1 Hz to 10 Hz Noise (0.1 Hz to 10 Hz BPF with Gain of 1000 Applied)

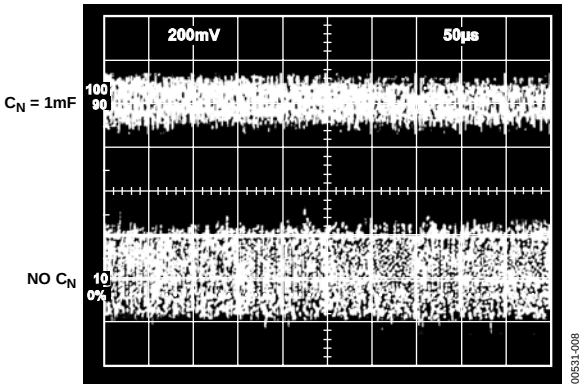


Figure 8. Effect of 1 µF Noise Reduction Capacitor on Broadband Noise

TURN-ON TIME

Upon application of power (cold start), the time required for the output voltage to reach its final value within a specified error band is the turn-on settling time. Two components normally associated with this are the time for active circuits to settle and the time for thermal gradients on the chip to stabilize.

Figure 9 and Figure 10 show the turn-on characteristics of the AD588. The settling is about 600 µs. Note the absence of any thermal tails when the horizontal scale is expanded to 2 ms/cm in Figure 10.

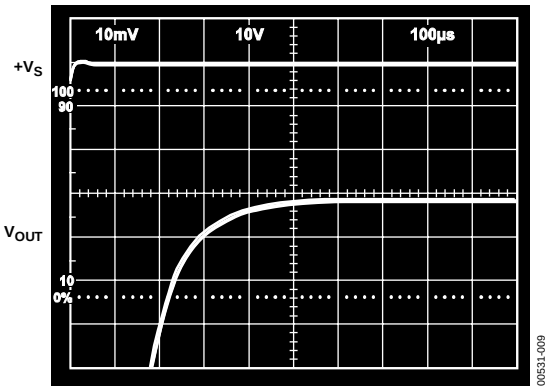


Figure 9. Electrical Turn-On

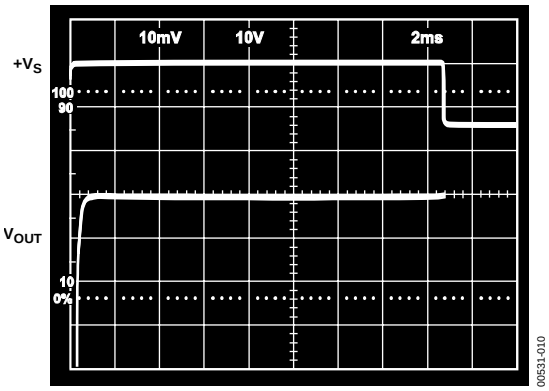


Figure 10. Extended Time Scale Turn-On

Output turn-on time is modified when an external noise reduction capacitor is used. When present, this capacitor presents an additional load to the internal Zener diode current source, resulting in a somewhat longer turn-on time. In the case of a 1 µF capacitor, the initial turn-on time is approximately 60 ms (see Figure 11).

Note that if the noise reduction feature is used in the ±5 V configuration, a 39 kΩ resistor between Pin 6 and Pin 2 is required for proper startup.

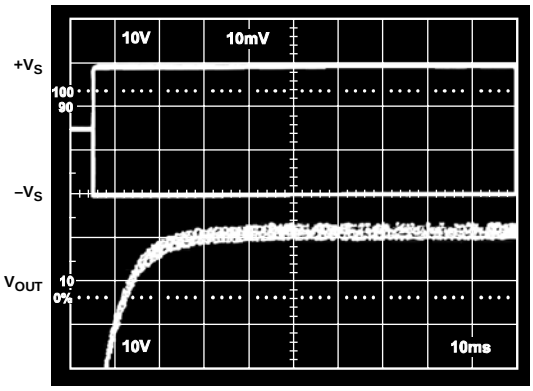


Figure 11. Turn-On with CN = 1 µF

TEMPERATURE PERFORMANCE

The AD588 is designed for precision reference applications where temperature performance is critical. Extensive temperature testing ensures that the device's high level of performance is maintained over the operating temperature range.

Figure 12 shows typical output temperature drift for the AD588BQ and illustrates the test methodology. The box in Figure 12 is bounded on the sides by the operating temperature extremes and on top and bottom by the maximum and minimum output voltages measured over the operating temperature range. The slope of the diagonal drawn from the lower left corner of the box determines the performance grade of the device.

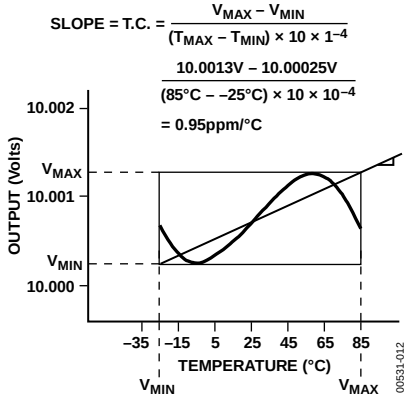


Figure 12. Typical AD588BQ Temperature Drift

Each AD588 A and B grade unit is tested at −25°C, 0°C, +25°C, +50°C, +70°C, and +85°C. This approach ensures that the variations of output voltage that occur as the temperature changes within the specified range is contained within a box whose diagonal has a slope equal to the maximum specified drift. The position of the box on the vertical scale changes from device to device as initial error and the shape of the curve vary. Maximum height of the box for the appropriate temperature range is shown in Figure 13. Duplication of these results requires a combination of high accuracy and stable temperature control in a test system. Evaluation of the AD588 produces a curve similar to that in Figure 12, but output readings may vary, depending on the test methods and equipment utilized.

DEVICE GRADE	MAXIMUM OUTPUT CHANGE (mV)	
	0°C TO +70°C	−25°C TO +85°C
AD588J	2.10	
AD588K	1.05	
AD588A	1.40 (TYP)	3.30
AD588B	1.05	3.30

00531-013

Figure 13. Maximum Output Change—mV

KELVIN CONNECTIONS

Force and sense connections, also referred to as Kelvin connections, offer a convenient method of eliminating the effects of voltage drops in circuit wires. As seen in Figure 14, the load current and wire resistance produce an error ($V_{ERROR} = R \times I_L$) at the load.

The Kelvin connection of Figure 14 overcomes the problem by including the wire resistance within the forcing loop of the amplifier and sensing the load voltage. The amplifier corrects for any errors in the load voltage. In the circuit shown, the output of the amplifier would actually be at 10 V + V_{ERROR}, and the voltage at the load would be the desired 10 V.

The AD588 has three amplifiers that can be used to implement Kelvin connections. Amplifier A2 is dedicated to the ground force-sense function, while uncommitted Amplifier A3 and Amplifier A4 are free for other force-sense chores.

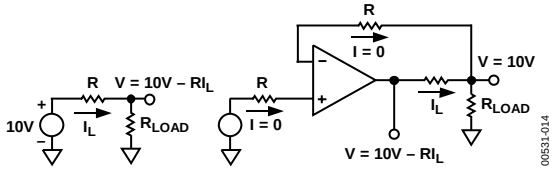


Figure 14. Advantage of Kelvin Connection

In some single-output applications, one amplifier can be unused. In such cases, the unused amplifier should be connected as a unity-gain follower (force and sense pin tied together), and the input should be connected to ground.

An unused amplifier section can be used for other circuit functions, as well. Figure 15 through Figure 19 show the typical performance of A3 and A4.

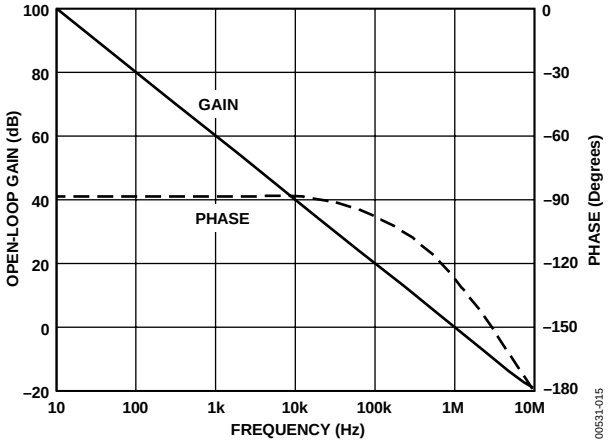


Figure 15. Open-Loop Frequency Response (A3, A4)

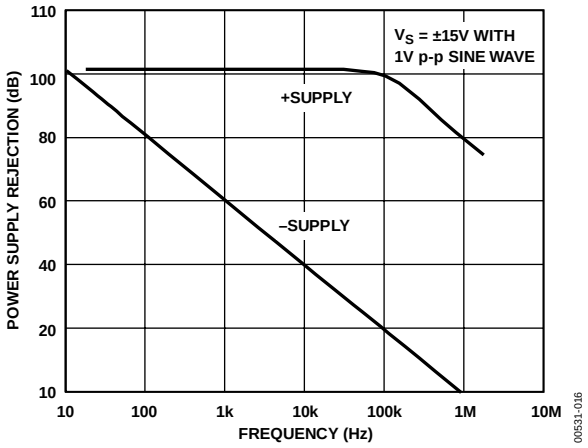


Figure 16. Power Supply Rejection vs. Frequency (A3, A4)

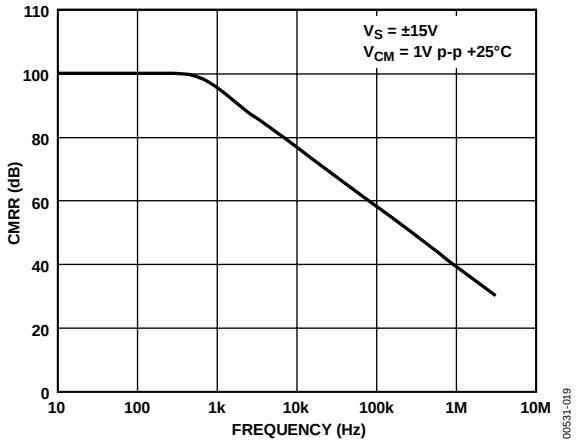


Figure 19. Common-Mode Rejection vs. Frequency (A3, A4)

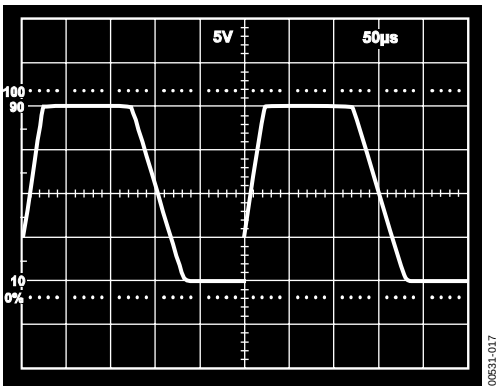


Figure 17. Unity-Gain Follower Pulse Response (Large Signal)

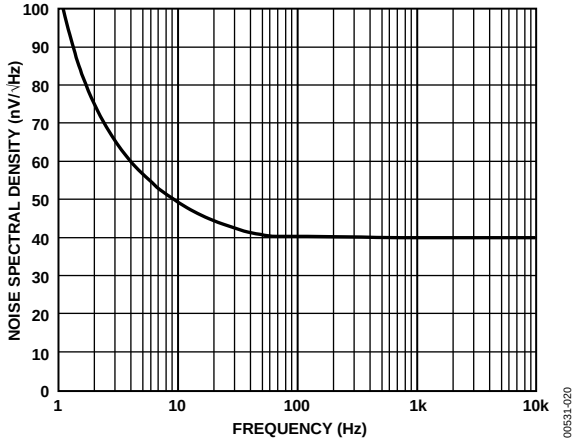


Figure 20. Input Noise Voltage Spectral Density

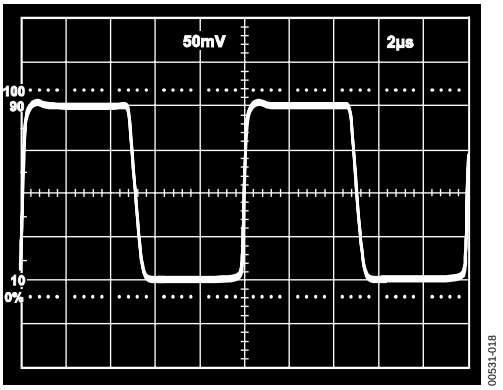


Figure 18. Unity-Gain Follower Pulse Response (Small Signal)

DYNAMIC PERFORMANCE

The output buffer amplifiers (A3 and A4) are designed to provide the AD588 with static and dynamic load regulation superior to less complete references. Many analog-to-digital and digital-to-analog converters present transient current loads to the reference, and poor reference response can degrade converter performance. Figure 21 and Figure 22 display the characteristics of the AD588 output amplifier driving a 0 mA to 10 mA load.

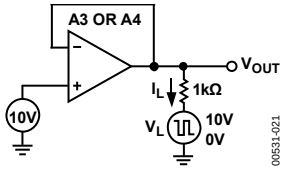


Figure 21. Transient Load Test Circuit

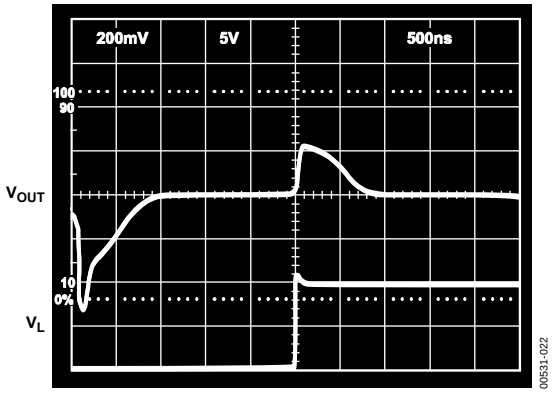


Figure 22. Large-Scale Transient Response

Figure 23 and Figure 24 display the output amplifier characteristics driving a 5 mA to 10 mA load, a common situation found when the reference is shared among multiple converters or is used to provide a bipolar offset current.

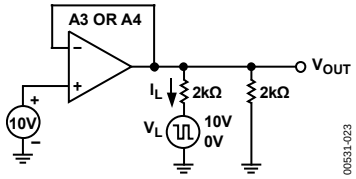


Figure 23. Transient and Constant Load Test Circuit

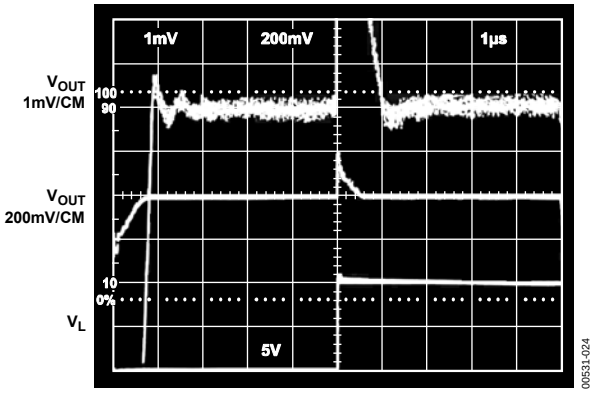


Figure 24. Transient Response 5 mA to10 mA Load

In some applications, a varying load can be both resistive and capacitive in nature or can be connected to the AD588 by a long capacitive cable. Figure 25 and Figure 26 display the output amplifier characteristics driving a 1000 pF, 0 mA to 10 mA load.

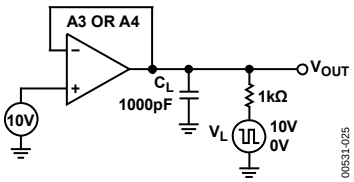


Figure 25. Capacitive Load Transient Response Test Circuit

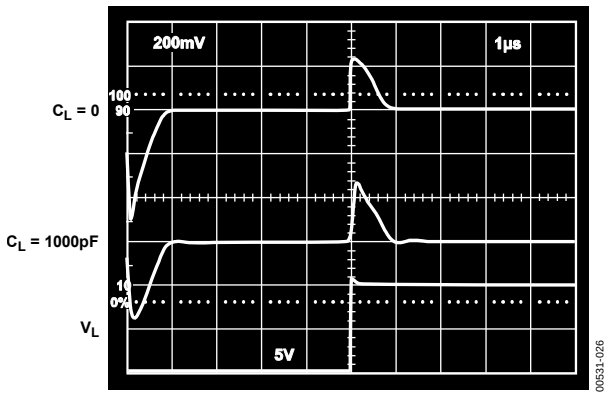


Figure 26. Output Response with Capacitive Load

Figure 27 and Figure 28 display the crosstalk between output amplifiers. The top trace shows the output of A4, dc-coupled and offset by 10 V, while the output of A3 is subjected to a 0 mA to 10 mA load current step. The transient at A4 settles in about 1 µs, and the load-induced offset is about 100 µV.

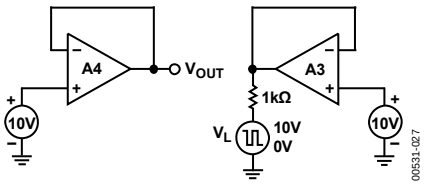


Figure 27. Load Crosstalk Test Circuit

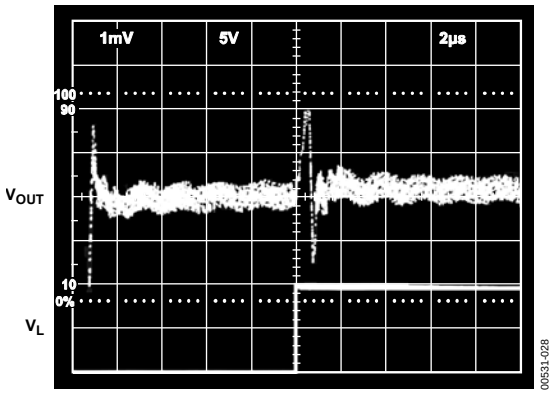


Figure 28. Load Crosstalk

Attempts to drive a large capacitive load (in excess of 1000 pF) can result in ringing or oscillation, as shown in the step response photo (Figure 29). This is due to the additional pole formed by the load capacitance and the output impedance of the amplifier, which consumes phase margin.

The recommended method of driving capacitive loads of this magnitude is shown in Figure 30. The 150 Ω resistor isolates the capacitive load from the output stage, while the 10 kΩ resistor provides a dc feedback path and preserves the output accuracy. The 1 μF capacitor provides a high frequency feedback loop. The performance of this circuit is shown in Figure 31.

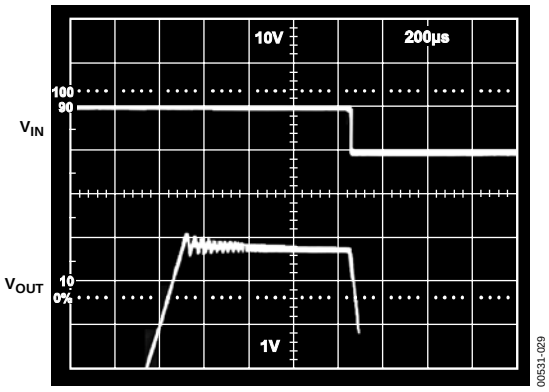


Figure 29. Output Amplifier Step Response, C_L = 1 µF

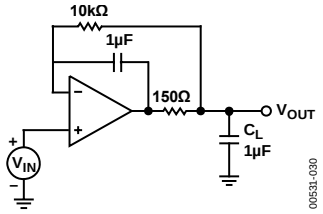


Figure 30. Compensation for Capacitive Loads

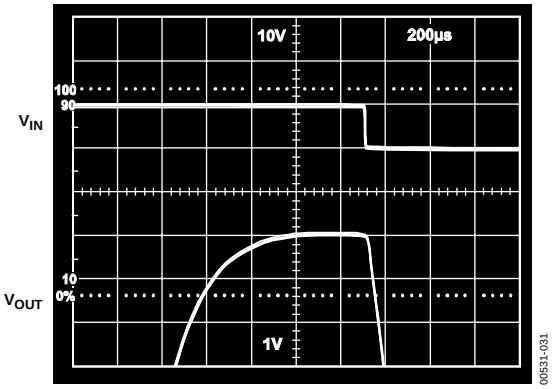


Figure 31. Output Amplifier Step Response Using Figure 30 Compensation

USING THE AD588 WITH CONVERTERS

The AD588 is an ideal reference for a wide variety of analog-to-digital and digital-to-analog converters. Several representative examples follow.

AD7535 14-BIT DIGITAL-TO-ANALOG CONVERTER

High resolution CMOS digital-to-analog converters require a reference voltage of high precision to maintain rated accuracy. The combination of the AD588 and AD7535 takes advantage of the initial accuracy, drift, and full Kelvin output capability of the AD588, as well as the resolution, monotonicity, and accuracy of the AD7535 to produce a subsystem with outstanding characteristics (see Figure 32).

AD569 16-BIT DIGITAL-TO-ANALOG CONVERTER

Another application that fully utilizes the capabilities of the AD588 is supplying a reference for the AD569, as shown in Figure 33. Amplifier A2 senses system common and forces V_{CT} to assume this value, producing +5 V and −5 V at Pin 6 and Pin 8, respectively. Amplifier A3 and Amplifier A4 buffer these voltages out to the appropriate reference force-sense pins of the AD569. The full Kelvin scheme eliminates the effect of the circuit traces or wires and the wire bonds of the AD588 and AD569 themselves, which would otherwise degrade system performance.

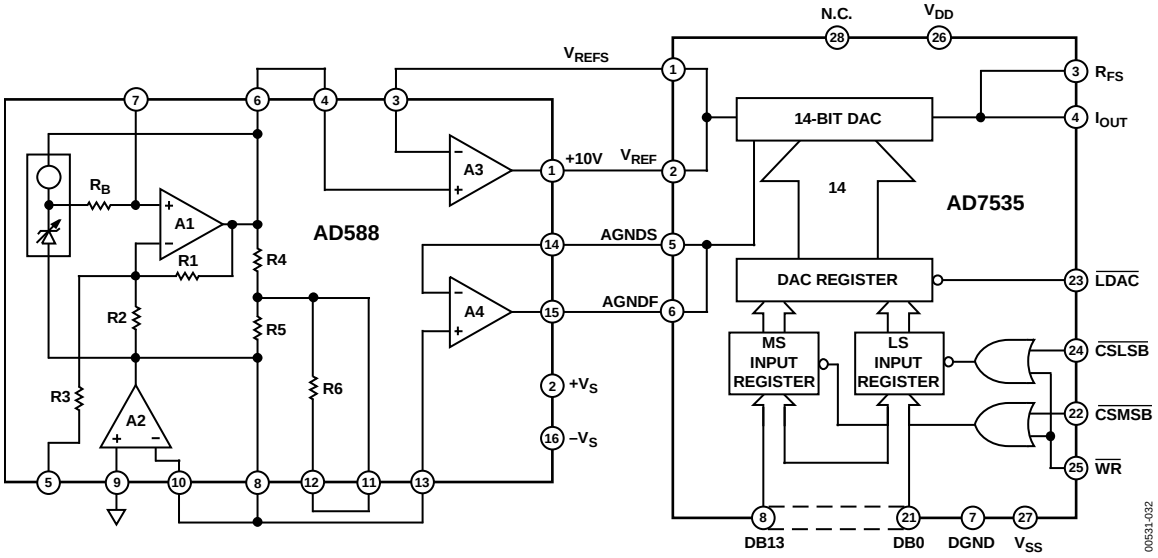


Figure 32. AD588/AD7535 Connections

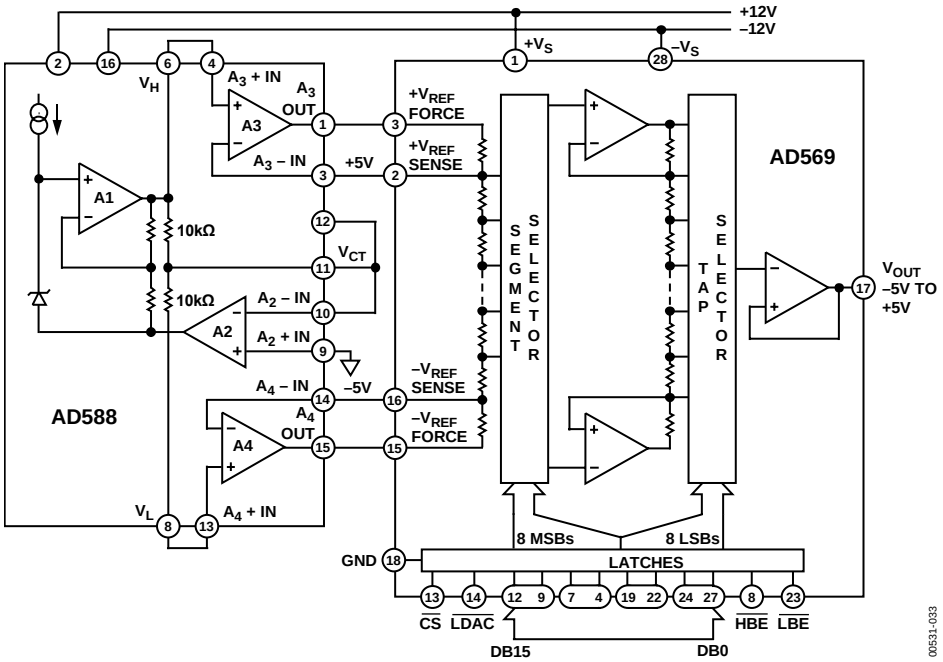


Figure 33. High Accuracy ±5 V Tracking Reference for AD569

SUBSTITUTING FOR INTERNAL REFERENCES

Many converters include built-in references. Unfortunately, such references are the major source of drift in these converters. By using a more stable external reference like the AD588, drift performance can be improved dramatically.

AD574A 12-BIT ANALOG-TO-DIGITAL CONVERTER

The AD574A is specified for gain drift from 10 ppm/°C to 50 ppm/°C (depending on grade), using its on-chip reference. The reference contributes typically 75% of this drift. Using an AD588 as a reference source can improve the total drift by a factor of 3 to 4.

Using this combination can result in apparent increases in full-scale error due to the difference between the on-board reference, by which the device is laser-trimmed, and the external reference, with which the device is actually applied. The on-board reference is specified to be 10 V ± 100 mV, while the external reference is specified to be 10 V ± 1 mV. This may result in up to 101 mV of apparent full-scale error beyond the ±25 mV specified AD574A gain error. External Resistor R2 and Resistor R3 allow this error to be nulled. Their contribution to full-scale drift is negligible.

The high output drive capability allows the AD588 to drive up to six converters in a multiconverter system. All converters have gain errors that track to better than ±5 ppm/°C.

RESISTANCE TEMPERATURE DETECTOR (RTD) EXCITATION

The RTD is a circuit element whose resistance is characterized by a positive temperature coefficient. A measurement of resistance indicates the measured temperature. Unfortunately, the resistance of the wires leading to the RTD often adds error to this measurement. The 4-wire ohms measurement overcomes this problem. This method uses two wires to bring an excitation current to the RTD and two additional wires to tap off the resulting RTD voltage. If these additional two wires go to a high input impedance measurement circuit, the effect of their resistance is negligible. They therefore transmit the true RTD voltage.

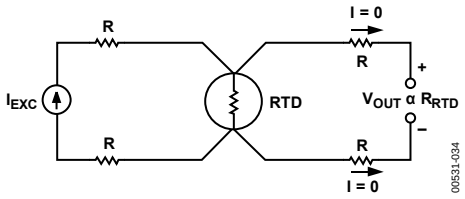


Figure 34. 4-Wire Ohms Measurement

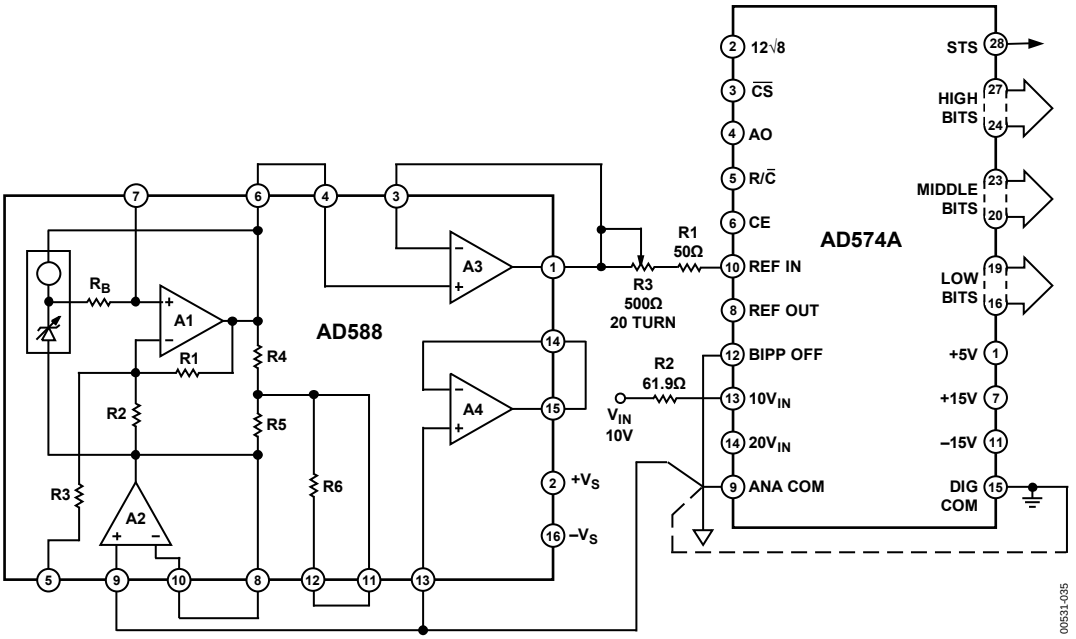


Figure 35. AD588/AD574A Connections

A practical consideration when using the 4-wire ohms technique with an RTD is the self-heating effect that the excitation current has on the temperature of the RTD. The designer must choose the smallest practical excitation current that still gives the desired resolution. RTD manufacturers usually specify the self-heating effect of each of their models or types of RTDs.

Figure 36 shows an AD588 providing the precision excitation current for a 100 Ω RTD. The small excitation current of 1 mA dissipates a mere 0.1 mW of power in the RTD.

BOOSTED PRECISION CURRENT SOURCE

In the RTD current-source application, the load current is limited to ±10 mA by the output drive capability of Amplifier A3. In the event that more drive current is needed, a series-pass transistor can be inserted inside the feedback loop to provide higher current. Accuracy and drift performance are unaffected by the pass transistor.

BRIDGE DRIVER CIRCUITS

The Wheatstone bridge is a common transducer. In its simplest form, a bridge consists of four two-terminal elements connected to form a quadrilateral, a source of excitation connected along one of the diagonals and a detector comprising the other diagonal.

Figure 38 shows a simple bridge driven from a unipolar excitation supply. EO, a differential voltage, is proportional to the deviation of the element from the initial bridge values. Unfortunately, this bridge output voltage is riding on a common-mode voltage equal to approximately $V_{IN}/2$. Further processing of this signal may necessarily be limited to high common-mode rejection techniques, such as instrumentation or isolation amplifiers.

Figure 39 shows the same bridge transducer, this time driven from a pair of bipolar supplies. This configuration ideally eliminates the common-mode voltage and relaxes the restrictions on any processing elements that follow.

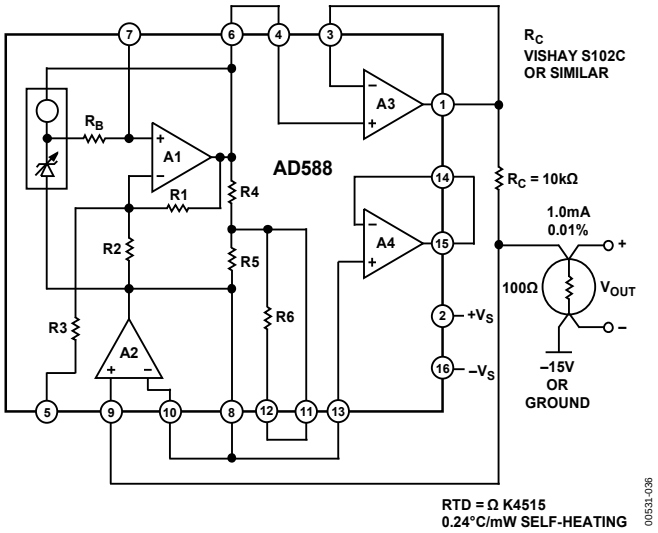


Figure 36. Precision Current Source for RTD

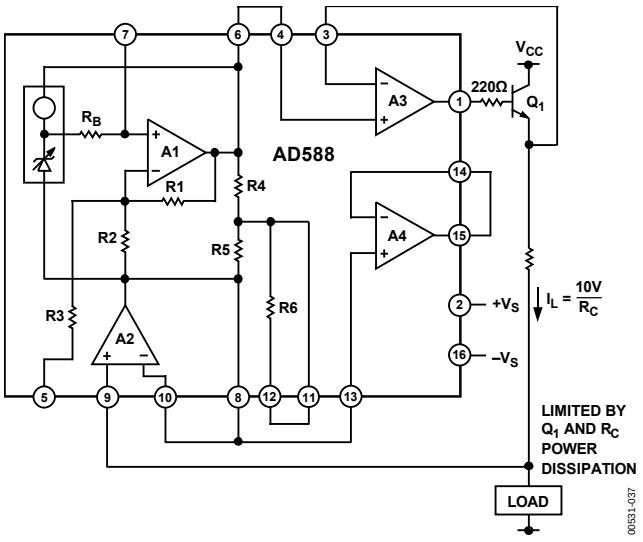


Figure 37. Boosted Precision Current Source

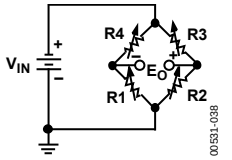


Figure 38. Bridge Transducer Excitation—Unipolar Drive

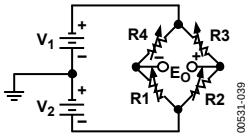


Figure 39. Bridge Transducer Excitation—Bipolar Drive

As shown in Figure 40, the AD588 is an excellent choice for the control element in a bipolar bridge driver scheme. Transistor Q1 and Transistor Q2 serve as series-pass elements to boost the current drive capability to the 28 mA required by a typical 350 Ω bridge. A differential gain stage can still be required if the bridge balance is not perfect. Such gain stages can be expensive.

Additional common-mode voltage reduction is realized by using the circuit illustrated in Figure 41. A1, the ground sense amplifier, serves the supplies on the bridge to maintain a virtual ground at one center tap. The voltage that appears on the opposite center tap is now single-ended (referenced to ground) and can be amplified by a less expensive circuit.

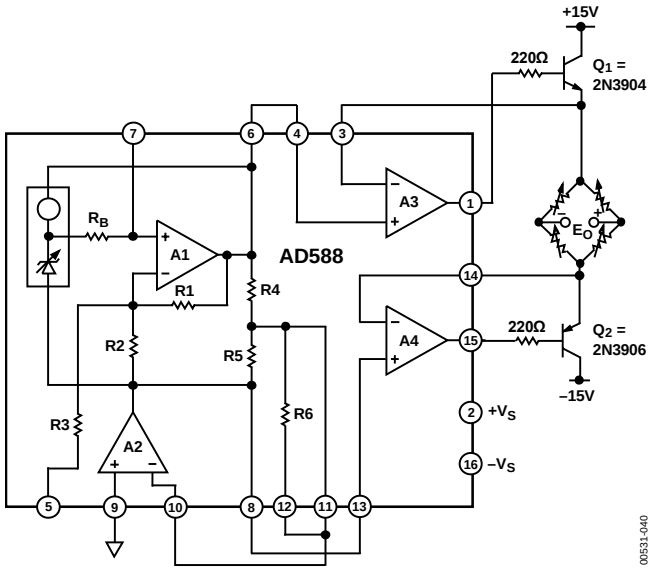


Figure 40. Bipolar Bridge Drive

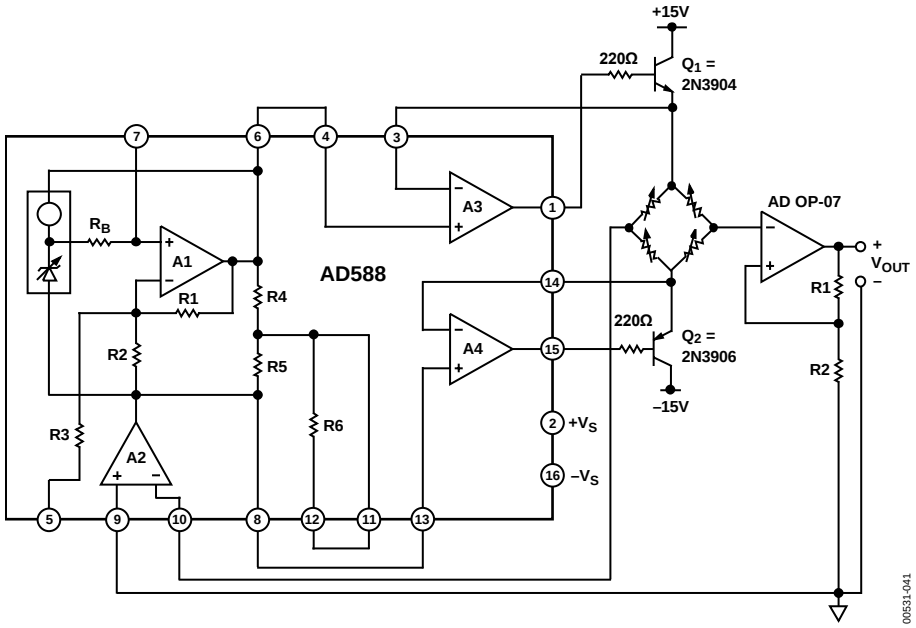
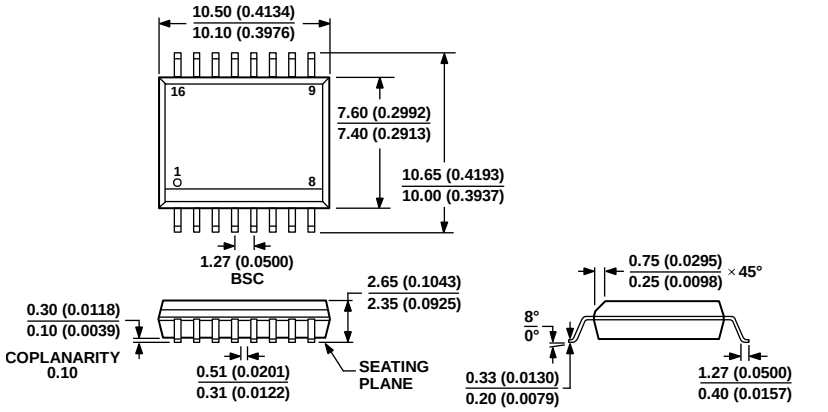


Figure 41. Floating Bipolar Bridge Drive with Minimum CMV

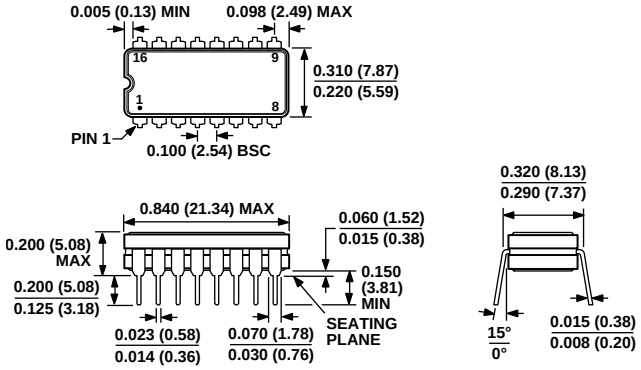
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013- AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

032707-B

Figure 42. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 43. 16-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-16)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1, 2]	Initial Error (mV)	Temperature Coefficient[3]	Temperature Range (°C)	Package Description	Package Option
AD588ARWZ	5	3 ppm/°C	−25 to +85	16-Lead Standard Small Outline Package [SOIC-W]	RW-16
AD588AQ	3	3 ppm/°C	−25 to +85	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16
AD588BQ	1	1.5 ppm/°C	−25 to +85	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16
AD588JQ	3	3 ppm/°C	0 to 70	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16
AD588KQ	1	1.5 ppm/°C	0 to 70	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16

[1] For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD588/883B data sheet.
[2] Z = RoHS Compliant Part.
[3] Temperature coefficient specified from 0°C to 70°C.

NOTES

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