

N-channel 600 V, 0.400 Ω typ., 6.5 A MDmesh™ M2 Power MOSFET in a PowerFLAT 5x6 HV package

Datasheet - production data

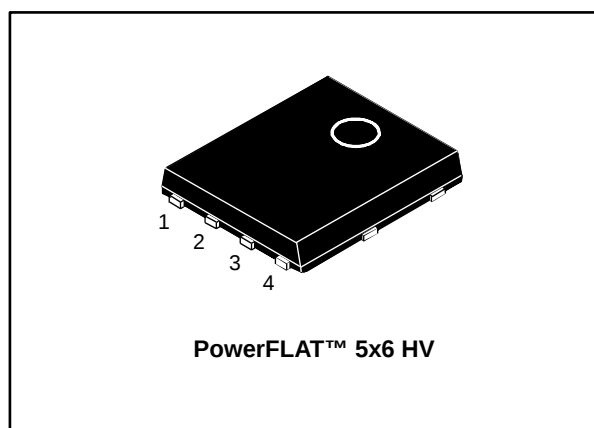
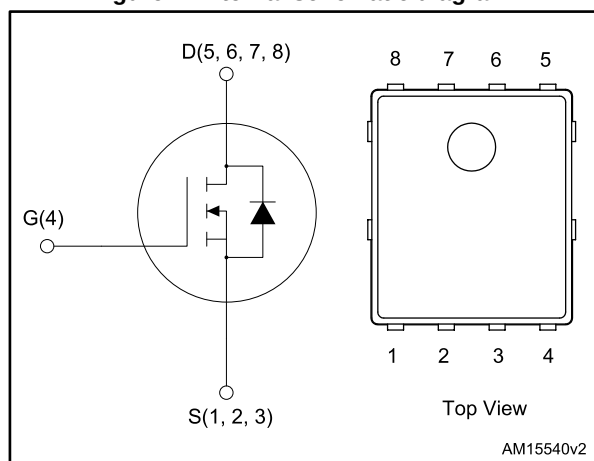


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STL12N60M2	600 V	0.495 Ω	6.5 A	52 W

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STL12N60M2	12N60M2	PowerFLAT 5x6 HV	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$	6.5	A
	Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$	4.1	
$I_{DM}^{(2)}$	Drain current (pulsed)	26	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$	52	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature	-55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature		

Notes:

- (1) Limited by maximum junction temperature.
 (2) Pulse width is limited by safe operating area.
 (3) $I_{SD} \leq 6.5\text{ A}$, $di/dt = 400\text{ A}/\mu\text{s}$; $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.
 (4) $V_{DS} \leq 480\text{ V}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.4	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	

Notes:

- (1) When mounted on a 1-inch² FR-4, 2 Oz copper board.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive	1.6	A
$E_{AR}^{(2)}$	Single pulse avalanche energy	120	mJ

Notes:

- (1) Pulse width limited by T_{jmax} .
 (2) starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 1 mA	600			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 600 V			1	μA
		V _{GS} = 0 V, V _{DS} = 600 V, T _{case} = 125 °C			100	
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±25 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 4.5 A		0.400	0.495	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	538	-	pF
C _{oss}	Output capacitance		-	29	-	
C _{rss}	Reverse transfer capacitance		-	1.1	-	
C _{oss eq.} ⁽¹⁾	Equivalent output capacitance	V _{DS} = 0 to 480 V, V _{GS} = 0 V	-	106	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz, I _D = 0 A	-	7	-	Ω
Q _g	Total gate charge	V _{DD} = 400 V, I _D = 9 A, V _{GS} = 10 V (see Figure 15: "Gate charge test circuit")	-	16	-	nC
Q _{gs}	Gate-source charge		-	2.3	-	
Q _{gd}	Gate-drain charge		-	8.5	-	

Notes:

⁽¹⁾ C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 300 V, I _D = 4.5 A R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 14: "Switching times test circuit for resistive load" and Figure 19: "Switching time waveform")	-	9.2	-	ns
t _r	Rise time		-	9.2	-	
t _{d(off)}	Turn-off delay time		-	56	-	
t _f	Fall time		-	18	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		9	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		36	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 9\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 9\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16 : "Test circuit for inductive load switching and diode recovery times")	-	284		ns
Q_{rr}	Reverse recovery charge		-	2.4		μC
I_{RRM}	Reverse recovery current		-	17		A
t_{rr}	Reverse recovery time	$I_{SD} = 9\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16 : "Test circuit for inductive load switching and diode recovery times")	-	404		ns
Q_{rr}	Reverse recovery charge		-	3.5		μC
I_{RRM}	Reverse recovery current		-	17.5		A

Notes:

⁽¹⁾ Pulse width is limited by safe operating area.

⁽²⁾ Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

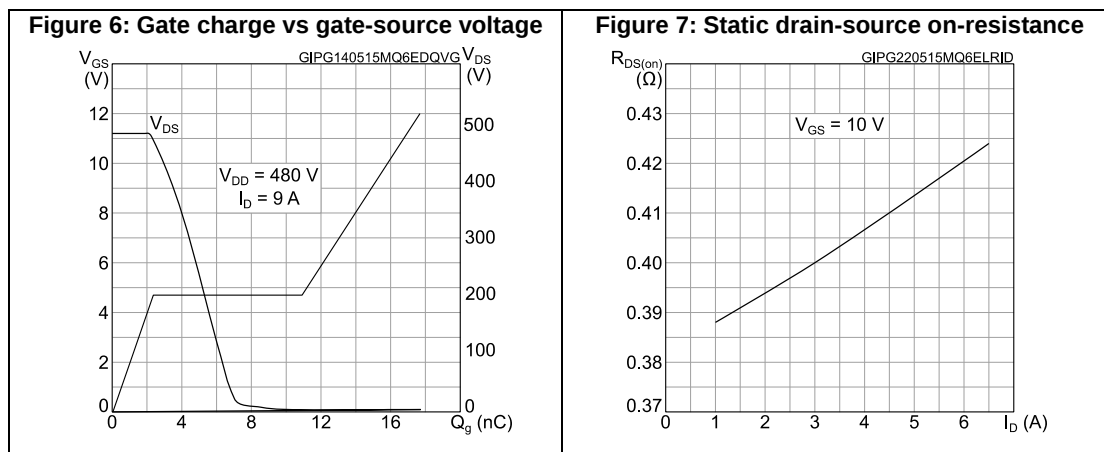
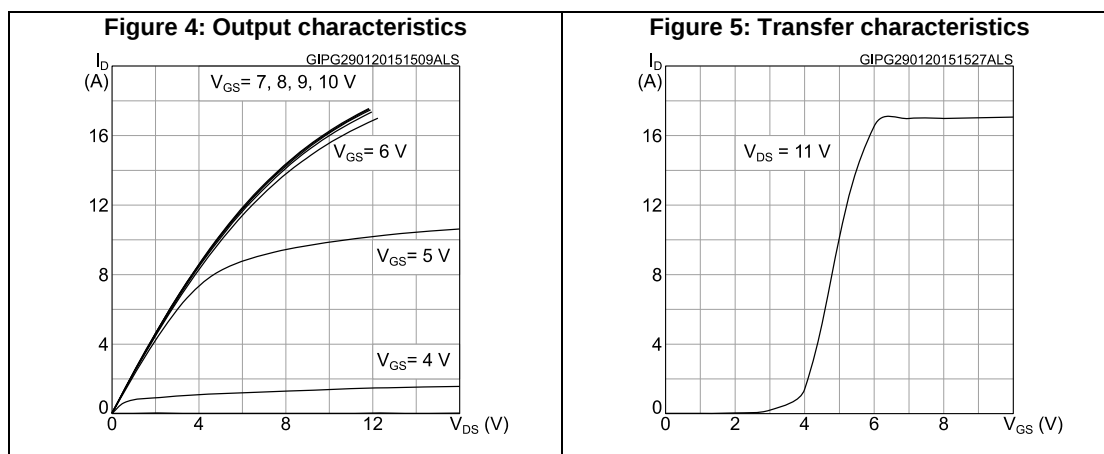
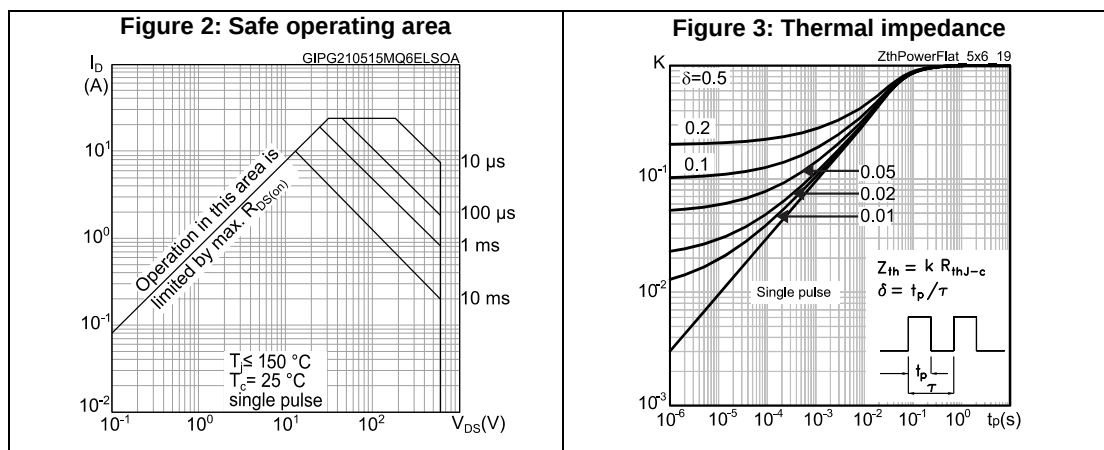


Figure 8: Capacitance variations

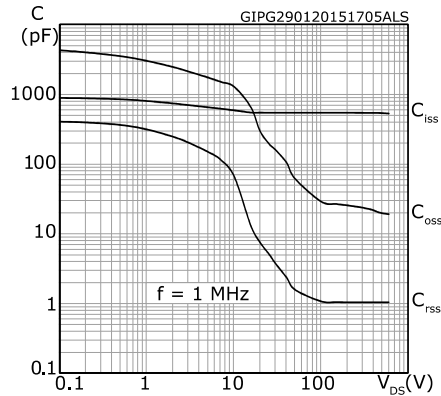


Figure 9: Normalized gate threshold voltage vs temperature

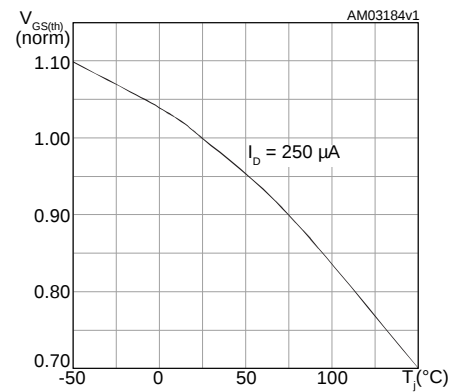


Figure 10: Normalized on-resistance vs temperature

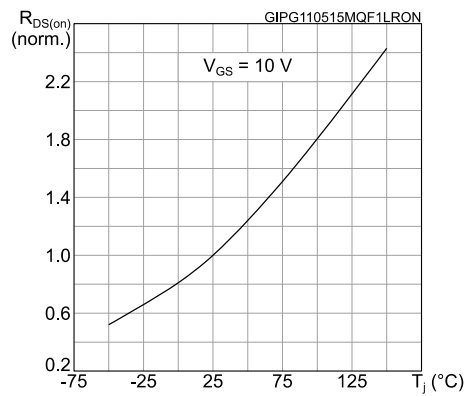


Figure 11: Normalized V(BR)DSS vs temperature

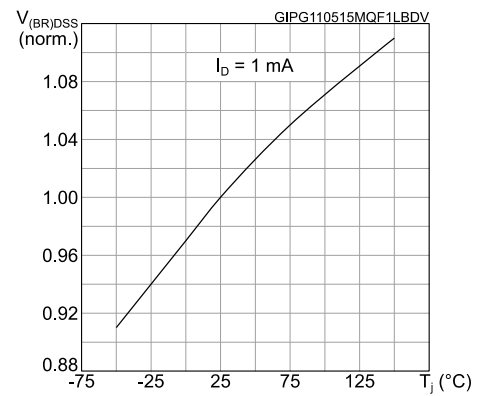


Figure 12: Output capacitance stored energy

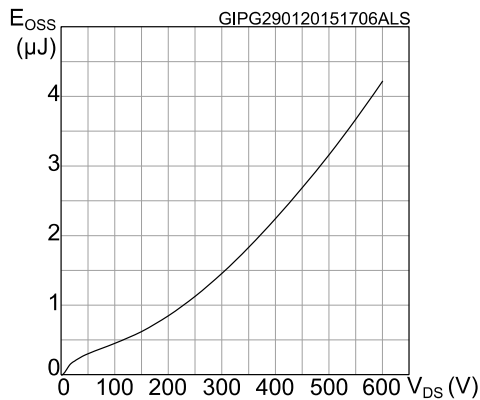
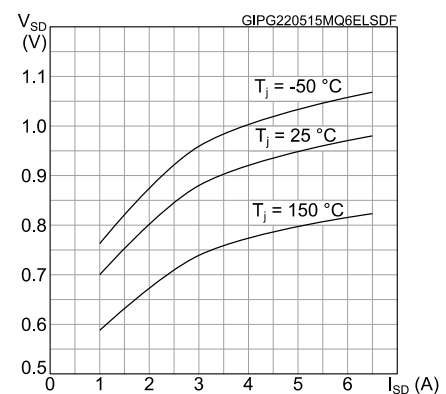
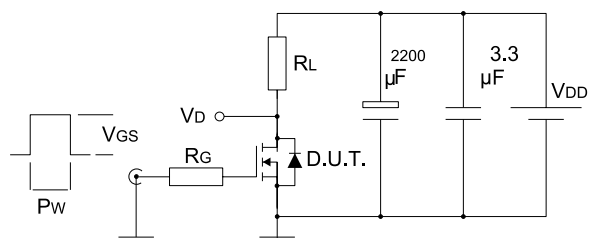


Figure 13: Source- drain diode forward characteristics



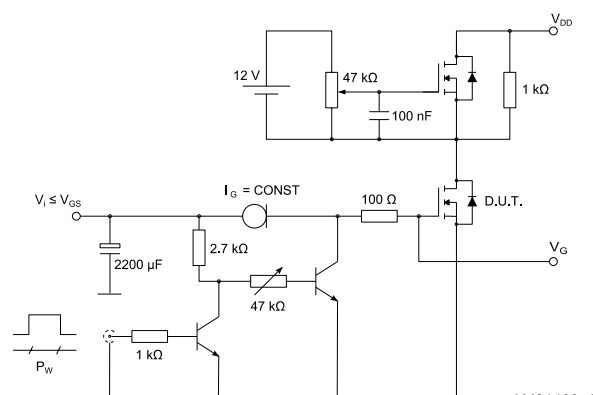
3 Test circuits

Figure 14: Switching times test circuit for resistive load



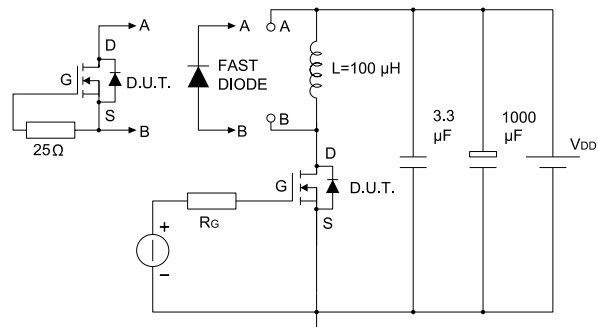
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Figure 15: Gate charge test circuit



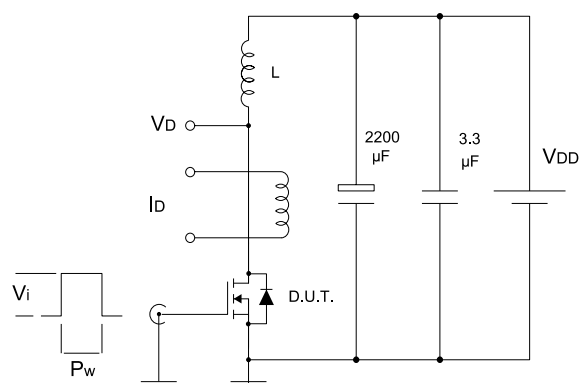
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Figure 16: Test circuit for inductive load switching and diode recovery times



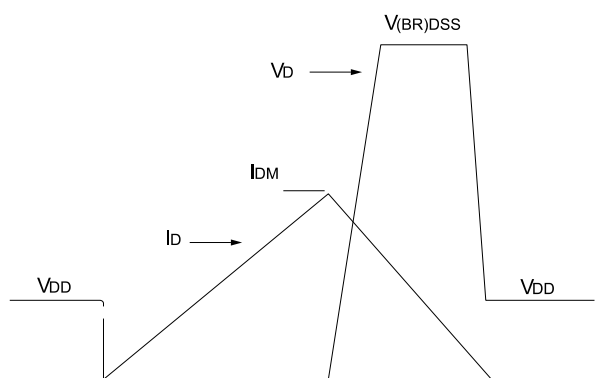
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Figure 17: Unclamped inductive load test circuit



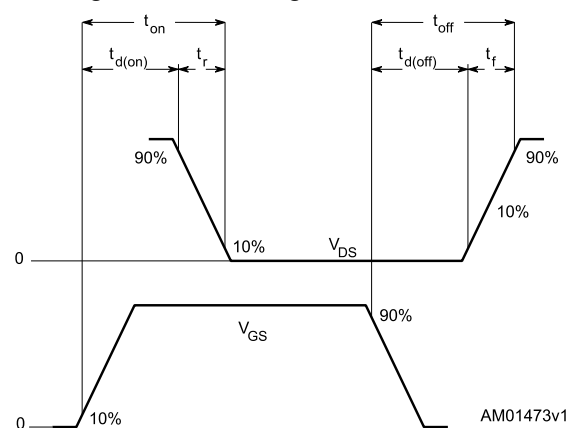
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Figure 18: Unclamped inductive waveform



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Figure 19: Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK[®] is an ST trademark.

4.1 PowerFLAT™ 5x6 HV package information

Figure 20: PowerFLAT™ 5x6 HV package outline

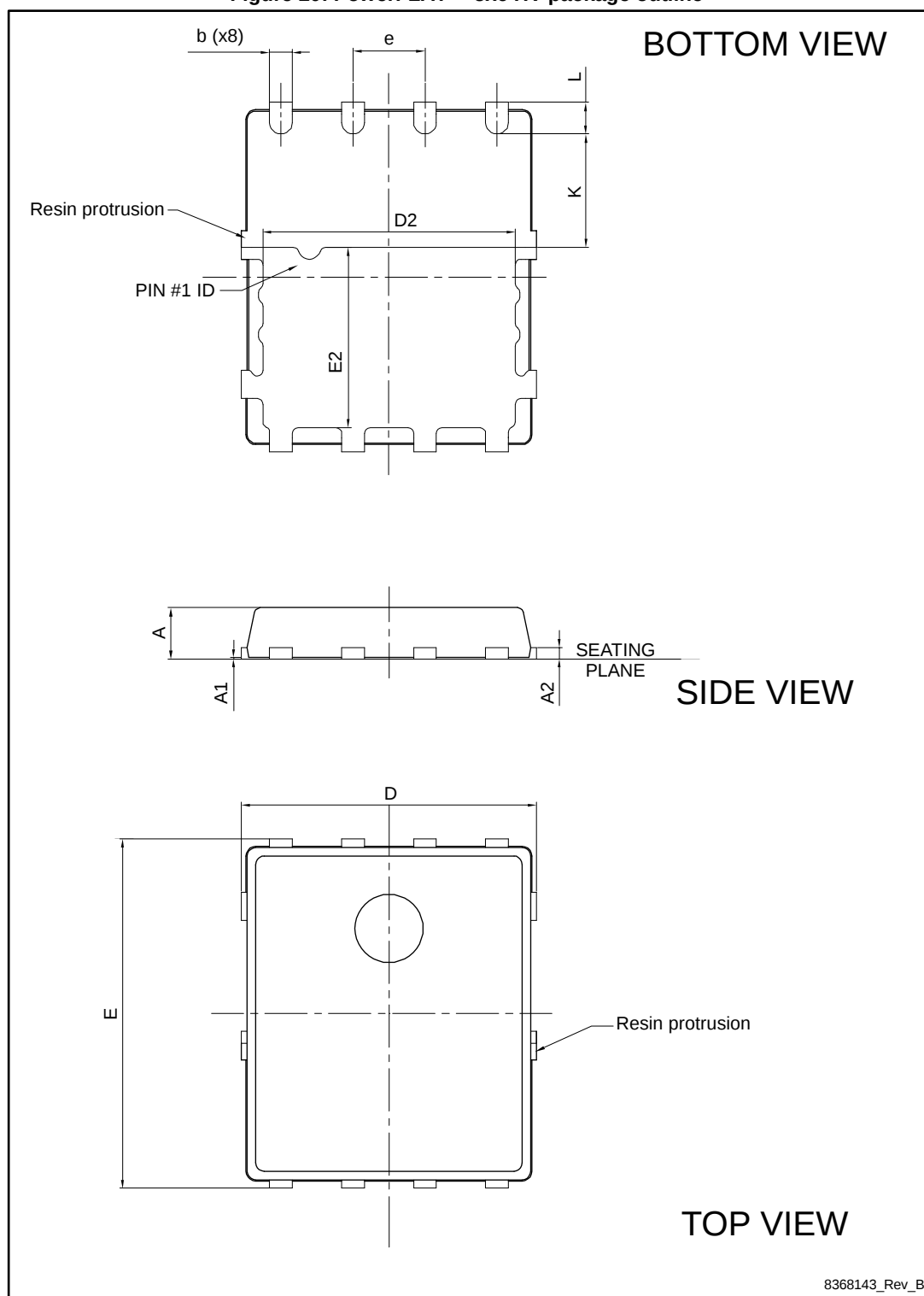
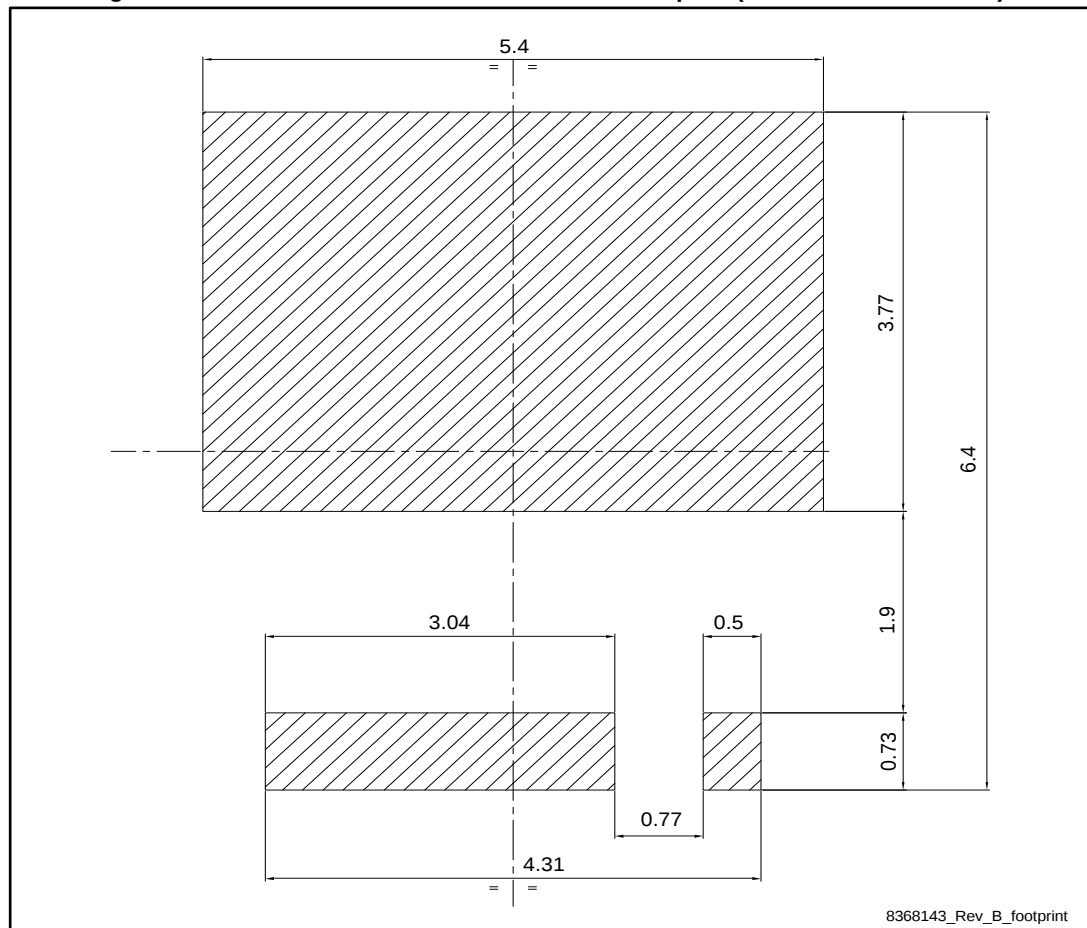


Table 9: PowerFLAT™ 5x6 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.30	4.40	4.50
E2	3.10	3.20	3.30
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

Figure 21: PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 packing information

Figure 22: PowerFLAT™ 5x6 tape (dimensions are in mm)

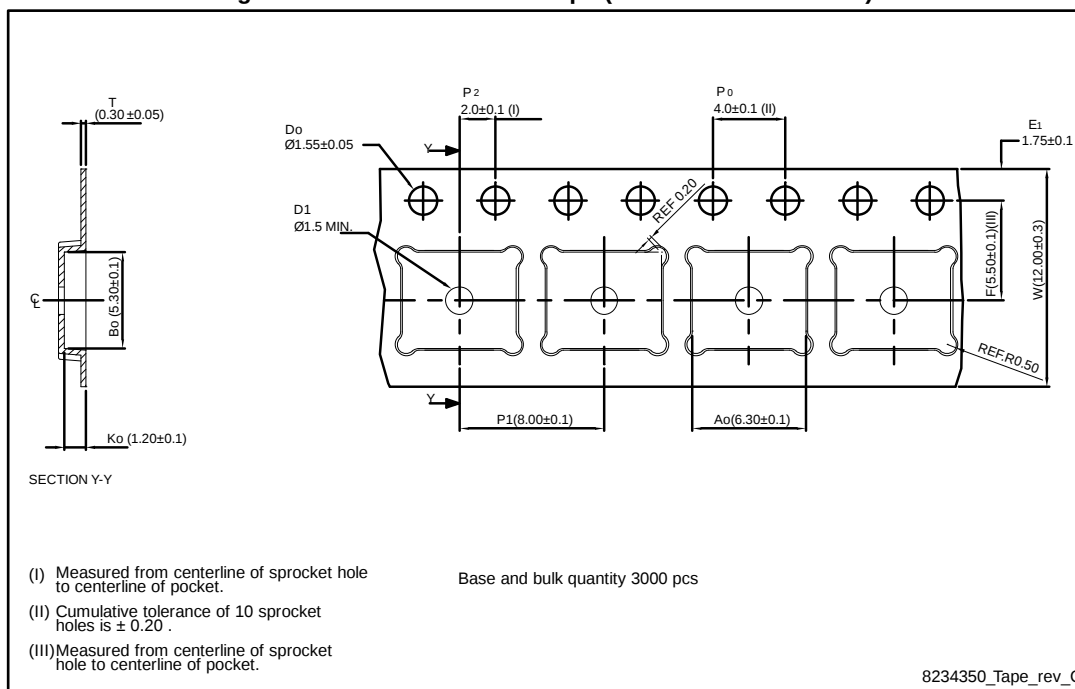
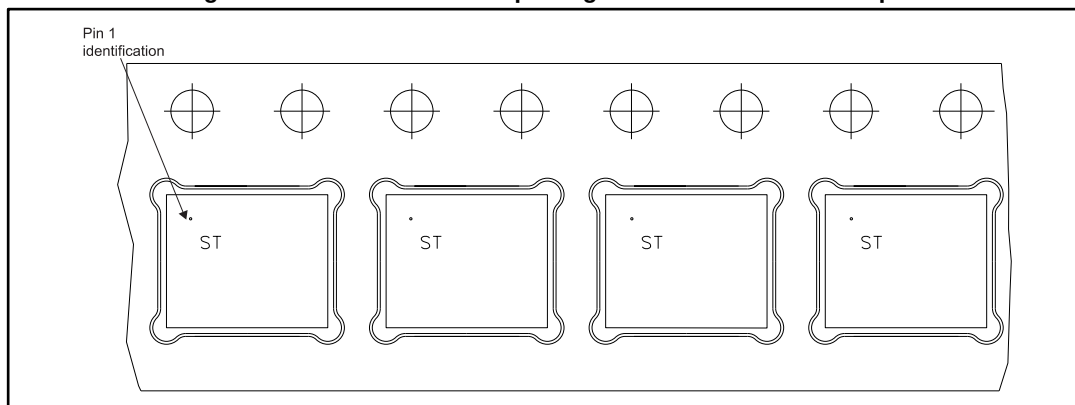


Figure 23: PowerFLAT™ 5x6 package orientation in carrier tape



Technical drawing of a 35mm film reel, showing front, side, and core detail views. Dimensions are in millimeters.

Front View (Left): Shows the reel's profile with a central hub and six spokes. Key dimensions include:

- Hub outer radius: R25.00
- Hub outer diameter: Ø25.00
- Spoke width: 2.50
- Spoke thickness: 1.90
- Spoke fillet radius: R0.60
- Spoke height: 2.50
- Spoke width at base: 1.90
- Spoke height at base: 2.50
- Spoke width at top: 1.90
- Spoke height at top: 2.50
- Spoke width at bottom: 1.90
- Spoke height at bottom: 2.50

Side View (Right): Shows the reel's side profile with dimensions:

- W3: 11.9/15.4
- W2: 18.4 (max)
- W1: 12.4 (+2/-0)
- ØN: 17.8(+2/-0)
- ESD LOGO
- Overall width: A 330 (+0/-4.0)

Core Detail (Bottom Left): Shows the core detail with dimensions:

- R1.10
- Ø21.2
- Ø13.00
- 2.20

Core Detail (Bottom Right): Shows the core detail with dimensions:

- R1.10
- Ø21.2
- Ø13.00
- 2.20

ESD LOGO: A logo indicating Electrostatic Discharge (ESD) protection.

Dimensions: All dimensions are in millimeters.

Part No.: 8234350

Reel rev: 8234350

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
22-May-2015	1	First release.

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