



3.3 VOLT TIME SLOT INTERCHANGE DIGITAL SWITCH WITH RATE MATCHING 4,096 x 4,096

IDT72V71643

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES JULY 31, 2015

FEATURES:

- Up to 32 serial input and output streams
- Maximum 4,096 x 4,096 channel non-blocking switching
- Accepts data streams at 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s
- Rate matching capability: Mux/Demux mode and Split mode
- Output Enable Indication Pins
- Per-channel Variable Delay mode for low-latency applications
- Per-channel Constant Delay mode for frame integrity applications
- Automatic identification of ST-BUS® and GCI serial streams
- Automatic frame offset delay measurement
- Per-stream frame delay offset programming
- Per-channel high-impedance output control
- Per-channel Processor mode to allow microprocessor writes to TX streams
- Direct microprocessor access to all internal memories
- Memory block programming for quick setup
- IEEE-1149.1 (JTAG) Test Port

- Internal Loopback for testing
- Available in 144-pin Thin Quad Flatpack (TQFP) and 144-pin Ball Grid Array (BGA) packages
- Operating Temperature Range -40°C to +85°C
- 3.3V I/O with 5V tolerant inputs and TTL compatible outputs

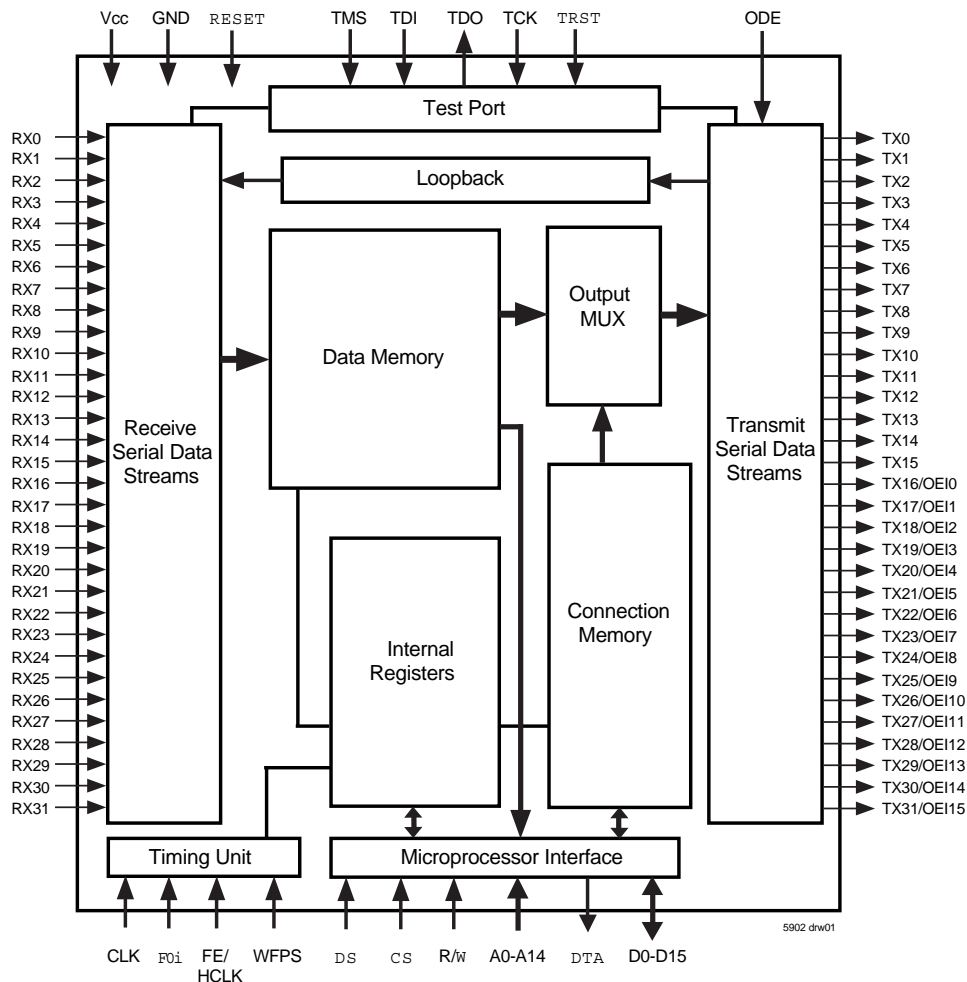
DESCRIPTION:

The IDT72V71643 has a maximum non-blocking switch capacity of 4,096 x 4,096 channels with data rates at 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s. With 32 inputs and 32 outputs, a variety of rate combinations is supported, under either Mux/Demux mode or Split mode, to allow for switching between streams of different data rates.

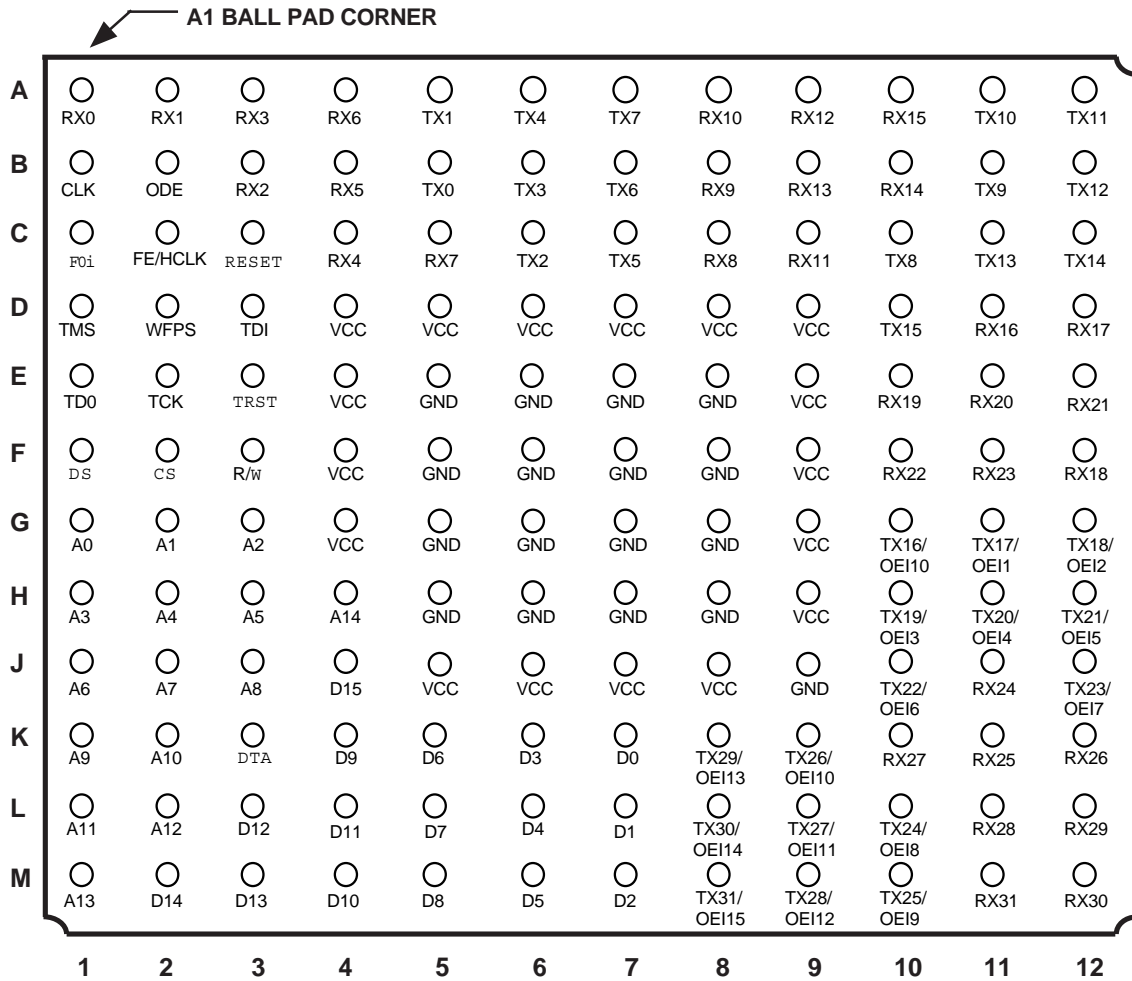
Output enable indications are provided through optional pins (one pin per output stream, only 16 output streams can be used in this mode) to facilitate external data bus control.

For applications requiring 32 streams and 32 per-stream Output Enable indicators, there is also an All Output Enable Feature.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



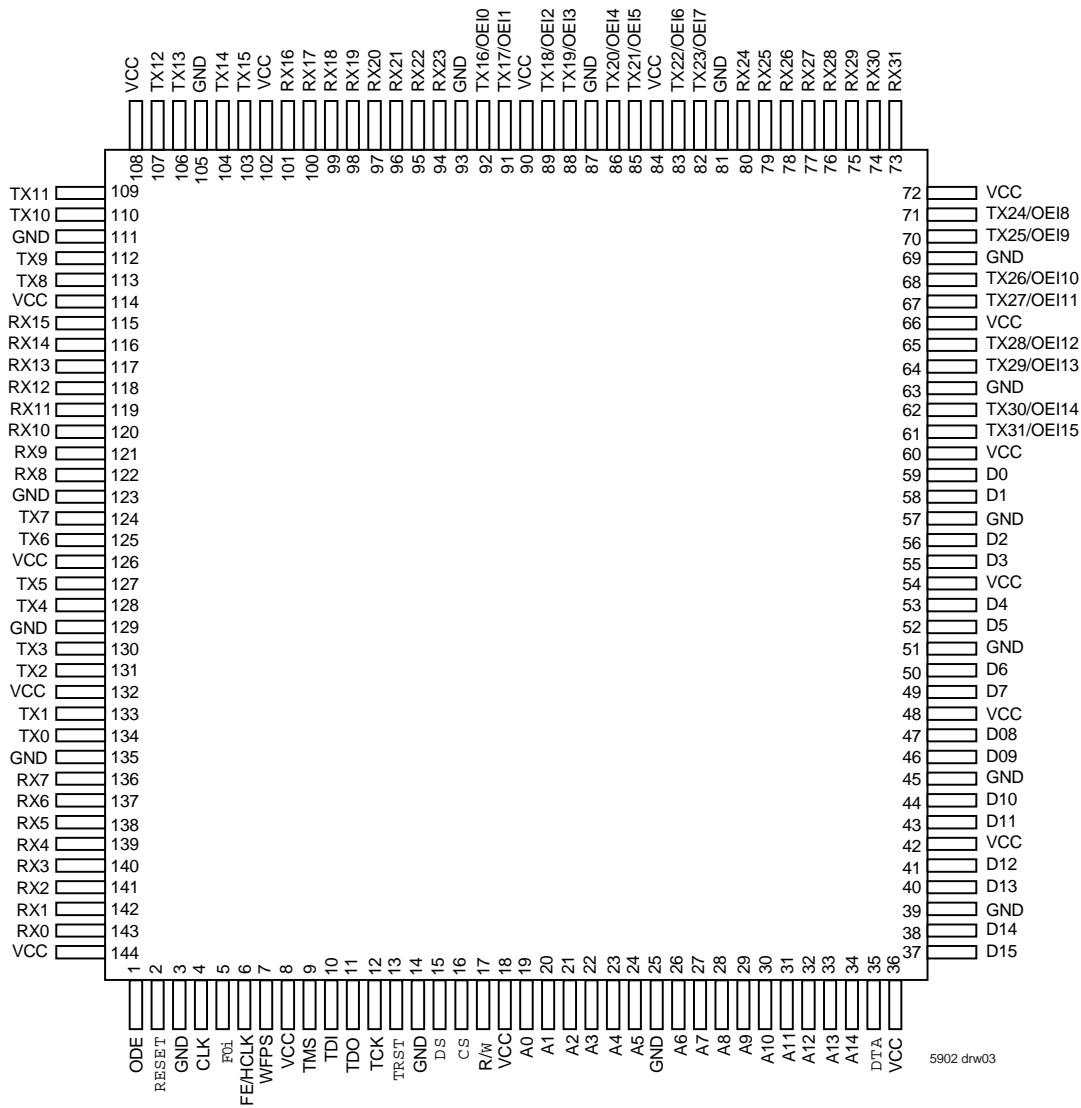
5902 drw02

BGA: 1mm pitch, 13mm x 13mm (BC144-1, order code: BC)
TOP VIEW

NOTES:

1. IC - Internal Connection, tie to Ground for normal operation.
2. All I/O pins are 5V tolerant except for TMS, TDI and TRST.

PIN CONFIGURATIONS (CONTINUED)



TQFP: 0.50mm pitch, 20mm x 20mm (DA144-1, order code: DA)
TOP VIEW

NOTES:

1. IC - Internal Connection, tie to Ground for normal operation.
2. All I/O pins are 5V tolerant except for TMS, TDI and TRST.

PIN DESCRIPTION

| SYMBOL | NAME | I/O | DESCRIPTION |
|---------------------|---|-----|--|
| GND | Ground. | | Ground Rail. |
| Vcc | Vcc | | +3.3 Volt Power Supply. |
| TX0-15 | TX Output 0 to 15 (Three-state Outputs) | O | Serial data output stream. These streams may have a data rate of 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s, or 16.384 Mb/s. |
| TX16-31/ OE10-15 | TX Output 16 to 31/ Output Enable Indication 0 to 15 (Three-state Outputs) | O | When all 32 output streams are selected via control register, these pins (TX16-31) are output streams 16 to 31 and may have a data rate of 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s or 16.384 Mb/s. When output enable indication function is selected, these pins (OE10-15) reflect the active or three-state status for the corresponding, (TX0-15) output streams. |
| RX0-31 | RX Input 0 to 31 | I | Serial data input stream. These streams may have a data rate of 2.048 Mb/s, 4.096 Mb/s, 8.192 Mb/s, or 16.384 Mb/s. |
| $\overline{F0i}$ | Frame Pulse | I | This input accepts and automatically identifies frame synchronization signals formatted according to ST-BUS [®] and GCI specifications. |
| FE/HCLK | Frame Evaluation/ HCLK Clock | I | When the WFPS pin is LOW, this pin is the frame measurement input. When the WFPS pin is HIGH, the HCLK (4.096 MHz clock) is required for frame alignment in the wide frame pulse (WFP) mode. |
| CLK | Clock | I | Serial clock for shifting data in/out on the serial streams (RX/TX 0-31). |
| TMS | Test Mode Select | I | JTAG signal that controls the state transitions of the TAP controller. This pin is pulled HIGH by an internal pull-up when not driven. |
| TDI | Test Serial Data In | I | JTAG serial test instructions and data are shifted in on this pin. This pin is pulled HIGH by an internal pull-up when not driven. |
| TDO | Test Serial Data Out | O | JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high-impedance state when JTAG scan is not enabled. |
| TCK | Test Clock | I | Provides the clock to the JTAG test logic. |
| \overline{TRST} | Test Reset | I | Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-reset state. This pin is pulled by an internal pull-up when not driven. This pin should be pulsed LOW on power-up, or held LOW, to ensure that the IDT72V71643 is in the normal functional mode. |
| \overline{RESET} | Device Reset | I | This input (active LOW) puts the IDT72V71643 in its reset state that clears the device internal counters, registers and brings TX0-31 and microport data outputs to a high-impedance state. In normal operation, the RESET pin must be held LOW for a minimum of 100ns to reset the device. |
| WFPS | Wide Frame Pulse Select | I | When 1, enables the wide frame pulse (WFP) Frame Alignment interface. When 0, the device operates in ST-BUS [®] /GCI mode. |
| \overline{DS} | Data Strobe | I | This active LOW input works in conjunction with \overline{CS} to enable the read and write operations. |
| $\overline{R/W}$ | Read/Write | I | This input controls the direction of the data bus lines during a microprocessor access. |
| \overline{CS} | Chip Select | I | Active LOW input used by a microprocessor to activate the microprocessor port of IDT72V71643. |
| A0-14 | Address Bus 0 to 14 | I | These pins allow direct access to Connection Memory, Data Memory and internal control registers. |
| D0-15 | Data Bus 0-15 | I/O | These pins are the data bits of the microprocessor port. |
| \overline{DTA} | Data Transfer Acknowledgment | O | This active LOW signal indicates that a data bus transfer is complete. When the bus cycle ends, this pin drives HIGH and then goes high-impedance, allowing for faster bus cycles with a weaker pull-up resistor. A pull-up resistor is required to hold a HIGH level when the pin is in high-impedance. |
| ODE | Output Drive Enable | I | This is the output enable control for the TX0-31 serial outputs. When ODE input is LOW and the OSB bit of the IMS register is LOW, TX0-31 are in a high-impedance state. If this input is HIGH, the TX0-31 output drivers are enabled. However, each channel may still be put into a high-impedance state by using the per channel control bit in the Connection Memory. |

DESCRIPTION (CONTINUED)

The IDT72V71643 is capable of switching up to 4,096 x 4,096 channels without blocking. Designed to switch 64 Kbit/s PCM or N x 64 Kbit/s data, the device maintains frame integrity in data applications and minimizes throughput delay for voice applications on a per channel basis.

The serial input streams (RX) and serial output streams (TX) of the IDT72V71643 can be run up to 16.384 Mb/s allowing 256 channels per 125 μ s frame. Depending on the input and output data rates the device can support up to 32 serial streams.

With two main operating modes, Processor mode and Connection Mode, the IDT72V71643 can easily switch data from incoming serial streams (Data Memory) or from the controlling microprocessor (Connection Memory). As control and status information is critical in data transmission, the Processor mode is especially useful when there are multiple devices sharing the input and output streams.

With three main configuration modes, Regular, Mux/Demux, and Split mode the IDT72V71643 is designed to work in a mixed data-rate environment. In Mux/Demux mode, all of the input streams work at one data rate and the output streams at another. Depending on the configuration, more or less serial streams will be available on the inputs or outputs to maintain a non-blocking switch. In Split Mode, half of the input streams are set at one rate, while the other half are set to another rate. In this mode, both input and output streams are symmetrical.

With data coming from multiple sources and through different paths, data entering the device is often delayed. To handle this problem, the IDT72V71643 has a frame evaluation feature to allow individual streams to be offset from the frame pulse in half clock-cycle intervals up to +4.5 clock cycles for speeds up to 8 Mb/s or +2.5 clock cycles for 16 Mb/s. (See Table 8 for maximum allowable skew).

The IDT72V71643 also provides a JTAG test access port, an internal loopback feature, memory block programming, a simple microprocessor interface and automatic ST-BUS[®]/GCI sensing to shorten setup time, aid in debugging and ease use of the device without sacrificing capabilities.

FUNCTIONAL DESCRIPTION

DATA AND CONNECTION MEMORY

All data that comes in through the RX inputs go through a serial-to-parallel conversion before being stored into internal Data Memory. The 8 KHz frame pulse (F0i) is used to mark the 125 μ s frame boundaries and to sequentially address the input channels in Data Memory. The Data Memory is only written by the device from the RX streams and can be read from either the TX streams or the microprocessor.

Data output on the TX streams may come from either the Serial Input Streams (Data Memory) or from the microprocessor (Connection Memory). In the case that RX input data is to be output, the addresses in Connection Memory are used to specify a stream and channel of the input. The Connection Memory is setup in such a way that each location corresponds to an output channel for each particular stream. In that way, more than one channel can output the same data. In Processor mode, the microprocessor writes data to the Connection Memory locations corresponding to the stream and channel that is to be output. The lower byte (8 least significant bits) of the Connection Memory is output every frame until the microprocessor changes the data or mode of the channel. By using this Processor mode capability, the microprocessor can access input and output time-slots on a per channel basis.

The most significant bits of the Connection Memory are used to control per channel functions such as Processor mode, Constant or Variable Delay mode, three-state of output drivers, and the Loopback function.

OPERATING MODES

In addition to Regular mode where input and output streams are operating at the same rate, the IDT72V71643 incorporates a rate matching function in two different modes: Split mode and Mux/Demux mode. In Split mode some of the input streams are set at one rate, while others are set to another rate. Both input and output streams are symmetrical. In Mux/Demux mode, all input streams are operating at the same rate, while output streams are operating at a different rate. All configurations are non-blocking. These two modes can be entered by setting the DR3-0 bits in the Control Register, see Table 5.

OUTPUT IMPEDANCE CONTROL

In order to put all streams in three-state, all per-channel three-state control bits in the Connection Memory are set (MOD0 and MOD1 = 1) or both the ODE pin and the OSB bit of the Control Register must be zero. If any combination other than 0-0, for the ODE pin and the OSB bit, is used, the three-state control of the streams will be left to the state of the MOD1 and MOD0 bits of the Connection Memory. The IDT72V71643 incorporates a memory block programming feature to facilitate three-state control after reset. See Table 1 for Output High-Impedance Control.

SERIAL DATA INTERFACE TIMING

When a 16Mb/s serial data rate is required, the master clock frequency will be running at 16.384MHz resulting in a single-bit per clock. For all other cases, 2Mb/s, 4Mb/s, and 8Mb/s, the master clock frequency will be twice the fastest data rate on the serial streams. Use Table 5 to determine clock speed and DR3-0 bits in the Control Register to setup the device. The IDT72V71643 provides two different interface timing modes, ST-BUS[®] or GCI. The IDT72V71643 automatically detects the presence of an input frame pulse and identifies it as either ST-BUS[®] or GCI.

In ST-BUS[®], when running at 16.384MHz, data is clocked out on the falling edge and is clocked in on the subsequent rising-edge. At all other data rates, there are two clock cycles per bit and every second falling edge of the master clock marks a bit boundary and the data is clocked in on the rising edge of CLK, three quarters of the way into the bit cell. See Figure 17 for timing.

In GCI format, when running at 16.384MHz, data is clocked out on the rising edge and is clocked in on the subsequent falling edge. At all other data rates, there are two clock cycles per bit and every second rising edge of the master clock marks the bit boundary and data is clocked in on the falling edge of CLK at three quarters of the way into the bit cell. See Figure 18 for timing.

INPUT FRAME OFFSET SELECTION

Input frame offset selection allows the channel alignment of individual input streams to be offset with respect to the output stream channel alignment (i.e. F0i). Although input data is synchronous, delays can be caused by variable path serial backplanes and variable path lengths, which may be implemented in large centralized and distributed switching systems. Because data is often delayed this feature is useful in compensating for the skew between clocks.

Each input stream can have its own delay offset value by programming the frame input offset registers (FOR, Table 7). The frame offset shown is a function of the data rate, and can be as large as +4.5 master clock (CLK) periods forward with a resolution of 1/2 clock period. To determine the maximum offset allowed see Table 8.

SERIAL INPUT FRAME ALIGNMENT EVALUATION

The IDT72V71643 provides the frame evaluation (FE) input to determine different data input delays with respect to the frame pulse F0i. Setting the start frame evaluation (SFE) bit low for at least one frame starts a measurement cycle.

When the SFE bit in the Control Register is changed from low to high, the evaluation starts. Two frames later, the complete frame evaluation (CFE) bit of the frame alignment register (FAR) changes from low to high to signal that a valid offset measurement is ready to be read from bits 0 to 11 of the FAR register. The SFE bit must be set to zero before a new measurement cycle is started.

In ST-BUS® mode, the falling edge of the frame measurement signal (FE) is evaluated against the falling edge of the ST-BUS® frame pulse. In GCI mode, the rising edge of FE is evaluated against the rising edge of the GCI frame pulse. See Table 6 and Figure 6 for the description of the frame alignment register.

MEMORY BLOCK PROGRAMMING

The IDT72V71643 provides users with the capability of initializing the entire Connection Memory block in two frames. To set bits 15 to 13 of every Connection Memory location, first program the desired pattern in bits 9 to 7 of the Control Register.

Setting the memory block program (MBP) bit of the control register high enables the block programming mode. When the block programming enable (BPE) bit of the Control Register is set to high, the block programming data will be loaded into the bits 15 to 13 of every Connection Memory location. The other Connection Memory bits (bit 12 to bit 0) are loaded with zeros. When the memory block programming is complete, the device resets the BPE bit to zero.

LOOPBACK CONTROL

The loopback control (LPBK) bit of each Connection Memory location allows the TX output data to be looped back internally to the RX input for diagnostic purposes.

If the LPBK bit is high, the associated TX output channel data is internally looped back to the RX input channel (i.e., data from TX_n channel *m* routes to the RX_n channel *m* internally); if the LPBK bit is low, the loopback feature is disabled. For proper per-channel loopback operation, the contents of frame delay offset registers must be set to zero and the device must be in regular switch mode (DR3-0 = 0x0, 0x1 or 0x2).

DELAY THROUGH THE IDT72V71643

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform time-slot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications, Variable throughput delay is best as it ensures minimum delay between input and output data. In wideband data applications, Constant throughput delay is best as the frame integrity of the information is maintained through the switch.

The delay through the device varies according to the type of throughput delay selected in the MOD1 and MOD0 bits of the Connection Memory.

VARIABLE DELAY MODE (MOD1-0 = 0x0)

In this mode, the delay is dependent only on the combination of source and destination serial stream speed. Although the minimum delay achievable is dependent on the input and output serial stream speed, if data is switched out +3 channels of the slowest data rate, the data will be switched out in the same frame except if the input and output data rates are both 16 Mb/s (DR3-0 = 0x3). (See Figure 2 for example).

For example, given the input data rate is 2 Mb/s and the output data rate is 8 Mb/s, input channel CH0 can be switch out by output channel CH12. In the above example the input streams are slower than the output streams. Also, for every 2 Mb/s time slot there are four 8 Mb/s time slots, thus a three 2 Mb/s channel

delay equates to 12 output channel time slots. See Figure 2 for this example and other examples of minimum delay to guarantee transmission in the same frame.

CONSTANT DELAY MODE (MOD1-0 = 0x1)

In this mode, frame integrity is maintained in all switching configurations by making use of a multiple Data Memory buffer. Input channel data is written into the Data Memory buffers during frame *n* will be read out during frame *n*+2. Figure 1 shows examples of Constant Delay mode.

MICROPROCESSOR INTERFACE

The IDT72V71643's microprocessor interface looks like a standard RAM interface to improve integration into a system. With a 15-bit address bus and a 16-bit data bus, read and writes are mapped directly into Data and Connection memories and require only one Master Clock cycle to access. By allowing the internal memories to be randomly accessed in one cycle, the controlling microprocessor has more time to manage other peripheral devices and can more easily and quickly gather information and setup the switch paths.

Table 2 shows the mapping of the addresses into internal memory blocks, Table 3 shows the Control Register information and Figure 13 and Figure 14 shows asynchronous and synchronous microprocessor accesses.

MEMORY MAPPING

The address bus on the microprocessor interface selects the internal registers and memories of the IDT72V71643. The two most significant bits of the address select between the registers, Data Memory, and Connection Memory. If A14 and A13 are HIGH, A12-A0 are used to address the Data Memory (Read Only). If A14 is HIGH and A13 is LOW, A12-A0 are used to address Connection Memory (Read/Write). If A14 is LOW and A13 is HIGH A12-A9 are used to select the Control Register, Frame Alignment Register, and Frame Offset Registers. See Table 2 for mappings.

CONTROL REGISTER

As explained in the Serial Data Interface Timing and Switching Configurations sections, after system power-up, the Control Register should be programmed immediately to establish the desired switching configuration.

The data in the Control Register consists of the Memory Block Programming bit (MBP), the Block Programming Data (BPD) bits, the Begin Block Programming Enable (BPE), the Output Stand By (OSB), Start Frame Evaluation (SFE), and Data Rate Select bits (DR 3-0). As explained in the Memory Block Programming section, the BPE begins the programming if the MBP bit is enabled. This allows the entire Connection Memory block to be programmed with the Block Programming Data bits.

CONNECTION MEMORY CONTROL

If the ODE pin or the OSB bit is high, the MOD1-0 bits of each Connection Memory location controls the output drivers. See Table 1 for detail. The Processor Channel (PC) mode is entered by a 1-0 of the MOD1-0 of the Connection Memory. In Processor Channel Mode, this allows the microprocessor to access TX output channels. Once the MOD1-0 bits are set, the lower 8 bits of the Connection Memory will be output on the TX serial streams. Also controlled in the Connection Memory is the Variable Delay mode or Constant Delay mode. Each Connection Memory location allows the per-channel selection between Variable and Constant throughput Delay modes and Processor mode.

If the LPBK bit is high, the associated TX output channel data is internally looped back to the RX input channel (i.e., RXn channel m data comes from the TXn channel m). If the LPBK bit is low, the loopback feature is disabled. For proper per-channel loopback operation, the contents of the frame delay offset registers must be set to zero and the device must be in regular switch mode (DR3-0 = 0x0, 0x1 or 0x2).

OUTPUT ENABLE INDICATION

The IDT72V71643 has the capability to indicate the state of the outputs (active or three-state) by enabling the Output Enable Indication (OEI) in the control register. In the OEI mode however, only half of the output streams are available. If this same capability is desired with all 32 streams, this can be accomplished by using two IDT72V71643 devices. In one device, the All Output Enable (AOE) bit is set to a one while in the other the AOE is set to zero. In this way, one device

acts as the switch and the other as a three-state control device. See Figure 8. It is important to note if the TSI device is programmed for AOE and the OEI is also set, the device will be in the AOE mode not OEI.

INITIALIZATION OF THE IDT72V71643

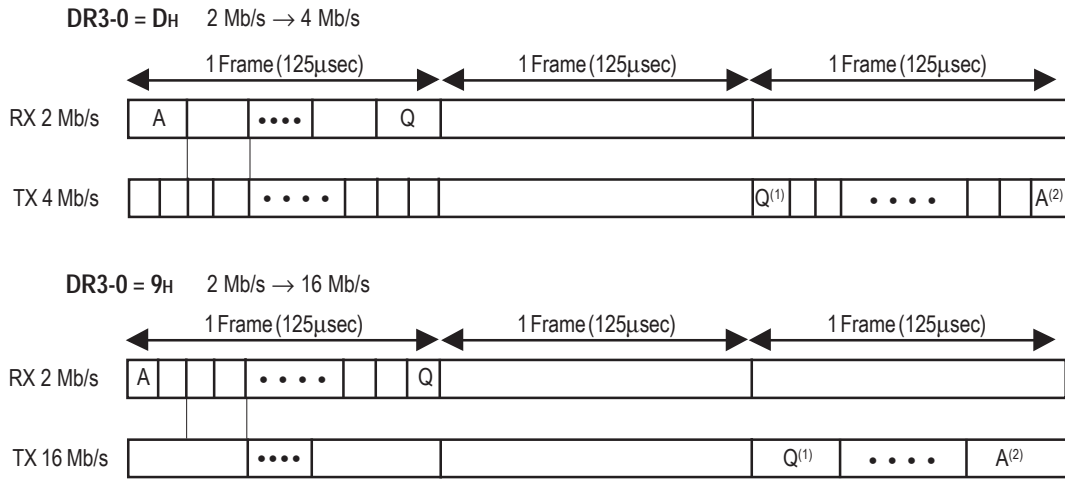
After power up, the IDT72V71643 should be reset. During reset, the internal registers are put into their default state and all TX outputs are put into three-state. After reset however, the state of Connection Memory is unknown. As such, the outputs should be put in high-impedance by holding the ODE low. While the ODE is low, the microprocessor can initialize the device, program the active paths, and disable unused outputs by programming the OE bit in Connection Memory. Once the device is configured, the ODE pin (or OSB bit depending on initialization) can be switched.

TABLE 1 — OUTPUT HIGH-IMPEDANCE CONTROL

| MOD1-0 BITS IN CONNECTION MEMORY | ODE PIN | OSB BIT IN CONTROL REGISTER | OUTPUT DRIVER STATUS |
|----------------------------------|------------|-----------------------------|----------------------------|
| 1 and 1 | Don't Care | Don't Care | Per Channel High-Impedance |
| Any, other than 1 and 1 | 0 | 0 | High-Impedance |
| Any, other than 1 and 1 | 0 | 1 | Enable |
| Any, other than 1 and 1 | 1 | 0 | Enable |
| Any, other than 1 and 1 | 1 | 1 | Enable |

TABLE 2 — INTERNAL REGISTER AND ADDRESS MEMORY MAPPING

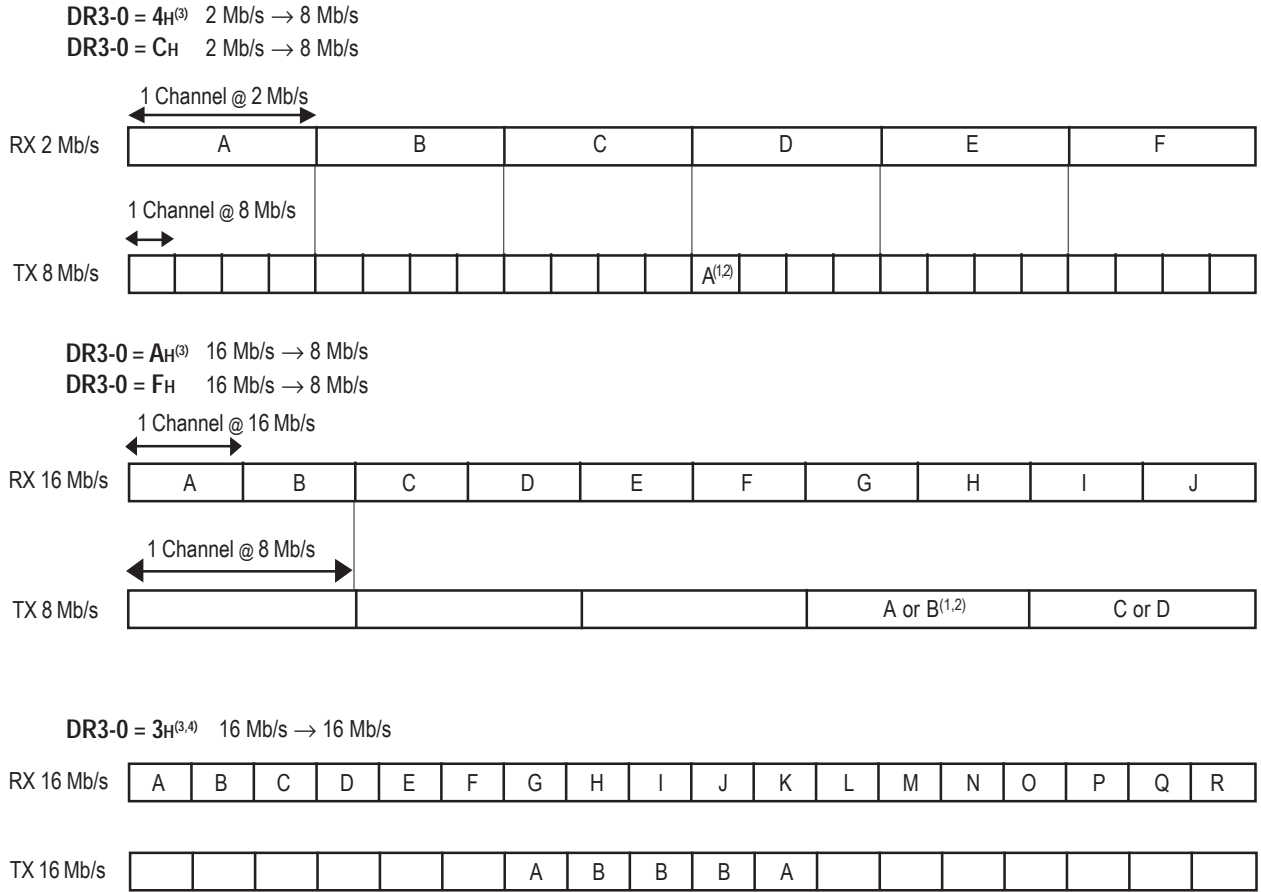
| A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W | Location |
|-----|-----|------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|----------------------|
| 1 | 1 | STA4 | STA3 | STA2 | STA1 | STA0 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 | R | Data Memory |
| 1 | 0 | STA4 | STA3 | STA2 | STA1 | STA0 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 | R/W | Connection Memory |
| 0 | 1 | 0 | 0 | 0 | 0 | x | x | x | x | x | x | x | x | x | R/W | Control Register |
| 0 | 1 | 0 | 0 | 0 | 1 | x | x | x | x | x | x | x | x | x | R | Frame Align Register |
| 0 | 1 | 0 | 0 | 1 | 0 | x | x | x | x | x | x | x | x | x | R/W | FOR0 |
| 0 | 1 | 0 | 0 | 1 | 1 | x | x | x | x | x | x | x | x | x | R/W | FOR1 |
| 0 | 1 | 0 | 1 | 0 | 0 | x | x | x | x | x | x | x | x | x | R/W | FOR2 |
| 0 | 1 | 0 | 1 | 0 | 1 | x | x | x | x | x | x | x | x | x | R/W | FOR3 |
| 0 | 1 | 0 | 1 | 1 | 0 | x | x | x | x | x | x | x | x | x | R/W | FOR4 |
| 0 | 1 | 0 | 1 | 1 | 1 | x | x | x | x | x | x | x | x | x | R/W | FOR5 |
| 0 | 1 | 1 | 0 | 0 | 0 | x | x | x | x | x | x | x | x | x | R/W | FOR6 |
| 0 | 1 | 1 | 0 | 0 | 1 | x | x | x | x | x | x | x | x | x | R/W | FOR7 |



NOTES:

1. Timeslot Q — 2 Frames — minimum delay.
2. Timeslot A — 3 Frames - 1 output channel period — maximum delay.

Figure 1. Constant Delay Mode Examples



NOTES:

1. If data is switched at least +3 channel periods of the slower data rate, the data will transmit out in the same frame except if the input and output data rates are both 16 Mb/s (DR3-0 = 0x3).
2. Delay is a function of input channel and output channel combinations, and input and output stream data rate.
3. See switching mode table for input and output speed combinations.
4. When the input and output data rates are both 16 Mb/s, the minimum delay achievable is 6 time slots.

Figure 2. Variable Delay Mode Examples

TABLE 3 — CONTROL REGISTER (CR) BITS

| Reset Value: 4000h. | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------------|---|--|-----|-----|-----|-----|----|------|------|------|-----|-----|-----|-----|-----|-----|-----|
| | | SRS | OEI | OEP | AOE | MBP | 0 | BPD2 | BPD1 | BPD0 | BPE | OSB | SFE | DR3 | DR2 | DR1 | DR0 |
| Bit | Name | Description | | | | | | | | | | | | | | | |
| 15 | Reset (Software Reset) | A one will reset the device and have the same effect as of the RESET pin. Must be zero for normal operation. | | | | | | | | | | | | | | | |
| 14 | OEI (Output Enable Indication) | When 1, TX16-31/OEI0-15 will behave as OEI0-15. These outputs will reflect the active or high-impedance state of the corresponding output data streams TX0-15. When 0, TX16-31/OEI0-15 will behave as TX16-31 and react in the same way as TX0-15. | | | | | | | | | | | | | | | |
| 13 | OEPOL (Output Enable Polarity) | When 1, a one on OEI pin denotes an active state on the output data stream; zero on OEI pin denotes high-impedance state. When 0, a one denotes high-impedance and a zero denotes an active state. | | | | | | | | | | | | | | | |
| 12 | AOE | When 1, TX0-31 will behave as OEI0-31 accordingly. These outputs will reflect the active or high-impedance state of the corresponding output data streams (TX0-31) in another IDT72V71643 if programmed identically. | | | | | | | | | | | | | | | |
| 11 | MBP (Memory Block Program) | When 1, the Connection Memory block programming feature is ready for the programming of Connection Memory high bits, bit 13 to bit 15. When 0, this feature is disabled. | | | | | | | | | | | | | | | |
| 10 | Unused | Must be zero for normal operation. | | | | | | | | | | | | | | | |
| 9-7 | BPD2-0 (Block Programming Data) | These bits carry the value to be loaded into the Connection Memory block whenever the memory block programming feature is activated. After the MBP bit in the control register is set to 1 and the BPE bit is set to 1, the contents of the bits BPD2-0 are loaded into bit 15 and 13 of the Connection Memory. Bit 12 to bit 0 of the Connection Memory are set to 0. | | | | | | | | | | | | | | | |
| 6 | BPE (Begin Block Programming Enable) | A zero to one transition of this bit enables the memory block programming function. The BPE and BPD2-0 bits in the CR register have to be defined in the same write operation. Once the BPE bit is set HIGH, the device requires two frames to complete the block programming. After the programming function has finished, the BPE bit returns to zero to indicate the operation is completed. When the BPE=1, the other bit in the control register must not be changed for two frames to ensure proper operation. | | | | | | | | | | | | | | | |
| 5 | OSB (Output Stand By) | When ODE=0 and OSB=0, the output drivers of transmit serial streams are in high-impedance mode. When ODE=1 or OSB=1, the output serial stream drivers function normally. | | | | | | | | | | | | | | | |
| 4 | SFE (Start Frame Evaluation) | A zero to one transition in this bit starts the frame evaluation procedure. When the CFE bit in the FAR register changes from zero to one, the evaluation procedure stops. To start another frame evaluation cycle, set this bit to zero for at least one frame. | | | | | | | | | | | | | | | |
| 3-0 | DR3-0 | Input/Output data rate selection. See Table 5 for detailed programming. | | | | | | | | | | | | | | | |

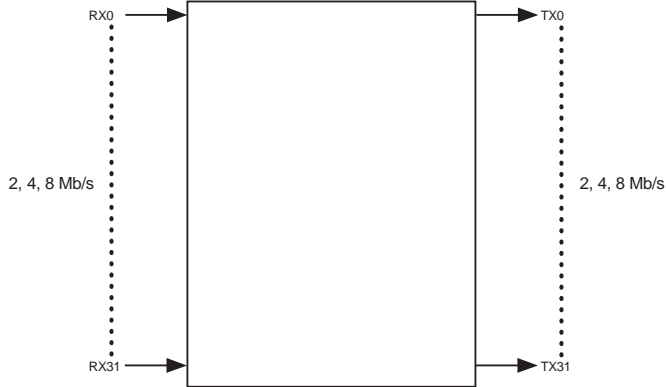
TABLE 4 — CONNECTION MEMORY BITS

| | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|-------------|-------------|------|------|------|---------------------|------|------|---------------------|------|------|----------------|------|------|-----------------------|
| | | LPBK | MOD1 | MOD0 | SAB4 | SAB3 | SAB2 | SAB1 | SAB0 | CAB7 | CAB6 | CAB5 | CAB4 | CAB3 | CAB2 | CAB1 | CAB0 |
| Bit | Name | Description | | | | | | | | | | | | | | | |
| 15 | LPBK (Per Channel Loopback) | When 1, the RX n channel m data comes from the TX n channel m. For proper per channel loopback operations, set the delay offset register bits OFn[2:0] to zero for the streams which are in the loopback mode. This feature is offered only when DR3-0 = 0000, 0001 or 0010 is selected via the control register. | | | | | | | | | | | | | | | |
| 14,13 | MOD1-0 (Switching Mode Selection) | <table border="1"> <tr> <td><u>MOD1</u></td> <td><u>MOD0</u></td> <td>MODE</td> </tr> <tr> <td>0</td> <td>0</td> <td>Variable Delay mode</td> </tr> <tr> <td>0</td> <td>1</td> <td>Constant Delay mode</td> </tr> <tr> <td>1</td> <td>0</td> <td>Processor mode</td> </tr> <tr> <td>1</td> <td>1</td> <td>Output High-Impedance</td> </tr> </table> | <u>MOD1</u> | <u>MOD0</u> | MODE | 0 | 0 | Variable Delay mode | 0 | 1 | Constant Delay mode | 1 | 0 | Processor mode | 1 | 1 | Output High-Impedance |
| <u>MOD1</u> | <u>MOD0</u> | MODE | | | | | | | | | | | | | | | |
| 0 | 0 | Variable Delay mode | | | | | | | | | | | | | | | |
| 0 | 1 | Constant Delay mode | | | | | | | | | | | | | | | |
| 1 | 0 | Processor mode | | | | | | | | | | | | | | | |
| 1 | 1 | Output High-Impedance | | | | | | | | | | | | | | | |
| 12-8 | SAB4-0 (Source Stream Address Bits) | The binary value is the number of the data stream for the source of the connection. Unused SAB bits must be zero for proper operation. | | | | | | | | | | | | | | | |
| 7-0 | CAB7-0 (Source Channel Address Bits) | The binary value is the number of the channel for the source of the connection. Unused CAB bits must be zero for proper operation. | | | | | | | | | | | | | | | |

TABLE 5 — SWITCH MODES

| Switching Mode | Control Bits | | | | Data Rate bits/s | | Clock Rate MHz |
|----------------|--------------|-----|-----|-----|------------------|------------------|----------------|
| | DR3 | DR2 | DR1 | DR0 | Receive Streams | Transmit Streams | |
| Regular | 0 | 0 | 0 | 0 | 2 M on RX0-31 | 2 M on TX0-31 | 4 |
| | 0 | 0 | 0 | 1 | 4 M on RX0-31 | 4 M on TX0-31 | 8 |
| | 0 | 0 | 1 | 0 | 8 M on RX0-31 | 8 M on TX0-31 | 16 |
| | 0 | 0 | 1 | 1 | 16 M on RX0-15 | 16 M on TX0-15 | 16 |
| Mux/Demux | 0 | 1 | 0 | 0 | 2 M on RX0-31 | 8 M on TX0-7 | 16 |
| | 0 | 1 | 0 | 1 | 8 M on RX0-7 | 2 M on TX0-31 | 16 |
| | 0 | 1 | 1 | 0 | 4 M on RX0-31 | 8 M on TX0-15 | 16 |
| | 0 | 1 | 1 | 1 | 8 M on RX0-15 | 4 M on TX0-31 | 16 |
| | 1 | 0 | 0 | 0 | 16 M on RX0-3 | 2 M on TX0-31 | 16 |
| | 1 | 0 | 0 | 1 | 2 M on RX0-31 | 16 M on TX0-3 | 16 |
| | 1 | 0 | 1 | 0 | 16 M on RX0-15 | 8 M on TX0-31 | 16 |
| | 1 | 0 | 1 | 1 | 8 M on RX0-31 | 16 M on TX0-15 | 16 |
| Split | 1 | 1 | 0 | 0 | 2 M on RX0-15; | 2 M on TX0-15; | 16 |
| | | | | | 8 M on RX16-31 | 8 M on TX16-31 | |
| | 1 | 1 | 0 | 1 | 2 M on RX0-15; | 2 M on TX0-15; | 8 |
| | | | | | 4 M on RX16-31 | 4 M on TX16-31 | |
| | 1 | 1 | 1 | 0 | 4 M on RX0-15; | 4 M on TX0-15; | 16 |
| | | | | | 8 M on RX16-31 | 8 M on TX16-31 | |
| | 1 | 1 | 1 | 1 | 8 M on RX0-15; | 8 M on TX0-15; | 16 |
| | | | | | 16 M on RX16-23 | 16 M on TX16-23 | |

DR3-0 = 0H, 1H, 2H 2 Mb/s → 2 Mb/s, 4 Mb/s → 4 Mb/s, 8 Mb/s → 8 Mb/s



DR3-0 = 3H 16 Mb/s → 16 Mb/s

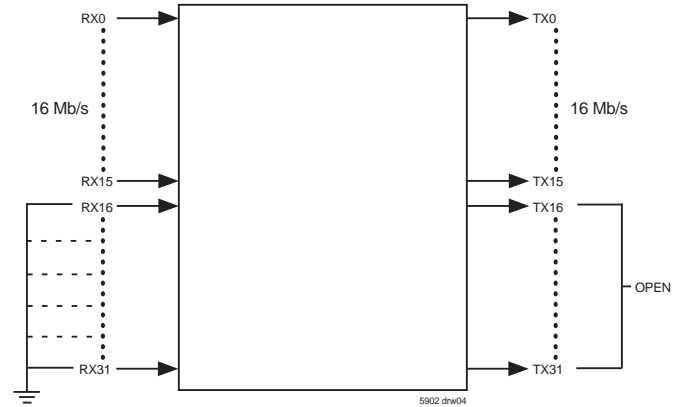
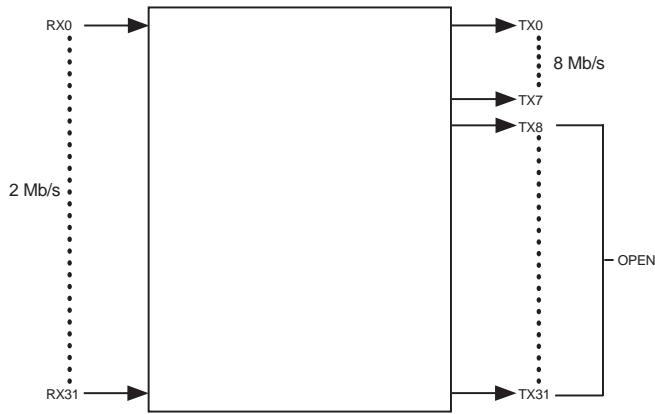


Figure 3. Regular Switch Mode

DR3-0 = 4H 2 Mb/s → 8 Mb/s



DR3-0 = 8H 16 Mb/s → 2 Mb/s

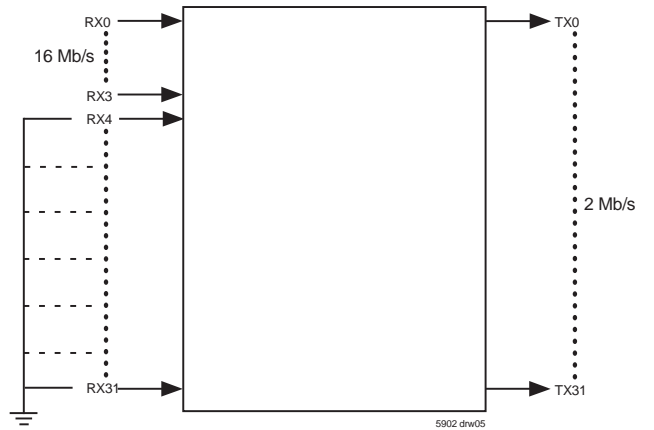
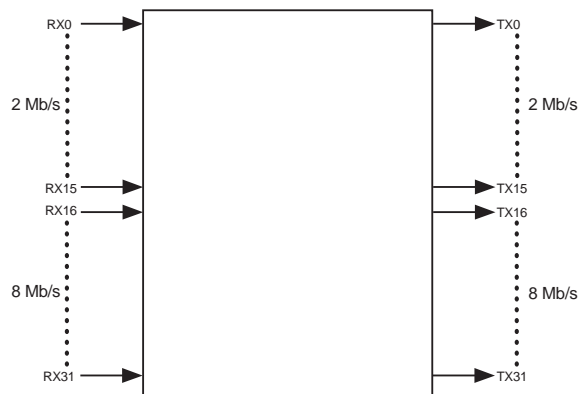


Figure 4. Mux/Demux Mode

DR3-0 = CH 2 Mb/s → 8 Mb/s & 8 Mb/s → 8 Mb/s



DR3-0 = FH 8 Mb/s → 8 Mb/s & 16 Mb/s → 16 Mb/s

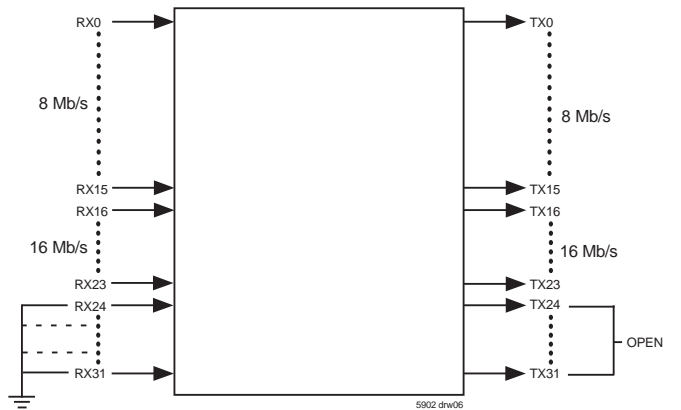
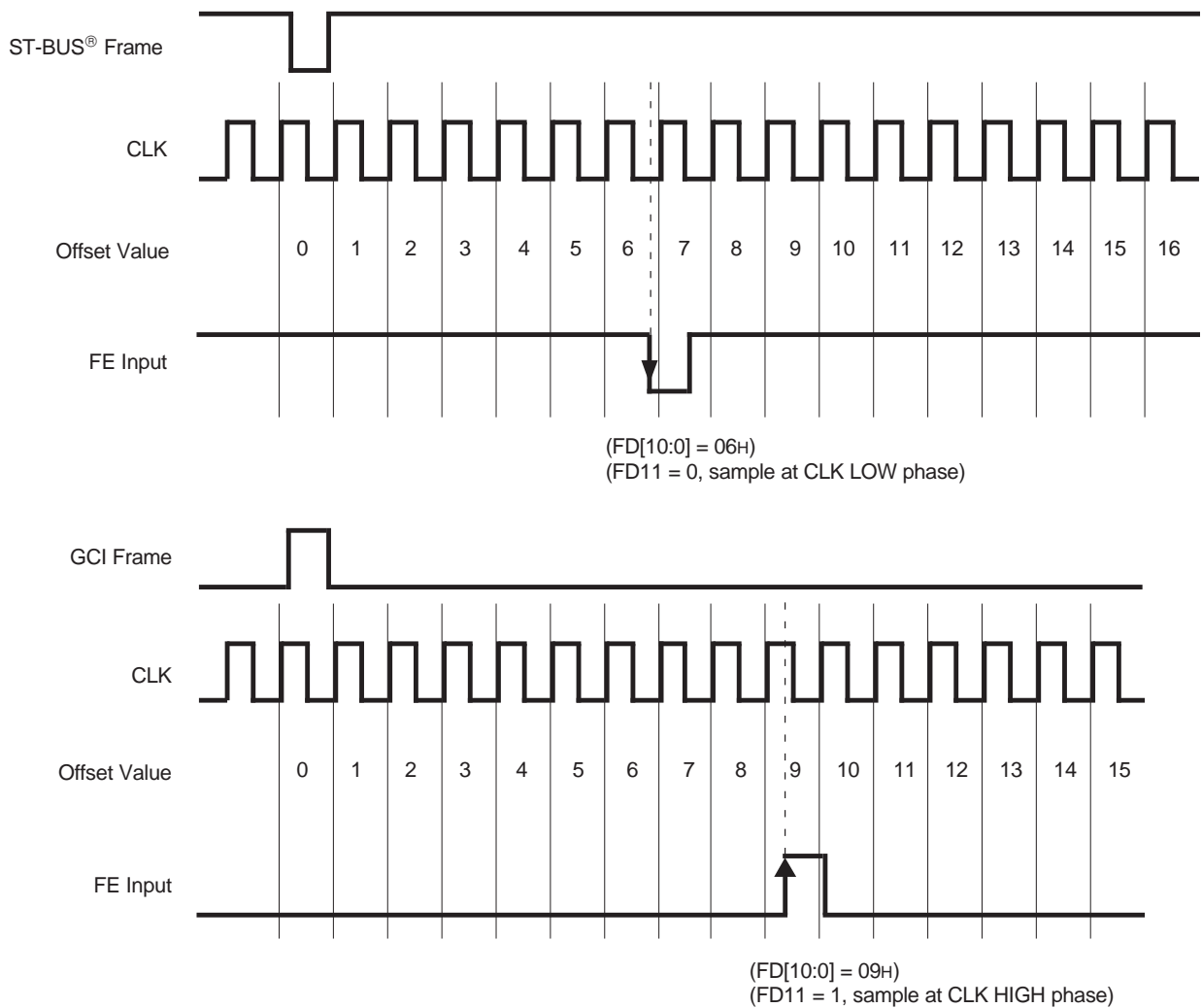


Figure 5. Split Mode

TABLE 6 — FRAME ALIGNMENT REGISTER (FAR) BITS

| Reset Value: | | 0000h. | | | | | | | | | | | | | |
|--------------|---------------------------------|---|-----|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | CFE | FD11 | FD10 | FD9 | FD8 | FD7 | FD6 | FD5 | FD4 | FD3 | FD2 | FD1 | FD0 |
| Bit | Name | Description | | | | | | | | | | | | | |
| 15-13 | Unused | Will be zero when read. | | | | | | | | | | | | | |
| 12 | CFE (Complete Frame Evaluation) | When CFE = 1, the frame evaluation is completed and bits FD10 to FD0 bits contains a valid frame alignment offset. This bit is reset to zero, when SFE bit in the CR register is changed from 1 to 0. | | | | | | | | | | | | | |
| 11 | FD11 (Frame Delay Bit 11) | The falling edge of FE (or rising edge for GCI mode) is sampled during the CLK-high phase (FD11 = 1) or during the CLK-low phase (FD11 = 0). This bit allows the measurement resolution to 1/2 CLK cycle. | | | | | | | | | | | | | |
| 10-0 | FD10-0 (Frame Delay Bits) | The binary value expressed in these bits refers to the measured input offset value. These bits are reset to zero when the SFE bit of the CR register changes from 1 to 0. (FD10 – MSB, FD0 – LSB) | | | | | | | | | | | | | |



5902 dnv07

Figure 6. Example for Frame Alignment Measurement

TABLE 7 — FRAME INPUT OFFSET REGISTER (FOR) BITS

Reset Value: 0000H for all FOR registers.

| | | | | | | | | | | | | | | | |
|----------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OF32 | OF31 | OF30 | DLE3 | OF22 | OF21 | OF20 | DLE2 | OF12 | OF11 | OF10 | DLE1 | OF02 | OF01 | OF00 | DLE0 |
| FOR0 Register | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OF72 | OF71 | OF70 | DLE7 | OF62 | OF61 | OF60 | DLE6 | OF52 | OF51 | OF50 | DLE5 | OF42 | OF41 | OF40 | DLE4 |
| FOR1 Register | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OF112 | OF111 | OF110 | DLE11 | OF102 | OF101 | OF100 | DLE10 | OF92 | OF91 | OF90 | DLE9 | OF82 | OF81 | OF80 | DLE8 |
| FOR2 Register | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OF312 | OF311 | OF310 | DLE31 | OF142 | OF141 | OF140 | DLE14 | OF132 | OF131 | OF130 | DLE13 | OF122 | OF121 | OF120 | DLE12 |
| FOR3 Register | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OF192 | OF191 | OF190 | DLE19 | OF182 | OF181 | OF180 | DLE18 | OF172 | OF171 | OF170 | DLE17 | OF162 | OF161 | OF160 | DLE16 |
| FOR4 Register | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OF232 | OF231 | OF230 | DLE23 | OF222 | OF221 | OF220 | DLE22 | OF212 | OF211 | OF210 | DLE21 | OF202 | OF201 | OF200 | DLE20 |
| FOR5 Register | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OF272 | OF271 | OF270 | DLE27 | OF262 | OF261 | OF260 | DLE26 | OF252 | OF251 | OF250 | DLE25 | OF242 | OF241 | OF240 | DLE24 |
| FOR6 Register | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OF312 | OF311 | OF310 | DLE31 | OF302 | OF301 | OF300 | DLE30 | OF292 | OF291 | OF290 | DLE29 | OF282 | OF281 | OF280 | DLE28 |
| FOR7 Register | | | | | | | | | | | | | | | |

| Name ⁽¹⁾ | Description |
|--|--|
| OFn2, OFn1, OFn0 (Offset Bits 2, 1 & 0) | These three bits define how long the serial interface receiver takes to recognize and store bit 0 from the RX input pin: i.e., to start a new frame. The input frame offset can be selected to +4.5 clock periods from the point where the external frame pulse input signal is applied to the \overline{FOI} input of the device. See Figure 7. |
| DLEn | ST-BUS [®] mode: DLEn = 0, if clock rising edge is at the $\frac{3}{4}$ point of the bit cell. (Data Latch Edge) DLEn = 1, if when clock falling edge is at the $\frac{3}{4}$ of the bit cell. GCI mode: DLEn = 0, if clock falling edge is at the $\frac{3}{4}$ point of the bit cell. DLEn = 1, if when clock rising edge is at the $\frac{3}{4}$ of the bit cell. |

NOTE:

1. n denotes an input stream number from 0 to 31.

TABLE 8 — MAXIMUM ALLOWABLE SKEW

| Switching Mode | Control Bits | | | | Data Rate bits/s | | Maximum allowable skew |
|----------------|--------------|-----|-----|-----|------------------|------------------|------------------------|
| | DR3 | DR2 | DR1 | DR0 | Receive Streams | Transmit Streams | |
| Regular | 0 | 0 | 0 | 0 | 2 M on RX0-31 | 2 M on TX0-31 | +4.5 |
| | 0 | 0 | 0 | 1 | 4 M on RX0-31 | 4 M on TX0-31 | +4.5 |
| | 0 | 0 | 1 | 0 | 8 M on RX0-31 | 8 M on TX0-31 | +4.5 |
| | 0 | 0 | 1 | 1 | 16 M on RX0-15 | 16 M on TX0-15 | +2.5 |
| Mux/Demux | 0 | 1 | 0 | 0 | 2 M on RX0-31 | 8 M on TX0-7 | +1.5 |
| | 0 | 1 | 0 | 1 | 8 M on RX0-7 | 2 M on TX0-31 | +4.5 |
| | 0 | 1 | 1 | 0 | 4 M on RX0-31 | 8 M on TX0-15 | +1.5 |
| | 0 | 1 | 1 | 1 | 8 M on RX0-15 | 4 M on TX0-31 | +4.5 |
| | 1 | 0 | 0 | 0 | 16 M on RX0-3 | 2 M on TX0-31 | +2.5 |
| | 1 | 0 | 0 | 1 | 2 M on RX0-31 | 16 M on TX0-3 | +1.5 |
| | 1 | 0 | 1 | 0 | 16 M on RX0-15 | 8 M on TX0-31 | +4.5 |
| | 1 | 0 | 1 | 1 | 8 M on RX0-31 | 16 M on TX0-15 | +4.5 |
| Split | 1 | 1 | 0 | 0 | 2 M on RX0-15; | 2 M on TX0-15; | +1.5 |
| | | | | | 8 M on RX16-31 | 8 M on TX16-31 | +4.5 |
| | 1 | 1 | 0 | 1 | 2 M on RX0-15; | 2 M on TX0-15; | +1.5 |
| | | | | | 4 M on RX16-31 | 4 M on TX16-31 | +4.5 |
| | 1 | 1 | 1 | 0 | 4 M on RX0-15; | 4 M on TX0-15; | +1.5 |
| | | | | | 8 M on RX16-31 | 8 M on TX16-31 | +4.5 |
| | 1 | 1 | 1 | 1 | 8 M on RX0-15; | 8 M on TX0-15; | +4.5 |
| | | | | | 16 M on RX16-23 | 16 M on TX16-23 | +2.5 |

TABLE 9 — OFFSET BITS (OFN2, OFN1, OFN0, DLEN) & FRAME DELAY BITS (FD11, FD2-0)

| Input Stream Offset | Measurement Result from Frame Delay Bits | | | | Corresponding Offset Bits | | | |
|---------------------------------|--|-----|-----|-----|---------------------------|------|------|------|
| | FD11 | FD2 | FD1 | FD0 | OFn2 | OFn1 | OFn0 | DLEn |
| No clock period shift (Default) | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| + 0.5 clock period shift | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| + 1.0 clock period shift | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| + 1.5 clock period shift | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| + 2.0 clock period shift | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| + 2.5 clock period shift | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| + 3.0 clock period shift | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| + 3.5 clock period shift | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| + 4.0 clock period shift | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| + 4.5 clock period shift | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |

NOTE:

1. See Table 8 for maximum allowable offsets.

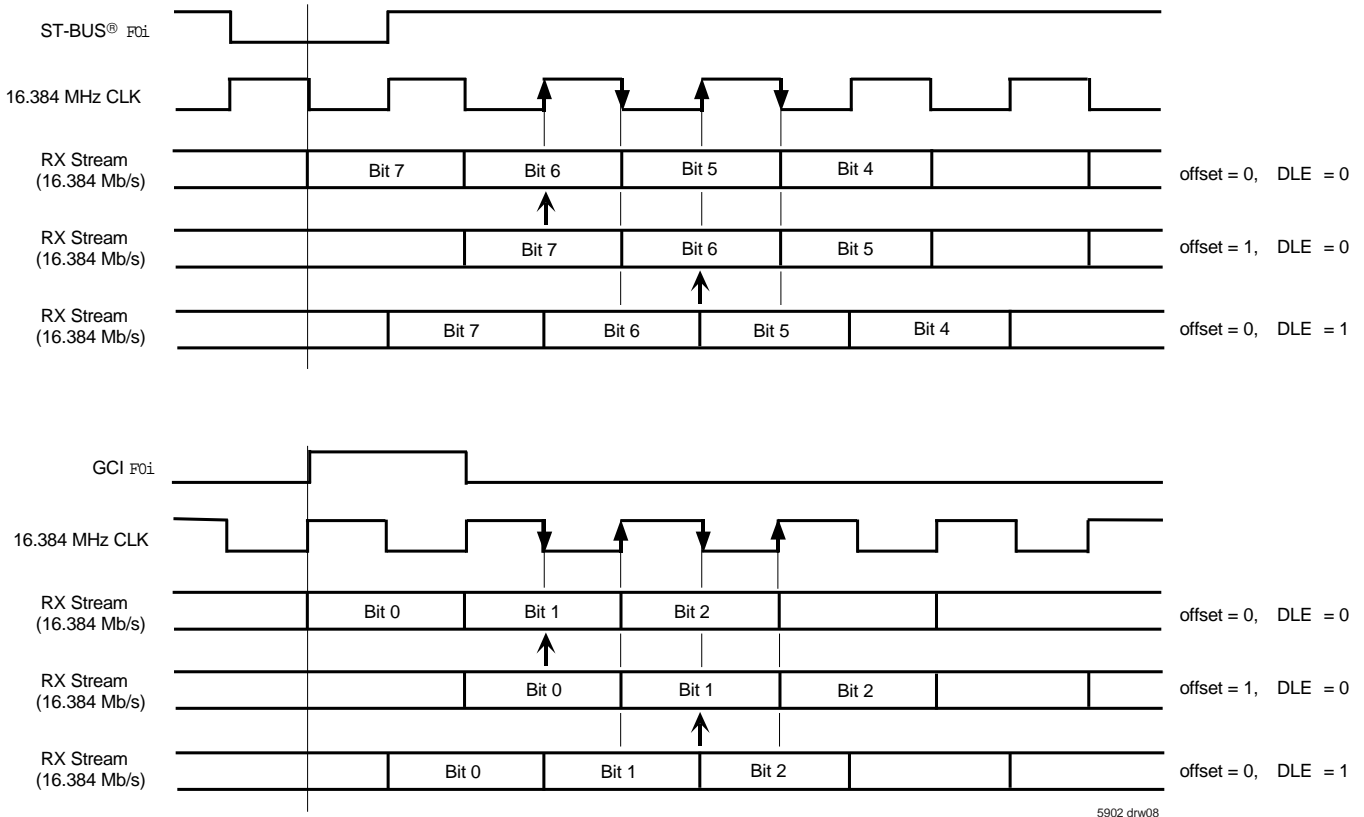


Figure 7. Examples for Input Offset Delay Timing in 16 Mb/s mode

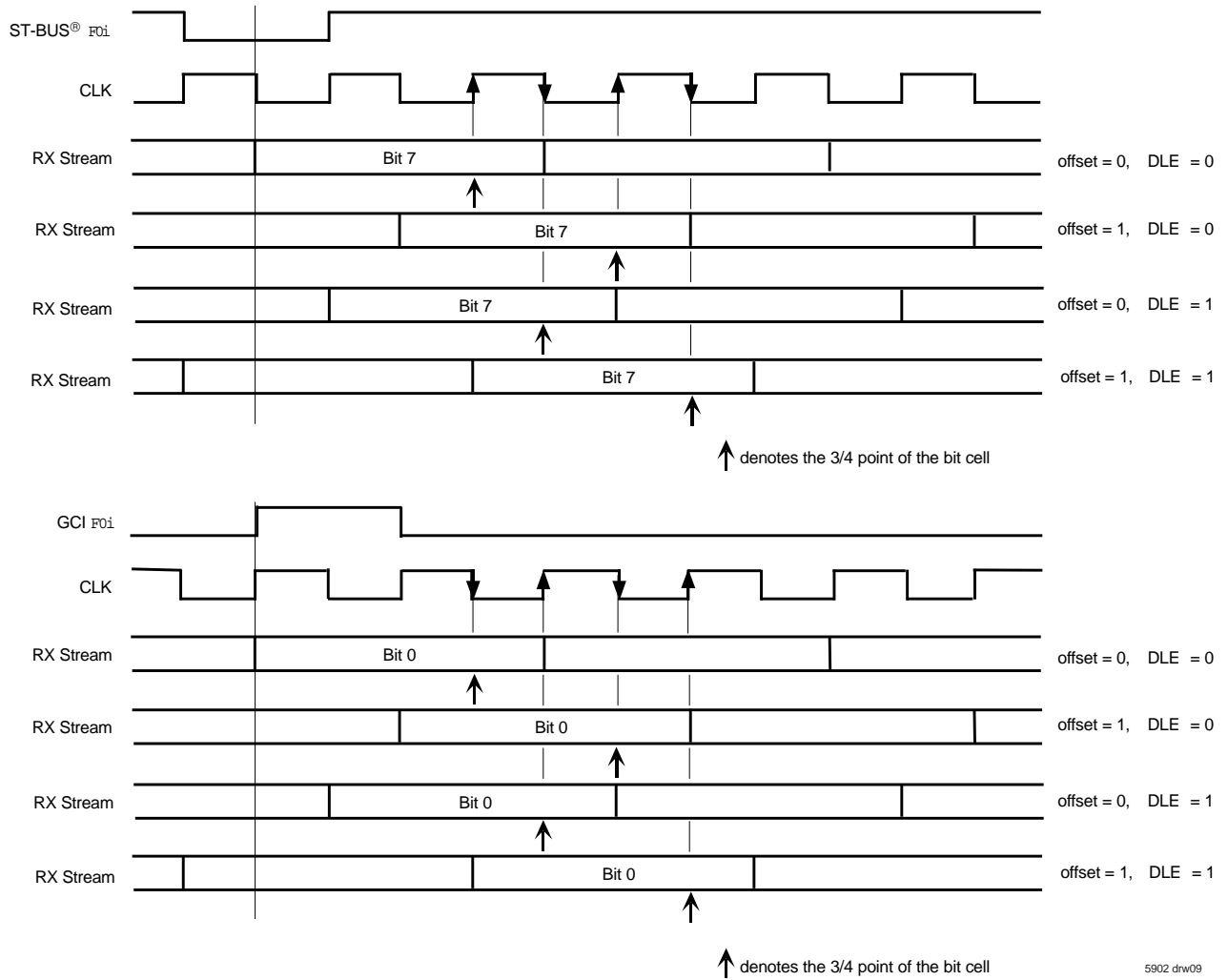


Figure 7. Examples for Input Offset Delay Timing in 8 Mb/s, 4 Mb/s and 2 Mb/s mode (Continued)

JTAG SUPPORT

The IDT72V71643 JTAG interface conforms to the Boundary-Scan standard IEEE-1149.1. This standard specifies a design-for-testability technique called Boundary-Scan test (BST). The operation of the boundary-scan circuitry is controlled by an external test access port (TAP) Controller.

TEST ACCESS PORT (TAP)

The Test Access Port (TAP) provides access to the test functions of the IDT72V71643. It consists of three input pins and one output pin.

- Test Clock Input (TCK)

TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clock and thus remain independent. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic.

- Test Mode Select Input (TMS)

The logic signals received at the TMS input are interpreted by the TAP Controller to control the test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to Vcc when it is not driven from an external source.

- Test Data Input (TDI)

Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to Vcc when it is not driven from an external source.

- Test Data Output (TDO)

Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out towards the TDO. The data out of the TDO is clocked on the falling edge of the TCK pulses. When no data is shifted through the boundary scan cells, the TDO driver is set to a high-impedance state.

- Test Reset (TRST)

Reset the JTAG scan structure. This pin is internally pulled to Vcc.

INSTRUCTION REGISTER

In accordance with the IEEE-1149.1 standard, the IDT72V71643 uses public instructions. The IDT72V71643 JTAG Interface contains a two-bit instruction register. Instructions are serially loaded into the instruction register from the TDI when the TAP Controller is in its shifted-IR state. Subsequently, the instructions are decoded to achieve two basic functions: to select the test data register that may operate while the instruction is current, and to define the serial test data register path, which is used to shift data between TDI and TDO during data register scanning.

| Value | Instruction |
|----------|----------------|
| 00 | EXTEST |
| 11 | BYPASS |
| 01 or 10 | SAMPLE/PRELOAD |

JTAG Instruction Register Decoding

TEST DATA REGISTER

As specified in IEEE-1149.1, the IDT72V71643 JTAG Interface contains two test data registers:

- The Boundary-Scan register

The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the IDT72V71643 core logic.

- The Bypass Register

The Bypass register is a single stage shift register that provides a one-bit path from TDI to its TDO. The IDT72V71643 boundary scan register bits are shown in Table 10. Bit 0 is the first bit clocked out. All three-state enable bits are active high.

TABLE 10—BOUNDARY SCAN REGISTER BITS

| Device Pin | Boundary Scan Bit 0 to bit 168 | | |
|-----------------|--------------------------------|------------------|-----------------|
| | Three-State Control | Output Scan Cell | Input Scan Cell |
| ODE | | | 0 |
| RESET | | | 1 |
| CLK | | | 2 |
| F _{0i} | | | 3 |
| FE/HCLK | | | 4 |
| WFPS | | | 5 |
| DS | | | 6 |
| CS | | | 7 |
| R/W | | | 8 |
| A0 | | | 9 |
| A1 | | | 10 |
| A2 | | | 11 |
| A3 | | | 12 |
| A4 | | | 13 |
| A5 | | | 14 |
| A6 | | | 15 |
| A7 | | | 16 |
| A8 | | | 17 |
| A9 | | | 18 |
| A10 | | | 19 |
| A11 | | | 20 |
| A12 | | | 21 |
| A13 | | | 22 |
| A14 | | | 23 |
| DTA | | 24 | |
| D15 | 25 | 26 | 27 |
| D14 | 28 | 29 | 30 |
| D13 | 31 | 32 | 33 |
| D12 | 34 | 35 | 36 |
| D11 | 37 | 38 | 39 |
| D10 | 40 | 41 | 42 |
| D9 | 43 | 44 | 45 |
| D8 | 46 | 47 | 48 |
| D7 | 49 | 50 | 51 |
| D6 | 52 | 53 | 54 |
| D5 | 55 | 56 | 57 |
| D4 | 58 | 59 | 60 |
| D3 | 61 | 62 | 63 |
| D2 | 64 | 65 | 66 |
| D1 | 67 | 68 | 69 |
| D0 | 70 | 71 | 72 |
| TX31/OEI15 | 73 | 74 | |
| TX30/OEI14 | 75 | 76 | |
| TX29/OEI13 | 77 | 78 | |
| TX28/OEI12 | 79 | 80 | |
| TX27/OEI11 | 81 | 82 | |
| TX26/OEI10 | 83 | 84 | |
| TX25/OEI9 | 85 | 86 | |
| TX24/OEI8 | 87 | 88 | |
| RX31 | | | 89 |
| RX30 | | | 90 |
| RX29 | | | 91 |
| RX28 | | | 92 |

| Device Pin | Boundary Scan Bit 0 to bit 168 | | |
|------------|--------------------------------|------------------|-----------------|
| | Three-State Control | Output Scan Cell | Input Scan Cell |
| RX27 | | | 93 |
| RX26 | | | 94 |
| RX25 | | | 95 |
| RX24 | | | 96 |
| TX23/OEI7 | 97 | 98 | |
| TX22/OEI6 | 99 | 100 | |
| TX21/OEI5 | 101 | 102 | |
| TX20/OEI4 | 103 | 104 | |
| TX19/OEI3 | 105 | 106 | |
| TX18/OEI2 | 107 | 108 | |
| TX17/OEI1 | 109 | 110 | |
| TX16/OEI0 | 111 | 112 | |
| RX23 | | | 113 |
| RX22 | | | 114 |
| RX21 | | | 115 |
| RX20 | | | 116 |
| RX19 | | | 117 |
| RX18 | | | 118 |
| RX17 | | | 119 |
| RX16 | | | 120 |
| TX15 | 121 | 122 | |
| TX14 | 123 | 124 | |
| TX13 | 125 | 126 | |
| TX12 | 127 | 128 | |
| TX11 | 129 | 130 | |
| TX10 | 131 | 132 | |
| TX9 | 133 | 134 | |
| TX8 | 135 | 136 | |
| RX15 | | | 137 |
| RX14 | | | 138 |
| RX13 | | | 139 |
| RX12 | | | 140 |
| RX11 | | | 141 |
| RX10 | | | 142 |
| RX9 | | | 143 |
| RX8 | | | 144 |
| TX7 | 145 | 146 | |
| TX6 | 147 | 148 | |
| TX5 | 149 | 150 | |
| TX4 | 151 | 152 | |
| TX3 | 153 | 154 | |
| TX2 | 155 | 156 | |
| TX1 | 157 | 158 | |
| TX0 | 159 | 160 | |
| RX7 | | | 161 |
| RX6 | | | 162 |
| RX5 | | | 163 |
| RX4 | | | 164 |
| RX3 | | | 165 |
| RX2 | | | 166 |
| RX1 | | | 167 |
| RX0 | | | 168 |

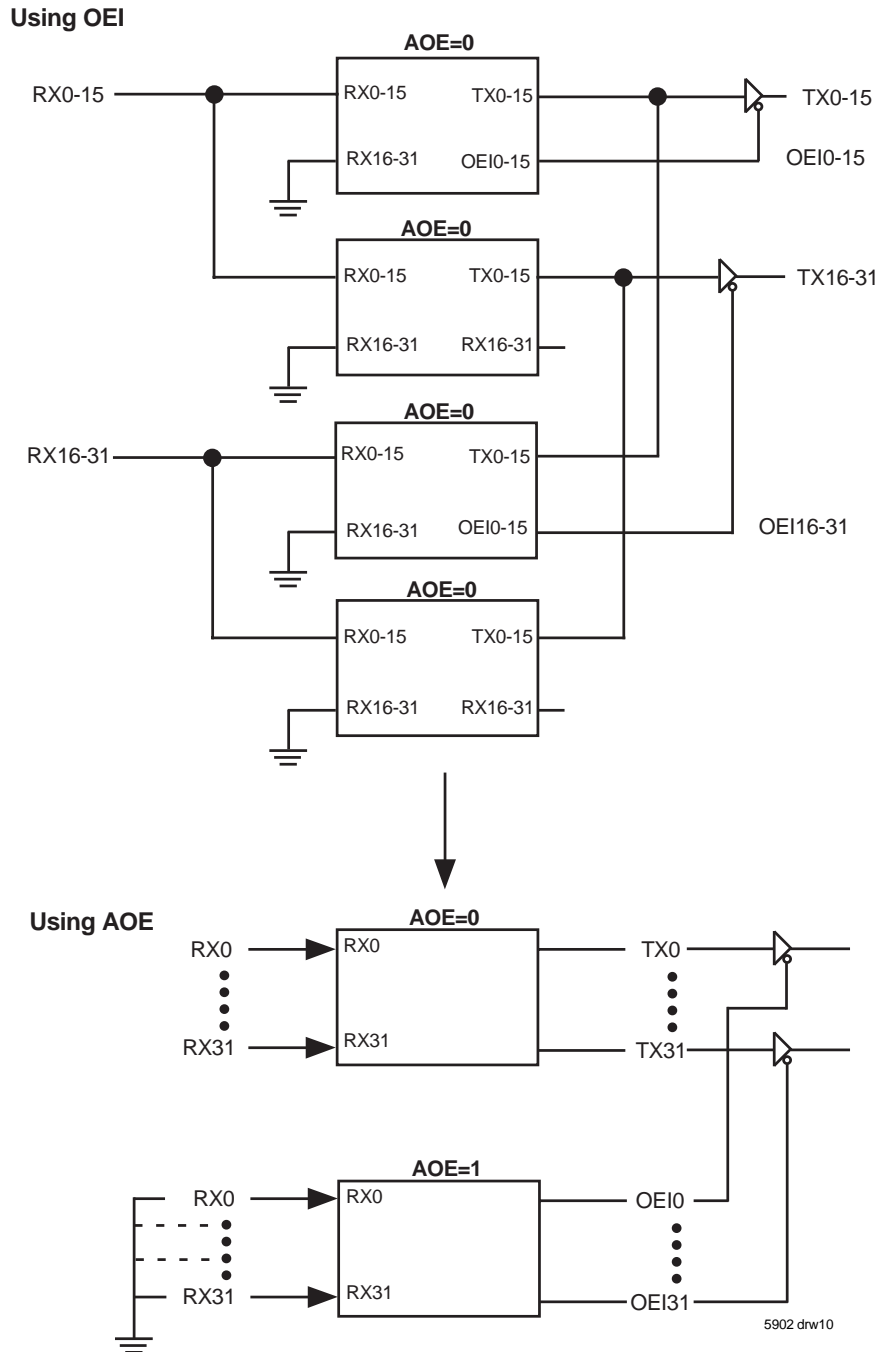


Figure 8. Using All Output Enable (AOE)

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Min. | Max. | Unit |
|-----------------|----------------------------|----------|------|------|
| V _{CC} | Supply Voltage | 3.0 | 3.6 | V |
| V _I | Voltage on Digital Inputs | GND -0.3 | 5.3 | V |
| I _O | Current at Digital Outputs | -50 | 50 | mA |
| T _s | Storage Temperature | -55 | +125 | °C |
| P _D | Package Power Dissipation | — | 2 | W |

NOTE:

1. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------|----------------------------------|------|------|------|------|
| V _{CC} | Positive Supply | 3.0 | 3.3 | 3.6 | V |
| V _{IH} | Input HIGH Voltage | 2.0 | — | 5.3 | V |
| V _{IL} | Input LOW Voltage | — | — | 0.8 | V |
| T _{OP} | Operating Temperature Commercial | -40 | 25 | +85 | °C |

NOTE:

1. Voltages are with respect to Ground unless otherwise stated.

DC ELECTRICAL CHARACTERISTICS

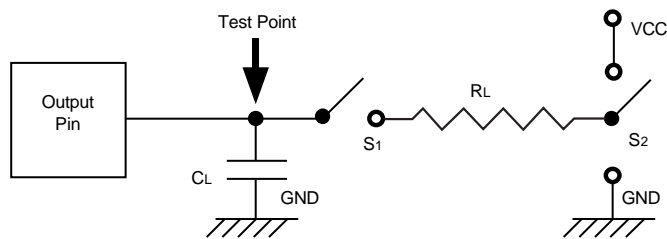
| Symbol | Parameter | Min. | Typ. | Max. | Units |
|----------------------------------|----------------------------|------|------|------|-------|
| I _{CC} ⁽²⁾ | Supply Current | - | - | 75 | mA |
| I _{IL} ^(3,4) | Input Leakage (input pins) | - | - | 60 | μA |
| I _{OZ} ^(3,4) | High-impedance Leakage | - | - | 60 | μA |
| V _{OH} ⁽⁵⁾ | Output HIGH Voltage | 2.4 | - | - | V |
| V _{OL} ⁽⁶⁾ | Output LOW Voltage | - | - | 0.4 | V |

NOTES:

1. Voltages are with respect to ground (GND) unless otherwise stated.
2. Outputs unloaded.
3. 0 ≤ V ≤ V_{CC}.
4. Maximum leakage on pins (output or I/O pins in high-impedance state) is over an applied voltage (V).
5. I_{OH} = 10 mA.
6. I_{OL} = 10 mA.

AC ELECTRICAL CHARACTERISTICS - TIMING PARAMETER MEASUREMENT VOLTAGE LEVELS

| Symbol | Rating | Level | Unit |
|-----------------|--------------------------------------|-------|------|
| V _{TT} | TTL Threshold | 1.5 | V |
| V _{HM} | TTL Rise/Fall Threshold Voltage HIGH | 2.0 | V |
| V _{LM} | TTL Rise/Fall Threshold Voltage LOW | 0.8 | V |



S1 is open circuit except when testing output levels or high-impedance states.

S2 is switched to VCC or GND when testing output levels or high-impedance states.

Figure 9. Output Load

AC ELECTRICAL CHARACTERISTICS - FRAME PULSE AND CLK

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|-----------------------------------|--|------|------------|------|----------|
| tFPW ⁽¹⁾ | Frame Pulse Width (ST-BUS®, GCI) | | | | |
| | Bit rate = 2.048 Mb/s | 26 | — | 295 | ns |
| | Bit rate = 4.096 Mb/s | 26 | — | 145 | ns |
| | Bit rate = 8.192 Mb/s or 16.384 Mb/s | 26 | — | 65 | ns |
| tFPS ⁽¹⁾ | Frame Pulse Setup time before CLK falling (ST-BUS® or GCI) | 5 | — | — | ns |
| tFPH ⁽¹⁾ | Frame Pulse Hold Time from CLK falling (ST-BUS® or GCI) | 10 | — | — | ns |
| tCP ⁽¹⁾ | CLK Period | | | | |
| | Bit rate = 2.048 Mb/s | 190 | — | 300 | ns |
| | Bit rate = 4.096 Mb/s | 110 | — | 150 | ns |
| | Bit rate = 8.192 Mb/s or 16.384 Mb/s | 58 | — | 70 | ns |
| tCH ⁽¹⁾ | CLK Pulse Width HIGH | | | | |
| | Bit rate = 2.048 Mb/s | 85 | — | 150 | ns |
| | Bit rate = 4.096 Mb/s | 50 | — | 75 | ns |
| | Bit rate = 8.192 Mb/s or 16.384 Mb/s | 20 | — | 40 | ns |
| tCL ⁽¹⁾ | CLK Pulse Width LOW | | | | |
| | Bit rate = 2.048 Mb/s | 85 | — | 150 | ns |
| | Bit rate = 4.096 Mb/s | 50 | — | 75 | ns |
| | Bit rate = 8.192 Mb/s or 16.384 Mb/s | 20 | — | 40 | ns |
| t _r , t _f | Clock Rise/Fall Time | — | — | 10 | ns |
| tHFPW ⁽²⁾ | Wide Frame Pulse Width | | | | |
| | HCLK = 4.096 MHz HCLK = 8.192 MHz | | 244 122 | | ns ns |
| tHFPS ⁽²⁾ | Frame Pulse Setup Time before HCLK 4 MHz falling | 50 | — | 150 | ns |
| tHFPH ⁽²⁾ | Frame Pulse Hold Time from HCLK 4 MHz falling | 50 | — | 150 | ns |
| tHFPS ⁽²⁾ | Frame Pulse Setup Time before HCLK 8 MHz rising | 45 | — | 90 | ns |
| tHFPH ⁽²⁾ | Frame Pulse Hold Time from HCLK 8 MHz rising | 45 | — | 90 | ns |
| tHCP ⁽²⁾ | HCLK Period | | | | |
| | @ 4.096 MHz @ 8.192 MHz | | 244 122 | | ns ns |
| t _{hr} , t _{hf} | HCLK Rise/Fall Time | — | — | 10 | ns |
| tDIF ⁽²⁾ | Delay between falling edge of HCLK and falling edge of CLK | -10 | — | 10 | ns |

NOTES:

1. WFPS Pin = 0.
2. WFPS Pin = 1.

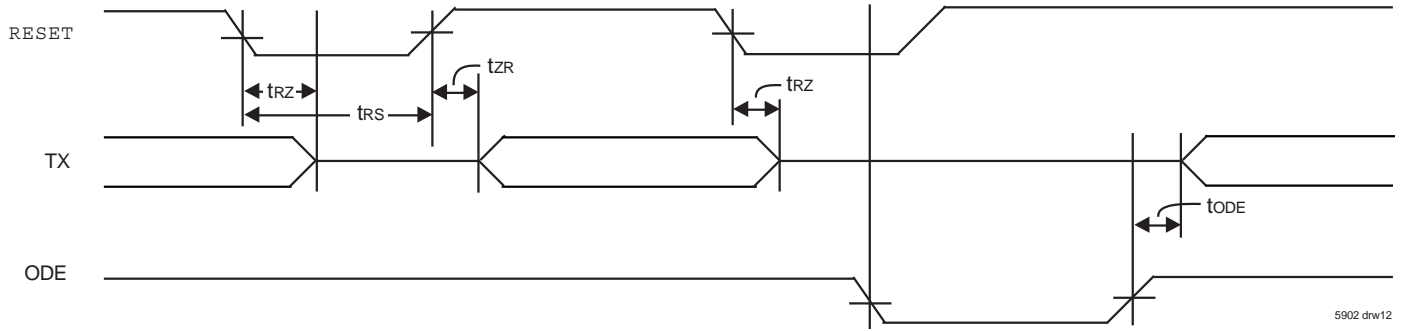


Figure 10. Reset and ODE Timing

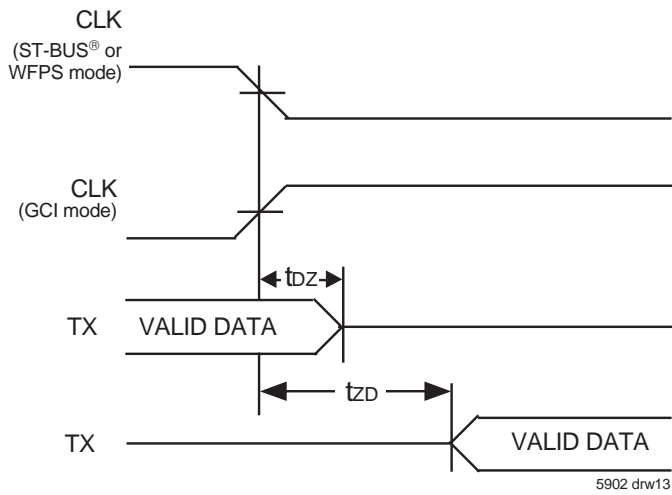


Figure 11. Serial Output and External Control

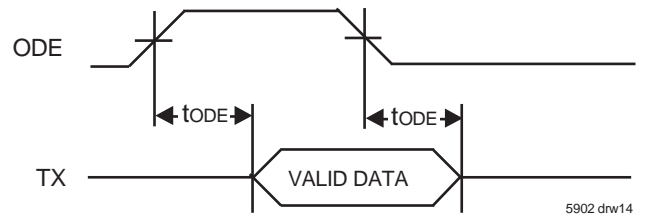


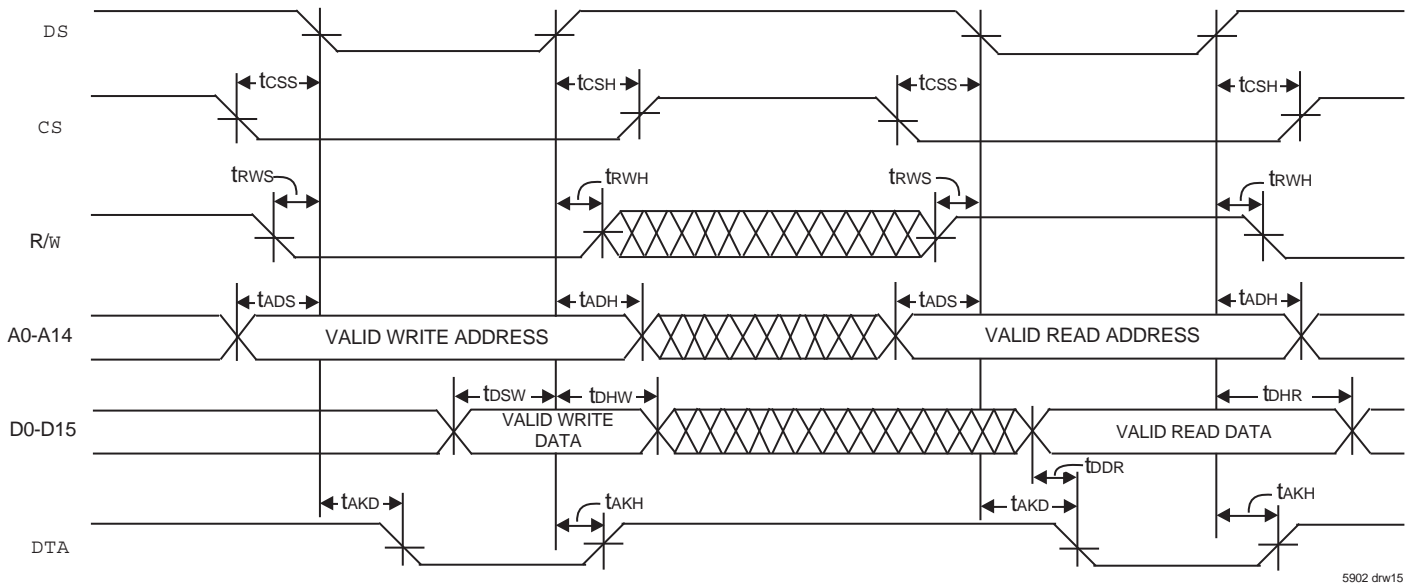
Figure 12. Output Driver Enable (ODE)

AC ELECTRICAL CHARACTERISTICS - MICROPROCESSOR INTERFACE TIMING

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|-------------------------------------|---|------|------|-------------------------|----------------------|
| t _{CSS} | CS Setup from DS falling | 0 | — | — | ns |
| t _{RWS} | R/W Setup from DS falling | 3 | — | — | ns |
| t _{ADS} | Address Setup from DS falling | 2 | — | — | ns |
| t _{CSH} | CS Hold after DS rising | 0 | — | — | ns |
| t _{RWH} | R/W Hold after DS Rising | 3 | — | — | ns |
| t _{ADH} | Address Hold after DS Rising | 2 | — | — | ns |
| t _{DDR} ⁽¹⁾ | Data Setup from \overline{DTA} LOW on Read | 2 | — | — | ns |
| t _{DHR} ^(1,2,3) | Data Hold on Read | 10 | 15 | 25 | ns |
| t _{DSW} | Data Setup on Write (Fast Write) | 10 | — | — | ns |
| t _{SWD} | Valid Data Delay on Write (Slow Write) | - | — | 0 | ns |
| t _{DHW} | Data Hold on Write | 5 | — | — | ns |
| t _{DSPW} | DS Pulse Width | 5 | — | — | ns |
| t _{CKAK} | Clock to ACK | — | — | 35 | ns |
| t _{AKD} ⁽¹⁾ | Acknowledgment Delay: Reading/Writing Registers Reading/Writing Memory @ 2.048 Mb/s @ 4.096 Mb/s @ 8.192 Mb/s or 16.384 Mb/s | | | 30 345 200 120 | ns ns ns ns |
| t _{AKH} ^(1,2,3) | Acknowledgment Hold Time | — | — | 15 | ns |
| t _{DSS} ⁽⁴⁾ | Data Strobe Setup Time | 2 | — | — | ns |

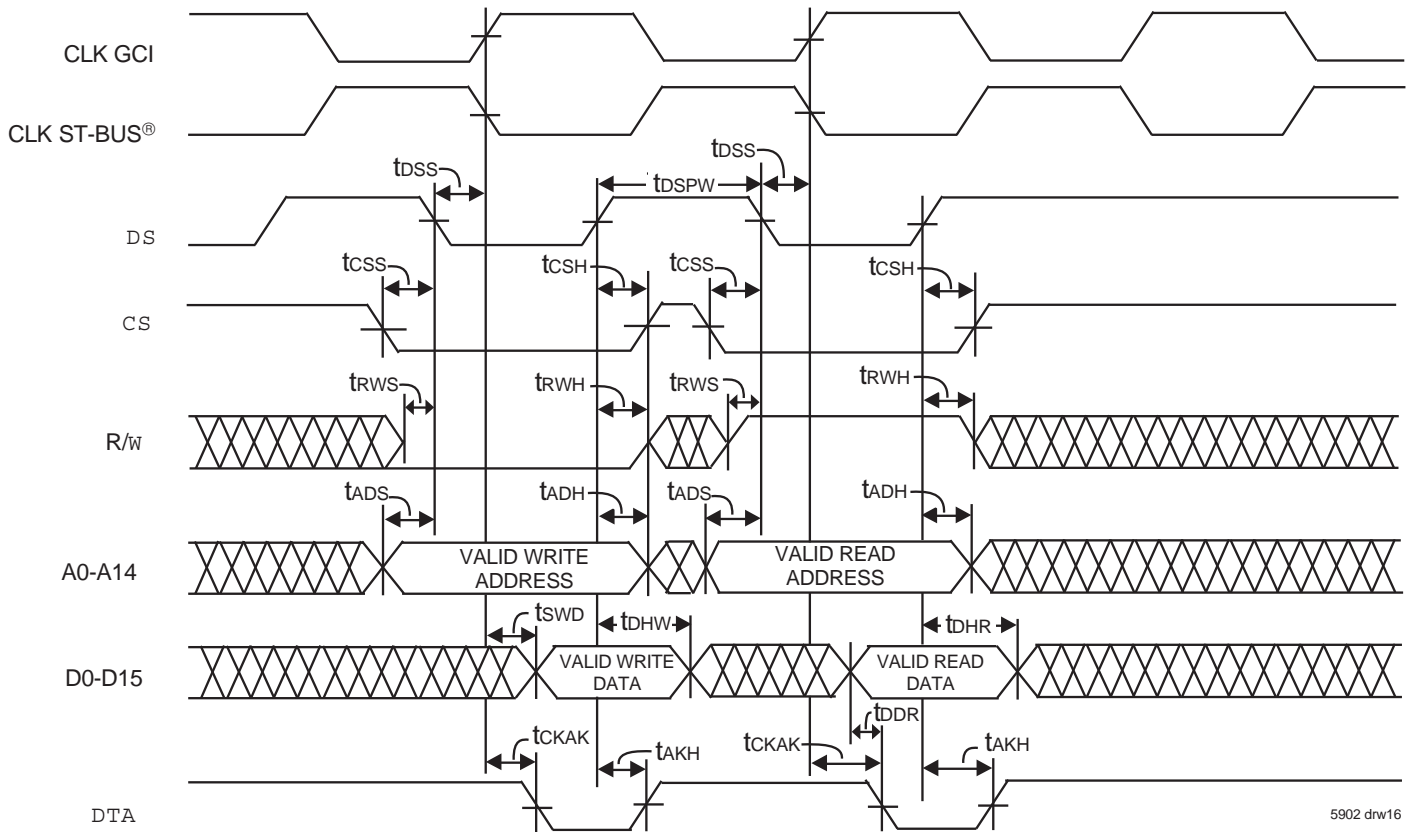
NOTES:

1. C_L = 150pF
2. R_L = 1K
3. High-Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.
4. To achieve one clock cycle fast memory access, this setup time, t_{DSS} should be met. Otherwise, worst case memory access operation is determined by t_{AKD}.



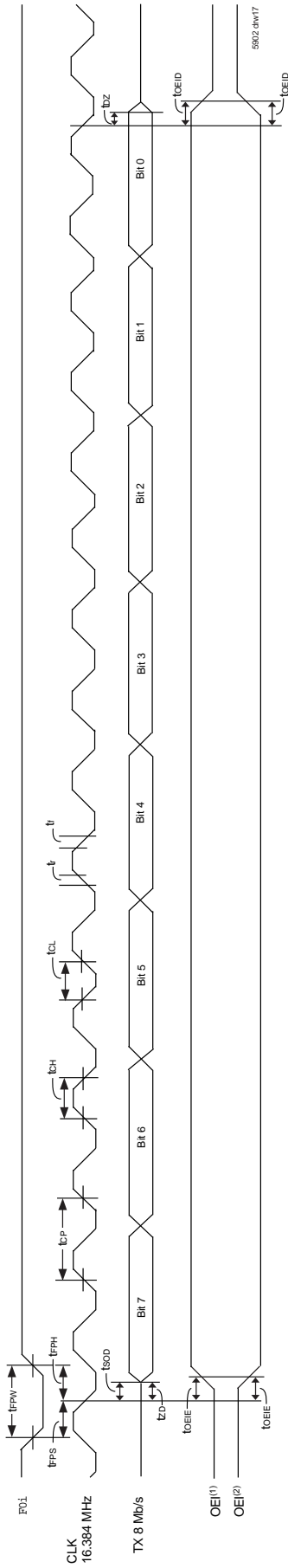
5902 drw15

Figure 13. Asynchronous Bus Timing



5902 drw16

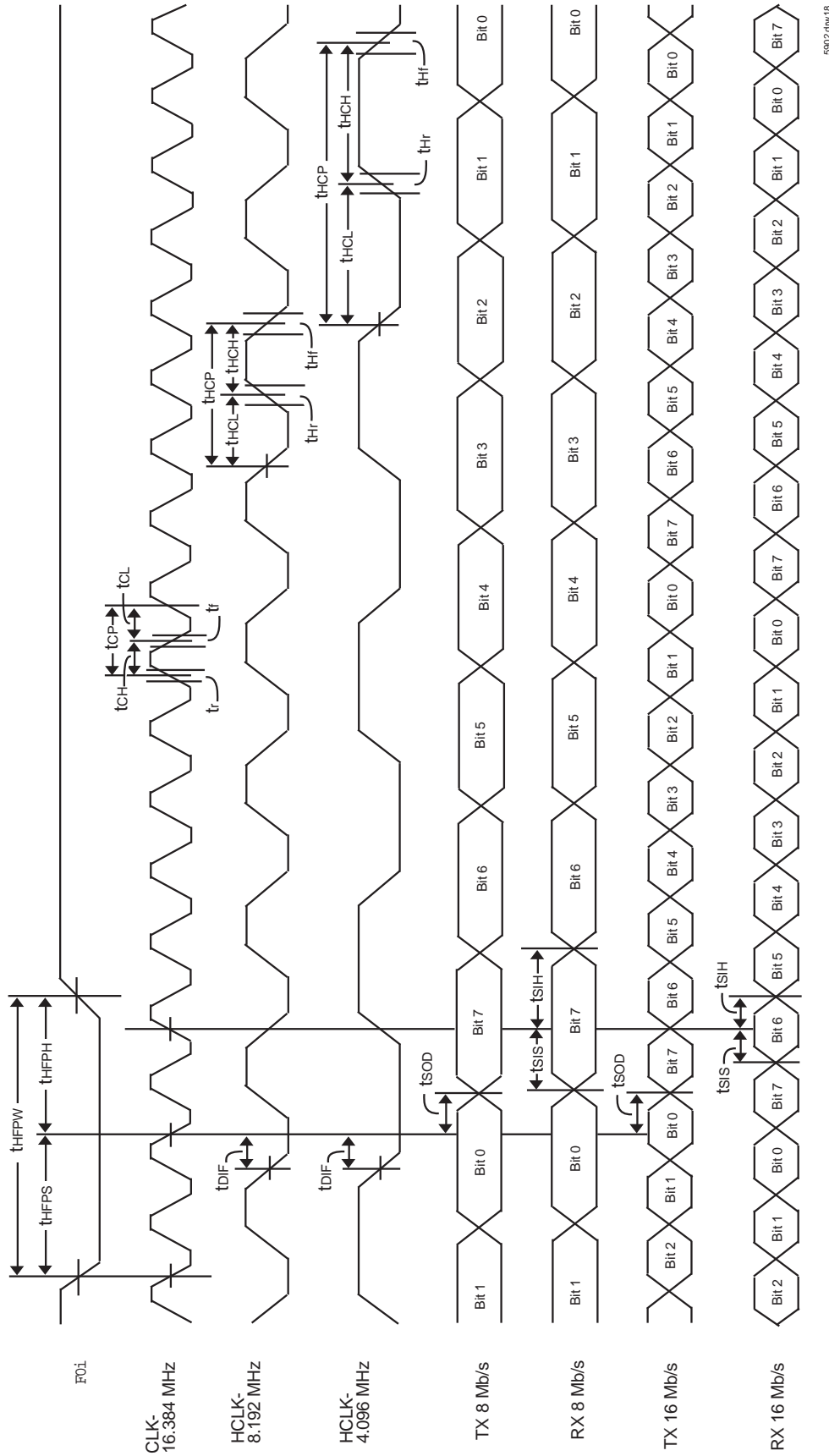
Figure 14. Synchronous Bus Timing



NOTES:

1. When OEPOL = 1, OEI is HIGH when TX is active and LOW when TX is in three-state.
2. When OEPOL = 0, OEI is LOW when TX is active and HIGH when TX is in three-state.

Figure 15. Output Enable Indicator Timing (8 Mb/s ST-BUS®)



5902.dwr18

Figure 16. WFPS Timing

AC ELECTRICAL CHARACTERISTICS⁽¹⁾ — SERIAL STREAM (ST-BUS® and GCI)

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---------------------|---------------------------------------|------|------|------|-------|
| tSIS | RX Setup Time | 5 | — | — | ns |
| tSH | RX Hold Time | 10 | — | — | ns |
| tSOD | TX Delay – Active to Active | — | — | 30 | ns |
| tDZ ⁽¹⁾ | TX Delay – Active to High-Z | — | — | 30 | ns |
| tZD ⁽¹⁾ | TX Delay – High-Z to Active | — | — | 30 | ns |
| tODE ⁽¹⁾ | Output Driver Enable (ODE) Delay | — | — | 30 | ns |
| tOEIE | Output Enable Indicator (OEI) Enable | — | — | 40 | ns |
| tOEID | Output Enable Indicator (OEI) Disable | — | — | 25 | ns |
| tRZ | Active to High-Z on Master Reset | — | — | 30 | ns |
| tZR | High-Z to Active on Master Reset | — | — | 30 | ns |
| tRs | Reset pulse width | 100 | — | — | ns |

NOTE:

1. High-Impedance is measured by pulling to the appropriate rail with R_L (1K Ω), with timing corrected to cancel time taken to discharge C_L (150 pF).

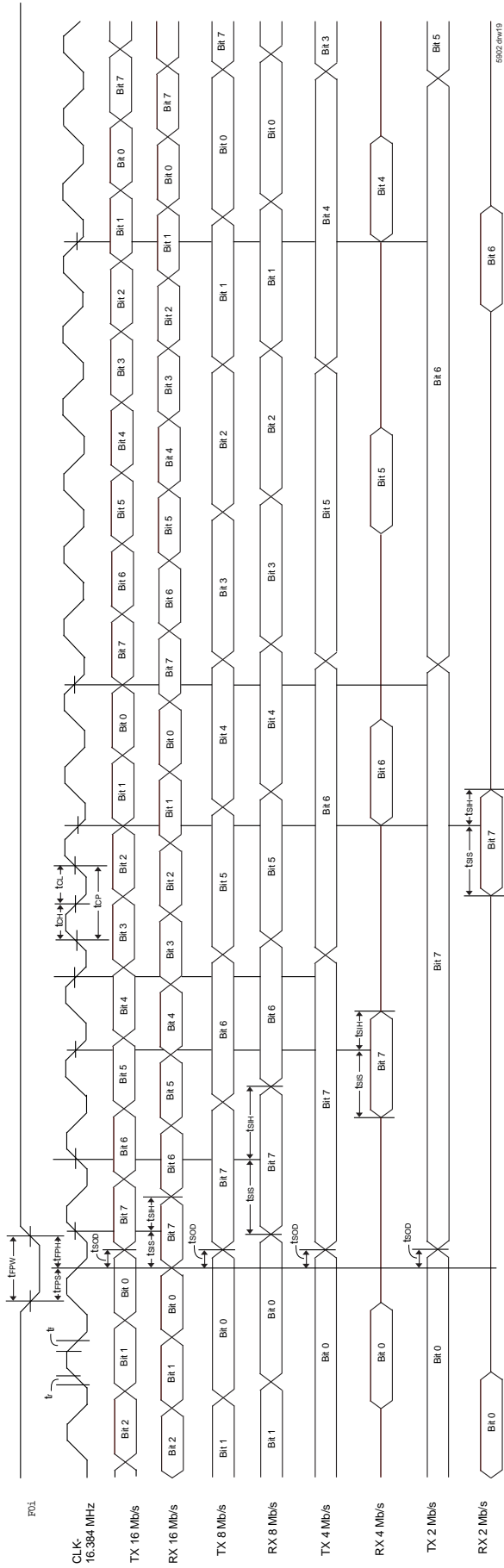


Figure 17. ST-BUS® Timing

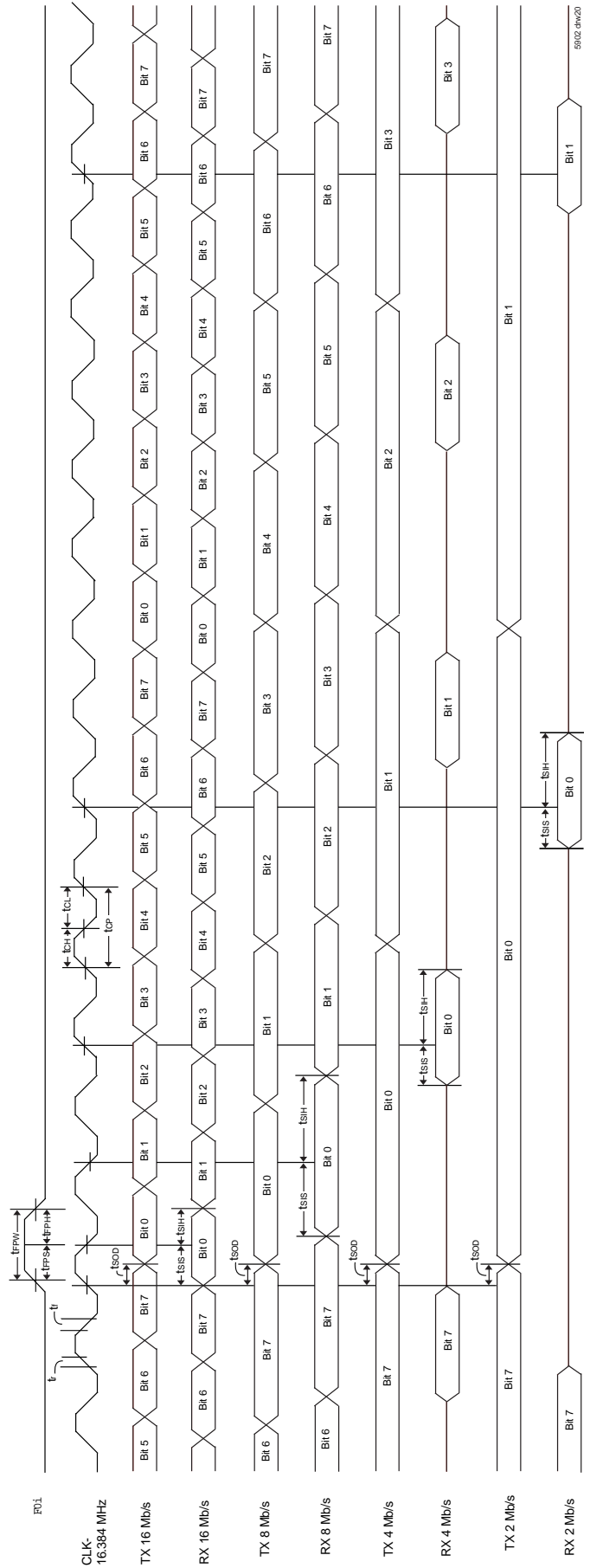


Figure 18. GCI Timing

ORDERING INFORMATION

| IDT | XXXXX | XX | XX | | |
|-----|-------------|---------|-------------------------|------------|--|
| | Device Type | Package | Process/ Temp. Range | | |
| | | | | Blank | Commercial (-40°C to +85°C) |
| | | | | BCG DAG | BGA - Green (BGA, BC144-1) TQFP – Green (TQFP, DA144-1) |
| | | | | 72V71643 | 4096 x 4096 – 3.3V Time Slot Interchange Digital Switch |

DATASHEET DOCUMENT HISTORY

| | |
|------------|---|
| 5/01/2000 | pg. 1 |
| 6/07/2000 | pgs. 3 and 4. |
| 10/10/2000 | pgs. 1 through 30. |
| 11/20/2000 | pgs.10. |
| 03/09/2001 | pg. 21 |
| 08/20/2001 | pg. 24. |
| 10/22/2001 | pg. 1. |
| 1/04/2002 | pgs. 1 and 21. |
| 12/03/2012 | pg. 30 |
| 8/12/2014 | pg 1 Product Discontinuation Notice, CQ-14-06 |



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