

Revision History

AS4C64M8D1-66pin TSOPII and 60-ball TFBGA PACKAGE

Revision	Details	Date
Rev 1.0	Preliminary datasheet	May 2015

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Features

- Fast clock rate: 250/200MHz
- Differential Clock CK & CK
- Bi-directional DQS
- DLL enable/disable by EMRS
- Fully synchronous operation
- Internal pipeline architecture
- Four internal banks, 16M x 8-bit for each bank
- Programmable Mode and Extended Mode registers
 - CAS Latency: 2, 2.5, 3
 - Burst length: 2, 4, 8
 - Burst Type: Sequential & Interleaved
- · Individual byte write mask control
- DM Write Latency = 0
- Auto Refresh and Self Refresh
- 8192 refresh cycles / 64ms
- Precharge & active power down
- Power supplies: VDD & VDDQ = $2.5V \pm 0.2V$
- Operating Temperature:
 - Commercial (0~70°C)
 - Industrial (-40~85°C)
- Interface: SSTL_2 I/O Interface
- Package: 66 Pin TSOP II, 0.65mm pin pitch - Pb and Halogen free
- Package: 60-Ball, 8x13x1.2 mm (max) TFBGA - Pb free and Halogen Free



Overview

The 512Mb DDR SDRAM is a high-speed CMOS double data rate synchronous DRAM containing 512 Mbits. It is internally configured as a quad 16M x 8-bit DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CK). Data outputs occur at both rising edges of CK and \overline{CK} . Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of a BankActivate command which is then followed by a Read or Write command. The device provides programmable Read or Write burst lengths of 2, 4, or 8. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The refresh functions, either Auto or Self Refresh are easy to use. In addition, 512Mb DDR SDRAM features programmable DLL option. By having a programmable mode register and extended mode register, the system can choose the most suitable modes to maximize its performance. These devices are well suited for applications requiring high memory bandwidth, result in a device particularly well suited to high performance main memory and graphics applications.

Table 1. Ordering Information

Product part No	Org	Temperature	Max Clock (MHz)	Package
AS4C64M8D1-5TCN	64M x 8	Commercial 0°C to 70°C	200	66pin TSOPII
AS4C64M8D1-5TIN	64M x 8	Industrial -40°C to 85°C	200	66pin TSOPII
AS4C64M8D1-5BCN	64M x 8	Commercial 0°C to 70°C	200	60ball FBGA
AS4C64M8D1-5BIN	64M x 8	Industrial -40°C to 85°C	200	60ball FBGA



Figure 1. Pin Assignment (Top View)



Figure 1.1 Ball Assignment (Top View)





Figure 2. Block Diagram





Pin Descriptions

Table 2. Pin Details

Symbol	Туре	Description
ск, СК	Input	Differential Clock: CK and \overline{CK} are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of \overline{CK} . Input and output data is referenced to the crossing of CK and \overline{CK} (both directions of the crossing)
CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CK signal. If CKE goes low synchronously with clock, the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes.
BA0, BA1	Input	Bank Activate: BA0 and BA1 define to which bank the BankActivate, Read, Write, or BankPrecharge command is being applied.
A0-A12	Input	Address Inputs: A0-A12 are sampled during the BankActivate command (row address A0-A12) and Read/Write command (column address A0-A9, A11 with A10 defining Auto Precharge).
CS	Input	Chip Select: \overline{CS} enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when \overline{CS} is sampled HIGH. \overline{CS} provides for external bank selection on systems with multiple banks. It is considered part of the command code.
RAS	Input	Row Address Strobe: The RAS signal defines the operation commands in conjunction with the CAS and WE signals and is latched at the positive edges of CK. When RAS and CS are asserted "LOW" and CAS is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the WE signal. When the WE is asserted "HIGH," the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the WE is asserted "LOW," the Precharge command is selected by BA is selected and the bank designated by BA is selected and the bank
CAS	Input	Column Address Strobe: The \overline{CAS} signal defines the operation commands in conjunction with the \overline{RAS} and \overline{WE} signals and is latched at the positive edges of CK. When \overline{RAS} is held "HIGH" and \overline{CS} is asserted "LOW," the column access is started by asserting \overline{CAS} "LOW." Then, the Read or Write command is selected by asserting \overline{WE} "HIGH" or "LOW".
WE	Input	Write Enable: The \overline{WE} signal defines the operation commands in conjunction with the \overline{RAS} and \overline{CAS} signals and is latched at the positive edges of CK. The \overline{WE} input is used to select the BankActivate or Precharge command and Read or Write command.
DQS	Input /	Data Strobe: Output with read data, input with write data. Edgealigned with read
	Output	data, centered in write data. Used to capture write data.
DM	Input	Data Input Mask: Input data is masked when DM is sampled HIGH during a write cycle.
DQ0 – DQ7	Input / Output	Data Bus: Data Input/output.
Vdd	Supply	Power Supply: $2.5V \pm 0.2V$
Vss	Supply	Ground



Vddq	Supply	DQ Power: 2.5V \pm 0.2V. Provide isolated power to DQs for improved noise immunity.
Vssq	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
Vref	Supply	SSTL_2 reference Voltage
NC	-	No Connect: These pins should be left unconnected.



Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CK. Table 3 shows the truth table for the operation commands.

		-						-			
Command	State	CKEn-1	CKEn	DM	BA0,1	A10	A0-9, 11-12	CS	RAS		WE
BankActivate	Idle ⁽³⁾	Н	Х	Х	V	Ro	w address	L	L	Н	Н
BankPrecharge	Any	Н	Х	Х	V	L	Х	L	L	Н	L
PrechargeAll	Any	Н	Х	Х	Х	Н	Х	L	L	Н	L
Write	Active ⁽³⁾	Н	Х	Х	V	L	Column	L	Н	L	L
Write and AutoPrecharge	Active ⁽³⁾	Н	Х	Х	V	Н	(A0 ~ A9)	L	Н	L	L
Read	Active ⁽³⁾	Н	Х	Х	V	L	Column	L	Н	L	Н
Read and Autoprecharge	Active ⁽³⁾	Н	Х	Х	V	Н	(A0 ~ A9)	L	Н	L	Н
Mode Register Set	Idle	Н	Х	Х		OP	code	L	L	L	L
Extended MRS	Idle	Н	Х	Х		OP	code	L	L	L	L
No-Operation	Any	Н	Х	Х	Х	Х	Х	L	Н	Н	Н
Burst Stop	Active ⁽⁴⁾	Н	Х	Х	Х	Х	Х	L	Н	Н	L
Device Deselect	Any	Н	Х	Х	Х	Х	Х	Н	Х	Х	Х
AutoRefresh	Idle	Н	Н	Х	Х	Х	Х	L	L	L	Н
SelfRefresh Entry	Idle	Н	L	Х	Х	Х	Х	L	L	L	Н
SelfRefresh Exit	Idle	L	Н	Х	Х	Х	Х	Н	Х	Х	Х
	(SelfRefresh)							L	Н	Н	Н
Precharge Power Down Mode	Idle	Н	L	Х	Х	Х	Х	Н	Х	Х	Х
Entry								L	Н	Н	Н
Precharge Power Down Mode	Any	L	Н	Х	Х	Х	Х	Н	Х	Х	Х
Exit	(PowerDown)							L	Н	Н	Н
Active Power Down Mode Entry	Active	Н	L	Х	Х	Х	Х	Н	Х	Х	Х
								L	V	V	V
Active Power Down Mode Exit	Any	L	Н	Х	Х	Х	Х	Н	Х	Х	Х
	(PowerDown)							L	Н	Н	Н
Data Input Mask Disable	Active	Н	Х	L	Х	Х	Х	Х	Х	Х	Х
Data Input Mask Enable	Active	Н	Х	Н	Х	Х	Х	Х	Х	Х	Х

Table 3. Truth Table (Note (1), (2))

Note: 1. V=Valid data, X=Don't Care, L=Low level, H=High level

2. CKE_n signal is input level when commands are provided.

CKE_{n-1} signal is input level one clock cycle before the commands are provided.

3. These are states of bank designated by BA signal.

4. Device state is 2, 4, and 8 burst operation.



Mode Register Set (MRS)

The Mode Register stores the data for controlling various operating modes of a DDR SDRAM. It programs CAS Latency, Burst Type, and Burst Length to make the DDR SDRAM useful for a variety of applications. The default value of the Mode Register is not defined; therefore the Mode Register must be written by the user. Values stored in the register will be retained until the register is reprogrammed. The Mode Register is written by asserting Low on \overline{CS} , \overline{RAS} , \overline{CAS} , \overline{WE} , BA1 and BA0 (the device should have all banks idle with no bursts in progress prior to writing into the mode register, and CKE should be High). The state of address pins A0~A12 and BA0, BA1 in the same cycle in which CS, RAS, CAS and WE are asserted Low is written into the Mode Register. A minimum of two clock cycles, tMRD, are required to complete the write operation in the Mode Register. The Mode Register is divided into various fields depending on functionality. The Burst Length uses A0~A2, Burst Type uses A3, and CAS Latency (read latency from column address) uses A4~A6. A logic 0 should be programmed to all the undefined addresses to ensure future compatibility. Reserved states should not be used to avoid unknown device operation or incompatibility with future versions. Refer to the table for specific codes for various burst lengths, burst types and CAS latencies.



Table 4. Mode Register Bitmap

Burst Length Field (A2~A0)

This field specifies the data length of column access using the A2~A0 pins and selects the Burst Length to be 2, 4, 8.

Table 5. Burst Length

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved



Addressing Mode Select Field (A3)

The Addressing Mode can be one of two modes, either Interleave Mode or Sequential Mode. Both Sequential Mode and Interleave Mode support burst length of 2, 4 and 8.

Table 6. Addressing Mode

A3	Addressing Mode
0	Sequential
1	Interleave

Burst Definition, Addressing Sequence of Sequential and Interleave Mode Table 7. Burst Address ordering

Burst Longth	Start Address		SS	Sequential	Interleave
Durst Length	A2	A1	A0	Sequential	Intelleave
0	Х	Х	0	0, 1	0, 1
2	Х	Х	1	1, 0	1, 0
	Х	0	0	0, 1, 2, 3	0, 1, 2, 3
4	Х	0	1	1, 2, 3, 0	1, 0, 3, 2
4	Х	1	0	2, 3, 0, 1	2, 3, 0, 1
	Х	1	1	3, 0, 1, 2	3, 2, 1, 0
	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0	0	1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	0	1	0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
0	0	1	1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
0	1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1	0	1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	1	1	0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	1	1	1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

CAS Latency Field (A6~A4)

This field specifies the number of clock cycles from the assertion of the Read command to the first read data. The minimum whole value of CAS Latency depends on the frequency of CK. The minimum whole value satisfying the following formula must be programmed into this field. tcac(min) ≤ CAS Latency X tck

Table 8. CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5 clocks
1	1	1	Reserved

Test Mode field (A8~A7) •

These two bits are used to enter the test mode and must be programmed to "00" in normal operation.

Table 9. Test Mode

A8	A7	Test Mode
0	0	Normal mode
1	0	DLL Reset



• (BA0, BA1)

Table 10. MRS/EMRS

BA1	BA0	A12 ~ A0
RFU	0	MRS Cycle
RFU	1	Extended Functions (EMRS)

Extended Mode Register Set (EMRS)

The Extended Mode Register Set stores the data for enabling or disabling DLL and selecting output driver strength. The default value of the extended mode register is not defined, therefore must be written after power

up for proper operation. The Extended Mode Register is written by asserting Low on \overline{CS} RAS, \overline{CAS} , \overline{WE} , BA1 and BA0 (the device should have all banks idle with no bursts in progress prior to writing into the mode register, and CKE should be High). The state of A0 ~ A12, BA0 and BA1 is written in the mode register in the same cycle as \overline{CS} , \overline{RAS} , \overline{CAS} , and \overline{WE} going low. The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register. A1 is used for setting driver strength to normal, or weak. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. "High" on BA0 is used for EMRS. Refer to the table for specific codes.



Table 11. Extended Mode Register Bitmap



Table 12. Absolute Maximum Rating

Symbol	Item		Rating	Unit
Vin, Vout	Input, Output Volta	age	- 0.5~ VDDQ + 0.5	V
Vdd, Vddq	Power Supply Volt	age	- 1~3.6	V
TA	Ambient Temperature	Commercial	0~70	∞°C
		Industrial	-40~85	∞°C
Tstg	Storage Temperature		- 55~150	∞°C
TSOLDER	Soldering Temperature		260	∞°C
PD	Power Dissipation		1	W
los	Short Circuit Output (Current	50	mA

Note1: Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Note2: These voltages are relatived to Vss

Table 13. Recommended D.C. (Operating	g Conditions	(V _{DD} = 2.5V ±0.2V, T _A = -40~85 °C))
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Symbol	Parameter	Min.	Max.	Unit
Vdd	Power Supply Voltage	2.3	2.7	V
Vddq	Power Supply Voltage (for I/O Buffer)	2.3	2.7	V
Vref	Input Reference Voltage	0.49 x Vddq	0.51 x Vddq	V
Vін (DC)	Input High Voltage (DC)	Vref + 0.15	Vddq + 0.3	V
VIL (DC)	Input Low Voltage (DC)	-0.3	Vref – 0.15	V
Vтт	Termination Voltage	Vref - 0.04	Vref + 0.04	V
VIN (DC)	Input Voltage Level, CK and \overline{CK} inputs	-0.3	Vddq + 0.3	V
VID (DC)	Input Different Voltage, CK and \overline{CK} inputs	0.36	Vddq + 0.6	V
lı	Input leakage current	-2	2	μA
loz	Output leakage current	-5	5	μA
Іон	Output High current (Vout = 1.95V)	-16.2	-	mA
lol	Output Low current (Vout = 0.35V)	16.2	-	mA

Note : All voltages are referenced to Vss.

Table 14. Capacitance ($V_{DD} = 2.5V$, f = 1MHz, T_A = 25 °C)

Symbol	Parameter	Min.	Max.	Unit
CIN1	Input Capacitance (CK, CK)	2	3	pF
CIN2	Input Capacitance (All other input-only pins)	2	3	рF
Ci/o	DQ, DQS, DM Input/Output Capacitance	4	5	рF

Note: These parameters are guaranteed by design, periodically sampled and are not 100% tested



Table 15. D.C. Characteristics ($V_{DD} = 2.5V \pm 0.2V$, $T_A = -40 \sim 85 \circ$ C)

		-5	
Parameter & Test Condition	Symbol	Max.	Unit
OPERATING CURRENT:			
One bank; Active-Precharge; tRc=tRc(min); tCk=tCk(min); DQ,DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles.	IDD0	80	mA
OPERATING CURRENT:			
One bank; BL=4; reads - Refer to the following page for detailed test conditions	IDD1	90	mA
PRECHARGE POWER-DOWN STANDBY CURRENT:	סכססו	F	m۸
All banks idle; power-down mode; tCK=tCK(min); CKE = LOW	IDD2P	5	ШA
PRECHARGE FLOATING STANDBY CURRENT:			
CS = HIGH; all banks idle; CKE = HIGH; tCK =tCK(min); address and other control inputs changing once per clock cycle; $VIN = VREF$ for DQ, DQS and DM	IDD2F	35	mA
PRECHARGE QUIET STANDBY CURRENT:			
CS =HIGH; all banks idle; CKE =HIGH; tck=tck(min) address and other control inputs stable at \geq VIH(min) or \leq VIL (max); VIN = VREF for DQ, DQS and DM	IDD2Q	35	mA
ACTIVE POWER-DOWN STANDBY CURRENT : one bank active;	IDD3P	20	mA
ACTIVE STANDBY CURRENT : CS=HIGH CKE=HIGH one bank			
active ; tRC=tRC(max);tCK=tCK(min);Address and control inputs changing once per clock cycle; DQ,DQS,and DM inputs changing twice per clock cycle	IDD3N	65	mA
OPERATING CURRENT BURST READ : BL=2; READS; Continuous burst; one bank active; Address and control inputs changing once per clock cycle; tck=tck(min); lout=0mA;50% of data changing on every transfer	IDD4R	130	mA
OPERATING CURRENT BURST Write : BL=2; WRITES; Continuous Burst ;one bank active; address and control inputs changing once per clock cycle; tck=tck(min); DQ,DQS,and DM changing twice per clock cycle; 50% of data changing on every transfer	IDD4W	130	mA
AUTO REFRESH CURRENT : trc=trFc(min); tck=tck(min)	IDD5	140	mA
SELF REFRESH CURRENT: Self Refresh Mode ; CKE≦ 0.2V;tcκ=tcκ(min)	IDD6	6	mA
BURST OPERATING CURRENT 4 bank operation:			
Four bank interleaving READs; BL=4;with Auto Precharge; tRC=tRC(min); tCK=tCK(min); Address and control inputs change only during Active, READ, or WRITE command	IDD7	210	mA



Table 16. Electrical Characteristics and Recommended A.C.Operating Condition $(V_{DD} = 2.5V \pm 0.2V, T_A = -40 \sim 85 °C)$

Sumbol	Symbol Barameter		-5		11014	Nata
Symbol	Parameter		Min.	Max.	Unit	Note
		CL = 2	7.5	12	ns	
tск	Clock cycle time	CL = 2.5	6	12	ns	
		CL = 3	5	12	ns	
tсн	Clock high level width		0.45	0.55	tск	
tc∟	Clock low level width		0.45	0.55	tск	
tнр	Clock half period		tclmin or tcнmin	-	ns	2
tHZ	Data-out-high impedance time from Ch	<, <u>CK</u>	-	0.7	ns	3
t∟z	Data-out-low impedance time from CK	, CK	-0.7	0.7	ns	3
t DQSCK	DQS-out access time from CK, \overline{CK}		-0.6	0.6	ns	
tac	Output access time from CK, \overline{CK}		-0.7	0.7	ns	
toqsq	DQS-DQ Skew		-	0.4	ns	
t RPRE	Read preamble		0.9	1.1	tск	
t RPST	Read postamble		0.4	0.6	tск	
toqss	CK to valid DQS-in		0.72	1.25	tск	
twpres	DQS-in setup time		0	-	ns	4
twpre	DQS Write preamble		0.25	-	tск	
twpst	DQS write postamble		0.4	0.6	tск	5
tdqsн	DQS in high level pulse width	0.35	-	tск		
t DQSL	DQS in low level pulse width	0.35	-	tск		
tıs	Address and Control input setup time	0.7	-	ns	6	
tıн	Address and Control input hold time		0.7	-	ns	6
tos	DQ & DM setup time to DQS		0.4	-	ns	
tон	DQ & DM hold time to DQS		0.4	-	ns	
tqн	DQ/DQS output hold time from DQS		thp - t _{QHS}	-	ns	
trc	Row cycle time		55	-	ns	
trfc	Refresh row cycle time		70	-	ns	
tras	Row active time		40	70K	ns	
trcd	Active to Read or Write delay		15	-	ns	
t _{RP}	Row precharge time		15	-	ns	
trrd	Row active to Row active delay		10	-	ns	
twr	Write recovery time		15	-	ns	
t wtr	Internal Write to Read Command Dela	у	2	-	tск	
t MRD	Mode register set cycle time		10	-	ns	
trefi	Average Periodic Refresh interval	-	7.8	μs	7	
txsrd	Self refresh exit to read command delay		200	-	tск	
t xsnr	Self refresh exit to non-read command delay		75	-	ns	
t DAL	Auto Precharge write recovery + precharge time		twr+trp	-	ns	
t DIPW	DQ and DM input pulse width	-	1.75	-	ns	
tipw	Control and Address input pulse width		2.2	-	ns	
t _{QHS}	Data Hold Skew Factor		-	0.5	ns	
t _{DSS}	DQS falling edge to CK setup time		0.2	-	tск	
t _{DSH}	DQS falling edge hold time from CK		0.2	-	tск	



Table 17. Recommended A.C. Operating Conditions (VDD = 2.5V ±0.2V, TA = -40~85 °C)

Symbol	Parameter	Min.	Max.	Unit
VIH (AC)	Input High Voltage (AC)	Vref + 0.31	-	V
Vı∟(AC)	Input Low Voltage (AC)	-	Vref – 0.31	V
VID (AC)	Input Different Voltage, CK and \overline{CK} inputs	0.7	Vddq + 0.6	V
Vix (AC)	Input Crossing Point Voltage, CK and \overline{CK} inputs	0.5 x Vddq-0.2	0.5 x Vddq+0.2	V

Note:

- 1) Enables on-chip refresh and address counters.
- 2) Min(t_{CL}, t_{CH}) refers to ther smaller of the actual clock low time and actual clock high time as provided to the device.
- t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving(HZ), or begins driving(LZ).
- 4) The specific requirement is that DQS be valid (High, Low, or at some point on a valid transition) on or before this CLK edge. A valid transition is defined as monotonic, and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tboss.
- 5) The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
- 6) For command/address and CK & \overline{CK} slew rate \geq 1.0V/ns.
- 7) A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
- 8) Power-up sequence is described in Note 10
- 9) A.C. Test Conditions



Table 18. SSTL _2 Interface

Reference Level of Output Signals (VREF)	0.5 x Vddq
Output Load	Reference to the Test Load
Input Signal Levels	Vref+0.31 V / Vref-0.31 V
Input Signals Slew Rate	1 V/ns
Reference Level of Input Signals	0.5 x Vddq

Figure 3. SSTL_2 A.C. Test Load



10) Power up Sequence

Power up must be performed in the following sequence.

- 1) Apply power to VDD before or at the same time as VDDQ, VTT and VREF when all input signals are held "NOP" state and maintain CKE "LOW".
- 2) Start clock and maintain stable condition for minimum $200\mu s$.
- 3) Issue a "NOP" command and keep CKE "HIGH"
- 4) Issue a "Precharge All" command.
- 5) Issue EMRS enable DLL.
- 6) Issue MRS reset DLL. (An additional 200 clock cycles are required to lock the DLL).
- 7) Precharge all banks of the device.
- 8) Issue two or more Auto Refresh commands.
- 9) Issue MRS with A8 to low to initialize the mode register.



Timing Waveforms

Figure 4. Activating a Specific Row in a Specific Bank



RA=Row Address BA=Bank Address





Figure 5. tRCD and tRRD Definition







CA=Column Address BA=Bank Address EN AP=Enable Autoprecharge DIS AP=Disable Autoprecharge





Figure 7. Read Burst Required CAS Latencies (CL=2)



DO n=Data Out from column n Burst Length=4 3 subsequent elements of Data Out appear in the programmed order following DO n





Read Burst Required CAS Latencies (CL=2.5)





Read Burst Required CAS Latencies (CL=3)







Figure 8. Consecutive Read Bursts Required CAS Latencies (CL=2)



DO n (or o)=Data Out from column n (or column o) Burst Length=4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first) 3 subsequent elements of Data Out appear in the programmed order following DO n 3 (or 7) subsequent elements of Data Out appear in the programmed order following DO o Read commands shown must be to the same device





Consecutive Read Bursts Required CAS Latencies (CL=2.5)



DO n (or o)=Data Out from column n (or column o) Burst Length=4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first) 3 subsequent elements of Data Out appear in the programmed order following DO n 3 (or 7) subsequent elements of Data Out appear in the programmed order following DO o Read commands shown must be to the same device





Consecutive Read Bursts Required CAS Latencies (CL=3)



DO n (or o)=Data Out from column n (or column o) Burst Length=4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first) 3 subsequent elements of Data Out appear in the programmed order following DO n 3 (or 7) subsequent elements of Data Out appear in the programmed order following DO o Read commands shown must be to the same device







Figure 9. Non-Consecutive Read Bursts Required CAS Latencies (CL=2)

DO n (or o)=Data Out from column n (or column o) Burst Length=4 3 subsequent elements of Data Out appear in the programmed order following DO n (and following DO o)



Non-Consecutive Read Bursts Required CAS Latencies (CL=2.5)









Non-Consecutive Read Bursts Required CAS Latencies (CL=3)







Figure 10. Random Read Accesses Required CAS Latencies (CL=2)

DO n, etc. =Data Out from column n, etc. n', etc. =the next Data Out following DO n, etc. according to the programmed burst order Burst Length=2,4 or 8 in cases shown. If burst of 4 or 8, the burst is interrupted Reads are to active rows in any banks







Random Read Accesses Required CAS Latencies (CL=2.5)

DO n, etc. =Data Out from column n, etc. n', etc. =the next Data Out following DO n, etc. according to the programmed burst order Burst Length=2,4 or 8 in cases shown. If burst of 4 or 8, the burst is interrupted Reads are to active rows in any banks



Random Read Accesses Required CAS Latencies (CL=3)



DO n, etc. =Data Out from column n, etc. n', etc. =the next Data Out following DO n, etc. according to the programmed burst order Burst Length=2,4 or 8 in cases shown. If burst of 4 or 8, the burst is interrupted Reads are to active rows in any banks





Figure 11. Terminating a Read Burst Required CAS Latencies (CL=2)

DO n = Data Out from column n Cases shown are bursts of 8 terminated after 4 data elements 3 subsequent elements of Data Out appear in the programmed order following DO n



Terminating a Read Burst Required CAS Latencies (CL=2.5)



3 subsequent elements of Data Out appear in the programmed order following DO n







Terminating a Read Burst Required CAS Latencies (CL=3)

DO n = Data Out from column n Cases shown are bursts of 8 terminated after 4 data elements 3 subsequent elements of Data Out appear in the programmed order following DO n







Figure 12. Read to Write Required CAS Latencies (CL=2)

DO n (or o)= Data Out from column n (or column o)

Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)

1 subsequent element of Data Out appears in the programmed order following DO n Data in elements are applied following DI o in the programmed order







Read to Write Required CAS Latencies (CL=2.5)

DO n (or o)= Data Out from column n (or column o)

Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)

1 subsequent element of Data Out appears in the programmed order following DO n Data in elements are applied following DI o in the programmed order







Read to Write Required CAS Latencies (CL=3)

DO n (or o)= Data Out from column n (or column o)

Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)

1 subsequent element of Data Out appears in the programmed order following DO n Data in elements are applied following DI o in the programmed order







Figure 13. Read to Precharge Required CAS Latencies (CL=2)

Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8 3 subsequent elements of Data Out appear in the programmed order following DO n Precharge may be applied at (BL/2) tCK after the READ command

Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

The Active command may be applied if tRC has been met







Read to Precharge Required CAS Latencies (CL=2.5)

Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8 3 subsequent elements of Data Out appear in the programmed order following DO n

Precharge may be applied at (BL/2) tCK after the READ command

Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

The Active command may be applied if tRC has been met







Read to Precharge Required CAS Latencies (CL=3)

The Active command may be applied if tRC has been met





Figure 14. Write Command



CA=Column Address BA=Bank Address EN AP=Enable Autoprecharge DIS AP=Disable Autoprecharge





Figure 15. Write Max DQSS



DI n = Data In for column n

3 subsequent elements of Data In are applied in the programmed order following DI n

A non-interrupted burst of 4 is shown

A10 is LOW with the WRITE command (AUTO PRECHARGE disabled)





Figure 16. Write Min DQSS



DI n = **Data** In for column n

3 subsequent elements of Data In are applied in the programmed order following DI n

A non-interrupted burst of 4 is shown

A10 is LOW with the WRITE command (AUTO PRECHARGE disabled) $\label{eq:command}$







Figure 17. Write Burst Nom, Min, and Max tDQSS

DI n = Data In for column n 3 subsequent elements of Data are applied in the programmed order following DI n A non-interrupted burst of 4 is shown A10 is LOW with the WRITE command (AUTO PRECHARGE disabled)







Figure 18. Write to Write Max tDQSS

DI n , etc. = Data In for column n,etc. 3 subsequent elements of Data In are applied in the programmed order following DI n 3 subsequent elements of Data In are applied in the programmed order following DI o Non-interrupted bursts of 4 are shown







Figure 19. Write to Write Max tDQSS, Non Consecutive

DI n, etc. = Data In for column n, etc.

3 subsequent elements of Data In are applied in the programmed order following DI n 3 subsequent elements of Data In are applied in the programmed order following DI o Non-interrupted bursts of 4 are shown







Figure 20. Random Write Cycles Max tDQSS

DI n, etc. = Data In for column n, etc. n', etc. = the next Data In following DI n, etc. according to the programmed burst order Programmed Burst Length 2, 4, or 8 in cases shown If burst of 4 or 8, the burst would be truncated Each WRITE command may be to any bank and may be to the same or different devices







Figure 21. Write to Read Max tDQSS Non Interrupting

The READ and WRITE commands are to the same devices but not necessarily to the same bank







Figure 22. Write to Read Max tDQSS Interrupting

DI n, etc. = Data In for column n, etc. 1 subsequent elements of Data In are applied in the programmed order following DI n An interrupted burst of 8 is shown, 2 data elements are written tWTR is referenced from the first positive CK edge after the last Data In Pair A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled) The READ and WRITE commands are to the same devices but not necessarily to the same bank







Figure 23. Write to Read Max tDQSS, ODD Number of Data, Interrupting

DI n = Data In for column n

An interrupted burst of 8 is shown, 1 data elements are written

tWTR is referenced from the first positive CK edge after the last Data In Pair (not the last desired Data In element)

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands are to the same devices but not necessarily to the same bank







Figure 24. Write to Precharge Max tDQSS, NON- Interrupting

DI n = Data In for column n

1 subsequent elements of Data In are applied in the programmed order following DI n A non-interrupted burst of 2 is shown

tWR is referenced from the first positive CK edge after the last Data In Pair A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)







Figure 25. Write to Precharge Max tDQSS, Interrupting

DI n = Data In for column n

An interrupted burst of 4 or 8 is shown, 2 data elements are written tWR is referenced from the first positive CK edge after the last Data In Pair A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled) *1 = can be don't care for programmed burst length of 4

*2 = for programmed burst length of 4, DQS becomes don't care at this point







Figure 26. Write to Precharge Max tDQSS ODD Number of Data Interrupting

DI n = Data In for column n

An interrupted burst of 4 or 8 is shown, 1 data element is written tWR is referenced from the first positive CK edge after the last Data In Pair A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled) *1 = can be don't care for programmed burst length of 4 *2 = for programmed burst length of 4, DQS becomes don't care at this point





Figure 27. Precharge Command



, otherwise don't care)





Figure 28. Power-Down





Figure 29. Clock Frequency Change in Precharge





Figure 30. Data input (Write) Timing



Burst Length = 4 in the case shown 3 subsequent elements of Data In are applied in the programmed order following DI n



Figure 31. Data Output (Read) Timing



Burst Length = 4 in the case shown







Figure 32. Initialize and Mode Register Sets

*=VTT is not applied directly to the device, however tVTD must be greater than or equal to zero to avoid device latch-up **=tMRD is required before any command can be applied, and 200 cycles of CK are required before any executable command can be applied The two Auto Refresh commands may be moved to follow the first MRS but precede the second PRECHARGE ALL command





Figure 33. Power Down Mode



No column accesses are allowed to be in progress at the time Power-Down is entered *=If this command is a PRECHARGE ALL (or if the device is already in the idle state) then the Power-Down mode shown is Precharge Power Down. If this command is an ACTIVE (or if at least one row is already active) then the Power-Down mode shown is active Power Down.







Figure 34. Auto Refresh Mode



* = " Don't Care", if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e., must precharge all active banks) PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH NOP commands are shown for ease of illustration; other valid commands may be possible after tRFC DM, DQ and DQS signals are all " Don't Care" /High-Z for operations shown





Figure 35. Self Refresh Mode



* = Device must be in the "All banks idle" state prior to entering Self Refresh mode ** = tXSNR is required before any non-READ command can be applied, and tXSRD (200 cycles of CK) is required before a READ command can be applied.





Figure 36. Read without Auto Precharge



Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks





Figure 37. Read with Auto Precharge



The READ command may not be issued until tRAP has been satisfied. If Fast Autoprecharge is supported, tRAP = tRCD, else the READ may not be issued prior to tRASmin - (BL*tCK/2)





Figure 38. Bank Read Access



NOP commands are shown for ease of illustration; other commands may be valid at these times

Note that tRCD > tRCD MIN so that the same timing applies if Autoprecharge is enabled (in which case tRAS would be limiting)







Figure 39. Write without Auto Precharge





Figure 40. Write with Auto Precharge

DI n = Data In from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DI n

EN AP = Enable Autoprecharge

ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other commands may be valid at these times

Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the \pm 25% window of the corresponding positive clock edge







Figure 41. Bank Write Access



Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DI n

DIS AP = Disable Autoprecharge

*=" Don't Care", if A10 is HIGH at this point

PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other commands may be valid at these times

Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the $\pm\,25\%$

window of the corresponding positive clock edge Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

Don't Care



Figure 42. Write DM Operation





Figure 43. 66 Pin TSOP II Package Outline Drawing Information Units: mm



۲.		
-	1	
	4	

Current al	Dim	Dimension in mm Dimension in inch			inch	
Symbol	Min	Nom	Max	Min	Nom	Max
А			1.2			0.047
A1	0.05		0.2	0.002		0.008
A2	0.9	1.0	1.1	0.035	0.039	0.043
b	0.22		0.45	0.009		0.018
е		0.65			0.026	
С	0.095	0.125	0.21	0.004	0.005	0.008
D	22.09	22.22	22.35	0.87	0.875	0.88
Е	10.03	10.16	10.29	0.395	0.4	0.405
HE	11.56	11.76	11.96	0.455	0.463	0.471
L	0.40	0.5	0.6	0.016	0.02	0.024
L1		0.8			0.032	
F		0.25			0.01	
θ	0 °		8°	0 °		8°
S		0.71			0.028	
QУ			0.10			0.004





Figure 44. BGA 60ball package Outline Drawing Information

Symbol	Dimension (inch)			D	imension (mr	n)
Symbol	Min	Nom	Max	Min	Nom	Max
Α			0.047			1.20
A1	0.012	0.014	0.016	0.30	0.35	0.40
A2			0.031			0.8
A3	0.005	0.007	0.009	0.13	0.18	0.23
D	0.311	0.315	0.319	7.90	8.00	8.10
Е	0.508	0.512	0.516	12.90	13.00	13.10
D1		0.252			6.40	
E1		0.433			11.00	
e1		0.039			1.00	
e2		0.031			0.80	
b	0.016	0.018	0.020	0.40	0.45	0.50
F		0.126			3.20	
SD		0.031			0.80	
SE		0.02			0.50	
D2			0.081			2.05



PART NUMBERING SYSTEM

AS4C	64M8D1	5	T/B	C/I	Ν
DRAM	64M8=64Mx8 D1=DDR1	5=200MHz	T = TSOPII B = FBGA	C=Commercial (0° C~70° C) I=Industrial (-40° C~85° C)	Indicates Pb and Halogen Free



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