

**MMS008PP3**

**Datasheet**

**DC–8 GHz GaAs MMIC SP4T Non-Reflective Switch**

Released

May 2017



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# 1 Revision History

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The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 1.0

Revision 1.0 was published in May 2017. It was the first publication of this document.

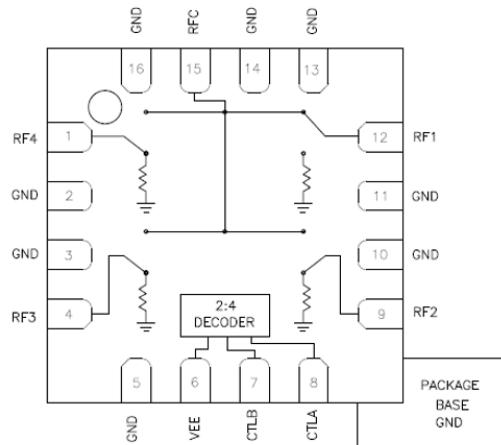
## 2 Product Overview

The MMS008PP3 device is a DC-to-8 GHz, non-reflective gallium arsenide (GaAs) pseudomorphic high-electron-mobility transistor (pHEMT) single-pole 4 throw (SP4T) monolithic microwave integrated circuit (MMIC) switch in a plastic leadless 3 mm × 3 mm surface-mount package. The switch delivers an average of 40 dB of isolation across the DC-to-8 GHz band while maintaining a low insertion loss of 1.8 dB. This switch includes an on-board binary 2:4 decoder circuit which reduces the required logic control lines. The control voltages are 0/–5 V, with a fixed bias of –5 V.

This device is also available in die form as the MMS008AA.

The following illustration shows the primary functional diagram of the MMS008PP3 device.

**Figure 1 • Functional Diagram**



### 2.1 Applications

The MMS008PP3 device is designed for the following applications:

- Test instrumentation
- Military radar, radio, EW, and ECM applications
- General purpose microwave applications

### 2.2 Key Features

The following are key features of the MMS008PP3 device:

- Non-reflective topology
- Broadband performance: DC–8 GHz
- Onboard 2:4 decoder
- Fast switching: 10 ns
- Low insertion loss: 1.5 dB at 6 GHz
- Excellent isolation: 40 dB at 6 GHz
- Compact 16-lead plastic QFN package: 3 mm × 3 mm × 0.85 mm
- High-input P1dB: 29 dBm
- High-input IP3: 44 dBm

## 3 Electrical Specifications

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This section details the electrical specifications of the MMS008PP3 device.

### 3.1 Absolute Maximum Ratings

The following table lists the absolute maximum ratings of the MMS008PP3 device.

**Table 1 • Absolute Maximum Ratings**

Parameter	Rating
Storage temperature	–65 °C to 150 °C
Operating temperature	–40 °C to 85 °C
Bias voltage range (Vee)	–7 VDC
Control voltage range (A/B)	Vee –0.5 V to +1.0 VDC
Maximum input power (low-loss state)	28 dBm
Channel temperature	150 °C
Thermal resistance (insertion loss path)	100 °C/W
Thermal resistance (terminated path)	180 °C/W
ESD sensitivity (HBM)	Class 1A

### 3.2 Specified Electrical Performance

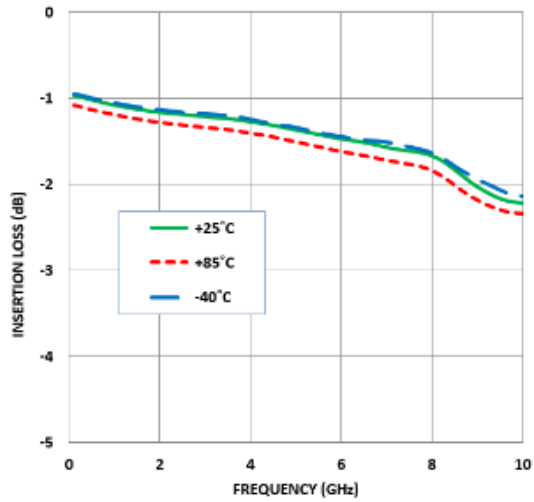
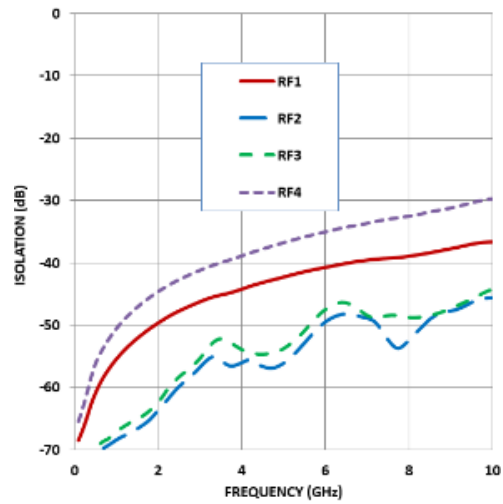
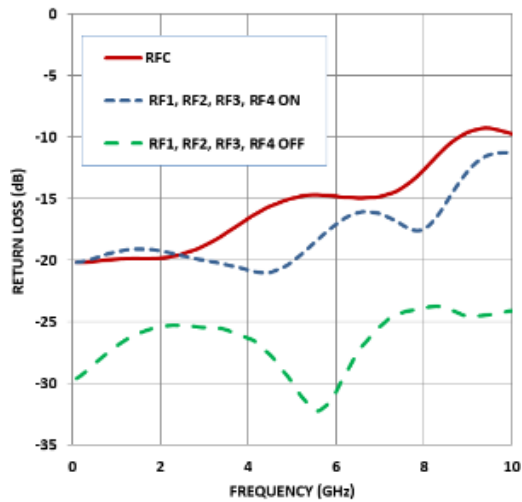
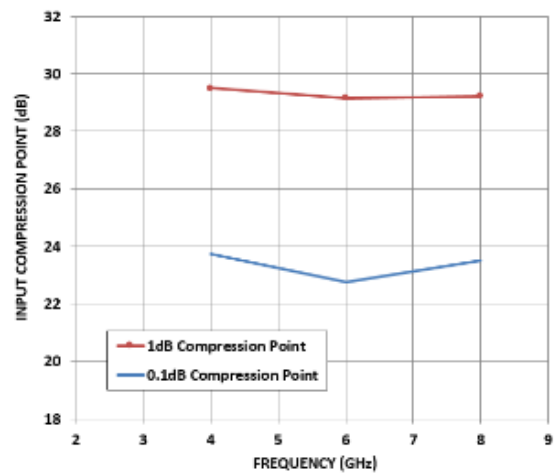
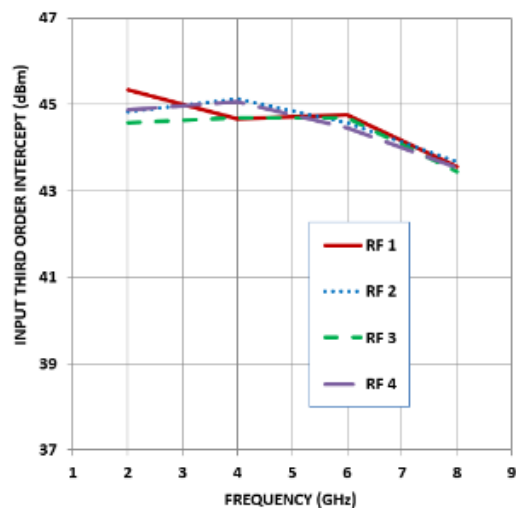
The following table lists the specified electrical performance of the MMS008PP3 device at 25 °C, where  $V_{\text{control}}$  (CTLA/CTLB) is 0 V, –5 V, and Vee is –5 V. The system is 50  $\Omega$ .

**Table 2 • Specified Electrical Performance**

Parameter	Frequency	Min	Typ	Max	Units
Operational frequency range		DC		8.0	GHz
Insertion loss	DC–2.0 GHz		1.2	2.0	dB
Insertion loss	DC–6.0 GHz		1.5	2.2	dB
Insertion loss	DC–8.0 GHz		1.7	2.5	dB
Isolation	DC–2.0 GHz	43	55		
Isolation	DC–4.0 GHz	35	48		dB
Isolation	DC–6.0 GHz	32	43		dB
Isolation	DC–8.0 GHz	30	43		dB
$T_{\text{RISE}}$ , $T_{\text{FALL}}$	DC–8.0 GHz  (10% to 90% and 90% to 10% RF)		10, 10		ns
$T_{\text{ON}}$ , $T_{\text{OFF}}$	DC–8.0 GHz  (50% control to 10/90%, and 90/10% RF)		85, 35		ns
Return loss (on state)	DC–2.0 GHz		19		dB
Return loss (on state)	DC–4.0 GHz		21		dB
Return loss (on state)	DC–6.0 GHz		17		dB
Return loss (on state)	DC–8.0 GHz		17		dB
Return loss (off state)	DC–8.0 GHz		24		dB
Input power for 0.1 dB compression	0.5 GHz–8.0 GHz		23		dBm
Input power for 1.0 dB compression	0.5 GHz–8.0 GHz		29		dBm
Input third-order intercept (IIP3)	0.5 GHz–8.0 GHz (two-tone input power, +7 dBm each tone)	40	45		dBm

### 3.3 Typical Performance Curves

This section details the typical performance curves of the MMS008PP3 device.

**Figure 2 • Insertion Loss vs. Temperature****Figure 3 • Isolation****Figure 4 • Return Loss****Figure 5 • 0.1 dB and 1 dB Input Compression Point****Figure 6 • Input Third Order Intercept Point**

### 3.4 Control Voltages

The following tables lists the control voltages of the MMS008PP3 device.

**Table 3 • Switch Control Truth**

Control Input A	Control Input B	Signal Path Condition RF Common to RF1	Signal Path Condition RF Common to RF2	Signal Path Condition RF Common to RF3	Signal Path Condition RF Common to RF4
High	High	On	Off	Off	Off
Low	High	Off	On	Off	Off
High	Low	Off	Off	On	Off
Low	Low	Off	Off	Off	On

**Table 4 • Digital Control Voltages**

State	Bias Condition
Low	–3 V to 0 V, 250 $\mu$ A typ
High	–5.0 V to –4.2 V, 0.95 $\mu$ A typ

The following table lists the bias voltage and current of the MMS008PP3 devices where the Vee range is –5.0 VDC  $\pm$ 10%.

**Table 5 • Bias Voltage and Current**

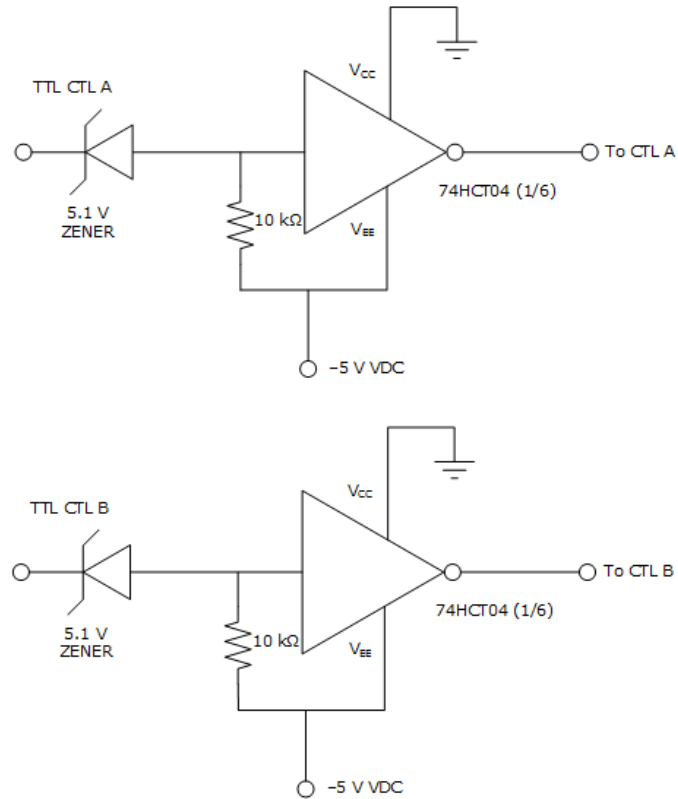
Vee	I <sub>ee</sub> (Typ)	I <sub>ee</sub> (Max)
–5.0 VDC	4.4 mA	6.0 mA



### 3.5 TTL Interface Circuit

The following image shows an example of a possible control voltage driver circuit.

**Figure 7 • Control Voltage Driver Circuit Example**



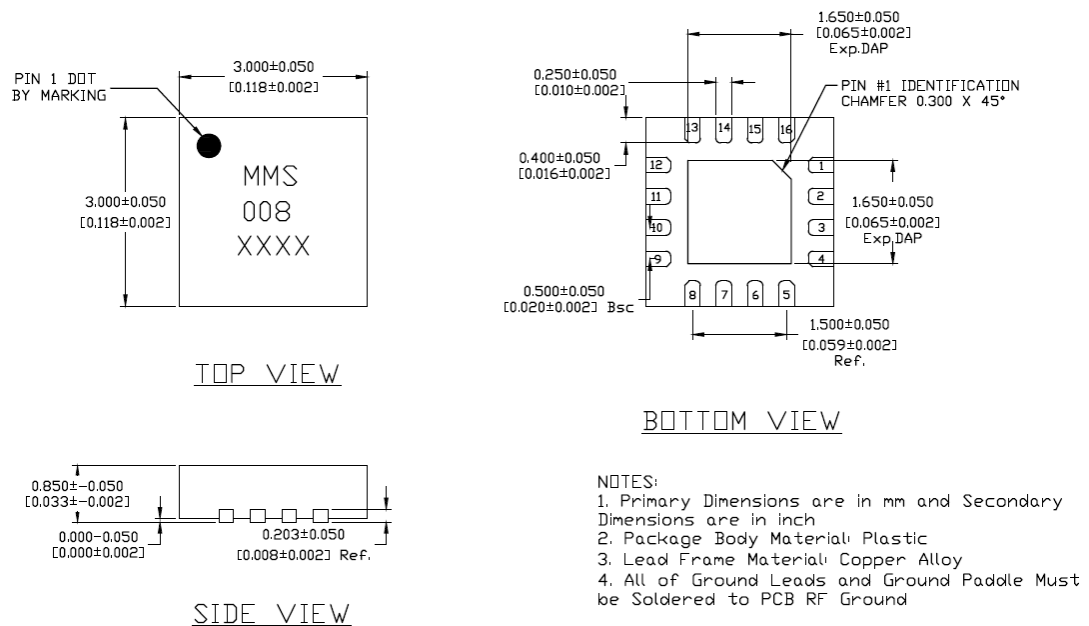
## 4 Package Outline Drawing, Package Information, and Pin Descriptions

This section details the package details of the MMS008PP3 device.

### 4.1 Package Outline

The following illustration shows the package outline of the MMS008PP3 device. Dimensions are in millimeters [inches].

**Figure 8 • Package Outline**



### 4.2 Package Information

The following table lists the package information for the MMS008PP3 device. Contact your Microsemi sales representative for additional packaging information.

**Table 6 • Package Information**

Part Number	Package body Material	Lead Finish	MSL Rating	Package Marking
MMS008PP3	Low-stress injection molded plastic	100% matte Sn	TBD	MMS 008 wwyy

## 4.3 Pin Descriptions

The following table lists the pin descriptions for the MMS008PP3 device.

**Table 7 • Pin Description Information**

Pin Number	Pin Name	Description
1, 4, 9, 12, 15	RF4, RF3, RF2, RF1, RFC	These pins are DC-coupled and matched to 50 Ω. DC-blocking capacitors are required if RF line potentials are not equal to 0 V.
2, 3, 5, 10, 11, 13, 14, 16	GND	Package bottom has exposed metal paddle that must be connected to PCB RF ground.
6	VEE	DC voltage supply: –5.0 VDC ±10%.
7	CTLB	See <a href="#">Switch Control Truth table (see page 6)</a> and <a href="#">Digital Control Voltage table (see page 6)</a> .
8	CTLA	See <a href="#">Switch Control Truth table (see page 6)</a> and <a href="#">Digital Control Voltage table (see page 6)</a> .
Backside Paddle	RF/DC GND	RF/DC ground.

## 5 Handling Recommendations

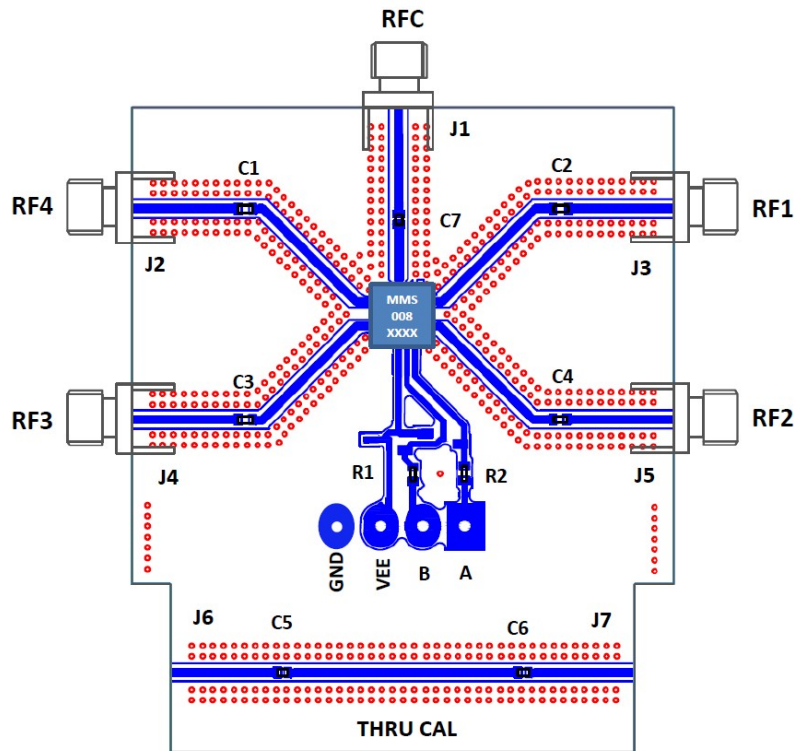
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Gallium arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note [AN01 GaAs MMIC Handling and Die Attach Recommendations](#).

## 6 Evaluation Board Information

The following image shows the evaluation board of the MMS008PP3 device.

**Figure 9 • Evaluation Board**



The circuit board used in the application should be generated with proper RF circuit design techniques. Signal lines at the RF port should have 50  $\Omega$  impedance, and the package ground leads and backside ground paddle should be connected directly to the ground plane similar to the previous image.

The following table lists the list of materials for the evaluation PCB MMS008PP3E.

**Table 8 • Materials for Evaluation PCB MMS008PP3E**

Item	Description
J1-J5	PCB mount SMA RF connector
A (CTLA), B (CTLB), VEE, GND	DC control pin
C1–C7	Zero ohm resistor, 0402package [3]
R1, R2	Zero ohm resistor, 0402 package
U1	MMS008PP3
PCB [1]	Evaluation PCB 1.29 inches × 1.55 inches

## 7 Ordering Information

The following table lists the ordering information for the MMS008PP3 device and for the MMS008PP3E evaluation PCB.

**Table 9 • Ordering Information**

Part Number	Package
MMS008PP3	3 mm × 3 mm plastic QFN package
MMS008PP3E	Evaluation board for MMS008PP3

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