NLAS54405

Low THD+N Stereo SPDT Switch with Click and Pop Elimination

The NLAS54405 is a single supply, bidirectional, dual single−pole / double−throw (SPDT) ultra-low distortion, high OFF−Isolation analog switch that can pass analog signals that are positive and negative with respect to ground. It is primarily targeted at consumer and professional audio switching applications such as computer sound cards and home theater products. The inputs can accommodate ground referenced signals up to 2 V_{RMS} while operating from a single 3.3 V or 5 V DC supply. The digital logic inputs are 1.8 V logic−compatible when using a single 3.3 V or 5 V supply. It can be used in both AC− or DC−coupled ground-referenced applications.

The NLAS54405 has a delayed turn−on feature and click/pop circuitry at each signal pin that eliminates clicks and pops associated with power−up/down conditions of the preceding amplifier outputs.

With −117 dB THD+N performance with a 2 V_{RMS} signal into 20 kΩ load, superior signal muting, high PSRR and very flat frequency response, the NLAS54405 meets the exacting requirements of consumer and professional audio engineers.

Features

- Dual SPDT Switch or 2−to−1 MUX
- Clickless Audio Switching
- 2 V_{RMS} Signal Switching from 3.3 V or 5 V Supply
- −117 dB THD+N into 20 kΩ Load at 2 V_{RMS}
- −106 dB THD+N into 32 Ω Load at 3.9 mW
- Signal to Noise Ratio: > 119 dBV
- ±0.006 dB Insertion Loss at 1 kHz, 20 kΩ Load
- ±0.002 dB Gain Variation 20 Hz to 20 kHz
- 107 dB Signal Muting into 20 kΩ Load
- 125 dB PSRR 20 Hz to 20 kHz
- Single Supply Operation: 3.3 V or 5 V
- 16−Lead WQFN Package, 1.8 mm x 2.6 mm
- This Device is Pb−Free, Halogen Free/BFR Free and is RoHS Compliant

Applications

- Computer Sound Cards
- Home Theater Audio Products
- SACD / DVD Audio
- DVD Player Audio Output Switching
- Headsets for MP3 / Cellphone Switching
- Hi−Fi Audio Switching Application

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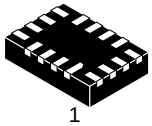

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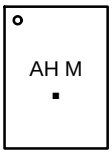
WQFN16
MT SUFFIX
CASE 488AP

MARKING DIAGRAM

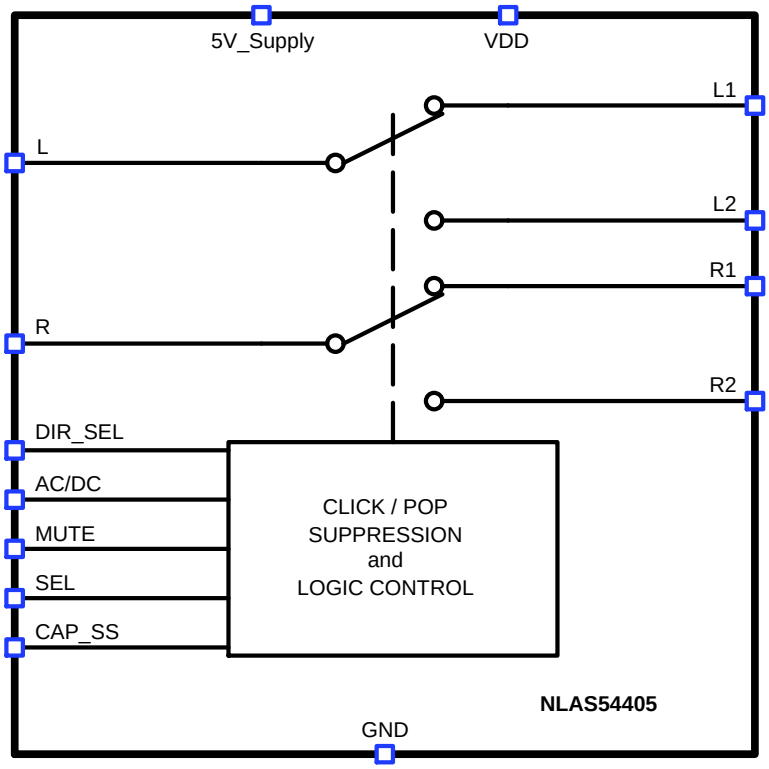


AH = Specific Device Code
M = Date Code & Assembly Location
▪ = Pb−Free Device

ORDERING INFORMATION

Device	Package	Shipping†
NLAS54405MT2TBG	WQFN16 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



For 5 V operation, connect the 5 V_Supply pin to 5 V and float the VDD pin. For 3.3 V operation, connect the VDD pin to 3.3 V and float the 5 V_Supply pin.

Figure 1. Block Diagram

Table 1. FUNCTION TABLE

Inputs				Outputs				
AC/DC	**DIR**	**MUTE**	**SEL**	**L1, R1**	**L2, R2**	**COM (L, R) C/P SHUNTS**	**L1, R1 C/P SHUNTS**	**L2, R2 C/P SHUNTS**
0	X	0	0	ON	OFF	OFF	OFF	OFF
0	X	0	1	OFF	ON	OFF	OFF	OFF
0	X	1	X	OFF	OFF	OFF	OFF	OFF
1	0	0	0	ON	OFF	OFF	OFF	ON
1	0	0	1	OFF	ON	OFF	ON	OFF
1	0	1	X	OFF	OFF	OFF	ON	ON
1	1	0	0	ON	OFF	OFF	OFF	OFF
1	1	0	1	OFF	ON	OFF	OFF	OFF
1	1	1	X	OFF	OFF	ON	OFF	OFF

NOTE: MUTE, AC/DC, DIR: Logic “0” ≤ 0.5 V, Logic “1” ≥ 1.4 V or float with a 3.3 V supply or 5 V supply.
SEL: Logic “0” ≤ 0.5 V, Logic “1” ≥ 1.4 V with a 3.3 V supply or 5 V supply.
X = Don’t Care

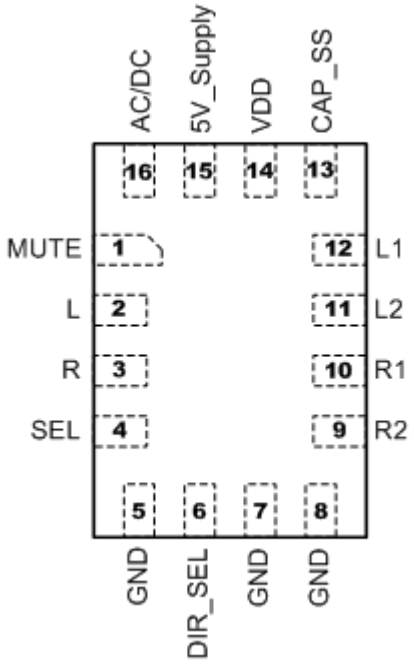


Figure 2. WQFN16 Pinout – Top View

Table 2. PIN DESCRIPTIONS

Pin Name	Pin Number	Description
VDD	14	System power supply pin (+3 V to +3.6 V) (float pin for 5 V applications)
5V_Supply	15	5 V supply pin (+4.5 V to +5.5 V) (float pin for 3.3 V applications)
GND	5, 7, 8	Ground connection
CAP_SS	13	Delayed turn−on capacitor pin
MUTE	1	Signal mute control pin
SEL	4	Input select control pin
AC/DC	16	AC/DC select control pin
DIR_SEL	6	Direction select control pin
R	3	Analog switch common pin for Right
L	2	Analog switch common pin for Left
R2, L2	9, 11	Analog switch normally open pin
R1, L1	10, 12	Analog switch normally closed pin

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{DD}	Positive 3 V DC Supply Voltage	−0.5 to +4.1	V
5V_Supply	Positive 5 V DC Supply Voltage	−0.5 to +7.0	V
V_{IS}	Analog Input/Output Voltage (L_1, L_2, R_1, R_2, L, R)	−3.1 to V_{DD} + 0.5	V
V_{IN}	Digital Select Input Voltage (SEL, MUTE, AC/DC, DIR_SEL)	−0.5 to V_{DD} + 0.5	V
I_{IO}	Switch Continuous Current (L_1, L_2, R_1, R_2, L, R)	±300	mA
I_{IO_PK}	Switch Peak Current (L_1, L_2, R_1, R_2, L, R) (Pulsed 1ms, 10% Duty Cycle, Max).	±500	mA
P_D	Power Dissipation in Still Air	800	mW
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C
T_J	Junction Bias Under Bias	150	°C
θ_{JA}	Thermal Resistance	80	°C/W
T_s	Storage Temperature	−65 to +150	°C
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 30% − 35%	UL94−V0 (0.125 in)	
ESD	ESD Protection Human Body Model Charged Device Model	> 1000 > 2000	V
I_L	Latch−up Current, Above V_{CC} and below GND at 125°C (Note 1)	±300	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Positive 3 V DC Supply Voltage	3.0	3.6	V
5V_Supply	Positive 5 V DC Supply Voltage	4.5	5.5	V
V_S	Switch Input / Output Voltage (L_1, L_2, R_1, R_2, L, R)	−2.9	V_{DD}	V
V_{IN}	Digital Select Input Voltage	GND	V_{DD}	V
T_A	Operating Temperature Range	−40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Voltages referenced to GND)
3.3 V Supply: V_{DD} = +3.0 V to +3.6 V, GND = 0 V, V_{DIR_SEL} = $V_{AC/DC}$ = GND, V_{5V_SUPPLY} = Float, V_{SIGNAL} = 2 VRMS, R_{LOAD} = 20 kΩ, f = 1 kHz, V_{SELH} = V_{MUTEH} = 1.4 V, V_{SELL} = V_{MUTEL} = 0.5 V, CAP_SS = 0.1 μF, (Note 2), Unless otherwise specified.

Parameter	Test Conditions	Supply (V)	Temp (°C)	Min (Notes 3, 4)	Typ	Max (Notes 3, 4)	Units
ANALOG SWITCH CHARACTERISTICS							
Analog Signal Range, V_{ANALOG}		3.3, 5	Full	−	2	−	V_{RMS}
ON−Resistance, r_{ON}	V_{DD} = 3.3 V, I_R or I_L = 80 mA, V_{Lx} or V_{Rx} = −2.828 V to +2.828 V (See Figure 6)	3.3	25	−	2.1	−	Ω
			Full	−	2.5	−	
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 3.3 V, I_R or I_L = 80 mA, V_{Lx} or V_{Rx} = Voltage at max r_{ON} over −2.828 V to +2.828 V (Note 7)	3.3	25	−	0.046	−	Ω
			Full	−	0.23	−	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V_{DD} = 3.3 V, I_R or I_L = 80 mA, V_{Lx} or V_{Rx} = −2.828 V, 0 V, +2.828 V (Note 5)	3.3	25	−	0.047	0.05	Ω
			Full	−	0.092	−	
L, R, Lx, Rx Pull−down Resistance	V_{DD} = 3.6 V, V_{Lx} or V_{Rx} = −2.83 V, 2.83 V, V_L or V_R = −2.83 V, 2.83 V, $V_{AC/DC}$ = 0 V, V_{MUTE} = 3.6 V, measure current, calculate resistance.	3.6	25	225	300	375	kΩ
			Full	−	345	−	
DYNAMIC CHARACTERISTICS							
THD+N	V_{SIGNAL} = 2 V_{RMS}, f = 1 kHz, A−weighted filter, R_{LOAD} = 20 kΩ	3.3, 5	25	−	< −117	−	dB
	V_{SIGNAL} = 1.9 V_{RMS}, f = 1 kHz, A−weighted filter, R_{LOAD} = 20 kΩ		25	−	< −117	−	
	V_{SIGNAL} = 1.8 V_{RMS}, f = 1 kHz, A−weighted filter, R_{LOAD} = 20 kΩ		25	−	< −117	−	
	V_{SIGNAL} = 0.707 V_{RMS}, f = 1 kHz, A−weighted filter, R_{LOAD} = 32 Ω		25	−	< −106	−	
SNR	f = 20 Hz to 20 kHz, A−weighted filter, inputs grounded, R_{LOAD} = 20 kΩ or 32 Ω	3.3, 5	25	−	> 119	−	dBV
Insertion Loss, G_{ON}	f = 1 kHz, R_{LOAD} = 20 kΩ	3.3	25	−	±0.006	−	dB
Gain vs Frequency, G_f	f = 20 Hz to 20 kHz, R_{LOAD} = 20 kΩ, reference to G_{ON} at 1 kHz	3.3	25	−	±0.002	−	dB
Stereo Channel Imbalance L_1 and R_1, L_2 and R_2	f = 20 Hz to 20 kHz, R_{LOAD} = 20 kΩ	3.3	25	−	±0.001	−	dB
OFF−Isolation (Muting)	f = 20 Hz to 22 kHz, L = R = 2 V_{RMS}, R_{LOAD} = 20 kΩ, MUTE = AC/DC = 3.3 V, DIR_SEL = GND, SEL = “X”	3.3, 5	25	−	107	−	dB
	f = 20 Hz to 22 kHz, L_1, R_1, L_2, R_2 = 2 V_{RMS}, R_{LOAD} = 20 kΩ, MUTE = AC/DC = DIR_SEL = 3.3 V, SEL = “X”		25	−	108.8	−	
	f = 20 Hz to 22 kHz, V_L or V_R = 0.7 V_{RMS}, R_{LOAD} = 32 Ω		25	−	108.5	−	

2. V_{IN} = input voltage to perform proper function.
3. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
4. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
5. Flatness is defined as the difference between maximum and minimum value of ON−resistance at the specified analog signal voltage points.
6. Limits established by characterization and are not production tested.
7. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value.
8. Crosstalk is inversely proportional to source impedance.

DC ELECTRICAL CHARACTERISTICS (Voltages referenced to GND)
3.3 V Supply: V_{DD} = +3.0 V to +3.6 V, GND = 0 V, V_{DIR_SEL} = $V_{AC/DC}$ = GND, V_{5V_SUPPLY} = Float, V_{SIGNAL} = 2 VRMS, R_{LOAD} = 20 kΩ, f = 1 kHz, V_{SELH} = V_{MUTEH} = 1.4 V, V_{SELL} = V_{MUTEL} = 0.5 V, CAP_SS = 0.1 μF, (Note 2), Unless otherwise specified.

Parameter	Test Conditions	Supply (V)	Temp (°C)	Min (Notes 3, 4)	Typ	Max (Notes 3, 4)	Units
DYNAMIC CHARACTERISTICS							
Crosstalk (Channel−to−Channel)	R_L = 20 kΩ, f = 20 Hz to 20 kHz, V_{SIGNAL} = 2 V_{RMS}, signal source impedance = 20 Ω, (Note 8)	3.3	25	−	97	−	dB
	R_L = 32 Ω, f = 20 Hz to 20 kHz, V_{SIGNAL} = 0.7 V_{RMS}, signal source impedance = 20 Ω, (Note 8)		25	−	108	−	
PSRR	f = 1 kHz, V_{SIGNAL}= 100 mV_{RMS}, inputs grounded	3.3, 5	25	−	125	−	dB
	f = 20 kHz, V_{SIGNAL}= 100 mV_{RMS}, inputs grounded		25	−	125	−	
Bandwidth, −3 dB	R_{LOAD} = 50 Ω	3.3	25	−	450	−	MHz
ON to Mute Time, $T_{TRANS-OM}$	CAP_SS = 0.1 μF	3.3	25	−	250	−	ns
Mute to ON Time, $T_{TRANS-MO}$	CAP_SS = 0.1 μF, R_{LOAD} = 32 Ω, V_{IS} = 1.5 V	3.3	25	−	1680	−	μs
Turn−ON Time, t_{ON}	V_{DD} = 3.3 V, V_{Lx} or V_{Rx} = 1.5 V, V_{MUTE} = 0 V, R_L = 32 Ω (See Figure 3)	3.3	25	−	11	−	μs
Turn−OFF Time, t_{OFF}	V_{DD} = 3.3 V, V_{Lx} or V_{Rx} = 1.5 V, V_{MUTE} = 0 V, R_L = 32 Ω (See Figure 3)	3.3	25	−	95	−	ns
Break−Before−Make Time Delay, t_D	V_{DD} = 3.6 V, V_{Lx} or V_{Rx} = 1.5 V, V_{MUTE} = 0 V, R_L = 32 Ω (See Figure 4)	3.6	25	−	10	−	μs
OFF−Isolation	R_L = 50 Ω, f = 1 MHz, V_L or V_R = 1 V_{RMS} (See Figure 5)	3.3	25	−	68	−	dB
Crosstalk (Channel−to−Channel)	R_L = 50 Ω, f = 1 MHz, V_L or V_R = 1 V_{RMS} (See Figure 7)	3.3	25	−	77	−	dB
Lx, Rx OFF Capacitance, C_{OFF}	f = 1 MHz, V_{Lx} or V_{Rx} = V_L or V_R = 0 V (See Figure 8)	3.3	25	−	3.3	−	pF
L, R ON Capacitance, $C_{COM(ON)}$	f = 1 MHz, V_{Lx} or V_{Rx} = V_{COM} = 0 V (See Figure 8)	3.3	25	−	10.5	−	pF
POWER SUPPLY CHARACTERISTICS							
Power Supply Range, V_{DD}	5V_Supply = Float	3.3	Full	3	−	3.6	V
Power Supply Range, 5V_Supply	V_{DD} = Float	5	Full	4.5	−	5.5	V
Positive Supply Current, I+	V_{DD} = +3.6 V, V_{MUTE} = 0 V,	3.6	25	−	54	65	μA
	V_{SEL} = 0 V or V_{DD}		Full	−	59	−	μA
	V_{DD} = +3.6 V, V_{MUTE} = V_{DD},	3.6	25	−	14	20	μA
	V_{SEL} = 0 V or V_{DD}		Full	−	15	−	μA
	V_{DD} = +3.6 V, V_{MUTE} = 0 V,	3.6	25	−	55	65	μA
	V_{SEL} = 1.8 V		Full	−	58	−	μA

2. V_{IN} = input voltage to perform proper function.
3. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
4. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
5. Flatness is defined as the difference between maximum and minimum value of ON−resistance at the specified analog signal voltage points.
6. Limits established by characterization and are not production tested.
7. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value.
8. Crosstalk is inversely proportional to source impedance.

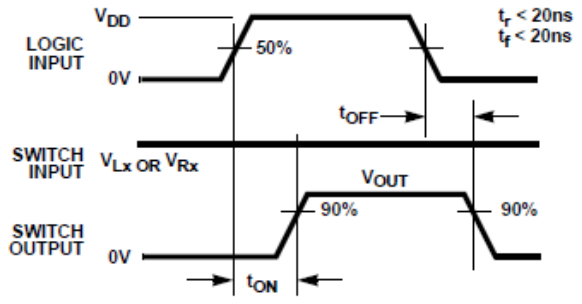
DC ELECTRICAL CHARACTERISTICS (Voltages referenced to GND)
3.3 V Supply: V_{DD} = +3.0 V to +3.6 V, GND = 0 V, V_{DIR_SEL} = $V_{AC/DC}$ = GND, V_{5V_SUPPLY} = Float, V_{SIGNAL} = 2 VRMS, R_{LOAD} = 20 kΩ, f = 1 kHz, V_{SELH} = V_{MUTEH} = 1.4 V, V_{SELL} = V_{MUTEL} = 0.5 V, CAP_SS = 0.1 μF, (Note 2), Unless otherwise specified.

Parameter	Test Conditions	Supply (V)	Temp (°C)	Min (Notes 3, 4)	Typ	Max (Notes 3, 4)	Units
DIGITAL INPUT CHARACTERISTICS							
Input Voltage Low, V_{SELL}, V_{MUTEL}		3.3, 5	Full	−	−	0.5	V
Input Voltage High, V_{SELH}, V_{MUTEH}		3.3, 5	Full	1.4	−	−	V
Input Current, I_{SELH}, I_{SELL}	V_{DD} = 3.6 V, V_{MUTE} = 0 V, V_{SEL} = 0 V or V_{DD}	3.6	Full	−0.5	0.01	0.5	μA
Input Current, $I_{AC/DCL}$, I_{DIR_SELL}	V_{DD} = 3.6 V, $V_{AC/DC}$, V_{DIR_SEL} = 0 V, V_{MUTE} = Float, V_{SEL} = V_{DD}	3.6	Full	−1.3	−0.7	0.3	μA
Input Current, $I_{AC/DCH}$, I_{DIR_SELH}	V_{DD} = 3.6 V, $V_{AC/DC}$, V_{DIR_SEL} = V_{DD}, V_{MUTE} = 0 V, V_{SEL} = 0 V	3.6	Full	−0.5	0.01	0.5	μA
Input Current, I_{MUTEL}	V_{DD} = 3.6 V, V_{SEL} = V_{DD}, V_{MUTE} = 0 V	3.6	Full	−1.3	−0.7	0.3	μA
Input Current, I_{MUTEH}	V_{DD} = 3.6 V, V_{SEL} = 0 V, V_{MUTE} = V_{DD}	3.6	Full	−0.5	0.01	0.5	μA

2. V_{IN} = input voltage to perform proper function.
3. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
4. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
5. Flatness is defined as the difference between maximum and minimum value of ON−resistance at the specified analog signal voltage points.
6. Limits established by characterization and are not production tested.
7. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value.
8. Crosstalk is inversely proportional to source impedance.

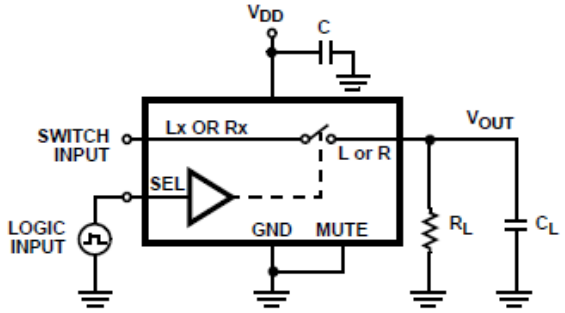
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TEST CIRCUITS AND WAVEFORMS



Logic input waveform is inverted for switches that have the opposite logic sense.

MEASUREMENT POINTS

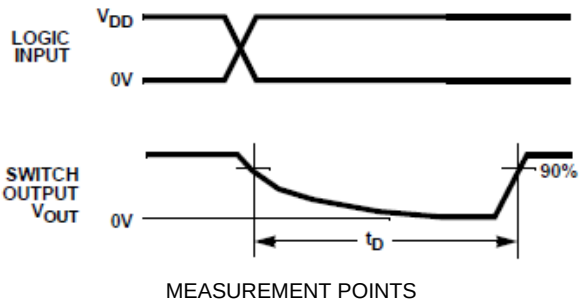


Repeat test for all switches. C_L includes fixture and stray capacitance.

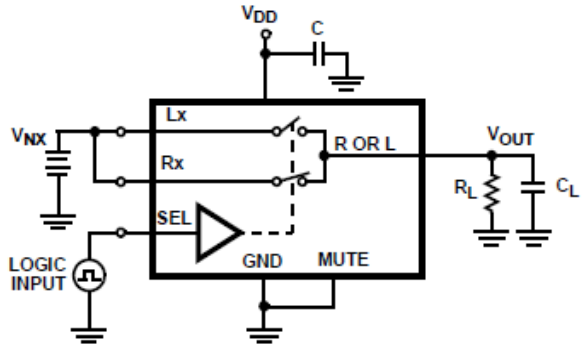
$$V_{OUT} = V_{(Lx \text{ or } Rx)} \frac{R_L}{R_L + r_{ON}}$$

TEST CIRCUIT

Figure 3. Switching Times



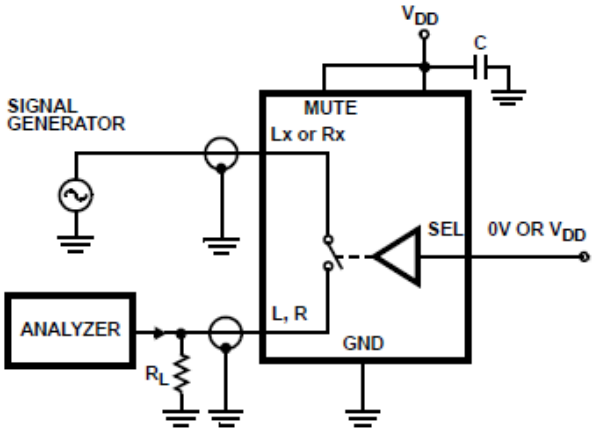
MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

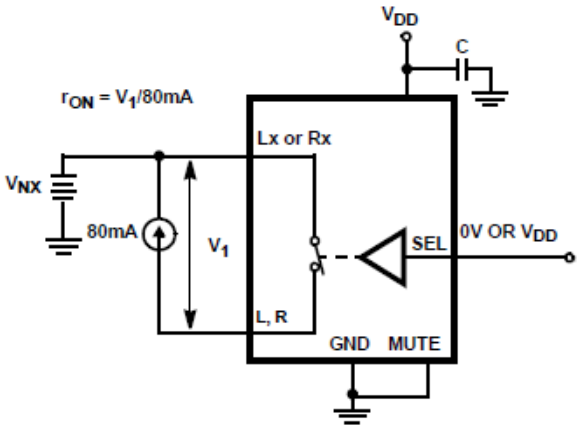
TEST CIRCUIT

Figure 4. Break−Before−Make Time



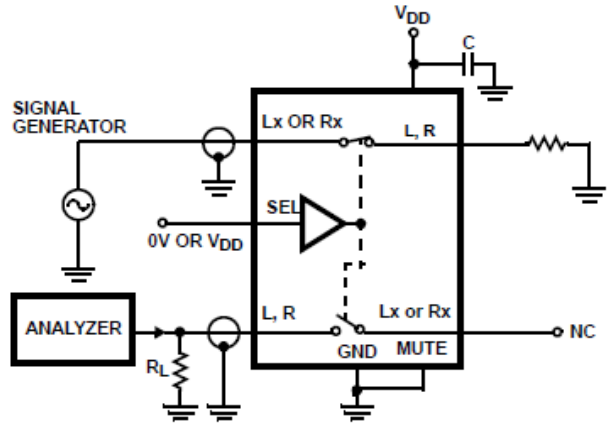
Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

Figure 5. Off−Isolation Test Circuit



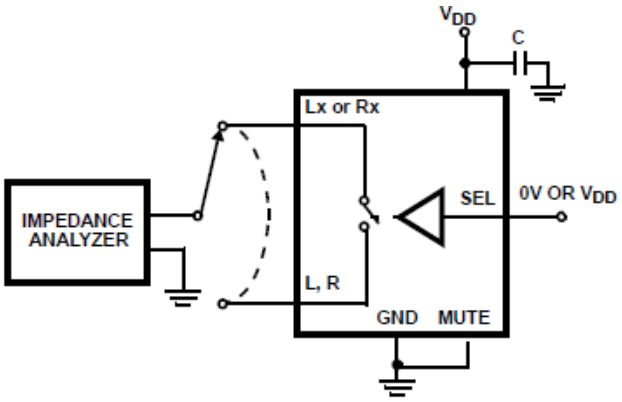
Repeat test for all switches.

Figure 6. r_{ON} Test Circuit



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

Figure 7. Crosstalk Test Circuit



Repeat test for all switches.

Figure 8. Capacitance Test Circuit

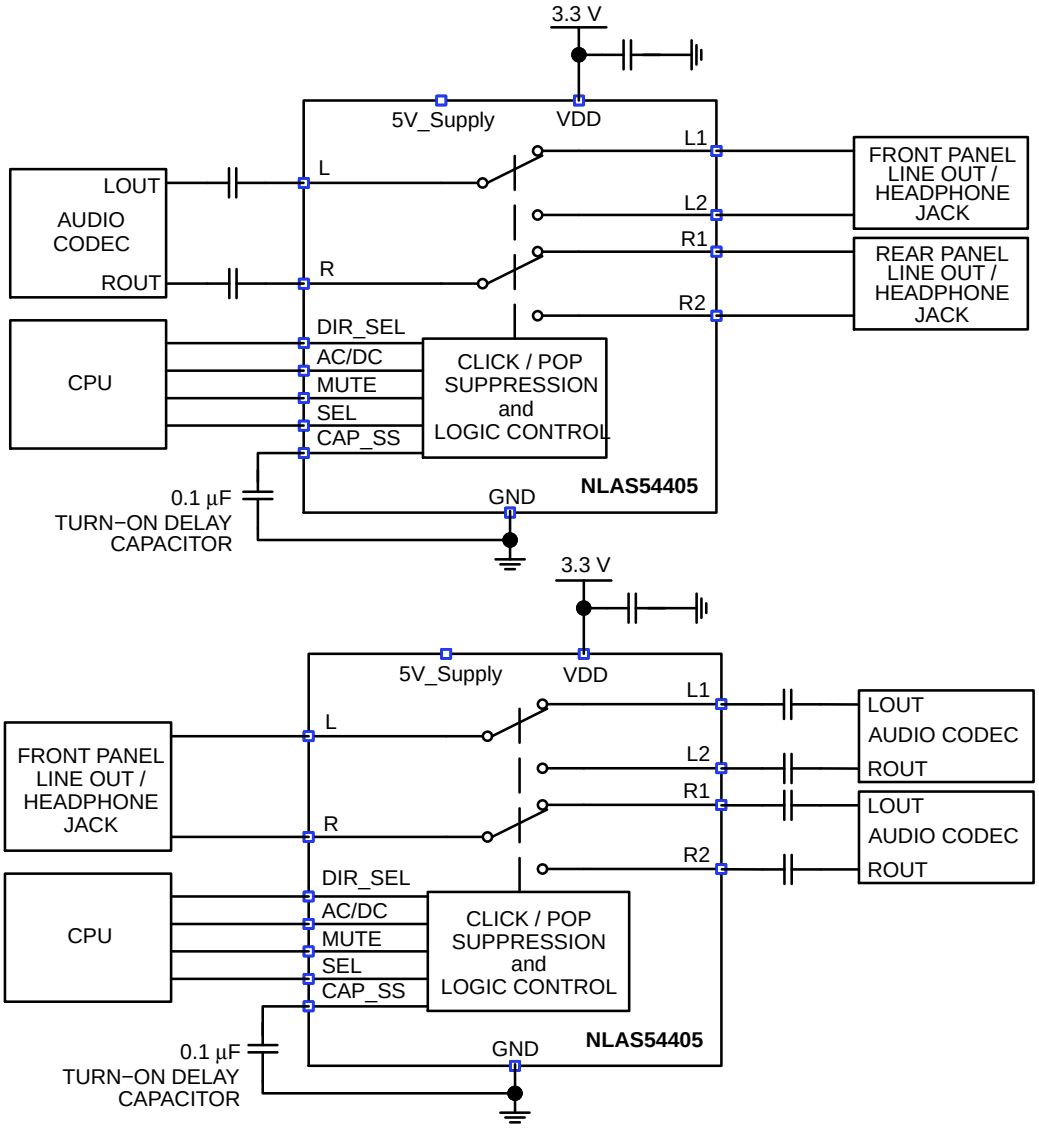


Figure 9. Sound Card AC Coupled Application Block Diagrams

Detailed Description

The NLAS54405 is a single supply, bidirectional, dual single pole/double throw (SPDT) ultra−low distortion, high OFF−Isolation analog switch. It was designed to operate from either a 3.3 V or 5 V single supply. When operated with a 3.3 V or 5 V single supply, the switches can accommodate ±2.828 V_{PEAK} (2 V_{RMS}) ground−referenced analog signals. The switch r_{ON} flatness across this range is extremely small resulting in excellent THD+N performance (0.0002% with 20 kΩ load and 0.0005% with 32 Ω load at 707 mV_{RMS}). The T−Type configuration of the switch cells prevents signals from getting through to the output when a switch is in the OFF−state providing for superior mute performance (>107 dB) in audio applications.

The NLAS54405 has special circuitry to eliminate click and pops in the speakers during power−up and power−down of the audio CODEC drivers, during removal and insertion of headphones, and while switching between sources and loads. The NLAS54405 was designed primarily for consumer and professional audio switching applications such as computer sound cards and home theater products. The “Sound Card AC Coupled Application Block Diagrams” show two typical sound card applications. In the upper block diagram, the NLAS54405 is being used to route a single stereo source to either the front or back panel line outs of the computer sound card. In the lower block diagram, the NLAS54405 is being used to multiplex two stereo sources to a single line out of the computer sound card.

SPDT Switch Cell Architecture and Performance Characteristics

The normally open (L_2, R_2) and normally closed (L_1, R_1) of the SPDT switches are T−Type switches that have a typical r_{ON} of 2.1 Ω and an OFF−isolation of > 107 dB. The low on−resistance (2.1 Ω and r_{ON} flatness (0.047 Ω) provide very low insertion loss and minimal distortion to applications that require hi−fidelity signal reproduction.

The SPDT switch cells have internal charge pumps that allow for signals to swing below ground. They were specifically designed to pass audio signals that are ground referenced and have a swing of ±2.828 V_{PEAK} while driving either 10 k / 20 kΩ (receiver) or 32 Ω (headphone) loads.

Each switch cell incorporates special circuitry to delay the switch transition from the OFF−state (high impedance) to the ON−state (2.1 Ω). This delayed turn−on may help reduce clicks and pops in the speaker by matching turn−on time to transient switching events. The delayed turn−on time is determined by the capacitor value of the delayed turn−on capacitor connected at the CAP_SS pin, the speaker load and the DC level of the audio signal. With a 0.1 μF ceramic chip capacitor, a 32 Ω load and 1.5 V DC level, the delayed turn−on is approximately 1700 μs. The delayed turn−on may be disabled by floating the CAP_SS pin.

In addition to the delayed turn−on feature of the in line switches, the part has special click and pop (C/P) shunt circuitry at each of the signal pins (L, R, L_1, L_2, R_1, and R_2). A pin’s C/P shunt circuitry is activated or deactivated depending on the logic levels applied at the AC/DC and DIR_SEL control pins. This shunt circuitry serves two functions:

1. In an AC coupled application, they are activated and directed to the source side of the switch to suppress or eliminate click/pop noise in the speaker load when powering up or down of the audio CODEC drivers.
2. For superior muting, the C/P shunt circuitry is activated and directed to the load side of the switch which gives >107 dB of OFF−Isolation when driving a 10 k / 20 kΩ receiver load with an audio signal in the range of 20 Hz to 22 kHz.

If the AC/DC pin is driven LOW, all C/P shunt circuitry at all the signal pins (L, R, L_1, R_1, L_2, and R_2) are deactivated and not operable.

If the AC/DC pin is driven HIGH, then the logic at the DIR_SEL pin will determine whether the L and R (COM) C/P shunt circuitry is activated or the L_1, L_2, R_1, and R_2 (NOx, NCx) C/P shunt circuitry is activated. When the DIR_SEL is driven LOW, the L_1, R_1, L_2, R_2 C/P shunt circuitry will be activated while the L and R C/P shunt circuitry will be deactivated. When the DIR_SEL is driven HIGH, the L and R C/P shunt circuitry will be activated while the L_1, R_1, L_2, R_2 C/P shunt circuitry will be deactivated. Note: Shunt circuitry that is activated will be turned ON when a switch cell is turned OFF and will be OFF when a switch cell is turned ON.

Supply Voltage, Signal Amplitude, and Grounding

The power supply connected at VDD or the 5 V_Supply pin provides power to the NLAS54405 part. The NLAS54405 is a single supply device that was designed to be operated with a 3.3 V ±10% DC supply connected at the VDD pin or a 5 V ±10% DC supply connected at the 5 V_Supply pin.

It was specifically designed to accept ground referenced 2 V_{RMS} (±2.828 V_{PEAK}) audio signals at its signal pins while driving either 10 k / 20 kΩ receiver loads or 32 Ω headphone loads.

When using the part in a 3.3 V application, the 5 V_Supply pin should be left floating. A 0.1 μF decoupling capacitor should be connected from the VDD pin to ground to minimize power supply noise and transients. This capacitor should be located as close to the pin as possible.

The part also has a 5 V supply pin (5 V_Supply) to allow it to be used in 5 V ±10% applications. Special circuitry within the device converts the 5 V, connected at the 5 V_Supply pin, to 3.3 V to properly power the internal circuitry of the device.

When using the part in a 5 V application, the VDD pin should be left floating. A 0.1 μF decoupling capacitor should

be connected from the 5 V_Supply pin to ground to minimize power supply noise. This capacitor should be located as close to the pin as possible.

Grounding of the NLAS54405 should follow a star configuration (see Figure 10). All grounds of the IC should be directly connected to the power supply ground return without cascading to other grounds. This configuration isolates shunt currents of the Click and Pop transients from the IC ground and optimizes device performance.

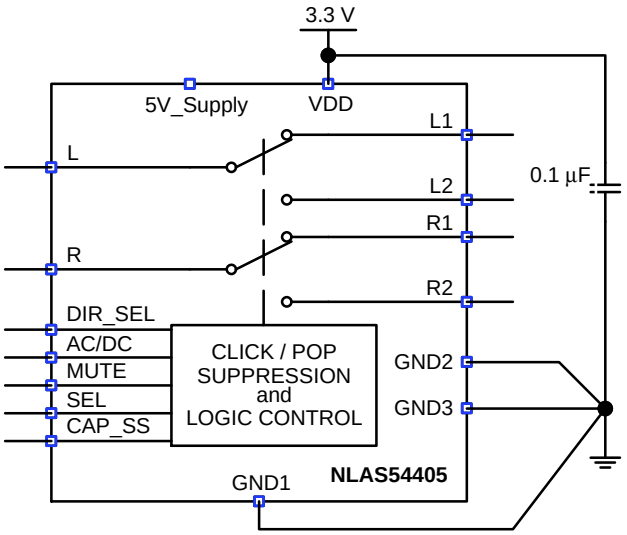


Figure 10. Star Grounding Configuration

Mute Operation

When the MUTE logic pin is driven HIGH, the part will go into the mute state. In the mute state, all switches of the SPDTs are open while the T−Shunt switches are closed. In addition, any activated click and pop shunt circuitry at the signal pins is turned on. See “Logic Control” below for more details.

Mute to On

When the MUTE pin is driven LOW, the NLAS54405 will transition to the ON−state in the following sequence:

1. All active shunt switches turn off quickly.
2. The resistance of the switches selected by the SEL pin will turn on from their high OFF−resistance to their ON−resistance of 2.1 Ω after a time delay. The delayed turn−on time is determined by the capacitor value of the delayed turn−on capacitor connected at the CAP_SS pin, the speaker load and the DC level of the audio signal. See Figures 30 and 31.

Table 3. SWITCH TURN−ON DELAY FOR A 32 Ω LOAD

Capacitor Value	V_{IS} DC Level	Turn−On Delay
No Capacitor	1.5 V	27.4 μs
0.05 μF	1.5 V	543 μs
0.1 μF	1.5 V	1680 μs
No Capacitor	60 mV	24.3 μs
0.05 μF	60 mV	38 μs
0.1 μF	60 mV	50 μs

Table 3 indicates how mute turn delay is affected by the CAP_SS capacitor value and the switch input DC voltage level.

On to Mute

When the MUTE pin is driven HIGH, the switches will turn off quickly (50 ns) and the active shunt switches will turn on quickly.

Off−Isolation in the Mute State

When in the mute state, the level of OFF−Isolation across the audio band is dependent on the signal amplitude, external loading, and location of the activated C/P (click/pop) shunt circuitry. During muting, the logic of the NLAS54405 can be configured to activate the C/P shunt circuitry on the load side of the switch or on the source side of the switch, or deactivated on both sides of the switch.

With a 0.707 V_{RMS} signal driving a 32 Ω headphone load, the location of the C/P shunt circuitry has little effect on the off−isolation performance (>109 dB of off−isolation in all configurations), see Figure 12.

With a 2 V_{RMS} signal driving a 20 kΩ amplifier load, the best OFF−Isolation is achieved by placing the C/P shunt circuitry on the load side of the switch (>120 dB across the audio band).

Note: For AC coupled applications, when powering up or down of the audio drivers, the C/P shunts should be activated on the source side of the switch. See “Click and Pop Operation”.

When using the switch for muting of the audio signal, the C/P shunt circuitry should be deactivated on the source side of the switch and directed to the load side of the switch for best possible OFF−Isolation.

Logic Control

The NLAS54405 has four logic control pins; the AC/DC, DIR_SEL, MUTE, and SEL. The MUTE and SEL control pins determine the state of the switches. The AC/DC and DIR_SEL control pins determine the location of the C/P (click/pop) shunt circuitry and if it will be active or not. See “Truth Table”.

The NLAS54405 logic is 1.8 V CMOS compatible (Low ≤ 0.5 V and High ≥ 1.4 V) over a supply range of 3.0 V to 3.6 V at the VDD pin or 4.5 V to 5.5 V at the 5 V_Supply pin. This allows control via 1.8 V or 3 V μ−controller.

SEL, Mute Control Pins

The state of the SPDT switches of the NLAS54405 device is determined by the voltage at the MUTE pin and the SEL pin. The SEL control pin is only active when MUTE is logic “0”. The MUTE has an internal pull−up resistor to the internal 3.3V supply rail and can be driven HIGH or tri−stated (floated) by the μ−processor.

These pins are 1.8 V logic compatible. When powering the part by the VDD pin, the logic voltage can be as high as the VDD voltage which is typically 3.3 V. When powering the part by the 5 V_Supply pin, the logic voltage can be as high as the 5 V_Supply voltage which is typically 5 V.

Logic Levels:

MUTE = Logic “0” (Low) when $\leq$ 0.5 V

MUTE = Logic “1” (High) when $\geq$ 1.4 V or floating

SEL = Logic “0” (Low) when $\leq$ 0.5 V

SEL = Logic “1” (High) when $\geq$ 1.4 V

AC/DC and DIR_SEL Control Pins

The NLAS54405 contains C/P (click/pop) shunt circuitry on its COM pins (L, R) and on its signal pins (L_1, R_1, L_2, R_2). The activation of this circuitry and whether it is located on the COM or signal side of the switch is determined by the logic levels applied at the AC/DC and DIR_SEL pins. The DIR_SEL control pin is only active when AC/DC is logic “1”.

Note: Any activated C/P shunt circuitry is ON when in the mute state (MUTE = Logic “1”) and OFF in the audio state (MUTE = Logic “0”).

When AC/DC is logic “0”, all of the C/P shunt circuitry on both sides of the switch is deactivated and not operable.

When AC/DC is logic “1”, then the DIR_SEL logic level determines whether the shunt circuitry will be activated on the COM side of the switch or on the signal side of the switch. When DIR_SEL = Logic “1”, the C/P shunts on the COM side (L,R) are activated and inoperable on the signal side (L_1, R_1, L_2, R_2) of the switch. When DIR_SEL = Logic “0”, the C/P shunts are activated on the signal side (L_1, R_1, L_2, R_2) and inoperable on the COM side (L, R).

Logic Levels:

AC/DC, DIR_SEL = Logic “0” (Low) when $\leq$ 0.5 V

AC/DC, DIR_SEL = Logic “1” (High) when $\geq$ 1.4 V or Floating.

The AC/DC and DIR_SEL have internal pull−up resistors to the internal 3.3 V supply rail and can be driven HIGH or tri−stated (floated by the μ−processor). They should be driven to ground for a logic “0” (Low).

Note: For 5 V applications, the AC/DC and DIR_SEL pins should never be driven to the external 5 V rail. They need to be driven with 1.8 V logic or 3 V logic circuit.

AC Coupled or DC Coupled Operation

The Audio CODEC drivers can be directly coupled to the NLAS54405 when the audio signals from the drivers are ground referenced or do not have a significant DC offset voltage, <50 mV. Otherwise, the signal should be AC coupled to the NLAS54405 part.

Click and Pop Operation

The NLAS54405 has special circuitry to eliminate click and pops in the speakers during power−up and power−down of the Audio CODEC Drivers and during removal and insertion of headphones.

A different click and pop scheme is required depending on whether the audio CODEC drivers are AC coupled or DC coupled to the inputs of the NLAS54405 part.

AC Coupled Click and Pop Operation

Single supply audio drivers have their signal biased at a DC offset voltage, usually at 1/2 the DC supply voltage of the driver. As this DC bias voltage comes up or goes down during power up or down of the driver, a transient can be coupled into the speaker load through the DC blocking capacitor (see the “Sound Card AC Coupled Application Block Diagrams”).

When a driver is off and suddenly turned on, the rapidly changing DC bias voltage at the output of the driver will cause an equal voltage at the input side of the switch due to the fact that the voltage across the blocking capacitor cannot change instantly. If the switch is in audio mode or there is no low impedance path to discharge the capacitor voltage at the input of the switch, before turning on the switch, a transient discharge will occur in the speaker, generating a click and pop noise.

Proper elimination of a click/pop transient at the speaker load while powering up or down of the audio driver requires that the NLAS54405 have its C/P shunts activated on the source side of the switch and then placed in mute mode. This allows the transient generated by the audio drivers to be discharged through the click and pop shunt circuitry.

Once the driver DC bias has reached VDD/2 and the transient on the switch side of the DC blocking capacitor has been discharged to ground through the C/P shunt circuitry, the switches can be turned on and connected through to the speaker loads without generating an undesirable click/pop in the speakers.

With a typical DC blocking capacitor of 220 μF and the C/P shunt circuitry designed to have a resistance of 40 Ω, allowing a 100 ms wait time to discharge the transient before placing the switch in the audio mode, will prevent the transient from getting through to the speaker load. See Figures 28 and 29.

Click and Pop Elimination when Connected to High Impedance Source and Load

By design, in order to flatten the R_{ON} resistance of the switch across the signal range (±3 V) a current gets added to the signal path. When the NLAS54405 part is connected to a high impedance source (i.e. AC coupled to the input of the switch) and a high impedance load, (such as the impedance of a 20 kΩ to 100 kΩ preamplifier stage) a DC offset voltage will be present on the signal line in the range of 35 mV to 135 mV.

When the switch is turned off, this offset voltage gets pulled to ground. During switching, this change in the offset voltage can cause a click and pop noise to be heard in the downstream speaker.

Placing a 1 kΩ resistor from the output of the switch to ground will lower the offset voltage to around 1.5 mV, thereby effectively eliminating the click and pop noise. The 1 kΩ resistor is small enough to reduce the voltage offset significantly while not increasing power dissipation

dramatically. Power consumption will need to be considered when using a smaller impedance under this scenario.

When connected to a low impedance load such as headphones (32 Ω), the current added to the signal line results in a minimal DC offset voltage on the signal line and does not cause click and pop noise when the switch is turned off.

DC Coupled Click and Pop Operation

The NLAS54405 can pass ground−referenced audio signals which allows it to be directly connected to audio drivers that output ground−referenced audio signals, eliminating the need for a DC blocking capacitor.

Audio drivers that swing around ground, however, do generate some DC offset, from a few millivolts to tens of millivolts. When switching between audio channels or muting the audio signal, these small DC offset levels of the drivers can generate a transient that can cause unwanted clicks and pops in the speaker loads.

In a DC coupled application, the C/P shunt resistors placed at the source side of the switch have no effect in eliminating the transients at the speaker loads when transitioning in and out of the mute state or switching between channels. In fact, having these C/P shunts active on the source side unnecessarily increases the power consumption. So, for DC coupled connection, the C/P shunt circuitry should not be applied at the source (driver) side of the switch.

For DC coupled applications, the NLAS54405 has a special turn−on delay feature that delays the connection from the audio driver output to the speaker load when turning on a switch channel. The delayed turn−on time is determined by the capacitor value of the delayed turn−on capacitor connected at the CAP_SS pin, the speaker load and the DC level of the audio signal.

The turn−on delay may help reduce clicks and pops in the speaker by matching turn−on time to transient switching events. A delayed turn−on capacitor value of 0.1 μF, coupled with a 32 Ω load and a 1.5 V DC level, provides a turn−on delayed of approximately 1700 μs. See Figures 30 and 31. See “MUTE to ON” section for more detail of how turn−on delay works.

Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes or diode stacks from the pin to VDD and to GND (see Figure 11). To prevent forward biasing these diodes, VDD must be applied before any input signals, and the signal voltages must remain between VDD and −3 V and the logic voltage must remain between VDD and ground.

If these conditions cannot be guaranteed, then precautions must be implemented to prohibit the current and voltage at the logic pin and signal pins from exceeding the maximum ratings of the switch. The following two methods can be used to provided additional protection to limit the current in the event that the voltage at a signal pin goes below ground by more than −3 V or above the VDD rail and the logic pin goes below ground or above the VDD rail.

Logic inputs can be protected by adding a 1 kΩ resistor in series with the logic input (see Figure 11). The resistor limits the input current below the threshold that produces permanent damage, and the sub−microamp input current produces an insignificant voltage drop during normal operation.

This method is not acceptable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low r_{ON} switch. Connecting Schottky diodes to the signal pins, as shown in Figure 11 will shunt the fault current to the supply or to ground thereby protecting the switch. These Schottky diodes must be sized to handle the expected fault current and to clamp when the voltage reaches the overvoltage limit.

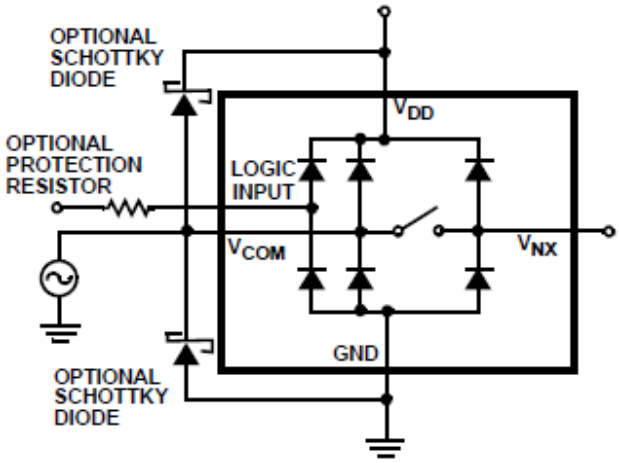


Figure 11. Overvoltage Protection

High−Frequency Performance

In 50 Ω systems, the NLAS54405 has a −3 dB bandwidth of 450 MHz (see Figure 32). The frequency response is very consistent over varying analog signal levels.

An OFF−switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feed−through from a switch’s input to its output. OFF−Isolation is the resistance to this feed−through, while crosstalk indicates the amount of feed−through from one switch to another. Figure 33 details the high OFF−Isolation and crosstalk rejection provided by this part. At 1 MHz, Off−Isolation is about 68 dB in 50 Ω systems, decreasing approximately 20 dB per decade as frequency increases. Higher load impedances decrease OFF−Isolation and crosstalk rejection due to the voltage divider action of the switch off impedance and the load impedance.

TYPICAL CHARACTERISTICS

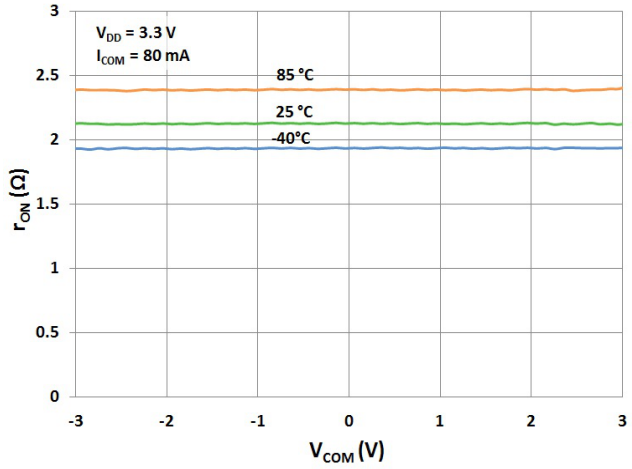


Figure 12. On−Resistance vs. Switch Voltage

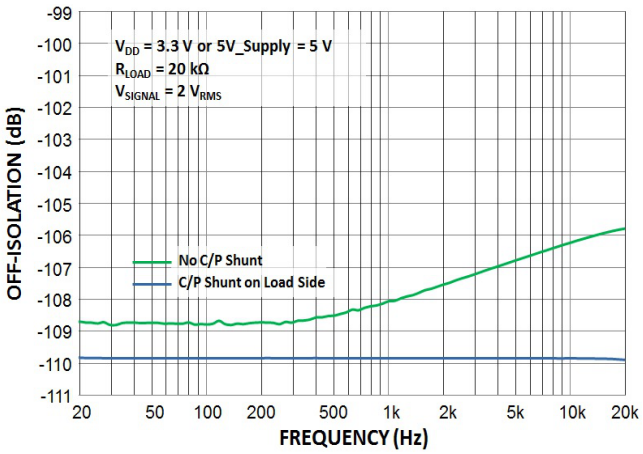


Figure 13. Off−Isolation, 2 V_{RMS} Signal, 20 kΩ Load

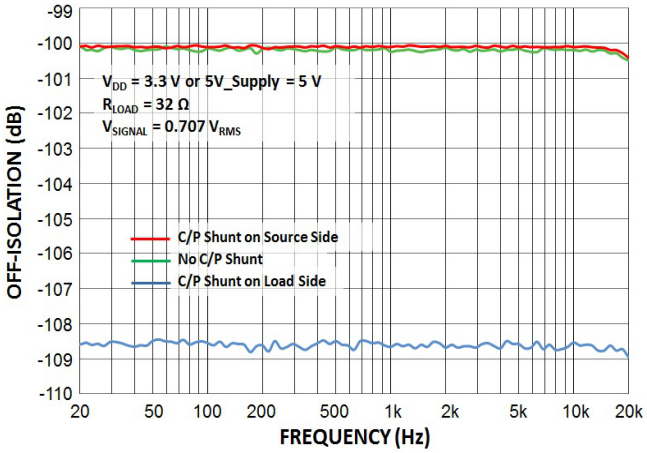


Figure 14. Off−Isolation, 0.707 V_{RMS} Signal, 32 Ω Load

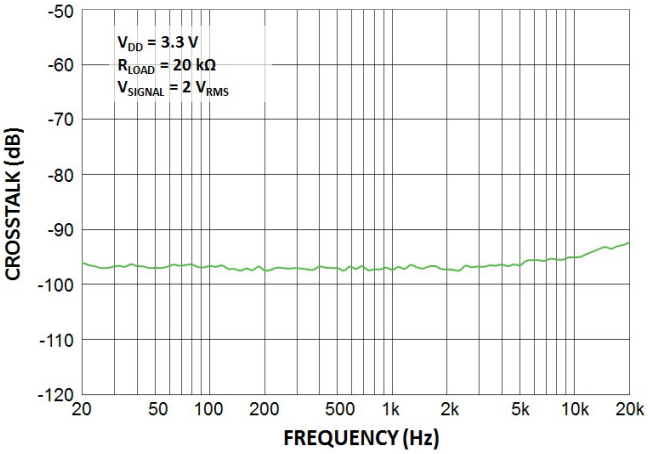


Figure 15. Channel−to−Channel Crosstalk

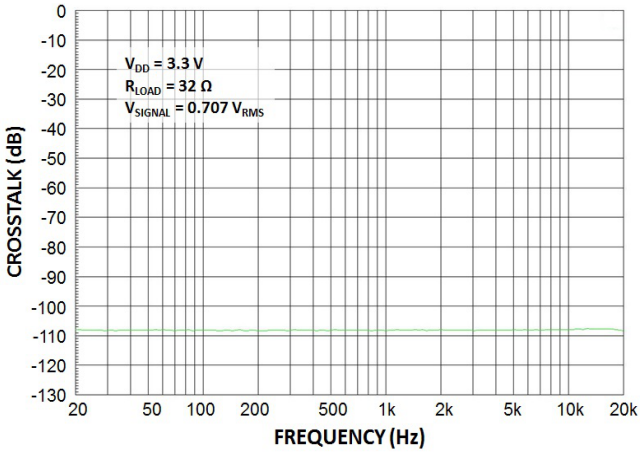


Figure 16. Channel−to−Channel Crosstalk

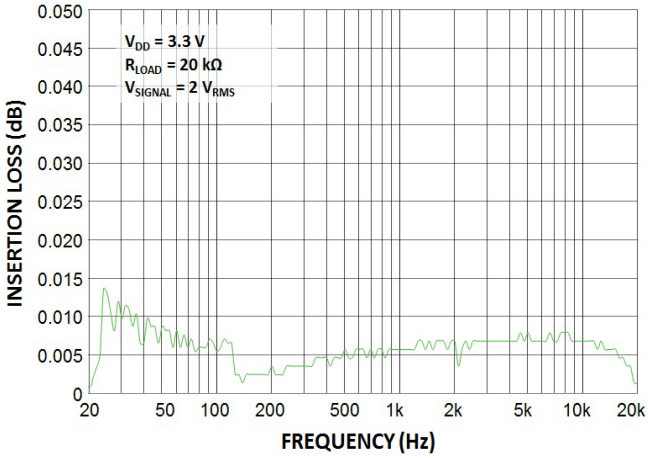


Figure 17. Insertion Loss vs. Frequency

TYPICAL CHARACTERISTICS

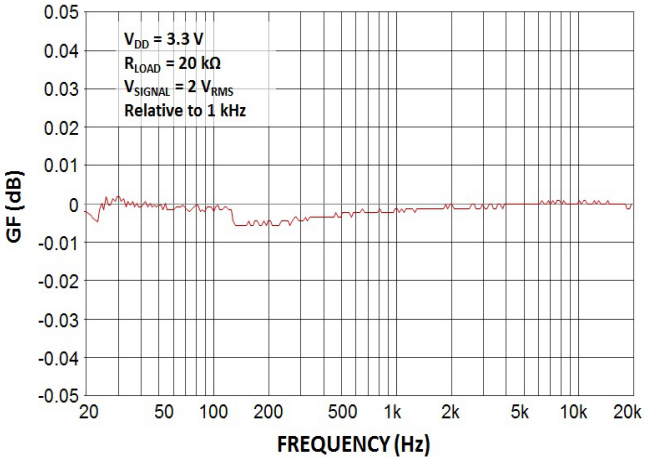


Figure 18. Gain vs. Frequency

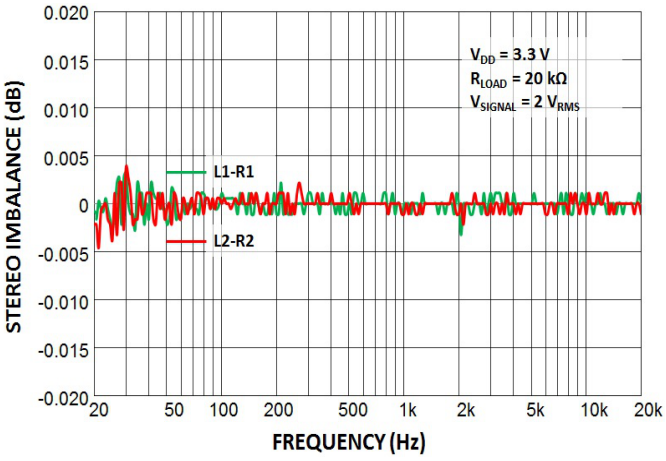


Figure 19. Stereo Imbalance vs. Frequency

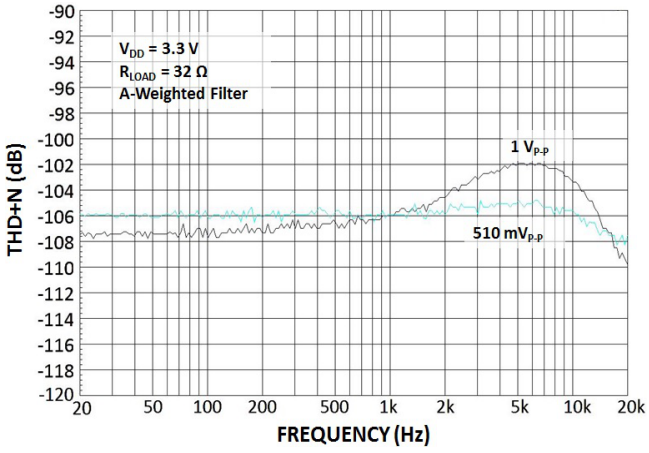


Figure 20. THD+N vs. Signal Levels vs. Frequency

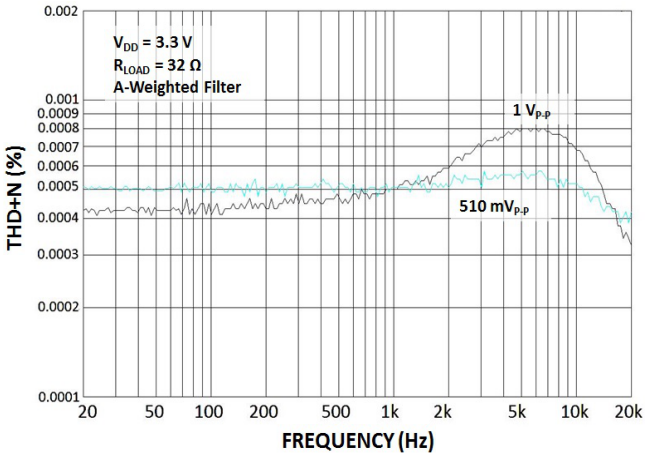


Figure 21. THD+N vs. Signal Levels vs. Frequency

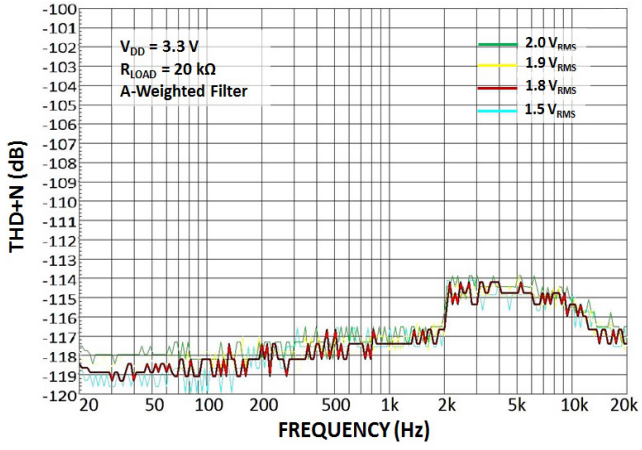


Figure 22. THD+N vs. Signal Levels vs. Frequency

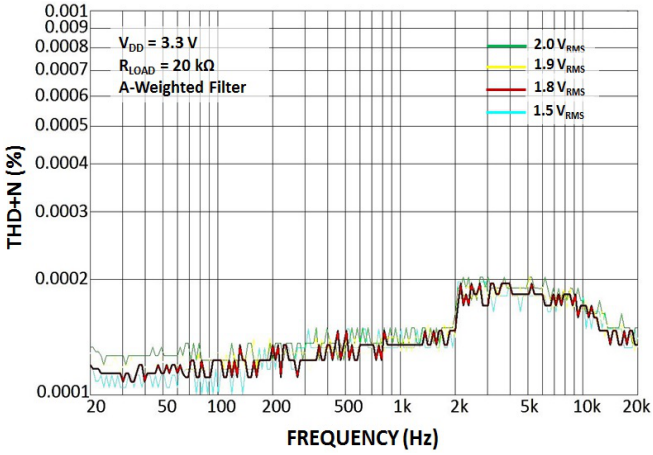


Figure 23. THD+N vs. Signal Levels vs. Frequency

TYPICAL CHARACTERISTICS

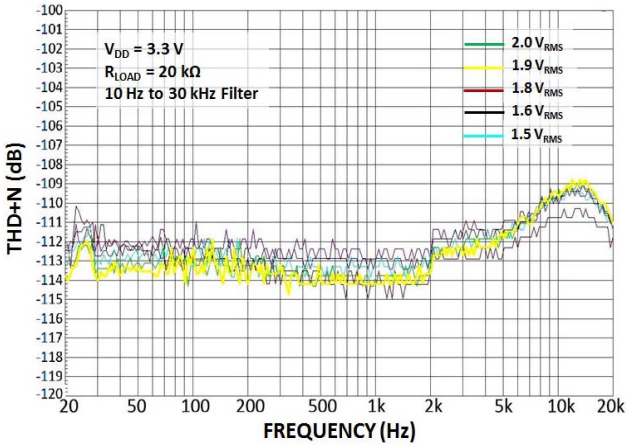


Figure 24. THD+N vs. Signal Levels vs. Frequency

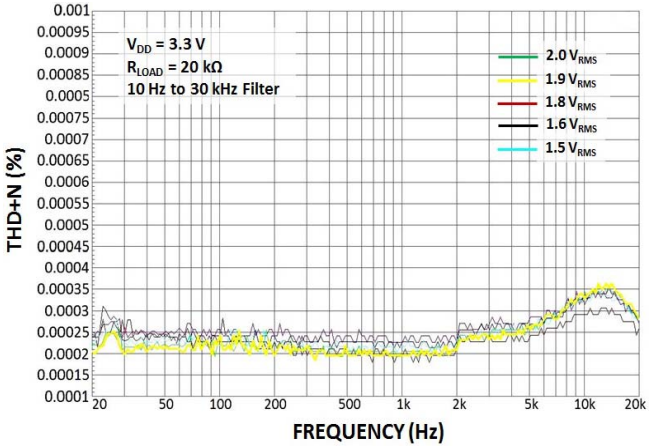


Figure 25. THD+N vs. Signal Levels vs. Frequency

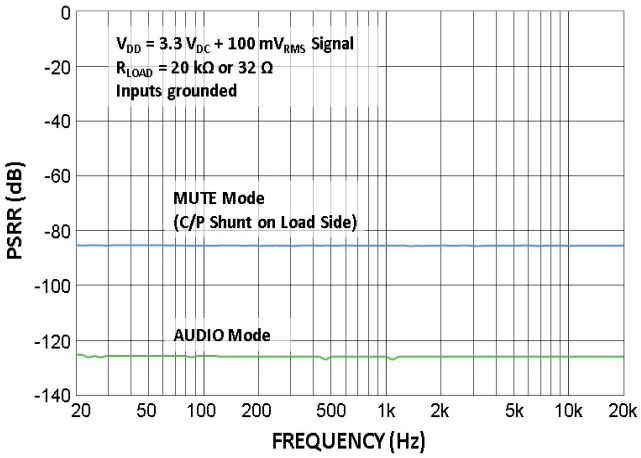


Figure 26. PSRR vs. Frequency

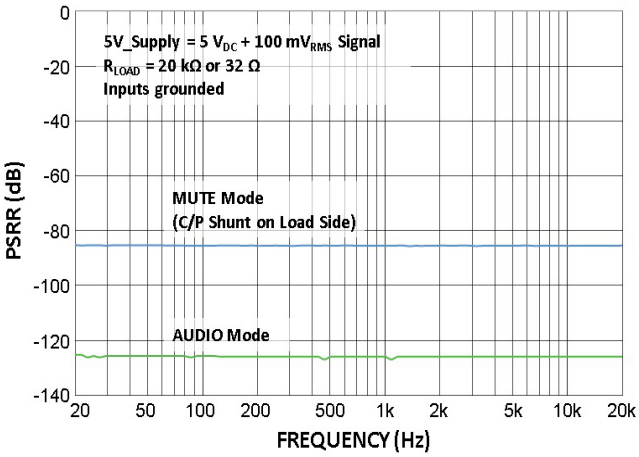


Figure 27. PSRR vs. Frequency

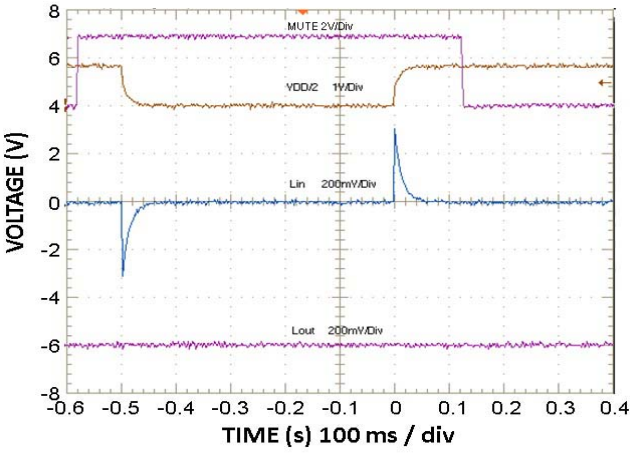


Figure 28. 20 kΩ AC Coupled Click / Pop Reduction

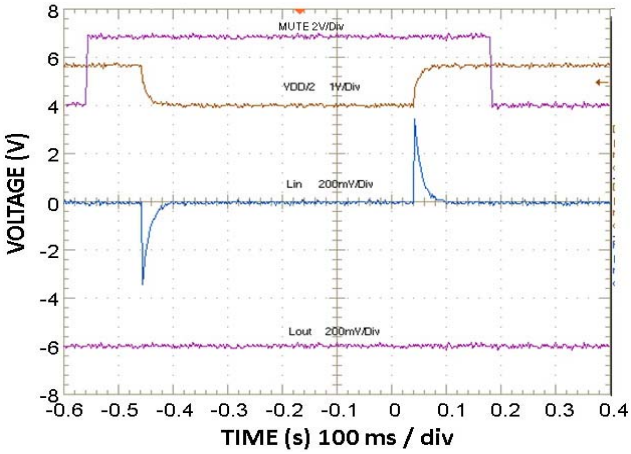


Figure 29. 32 Ω AC Coupled Click / Pop Reduction

TYPICAL CHARACTERISTICS

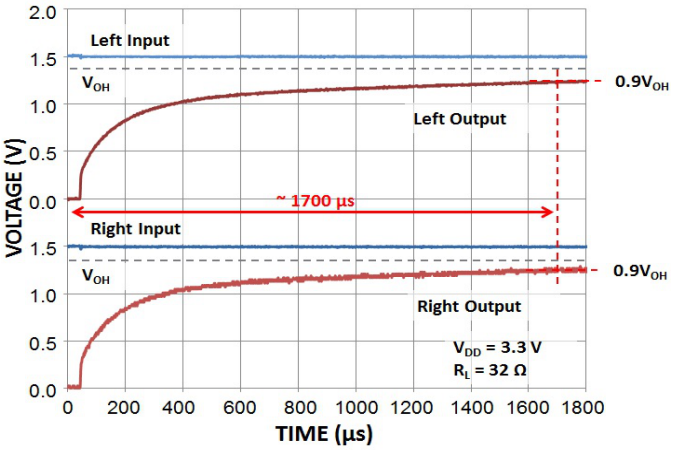


Figure 30. Turn−on Delay (0.1 µF) Click/Pop Reduction

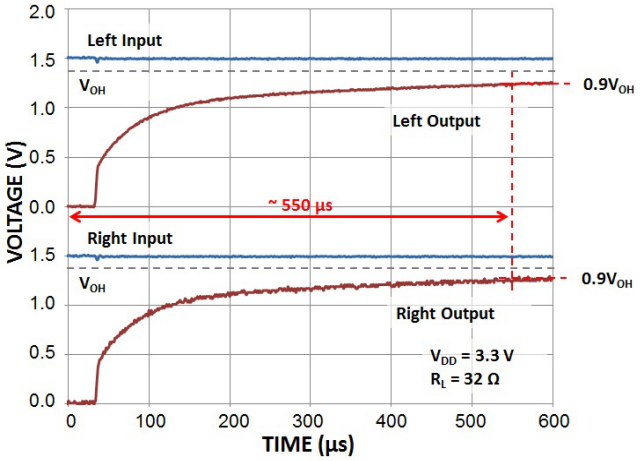


Figure 31. Turn−on Delay (0.05 µF) Click/Pop Reduction

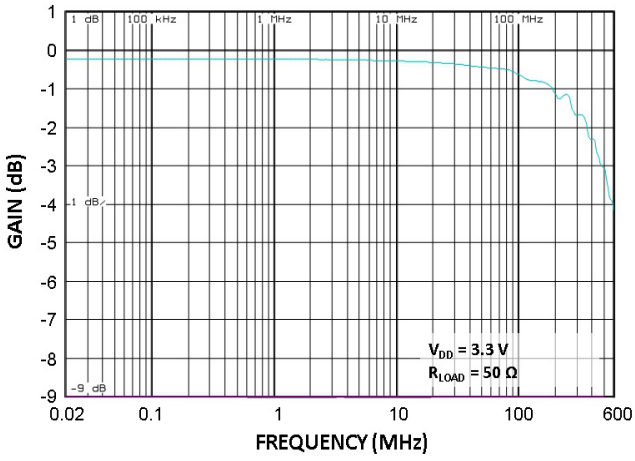


Figure 32. Frequency Response

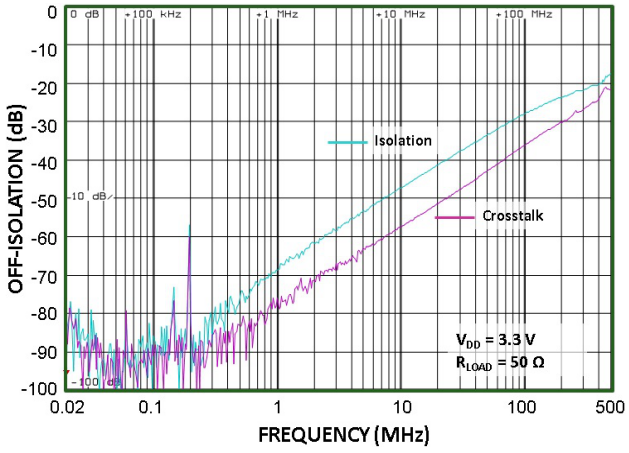
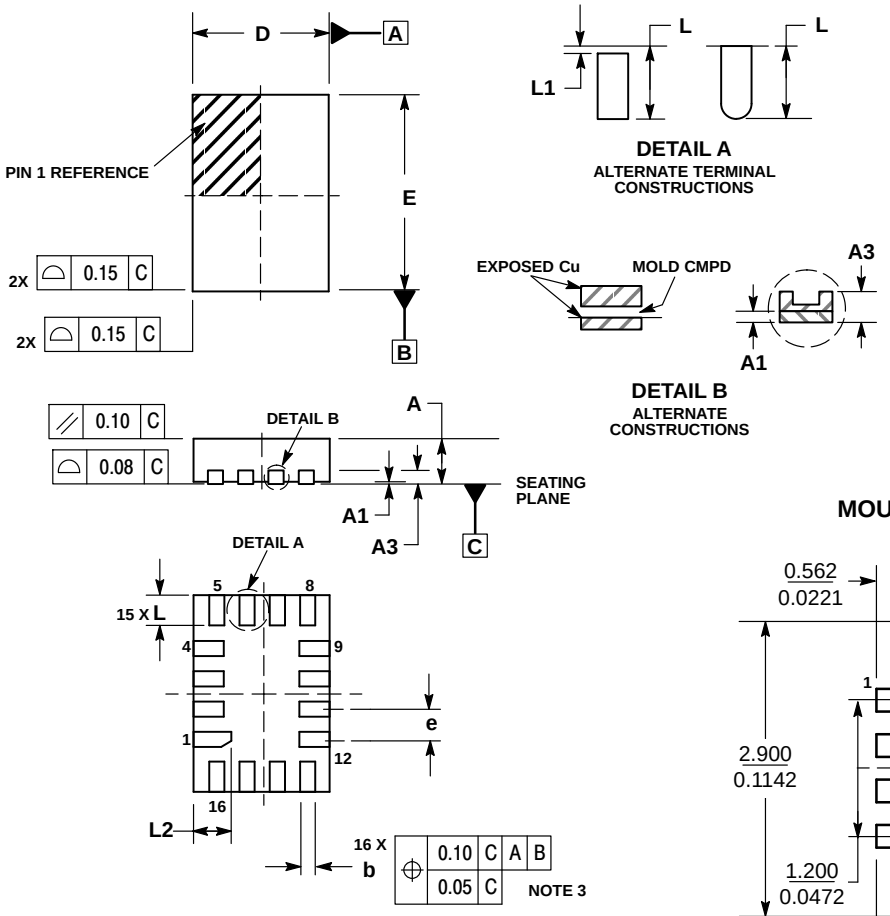


Figure 33. Crosstalk and Off−Isolation

PACKAGE DIMENSIONS

WQFN16, 1.8x2.6, 0.4P
CASE 488AP
ISSUE B



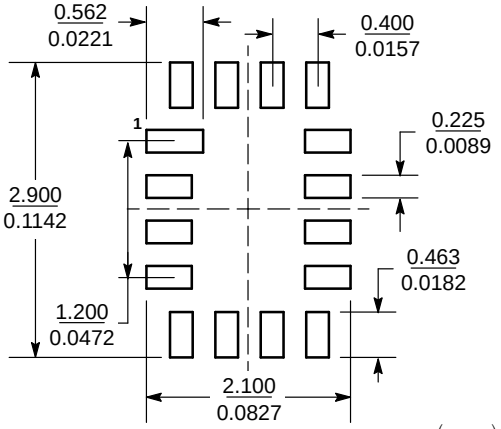
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

DETAIL B
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. EXPOSED PADS CONNECTED TO DIE FLAG. USED AS TEST CONTACTS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.050
A3	0.20 REF	
b	0.15	0.25
D	1.80 BSC	
E	2.60 BSC	
e	0.40 BSC	
L	0.30	0.50
L1	0.00	0.15
L2	0.40	0.60

MOUNTING FOOTPRINT*



SCALE 20:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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