

# Dual Slot Hot Swap Controller for PCI Express

## FEATURES

- Allows Live Insertion into PCI Express® Backplane
- Controls Two Independent PCI Express Slots
- Independent Control of Main and Auxiliary Supplies
- 20V Rating for 12V Supply Input Pins
- Integrated 0.25Ω AUX Switches
- Limits Fault Current in  $\leq 1\mu\text{s}$
- Force On Test Mode
- Adjustable Supply Voltage Power-Up Rate
- High Side Drivers for N-Channel MOSFETs
- Thermal Shutdown Protection
- Available in 38-Lead QFN and 36-Lead SSOP Packages

## APPLICATIONS

- PCI Express-Based PC and Servers
- Hot Swap Application for Triple Supply Systems

## DESCRIPTION

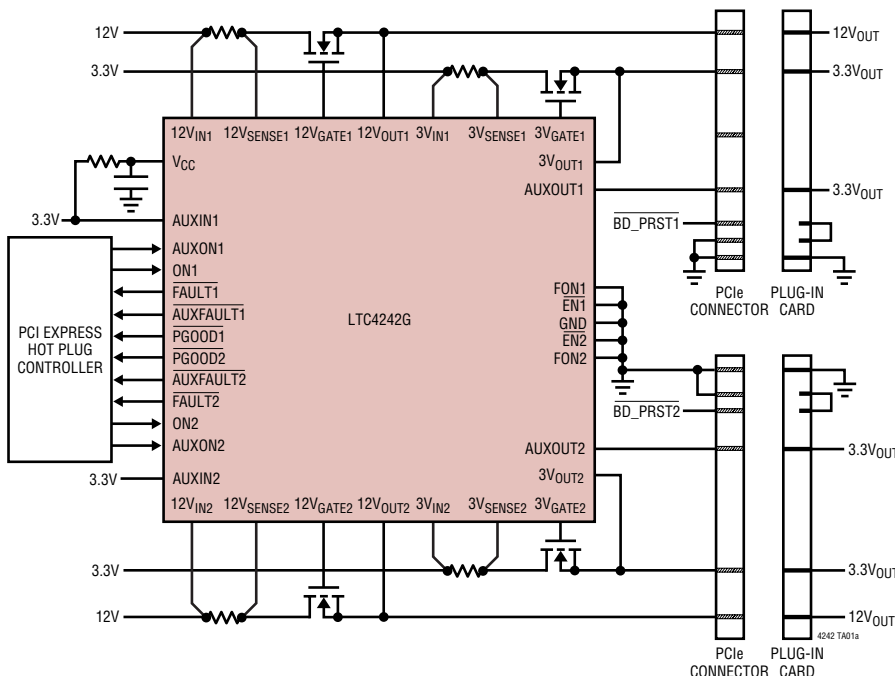
The LTC®4242 Hot Swap™ controller allows safe board insertion and removal for two independent slots on a PCI Express backplane. External N-channel transistors control the 12V and 3.3V supplies while integrated switches control the 3.3V auxiliary supplies. Both 12V and 3.3V supplies can be ramped up at an adjustable rate. Dual level circuit breakers and fast active current limiting protect all supplies against overcurrent faults.

A supply filter at the  $V_{CC}$  pin allows the LTC4242 to endure supply transients. The  $\overline{\text{EN}}$  input detects the presence of a card in the PCI Express slot. The  $\overline{\text{FAULT}}$  and  $\overline{\text{AUXFAULT}}$  outputs alert the system of overcurrent conditions on the main and auxiliary supplies, respectively.  $\overline{\text{PGOOD}}$  and  $\overline{\text{AUXPGOOD}}$  outputs indicate proper main and auxiliary supply outputs.

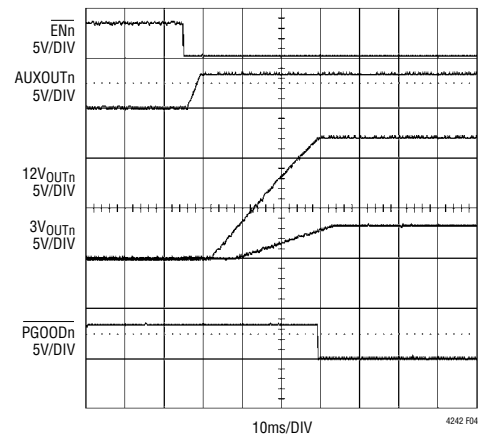
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## TYPICAL APPLICATION

PCI Express Application



Normal Power-Up Sequence



# LTC4242

## ABSOLUTE MAXIMUM RATINGS (Note 1)

### Supply Voltages

$V_{CC}$ .....	-0.3V to 7V
$12V_{INn}$ .....	-0.3V to 20V
$3V_{INn}$ .....	-0.3V to 10V
AUXINn.....	-0.3V to 10V

### Input Voltages

$ONn$ , AUXONn, FONn.....	-0.3V to 7V
ENn.....	-0.3V to 7V

### Output Voltages

$FAULTn$ , $PGOODn$ , $AUXFAULTn$ , AUXPGOODn.....	-0.3V to 7V
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### Analog Voltages

$12V_{SENSEn}$ .....	-0.3V to 20V
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$12V_{GATEn}$ .....	-0.3V to 25V
$12V_{OUTn}$ (Note 3) .. $12V_{GATEn} - 5V$ to $12V_{GATEn} + 0.3V$	
AUXOUTn, $3V_{SENSEn}$ .....	-0.3V to 10V
$3V_{GATEn}$ .....	-0.3V to 14V
$3V_{OUTn}$ (Note 3) .....	$3V_{GATEn} - 5V$ to $3V_{GATEn} + 0.3V$

### Operating Temperature Range

LTC4242C.....	0°C to 70°C
LTC4242I.....	-40°C to 85°C

### Storage Temperature Range

SSOP.....	-65°C to 150°C
QFN.....	-65°C to 125°C

### Lead Temperature (Soldering, 10 sec)

SSOP.....	300°C
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## PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>G PACKAGE 36-LEAD PLASTIC SSOP <math>T_{JMAX} = 125^{\circ}C</math>, <math>\theta_{JA} = 95^{\circ}C/W</math></p>	<p>TOP VIEW</p> <p>UHF PACKAGE 38-LEAD (5mm x 7mm) PLASTIC QFN <math>T_{JMAX} = 125^{\circ}C</math>, <math>\theta_{JA} = 34^{\circ}C/W</math> EXPOSED PAD (PIN 39) IS GND, PCB ELECTRICAL CONNECTION OPTIONAL</p>	
<p>ORDER PART NUMBER</p>	<p>ORDER PART NUMBER</p>	<p>UHF PART MARKING*</p>
<p>LTC4242CG LTC4242IG</p>	<p>LTC4242CUHF LTC4242IUHF</p>	<p>4242 4242</p>

**Order Options** Tape and Reel: Add #TR  
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF  
Lead Free Part Marking: <http://www.linear.com/leadfree/>

\*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for parts specified with wider operating temperature ranges.

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = V_{AUXINn} = V_{3VINn} = 3.3\text{V}$ ,  $V_{12VINn} = 12\text{V}$ , unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Supplies</b>							
$V_{IN}$	Operating Voltage	$V_{CC}$	●	2.7		6.0	V
		$12V_{INn}$	●	10.1		14.4	V
		$3V_{INn}$	●	3.0		6.0	V
		AUXINn	●	3.0		6.0	V
$I_{DD}$	Input Supply Current	$V_{AUXONn} = 2\text{V}$ , $V_{ONn} = 2\text{V}$	●		1.6	4	mA
		$V_{CC}$	●		0.5	1	mA
		$3V_{INn}$	●		0.35	1	mA
$V_{UVL}$	Supply Undervoltage Lockout	$V_{CC}$ Rising	●	2.3	2.45	2.6	V
		$12V_{INn}$ Rising	●	9.48	9.78	10.08	V
		$3V_{INn}$ Rising	●	2.57	2.67	2.77	V
		AUXINn Rising	●	2.57	2.67	2.77	V
$\Delta V_{LKO(HYST)}$	Supply Undervoltage Lockout Hysteresis	$V_{CC}$	●	30	100	200	mV
		$12V_{INn}$	●	90	130	170	mV
		$3V_{INn}$	●	20	35	50	mV
		AUXINn	●	20	35	50	mV
<b>Current Limit</b>							
$\Delta V_{SENSE(CB)}$	Circuit Breaker Trip Sense Voltage	$12V_{INn} - 12V_{SENSEn}$	●	45	50	55	mV
		$3V_{INn} - 3V_{SENSEn}$	●	45	50	55	mV
$\Delta V_{SENSE(ACL)}$	Active Current Limit Sense Voltage	$12V_{INn} - 12V_{SENSEn}$	●	75	100	125	mV
		$3V_{INn} - 3V_{SENSEn}$	●	75	100	125	mV
$I_{CBAUX}$	Circuit Breaking Current for AUX Supply		●	385	550	715	mA
$t_{CB}$	Circuit Breaker Response Time		●	10	20	40	$\mu\text{s}$
<b>Switch Resistance</b>							
$R_{AUX}$	Internal Switch Resistance $R_{AUX} = (V_{AUXINn} - V_{AUXOUTn})/I$	(Note 4) $I = 375\text{mA}$	●		0.25	0.4	$\Omega$
<b>External Gate Drive</b>							
$I_{GATE(UP)}$	External N-Channel Gate Pull-Up Current	Gate Drive On	●	-5	-9	-13	$\mu\text{A}$
		$V_{12VGATEn} = 1\text{V}$ $V_{3VGATEn} = 1\text{V}$	●	-5	-9	-13	$\mu\text{A}$
$I_{GATE(DN)}$	External N-Channel Gate Pull-Down Current	Gate Drive Off	●	0.5	1	2	mA
		$V_{12VGATEn} = 17\text{V}$ , $V_{12VOUTn} = 12\text{V}$ $V_{3VGATEn} = 8.3\text{V}$ , $V_{3VOUTn} = 3.3\text{V}$	●	0.5	1	2	mA
$I_{GATE(FPD)}$	External N-Channel Gate Fast Pull-Down Current	Fast Turn Off	●	150	250	400	mA
		$V_{12VGATEn} = 17\text{V}$ , $V_{12VOUTn} = 12\text{V}$ $V_{3VGATEn} = 8.3\text{V}$ , $V_{3VOUTn} = 3.3\text{V}$	●	150	250	400	mA
$\Delta V_{GATE}$	External N-Channel Gate Drive $12V_{GATEn} - 12V_{OUTn}$ $3V_{GATEn} - 3V_{OUTn}$	$I_{GATE} = 1\mu\text{A}$ (Note 3)	●	4.5	5.5	7.9	V
			●	4.5	5.5	7.9	V
<b>Input Pins</b>							
$V_{PG(TH)}$	Power Good Threshold Voltage	$12V_{OUTn}$ Falling	●	10.08	10.38	10.68	V
		$3V_{OUTn}$ Falling	●	2.772	2.855	2.937	V
		AUXOUTn Falling (Note 5)	●	2.772	2.855	2.937	V
$V_{PG(HYST)}$	Power Good Hysteresis	$12V_{OUTn}$	●	20	70	110	mV
		$3V_{OUTn}$	●	5	20	30	mV
		AUXOUTn (Note 5)	●	5	20	30	mV

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = V_{AUXINn} = V_{3VINn} = 3.3\text{V}$ ,  $V_{12VINn} = 12\text{V}$ , unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{ON(TH)}$	ONn, AUXONn Pin Threshold Voltage	Rising Edge	●	1.173	1.235	1.297	V
$\Delta V_{ON(TH)}$	ONn, AUXONn Pin Hysteresis		●	30	70	120	mV
$V_{ON(RTH)}$	ONn, AUXONn Pin Reset Threshold Voltage	Falling Edge	●	0.5	0.6	0.7	V
$I_{ON(IN)}$	ONn, AUXONn Pin Input Current	$V_{ONn} = V_{AUXONn} = 1.2\text{V}$	●			$\pm 1$	$\mu\text{A}$
$V_{\overline{EN}(TH)}$	$\overline{EN}n$ Pin Threshold Voltage	$\overline{EN}n$ Rising	●	1.173	1.235	1.297	V
$\Delta V_{\overline{EN}(HYST)}$	$\overline{EN}n$ Pin Hysteresis		●	30	70	120	mV
$I_{\overline{EN}(UP)}$	$\overline{EN}n$ Pull-Up Current	$V_{\overline{EN}n} = 1\text{V}$	●	-5	-9	-13	$\mu\text{A}$
$V_{FON}$	FONn Pin Logic Threshold		●	0.7		2.6	V
$I_{SENSE}$	SENSE Pin Input Current $12V_{SENSEn}$ $3V_{SENSEn}$	$V_{12VSENSEn} = 12\text{V}$	●		40	100	$\mu\text{A}$
		$V_{3VSENSEn} = 3.3\text{V}$	●		40	100	$\mu\text{A}$
$I_{OUT}$	OUT Pin Input Current $12V_{OUTn}$ $3V_{OUTn}$	Gate Drive On $V_{12VOUTn} = 12\text{V}$	●		45	90	$\mu\text{A}$
		$V_{3VOUTn} = 3.3\text{V}$	●		27	60	$\mu\text{A}$
$R_{OUT(DIS)}$	OUT Pin Discharge Resistance $12V_{OUTn}$ $3V_{OUTn}$ AUXOUTn	Gate Drive Off $V_{12VOUTn} = 6\text{V}$	●	350	700	1400	$\Omega$
		$V_{3VOUTn} = 2\text{V}$	●	165	330	660	$\Omega$
		$V_{AUXOUTn} = 2\text{V}$	●	375	750	1500	$\Omega$

### Output Pins

$V_{OL}$	Output Low Voltage $\overline{FAULTn}$ , $\overline{AUXFAULTn}$ , $\overline{PGOODn}$ , $\overline{AUXPGOODn}$ (Note 5)	$I_{PIN} = 3\text{mA}$	●		0.14	0.4	V
$I_{PU}$	Pull-Up Current $\overline{FAULTn}$ , $\overline{AUXFAULTn}$ , $\overline{PGOODn}$ , $\overline{AUXPGOODn}$ (Note 5)	$V_{PIN} = 1.5\text{V}$	●	-5	-9	-13	$\mu\text{A}$

### Slew Rate

$SR_{AUXOUT}$	AUXOUTn Slew Rate		●		1.25	1.7	V/ms
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### Delays

$t_{PLH(GATE)}$	Input High (ONn) to GATEs High Prop Delay		●		7	14	$\mu\text{s}$
$t_{PLH(UVL)}$	Input Supply Low ( $12V_{INn}$ , $3V_{INn}$ ) to GATEs Low Prop Delay		●		18	36	$\mu\text{s}$
$t_{PLH(PG)}$	Out Low ( $12V_{OUTn}$ , $3V_{OUTn}$ ) to $\overline{PGOOD}$ High Prop Delay		●		20	40	$\mu\text{s}$
$t_{PHL(SENSE)}$	Sense Voltage High to GATE Low	$\Delta V_{SENSE} = 200\text{mV}$ , $C_{GATE} = 10\text{nF}$	●		0.4	1	$\mu\text{s}$

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All current into device pins is positive, all current out of the device pins is negative. All voltages are referenced to GND unless otherwise specified.

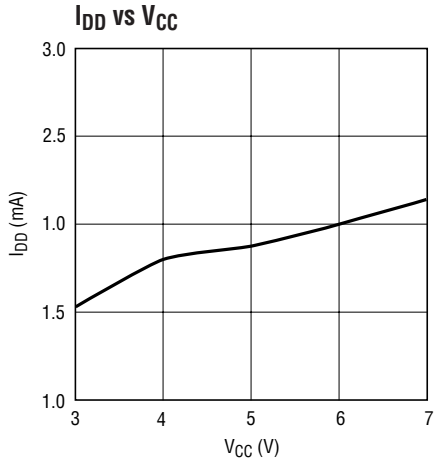
**Note 3:** An internal clamp limits the GATE pins to a minimum of 5V above  $V_{OUT}$ . Driving this pin to voltages beyond the clamp may damage the device.

**Note 4:** For the QFN package, the AUX FET on resistance is guaranteed by correlation to wafer level measurements.

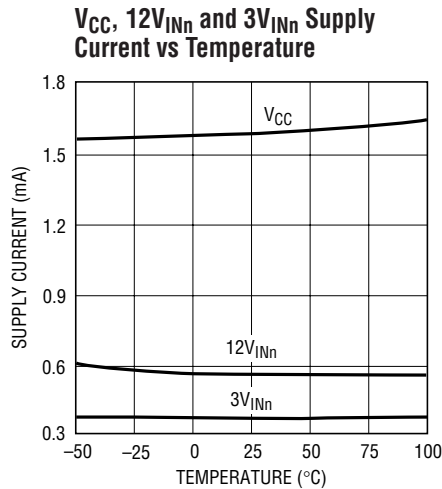
**Note 5:** Available on QFN package only.

# TYPICAL PERFORMANCE CHARACTERISTICS

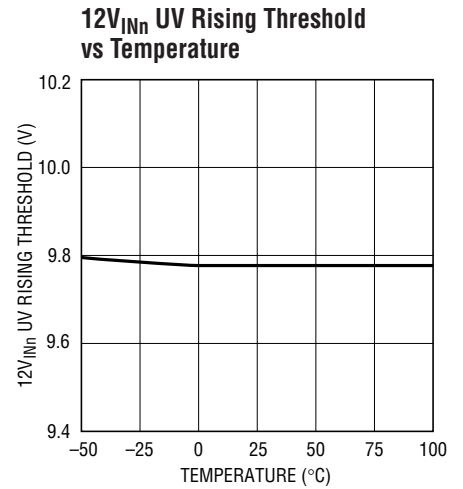
$T_A = 25^\circ\text{C}$ .  $V_{CC} = V_{AUXINn} = V_{3VINn} = 3.3\text{V}$ ,  $V_{12VINn} = 12\text{V}$ , unless otherwise noted. (Note 2)



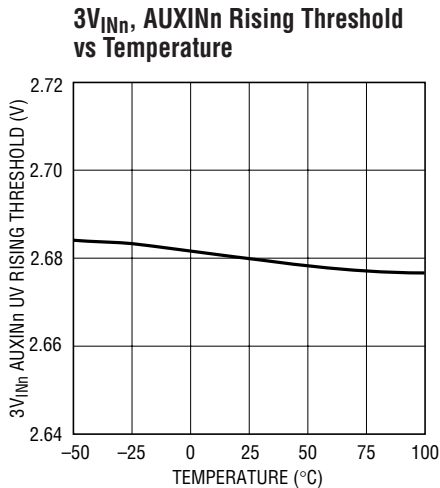
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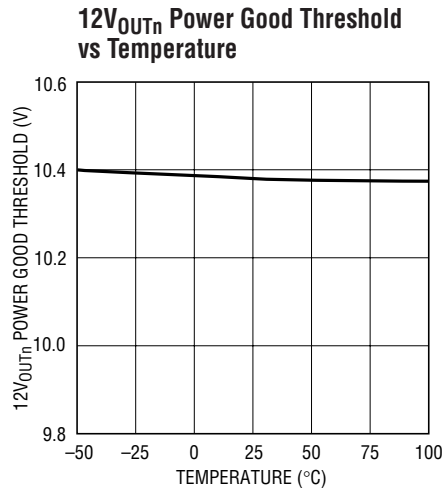
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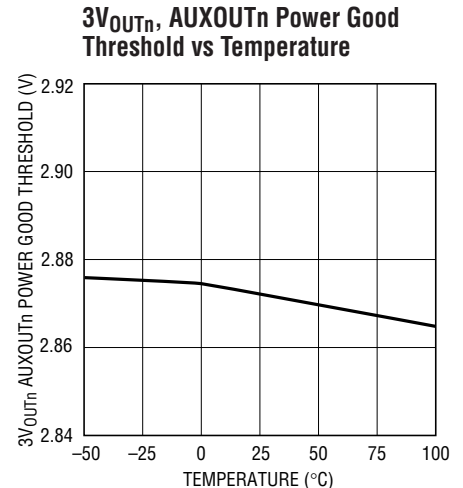
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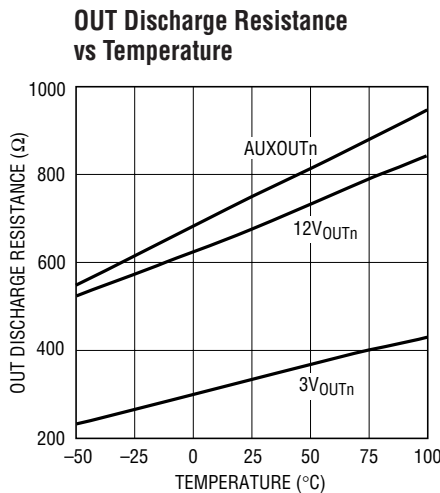
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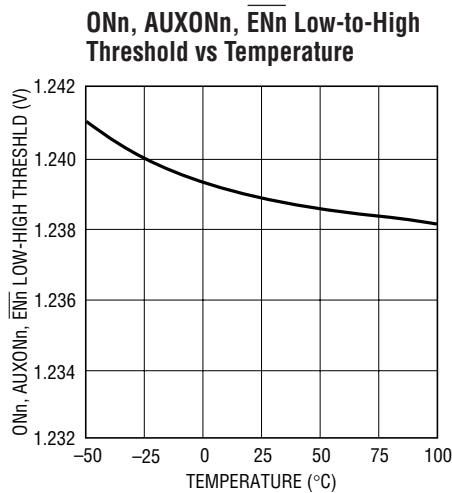
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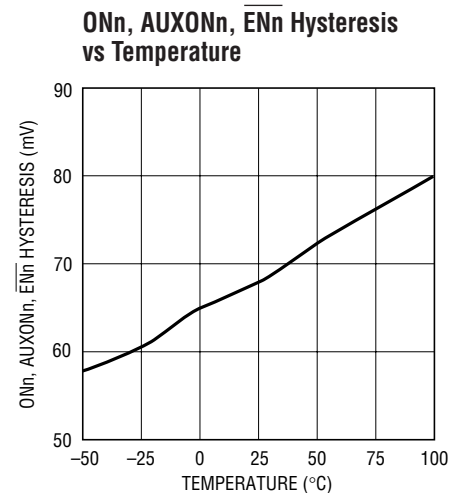
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4242 G07



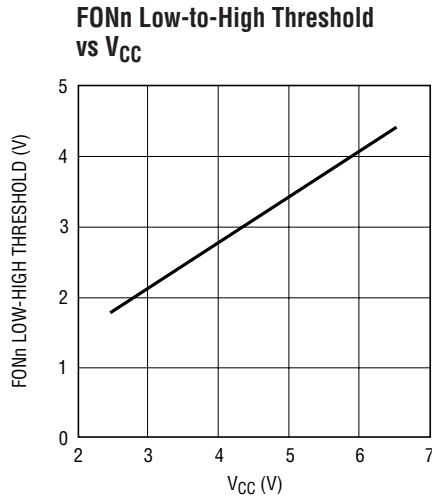
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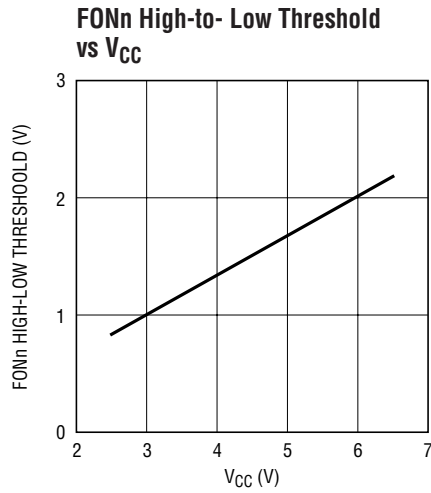
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## TYPICAL PERFORMANCE CHARACTERISTICS

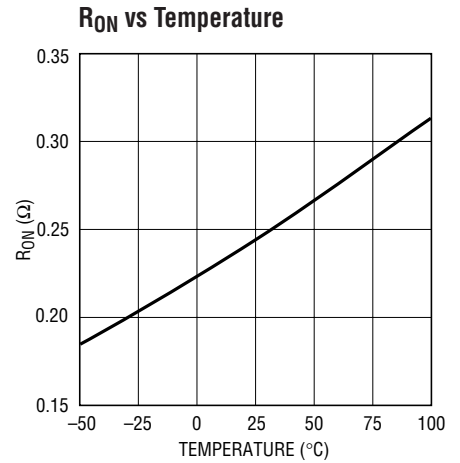
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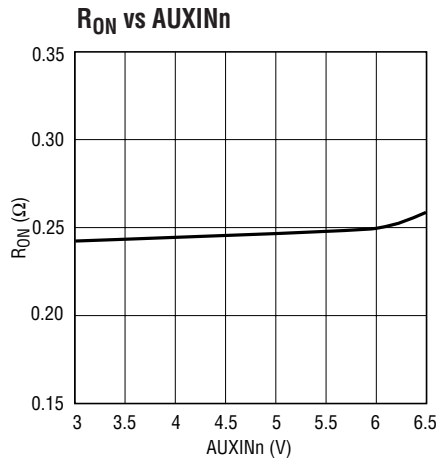
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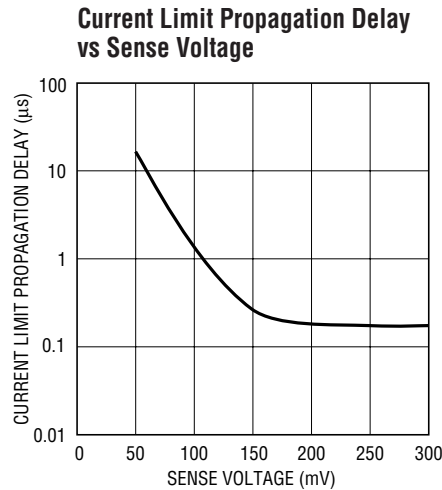
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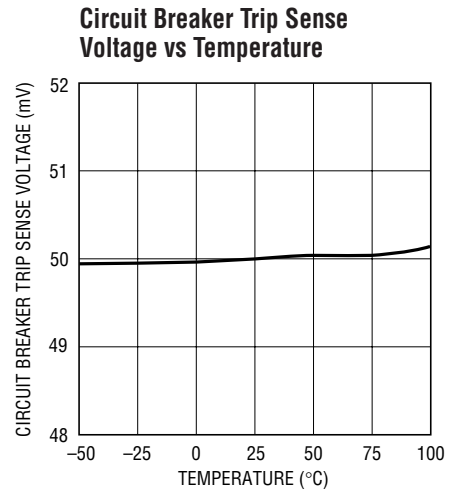
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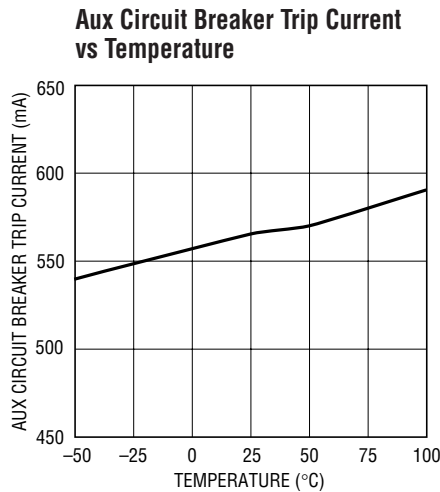
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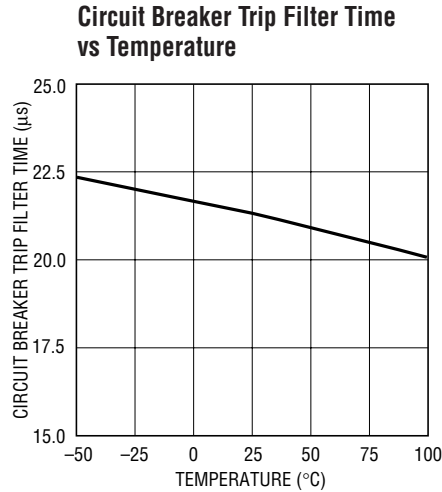
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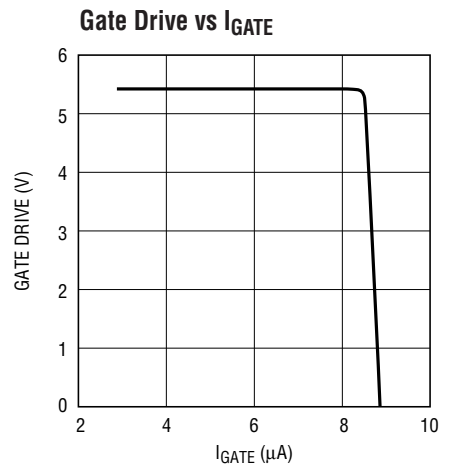
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4242 G14



4242 G17

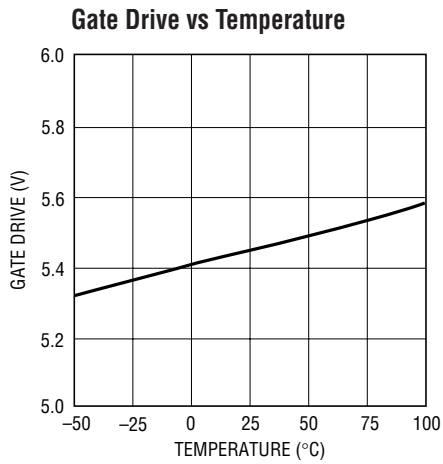


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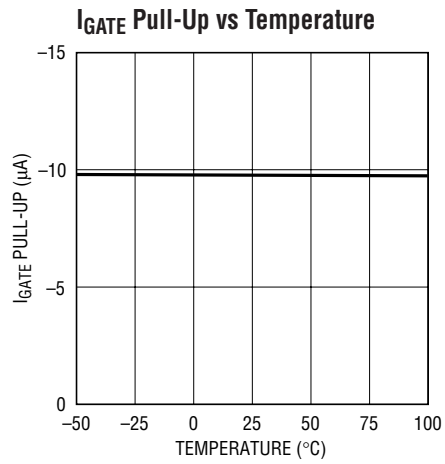
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# TYPICAL PERFORMANCE CHARACTERISTICS

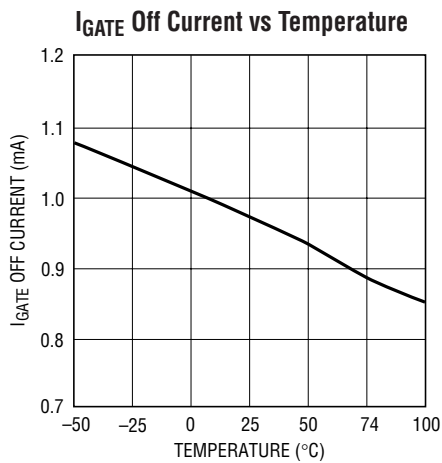
$T_A = 25^\circ\text{C}$ .  $V_{CC} = V_{AUXINn} = V_{3VINn} = 3.3\text{V}$ ,  $V_{12VINn} = 12\text{V}$ , unless otherwise noted. (Note 2)



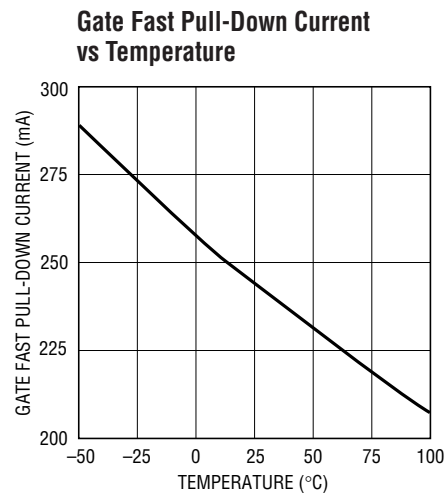
4242 G19



4242 G20



4242 G21



4242 G22

## PIN FUNCTIONS

**12V<sub>GATE1</sub>/12V<sub>GATE2</sub>:** Gate Drive for 12V Supply External N-Channel MOSFET. An internal charge pump provides a 9 $\mu$ A pull-up current to ramp up 12V<sub>GATE<sub>n</sub></sub>. During turn off, a 1mA pull-down current source discharges 12V<sub>GATE<sub>n</sub></sub> to ground. 12V<sub>GATE<sub>n</sub></sub> is internally clamped to 5.5V above 12V<sub>OUT<sub>n</sub></sub>. During an overcurrent fault, a 250mA pull-down current source between 12V<sub>GATE<sub>n</sub></sub> and 12V<sub>OUT<sub>n</sub></sub> is activated. An external RC network is required at the pin for optimum current limit response.

**12V<sub>SENSE1</sub>/12V<sub>SENSE2</sub>:** 12V Supply Current Limit Sense Input. A sense resistor is placed in the supply path between 12V<sub>IN<sub>n</sub></sub> and 12V<sub>SENSE<sub>n</sub></sub> to sense the 12V channel's load current. The voltage across the sense resistor is monitored for active current limit and circuit breaker fault detection. To disable the circuit breaker function for the 12V channel, connect 12V<sub>SENSE<sub>n</sub></sub> to 12V<sub>IN<sub>n</sub></sub>.

**12V<sub>IN1</sub>/12V<sub>IN2</sub>:** 12V Supply Input. An undervoltage lockout circuit disables the 12V and 3.3V supplies when 12V<sub>IN<sub>n</sub></sub> voltage is less than 9.78V.

**12V<sub>OUT1</sub>/12V<sub>OUT2</sub>:** 12V Output Connection. Connect this pin to the source of the 12V supply external N-channel MOSFET for gate drive return. PGOOD1/PGOOD2 cannot pull low until this pin goes above 10.38V. A 700 $\Omega$  active pull-down discharges 12V<sub>OUT<sub>n</sub></sub> to ground when the external MOSFET is turned off.

**3V<sub>GATE1</sub>/3V<sub>GATE2</sub>:** Gate Drive for 3.3V Supply External N-Channel MOSFET. An internal charge pump provides a 9 $\mu$ A pull-up current to ramp up 3V<sub>GATE<sub>n</sub></sub>. During turn off, a 1mA pull-down current source discharges 3V<sub>GATE<sub>n</sub></sub> to ground. 3V<sub>GATE<sub>n</sub></sub> is internally clamped to 5.5V above 3V<sub>OUT<sub>n</sub></sub>. During an overcurrent fault, a 250mA pull-down current source between 3V<sub>GATE<sub>n</sub></sub> and 3V<sub>OUT<sub>n</sub></sub> is activated. An external RC network is required at the pin for optimum current limit response.

**3V<sub>SENSE1</sub>/3V<sub>SENSE2</sub>:** 3.3V Supply Current Limit Sense Input. A sense resistor is placed in the supply path between 3V<sub>IN<sub>n</sub></sub> and 3V<sub>SENSE<sub>n</sub></sub> to sense 3.3V channel's load current. The voltage across the sense resistor is monitored for active current limit and circuit breaker fault detection. To disable the circuit breaker function for the 3.3V channel, connect 3V<sub>SENSE<sub>n</sub></sub> to 3V<sub>IN<sub>n</sub></sub>.

**3V<sub>IN1</sub>/3V<sub>IN2</sub>:** 3.3V Supply Input. An undervoltage lockout circuit disables the 3.3V and 12V supplies when 3V<sub>IN<sub>n</sub></sub> voltage is less than 2.67V.

**3V<sub>OUT1</sub>/3V<sub>OUT2</sub>:** 3.3V Output Connection. Connect this pin to the source of the 3.3V supply external N-channel MOSFET for gate drive return. PGOOD1/PGOOD2 cannot pull low until this pin goes above 2.855V. A 375 $\Omega$  active pull-down discharges 3V<sub>OUT<sub>n</sub></sub> to ground when the external MOSFET is turned off.

**AUXFAULT1/AUXFAULT2:** AUX Supply Fault Status Output. AUXFAULT<sub>n</sub> is normally pulled high by an internal 9 $\mu$ A pull-up. It asserts low if the AUX channel shuts off due to an overcurrent fault or due to the device temperature rising above 150°C. Indicates switch ON status when FON<sub>n</sub> and EN<sub>n</sub> are high.

**AUXON1/AUXON2:** AUX Supply On Control Input. A rising edge turns on the internal FET, while a falling edge turns it off. Pulling this pin below 0.6V for more than 3.5 $\mu$ s clears the fault on the AUX channel.

**AUXIN1/AUXIN2:** AUX Supply Input. An undervoltage lockout circuit disables the AUX supply when the voltage at AUXIN<sub>n</sub> is less than 2.67V. AUXIN<sub>n</sub> is the input to the internal pass FET.

**AUXOUT1/AUXOUT2:** AUX Supply Output. AUXOUT<sub>n</sub> is the output from the internal pass FET. AUXPGOOD1/AUXPGOOD2 cannot pull low until this pin goes above 2.855V. A 750 $\Omega$  active pull-down discharges AUXOUT<sub>n</sub> to ground when the internal FET is turned off.



## PIN FUNCTIONS

**AUXPGOOD1/AUXPGOOD2 (QFN):** AUX Supply Power Status Output. This open-drain pin is pulled high by an internal  $9\mu\text{A}$  pull-up when  $\text{AUXOUT}_n$  is below power good threshold, when  $\overline{\text{EN}}_n$  is high, during thermal shutdown,  $\text{AUXON}_n$  is low or when  $V_{\text{CC}}$  or  $\text{AUXIN}_n$  are in UVLO.

**$\overline{\text{EN}}_1/\overline{\text{EN}}_2$ :** Card Presence/Slot Insert Detect Input.  $\overline{\text{EN}}_n$  pin must be pulled below  $1.235\text{V}$  to enable the system. An internal  $9\mu\text{A}$  pull-up current source is present on this pin.

**Exposed Pad (QFN):** Power Ground. PCB electrical connection is optional.

**$\overline{\text{FAULT}}_1/\overline{\text{FAULT}}_2$ :** Main Supplies Fault Status Output.  $\overline{\text{FAULT}}_n$  is pulled high by an internal  $9\mu\text{A}$  pull-up. When an overcurrent fault occurs at either the 12V or 3.3V supply,  $\overline{\text{FAULT}}_n$  is latched low.

**FON1/FON2:** Force On Digital Input. For diagnostic purposes, a high input overrides undervoltage and overcurrent faults on 12V, 3.3V and AUX channels and input commands

on the  $\text{ON}_n$  and  $\text{AUXON}_n$  pins. However, UVLO on  $V_{\text{CC}}$  would shut off the switches. Caution! There is no current limit mechanism in this mode. Connect  $\text{FON}_n$  to ground to disable the fault override feature.

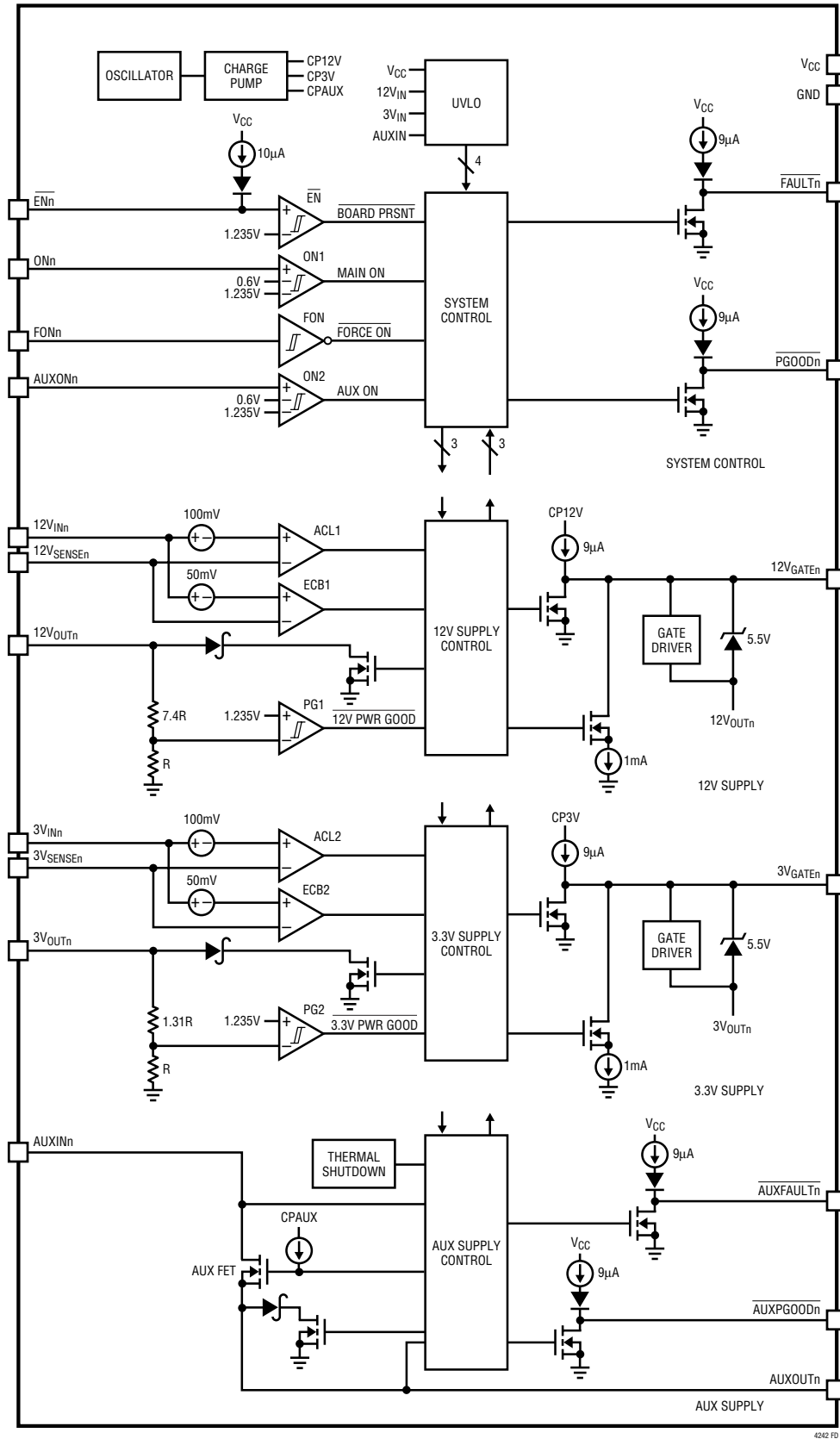
**GND:** Device Ground. Connect to a ground plane.

**ON1/ON2:** Main Supply On Control Input. A rising edge turns on the external MOSFETs for the 12V and 3.3V supplies, while a falling edge turns them off. Pull this pin below  $0.6\text{V}$  to clear the faults on 12V and 3.3V channels.

**PGOOD1/PGOOD2:** Main Supply Power Status Output. This open-drain pin is pulled high by an internal  $9\mu\text{A}$  pull-up when  $12\text{V}_{\text{OUT}_n}$  or  $3\text{V}_{\text{OUT}_n}$  is below power good threshold, when  $\overline{\text{EN}}_n$  is high,  $\text{ON}_n$  is low or when  $V_{\text{CC}}$  or any of the main supplies are in UVLO.

**$V_{\text{CC}}$ :** Device Supply Input. Operates from  $2.7\text{V}$  to  $6\text{V}$ . An internal undervoltage lockout circuit disables the part until the voltage at  $V_{\text{CC}}$  exceeds  $2.45\text{V}$ .

FUNCTIONAL DIAGRAM



4242 FD

## OPERATION

The Functional Diagram displays the main functional elements of this device. The LTC4242 is designed to control the power for two independent slots on a PCI Express backplane, allowing two boards to be safely inserted and removed. During normal operation, the charge pump sources 9 $\mu$ A to turn on the gate of the external N-channel MOSFETs to pass power to the load. The gates of the external MOSFETs are clamped about 5.5V above their sources. The gates of the AUX FETs rise at a slew rate of about 1.25V/ms to control the inrush current.

The electronic circuit breaker (ECB) comparator and analog current limit (ACL) amplifier monitor the load current using the difference between the  $V_{IN}$  and SENSE voltage. The threshold of the ACL is set at 2x the ECB threshold. The ACL amplifier limits the current in the load by reducing the gate-to-source voltage of the external MOSFETs in an active control loop. When an overcurrent condition persists for more than 20 $\mu$ s, the MOSFETs are shut off to prevent overheating. FAULT is latched low to signal that an overcurrent condition has occurred on the external MOSFETs controlling the main channels.

The AUX FET's control circuitry has a circuit breaker that trips at 550mA after 20 $\mu$ s. It also incorporates an active current limit amplifier that would limit the current flowing in the AUX FET to about 1.65A. A thermal shutdown circuit shuts off the AUX FET when the die temperature rises above 150°C. AUXFAULT is latched low to signal

an overcurrent condition on the internal FET or thermal shutdown has occurred.

When the switches are off (both internal and external), the OUT pins are discharged to ground through internal N-channel transistors.

The output voltages are monitored using the OUT pins and the PG comparators to determine if the voltage is valid. The power good condition is signaled by the PGOOD/AUXPGOOD pins using open-drain pull-down transistors.

The Functional Diagram shows the monitoring blocks of the LTC4242. The group of comparators in the system control includes the UVLO, ON and EN comparators. These comparators are used to determine if the external conditions are valid prior to turning on the switches. But first the undervoltage lockout circuit (UVLO) must validate the input supplies and the main supply  $V_{CC}$  and generate the power up initialization to the logic circuits.

The FON inverter in the system control is used for operating the LTC4242 in diagnostic mode. In this mode of operation, all pass transistors are forced to turn on, ignoring the undervoltage, circuit breaker/current limiting status and input commands. However, if  $V_{CC}$  drops below its UVLO voltage, all switches would be shut off, regardless of FON.

## APPLICATIONS INFORMATION

The typical LTC4242 application is in a backplane or motherboard that controls power to two PCI Express slots. The device reports fault and power good status to the system hot plug controller (HPC).

The basic LTC4242 application circuit is shown in Figure 1. Discussion begins with board presence detection in a PCI Express system, the normal turn on and off sequence, the various fault conditions and recovery from fault situations. The force on operation is discussed next followed by the considerations for PCB layout. External component selection is discussed in detail in the Design Example section.

### Board Presence Detect

In PCI Express systems, the system board connector uses two signals, PRSNT1 and PRSNT2, to detect the presence of a board and ensure a fully inserted board in the connector as shown in Figure 2. PRSNT2 is routed to the system HPC. Upon a board insertion into the connector, a turn-on command is generated by the HPC to LTC4242 after a programmed HPC debounce delay, as shown in Figure 1. Another method to generate the debounce delay is through the delay network shown in Figure 3.

APPLICATIONS INFORMATION

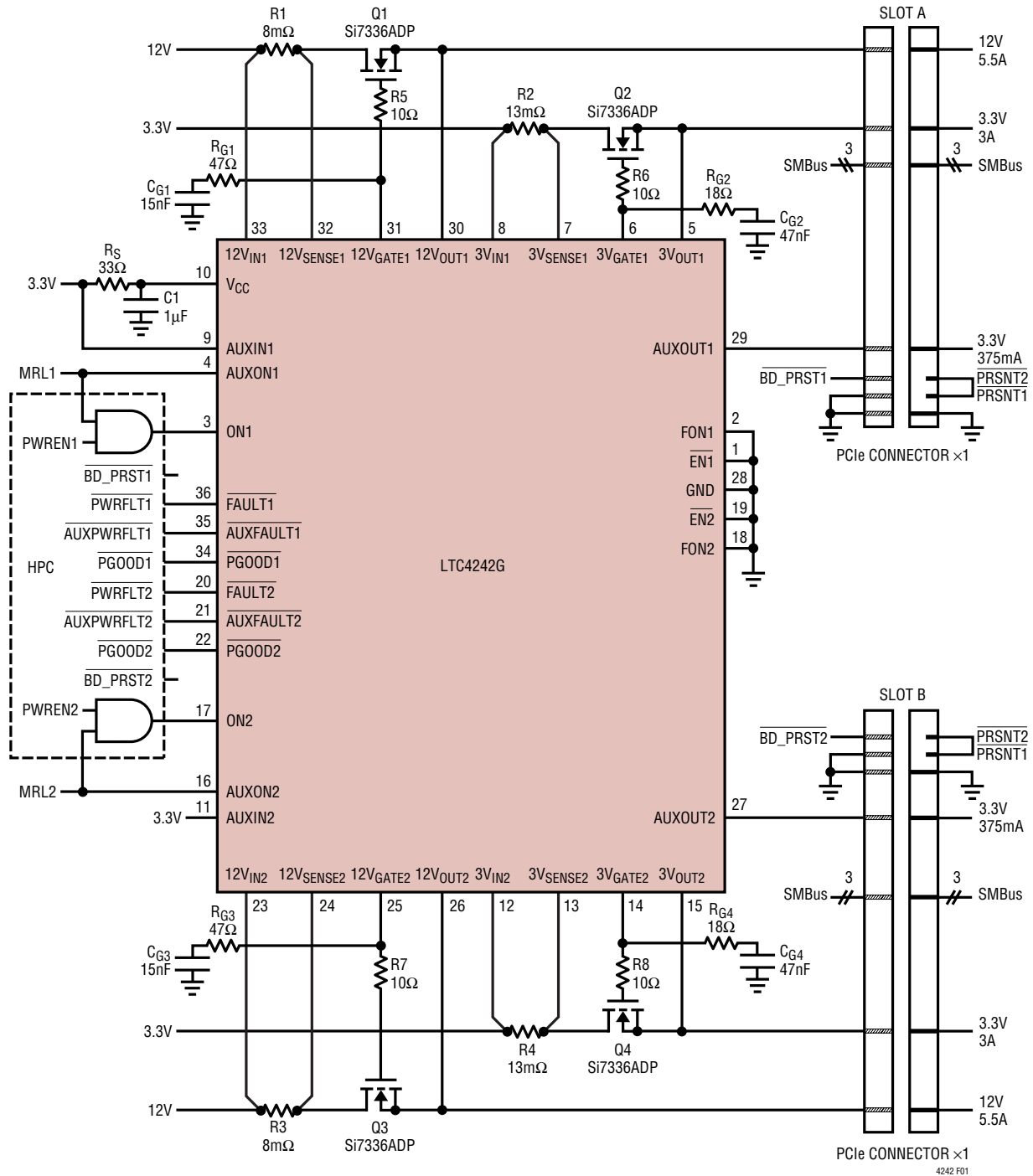


Figure 1. Typical PCI Express Application

## APPLICATIONS INFORMATION

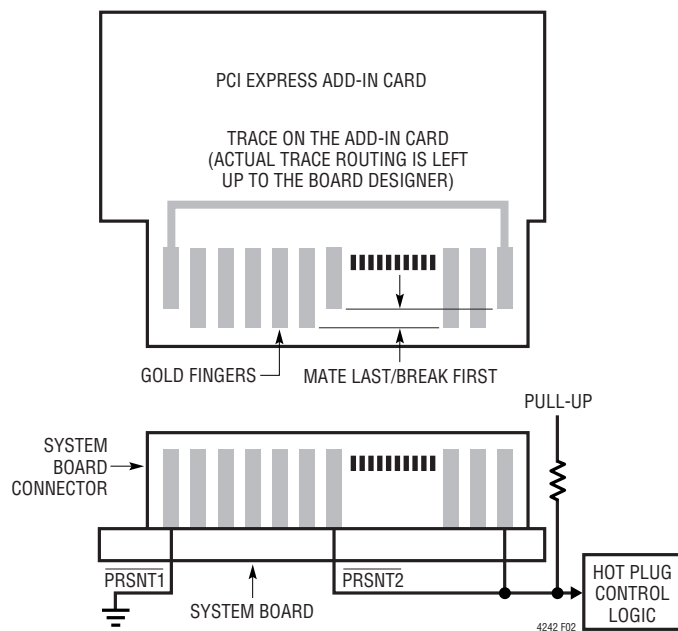


Figure 2. Plug-In Card Insertion/Removal

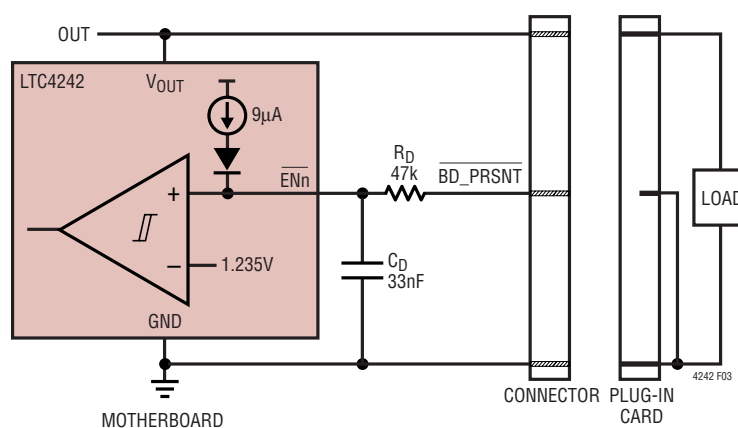


Figure 3. RC Network to Generate Delay During Card Plug-In

When  $\overline{\text{PRSENT2}}$  pulls low after insertion of a board, the  $\overline{\text{ENn}}$  pin goes low after a delay as determined by the values of  $C_D$  and  $R_D$ . For plug-in debounce delay of 1ms and  $R_D$  of 47k:

$$C_D = \frac{t_{\text{DELAY1}} (\text{ms})}{43.5} \mu\text{F} = 0.023 \mu\text{F}$$

Choose  $C_D$  to be 33nF.

When the board is removed, the power to the slot is disabled after a delay of:

$$t_{\text{DELAY2}} = \frac{0.765 C_D}{9} \text{ s} = 2.8 \text{ ms}$$

### Turn-On Sequence

The PCI Express power supplies are controlled by the external N-channel pass transistors, Q1 through Q4, in the 12V and 3.3V power paths, and internal pass transistors

## APPLICATIONS INFORMATION

for the 3.3V auxiliary power paths. Sense resistors R1 to R4 provide input for current fault detection. Resistors R<sub>G1</sub> to R<sub>G4</sub> and capacitors C<sub>G1</sub> to C<sub>G4</sub> compensate the current control loops. Capacitors C<sub>G1</sub> to C<sub>G4</sub> also control the output power-up rate and the inrush current while resistors R5 to R8 prevent high frequency oscillations in N-channel MOSFETs, Q1 to Q4 respectively.

The following conditions must be satisfied before the external and internal switches can be turned on.

1. The device's power supply, V<sub>CC</sub>, must exceed its undervoltage lockout threshold. To turn on the external/internal switches, the main/auxiliary input supplies must exceed their UVLO thresholds.
2. The  $\overline{\text{EN}}$  pin must be pulled low to begin the start-up sequence.

When these initial conditions are satisfied, the ON pins are checked. The LTC4242 features per slot ON pins, the AUXON and ON, to allow independent control of the main input supplies (12V and 3.3V) and the 3.3V auxiliary supplies. If the ON pin is high, the switches turn on. If ON is low, the switches turn on when the ON pin is brought high. Figure 4 shows all supplies turning on after  $\overline{\text{EN}}$  goes low.

Each of the external switches is turned on by charging the GATE with a 9 $\mu$ A current source. The voltage at the GATE pins rises with a slope equal to 9 $\mu$ A/C<sub>G</sub> and the supply inrush current is set at C<sub>L</sub>/C<sub>G</sub> • 9 $\mu$ A, where C<sub>L</sub> is the capacitance at the supply output.

The gate of the internal switch is slewed resulting in the 3.3V<sub>AUX</sub> supply output powering up at an internally set rate of about 1.25V/ms.

The circuit breaker (ECB) of the input supplies is armed after the input supplies clear UVLO. Once the supplies have been turned on and the outputs are within tolerance, PGOOD for the main input supplies and AUXPGOOD for the auxiliary input supplies (available for the QFN only) are pulled low.

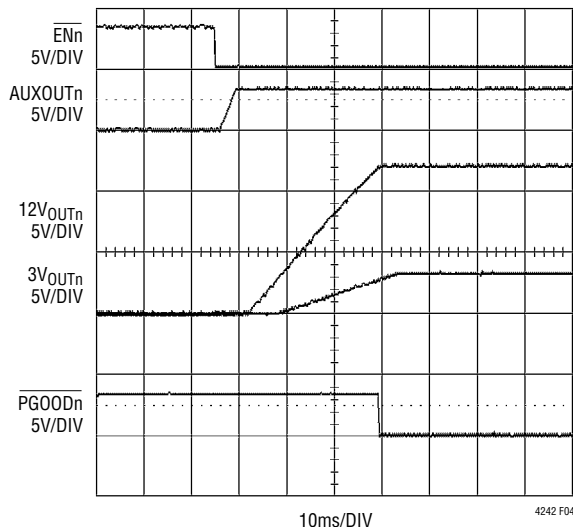


Figure 4. Normal Power-Up Sequence

### Turn-Off Sequence

The switches can be turned off by a variety of conditions.

1. The ON/AUXON pin going low would turn off the main/internal switches.
2.  $\overline{\text{EN}}$  going high turns off all switches.
3. A variety of fault conditions will turn off the switches. These include supply undervoltage and overcurrent circuit breaker faults.
4. When thermal shutdown activates, the internal switch is shut off.

When ON goes low, the main switches are turned off with a 1mA current pulling down the gate to ground. When the main supplies are shut off, the PGOOD signal pulls high and the outputs are discharged to ground through internal switches. Similarly, when an auxiliary supply is turned off, the AUXPGOOD signal pulls high and its output is discharged to ground through internal switches. Figure 5 shows all supplies being turned off by  $\overline{\text{EN}}$  going high.

## APPLICATIONS INFORMATION

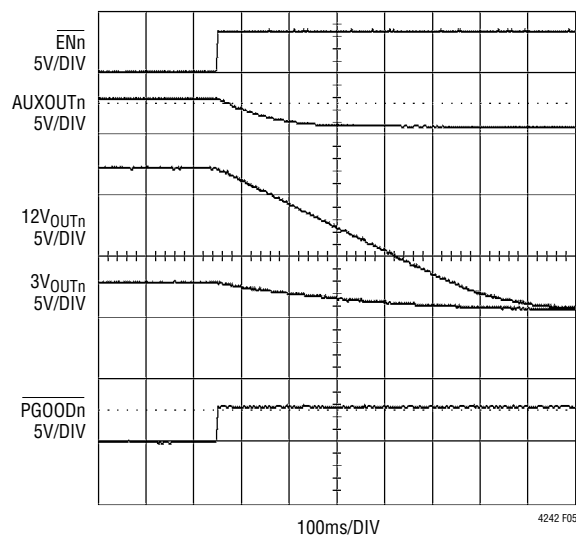


Figure 5. Normal Power-Down Sequence

### Thermal Shutdown

Each of the two internal switches for the 3.3V auxiliary supplies is protected by an independent thermal shutdown circuit. If the temperature of an internal switch reaches 150°C, the switch shuts down immediately and AUXFAULT is latched low. All other power switches are not affected. The switch is allowed to turn on again by recycling the AUXON pin low then high with the temperature falling below 120°C.

### Overcurrent Fault

The LTC4242 features dual level glitch tolerant protection against overcurrent faults for all the supplies. The sense resistor (both internal and external) voltage drop is monitored by an electronic circuit breaker (ECB) comparator and an active current limit (ACL) amplifier. In the event that a supply's current exceeds the ECB threshold, an internal timer is started. If the supply is still overcurrent after 20 $\mu$ s, the ECB trips and the MOSFET turns off immediately, as shown in Figure 6.

During start-up, a supply output could be shorted to ground in the worst case. The inrush current would be limited to the ACL threshold, which is 2x the ECB threshold, and the part will latch off after 20 $\mu$ s.

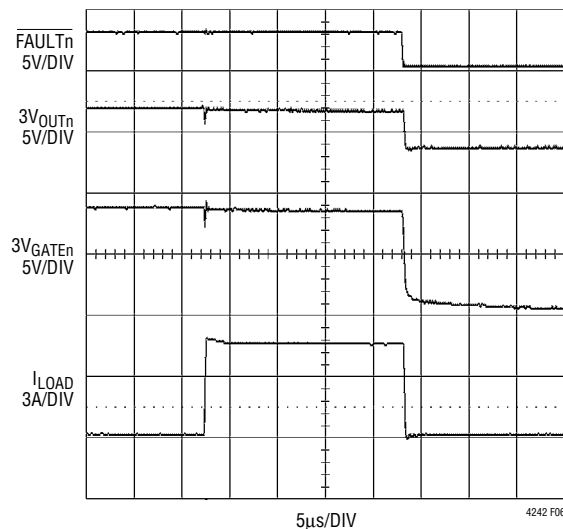


Figure 6. Overcurrent Fault on 3.3V Output

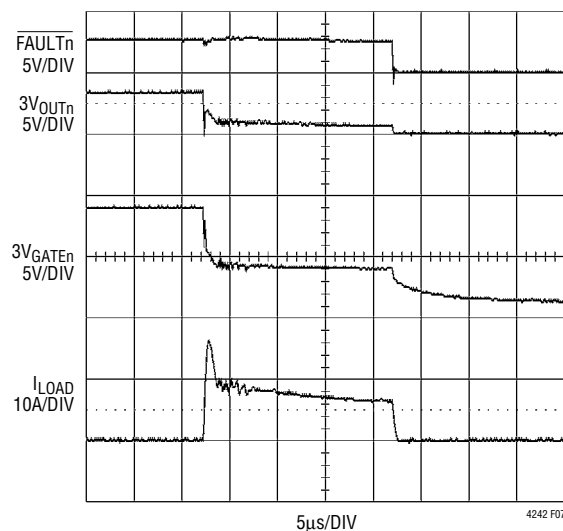


Figure 7. Short-Circuit Fault on 3.3V Output

During an output short circuit, the surge current must be brought to a controlled level within the shortest amount of time to protect the system. The LTC4242's active current limit enters a high current protection mode that immediately turns off the output MOSFET by pulling its gate-to-source voltage to zero. Current in the output MOSFET drops from tens of amps to zero in a few hundred nanoseconds. The input voltage drops during the high current and then spikes upwards due to lead parasitic inductances as the

## APPLICATIONS INFORMATION

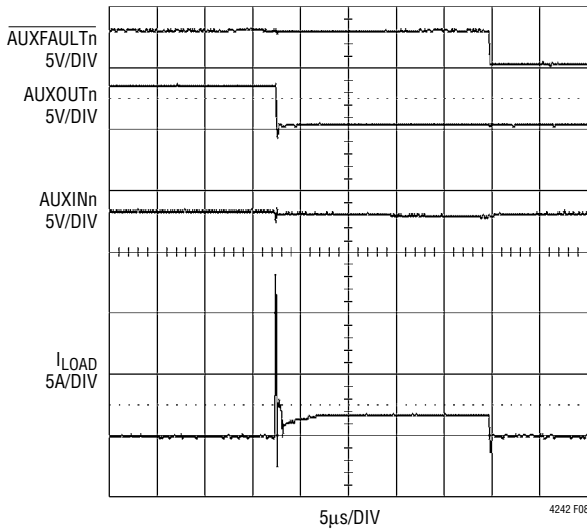


Figure 8. Short-Circuit Fault on 3.3V<sub>AUX</sub> Output

MOSFET shuts off (see Supply Transients). The compensation network  $R_G/C_G$  assists the gate voltage recovery. The ACL limits the current level to 2x the ECB threshold by regulating the gate voltage.

For the internal switch, the ACL limits the supply current to about 3x the circuit breaker current level of 550mA.

The ECB has a 20µs filter delay before latching off to prevent unnecessary resets of the system due to minor transient surges. An overcurrent fault on any of the main outputs (12V or 3.3V) latches off both main outputs without affecting the 3.3V auxiliary output. Similarly, an overcurrent fault on the 3.3V auxiliary output latches off the auxiliary output, without affecting the main outputs.

When there is a shorted load with significant supply lead inductance, the supply pin voltage could collapse before the ACL brings down the gate of the external MOSFET. In this case, the undervoltage lockout circuit, with 18µs filter time, turns off the pass MOSFETs.

### Undervoltage Fault

An undervoltage fault occurs when any of the input supplies, 12V<sub>IN</sub>, 3V<sub>IN</sub> or AUXIN, falls below its undervoltage threshold for more than 18µs. This turns off the switches immediately. An undervoltage on the 3.3V auxiliary supply will not cause the main supplies to shut off and vice versa. An undervoltage fault on any of the main supplies shuts off both main supply switches. If  $V_{CC}$  falls below

its UVLO threshold for more than 38µs, all switches are turned off. The switches are allowed to turn on when the supply voltages and  $V_{CC}$  rise above their respective undervoltage thresholds.

### Power Good Fault

A power good fault occurs when any supply output drops below its power good threshold for more than 20µs. A power good fault on the main/AUX supplies causes the  $\overline{\text{PGOOD}}/\overline{\text{AUXPGOOD}}$  to be pulled high. There are a variety of conditions which must be satisfied for  $\overline{\text{PGOOD}}/\overline{\text{AUXPGOOD}}$  to be asserted low:

1. The output voltage is above power good threshold
2.  $\overline{\text{EN}}$  pin is low
3. The input voltage is above the undervoltage threshold
4. ON pin is high
5. Thermal shutdown not activated

### Resetting Faults

To reset an overcurrent fault on the main outputs, bring ON low or the faulting supply below its undervoltage lockout (UVLO) threshold. To reset an overcurrent or thermal shutdown fault on the auxiliary output, bring AUXON low or the auxiliary supply below its UVLO threshold. Bringing  $V_{CC}$  below its UVLO threshold resets all overcurrent and thermal shutdown faults. The part cannot be reset when fault override, FON, is high.

### Auto-Retry After a Fault

As shown in Figure 9, the LTC4242 can be configured to automatically retry after a fault condition by connecting both the  $\overline{\text{FAULT}}$  and ON pins together with an RC network. The auto-retry circuit will attempt to restart the LTC4242 after a circuit breaker trip, as shown in the timing diagram of Figure 10.

$$t_{\text{OFF}} \approx \frac{R_{\text{AUTO}} \cdot C_{\text{AUTO}} \cdot (1.235 - V_{\text{OL}})}{2.065 + R_{\text{AUTO}} \cdot 9\mu\text{A}}$$

For the component values shown,  $t_{\text{OFF}} = 3.3\text{ms}$ . Since the duration of a short is less than 40µs in the worst case, the auto-retry duty cycle is 1.3%.



## APPLICATIONS INFORMATION

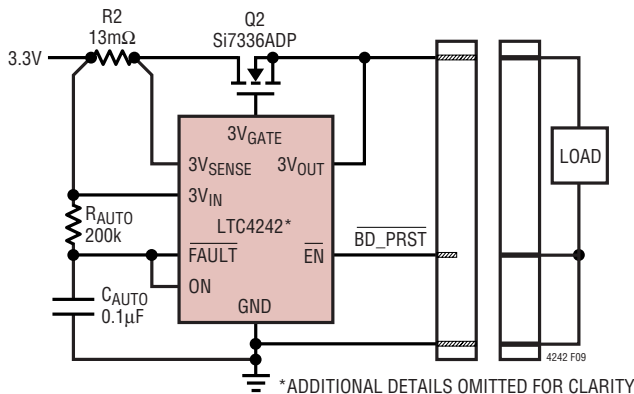


Figure 9. Auto-Retry Application

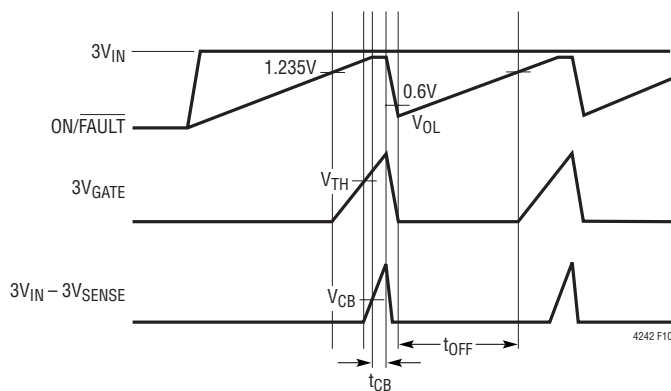


Figure 10. Auto-Retry Timing

### GATE Pin Voltage

The minimum gate drive voltage is 4.5V, therefore, logic level N-channel MOSFETs should be used for the external switches to maintain adequate gate enhancement. The GATE pins are clamped at a typical value of 5.5V above the respective OUT pins.

### Compensating the Active Current Loop

The active current limit circuit is compensated using the resistor  $R_G$  and the slew rate control capacitor  $C_G$ . The value of  $C_G$  is selected based on the inrush current allowed. The  $R_G$  value should be experimentally determined. A suggested value range for  $R_G$  is between 10 $\Omega$  and 100 $\Omega$ .

### V<sub>CC</sub> Power Supply

The LTC4242 derives its power from  $V_{CC}$ . A bypass capacitor of 1 $\mu$ F should be connected between this pin and ground. If  $V_{CC}$  is derived from the input supplies of 3V<sub>IN</sub> or AUXIN, a lowpass filter shown in Figure 11 should be used.

This RC network allows the LTC4242 to ride through a 3V<sub>IN</sub>/AUXIN short-circuit transient without collapsing below the  $V_{CC}$  UVLO threshold. AUXIN or 3V<sub>IN</sub> may have narrow but high glitches due to parasitic inductance. Since the absolute maximum rating for  $V_{CC}$  is 7V compared to 10V for AUXIN and 3V<sub>IN</sub>, the  $R_S$  and  $C_1$  values should be chosen to damp the peak voltage seen by  $V_{CC}$  below 7V.

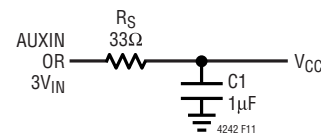


Figure 11. RC Network for  $V_{CC}$  Filtering

### Force ON Operation

When the FON pin is pulled high and  $\overline{EN}$  is low, the LTC4242 operates in the diagnostic mode. All the input supplies' power switches are forced to turn on, regardless of undervoltage conditions on the input supplies, status of the ON pins and the fault latch. The contents in the fault latch would be preserved during this time and no change of state would occur after the part is configured to operate in the diagnostic mode. If the output current exceeds the ECB threshold, FAULT/AUXFAULT is pulled low immediately, but does not latch. The undervoltage lockout on  $V_{CC}$  turns off all the switches, regardless of the status of FON. During thermal shutdown, the internal switch is shut off to prevent overheating, even if FON is high. The main power switches remain on as FON is high. Care must be taken to ensure the outputs are not short circuited since there is no current limit mechanism in diagnostic mode.

## APPLICATIONS INFORMATION

Yet another mode of operation is the Force ON with current limit mode. To enter this mode, pull both FON and  $\overline{\text{EN}}$  high. In this mode of operation, the ACLs are enabled with the 20 $\mu\text{s}$  filter time disabled. The fault latch of the AUX supply can be latched if the AUX's  $I_{\text{CBAUX}}$  is exceeded. AUXFAULT indicates whether the AUX channel FET is on or off. To enter normal operation, pull FON and  $\overline{\text{EN}}$  low and recycle the ON and AUXON pins.

### PCB Layout Considerations

For proper operation of the LTC4242's circuit breaker, a Kelvin connection to the sense resistors is required. The Kelvin sense PCB layout traces should be minimum length, closed together, balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistors and the power MOSFETs should include good thermal management techniques for optimal device power dissipation. A recommended PCB layout for the 12V sense resistor and the power MOSFET is illustrated in Figure 12.

In Hot Swap applications where load currents can be 10A, narrow PCB tracks exhibit more resistance than wider tracks and hence, operate at higher temperatures. Since the sheet resistance of 1oz copper foil is approximately 0.5m $\Omega$ /square, track resistances and voltage drops add up quickly in high current applications. Thus, to keep PCB track resistance, voltage drop and temperature rise to a minimum, the suggested trace width in these applications for 1oz copper foil is 0.03" for each ampere of DC current.

In the majority of applications, it will be necessary to use plated-through vias to make circuitry connections from components layers to power and ground layers internal to the PCB. For 1oz copper foil plating, a general rule is 1A of DC current per via making sure the via is properly dimensioned so that solder completely fills any void. Check with your PCB fabrication facility for via current specifications.

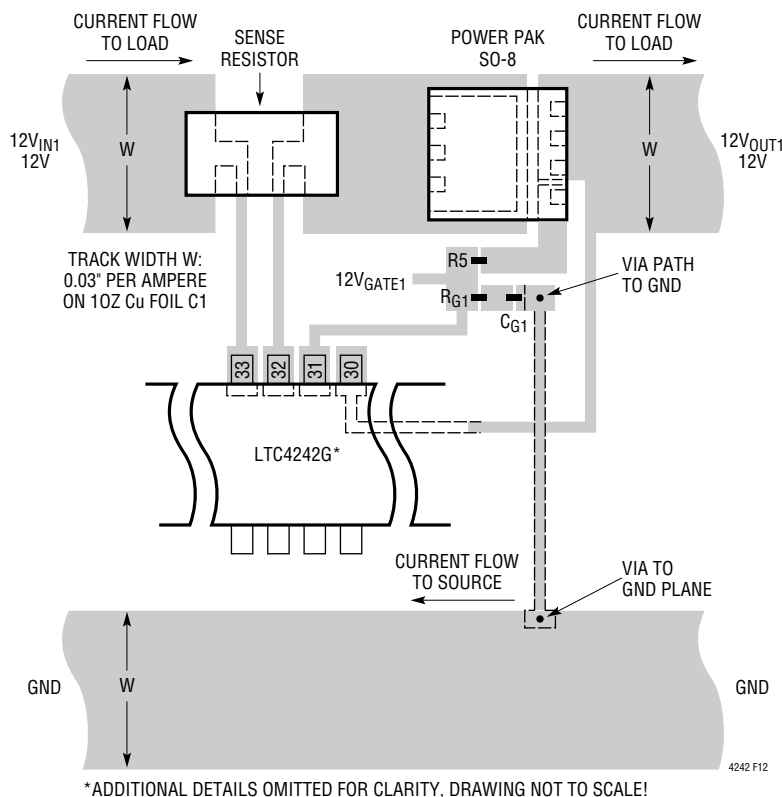


Figure 12. Recommended Layout for Power MOSFET, Sense Resistor and GATE Components for the 12V Rail

## APPLICATIONS INFORMATION

In system board applications, large bypass capacitors ( $\geq 10\mu\text{F}$ ) are recommended at each of the system input supplies to minimize supply glitches as a result of large inrush or fault currents.

It is important to put C1, the bypass capacitor for the  $V_{CC}$  pin as close as possible between the  $V_{CC}$  and GND pins.

### Design Example

Consider a PCI Express Hot Swap application example with the following power supply requirements:

**Table 1. PCI Express Power Supply Requirements**

SUPPLY VOLTAGE	MAXIMUM SUPPLY CURRENT	MAXIMUM LOAD CAPACITANCE
12V	5.5A	2000 $\mu\text{F}$
3.3V	3.0A	1000 $\mu\text{F}$
3.3V <sub>AUX</sub>	375mA	150 $\mu\text{F}$

1. Select an  $R_{\text{SENSE}}$  value for each supply. Calculate the  $R_{\text{SENSE}}$  value based on the maximum load current and the lower circuit breaker threshold limit,  $\Delta V_{\text{SENSE(CB)(MIN)}}$ . In a PCI Express connector, five pins are allocated for the 12V supply, three pins for the 3.3V supply and one pin for 3.3V<sub>AUX</sub>. The current rating of a connector pin is 1.1A. If a 1% tolerance is assumed for the sense resistors, then the following values of resistances should suffice:

**Table 2. Sense Resistance Values**

VOLTAGE SUPPLY	$R_{\text{SENSE}}$ (1%)	$I_{\text{TRIP(MIN)}}$	$I_{\text{TRIP(MAX)}}$
12V	8m $\Omega$	5.6A	6.9A
3.3V	13m $\Omega$	3.4A	4.3A

2. Assume no load current at start-up and the inrush current charges the load capacitance. Compute gate capacitance with:

$$C_{\text{GATE}} = \frac{I_{\text{GATE(UP)}} \cdot t_1}{V_{\text{OUT}}} \quad (2)$$

$t_1$  is the time to charge up the load capacitor.

With  $I_{\text{GATE(UP)(MAX)}} = 13\mu\text{A}$  and  $t_1 = 10\text{ms}$ :

- For 12V Supply,  $C_{\text{GATE}} = 11\text{nF}$
- For 3.3V Supply,  $C_{\text{GATE}} = 39\text{nF}$

So a value of 15nF and 47nF ( $\pm 10\%$ ) should suffice for the 12V and 3.3V supplies respectively. The worst-case  $t_1$  and inrush currents are tabulated in Table 3.

**Table 3. Worst-Case  $t_1$  and Inrush Current**

VOLTAGE SUPPLY	$t_1(\text{MIN})$	$t_1(\text{MAX})$	MAX $I_{\text{INRUSH}}$
12V	13ms	40ms	2.4A
3.3V	11ms	34ms	0.4A

For the internal switch, the slew rate (SR) at the 3.3V<sub>AUX</sub> supply output is limited to 1.7V/ms max. The inrush current can then be calculated according to:

$$I_{\text{INRUSH(MAX)}} = C_{\text{LOAD}} \cdot \text{SR}_{\text{MAX}} \quad (3)$$

The inrush current must be lower than 385mA ( $I_{\text{CBAUX(MIN)}}$ ) for proper start-up. Assuming a tolerance of 30% for the load capacitance, the value of  $C_{\text{LOAD}}$  should not exceed 170 $\mu\text{F}$ .

3. Next is the selection of MOSFETs for the 12V and 3.3V main input supplies. The Si7336ADP's on resistance is less than 4m $\Omega$  at  $V_{\text{GS}} = 4.5\text{V}$ , 25°C and it is a good choice for 3.3V and 12V main supplies.

Since the maximum load for the 3.3V supply is 3A, the MOSFET may dissipate up to 36mW. The Si7336ADP has a maximum junction-to-ambient thermal resistance of 50°C/W. This gives a junction temperature of 51.8°C when operating at a case temperature of 50°C. According to the Si7336ADP's Normalized On-Resistance vs Junction Temperature curve, the device's on resistance can be expected to increase by about 12% over its room temperature value. Recalculation for steady-state  $R_{\text{ON}}$  and junction temperature yield approximately 4.5m $\Omega$  and 52°C, respectively. The voltage drop across the 3.3V sense resistor and series MOSFET at 3A and at 50°C PCB temperature is less than 53mV.

The MOSFET dissipates power during inrush charging of the output load capacitor. Assuming no load current, the MOSFET's dissipated power equals the final load capacitor stored energy. Therefore, average MOSFET dissipated power is:

$$P_{\text{ON}} = \frac{C_{\text{L}} \cdot V_{\text{OUT}}^2}{2 \cdot t_1} \quad (4)$$

## APPLICATIONS INFORMATION

Using  $P_{ON}$  and  $t_1$  to look up the MOSFETs' single pulse  $\theta_{JA(MAX)}$  from the manufacturer's Transient Thermal Impedance Graph, the worst-case junction-to-ambient temperature rise occurs for the 12V MOSFET.

**Table 4. MOSFET Power-Up Temperature Rise Calculation**

VOLTAGE SUPPLY	$P_{ON}$	$\theta_{JA(MAX)}$	$\Delta T$
12V	11W	0.75°C/W	8.3°C
3.3V	0.5W	0.6°C/W	0.3°C

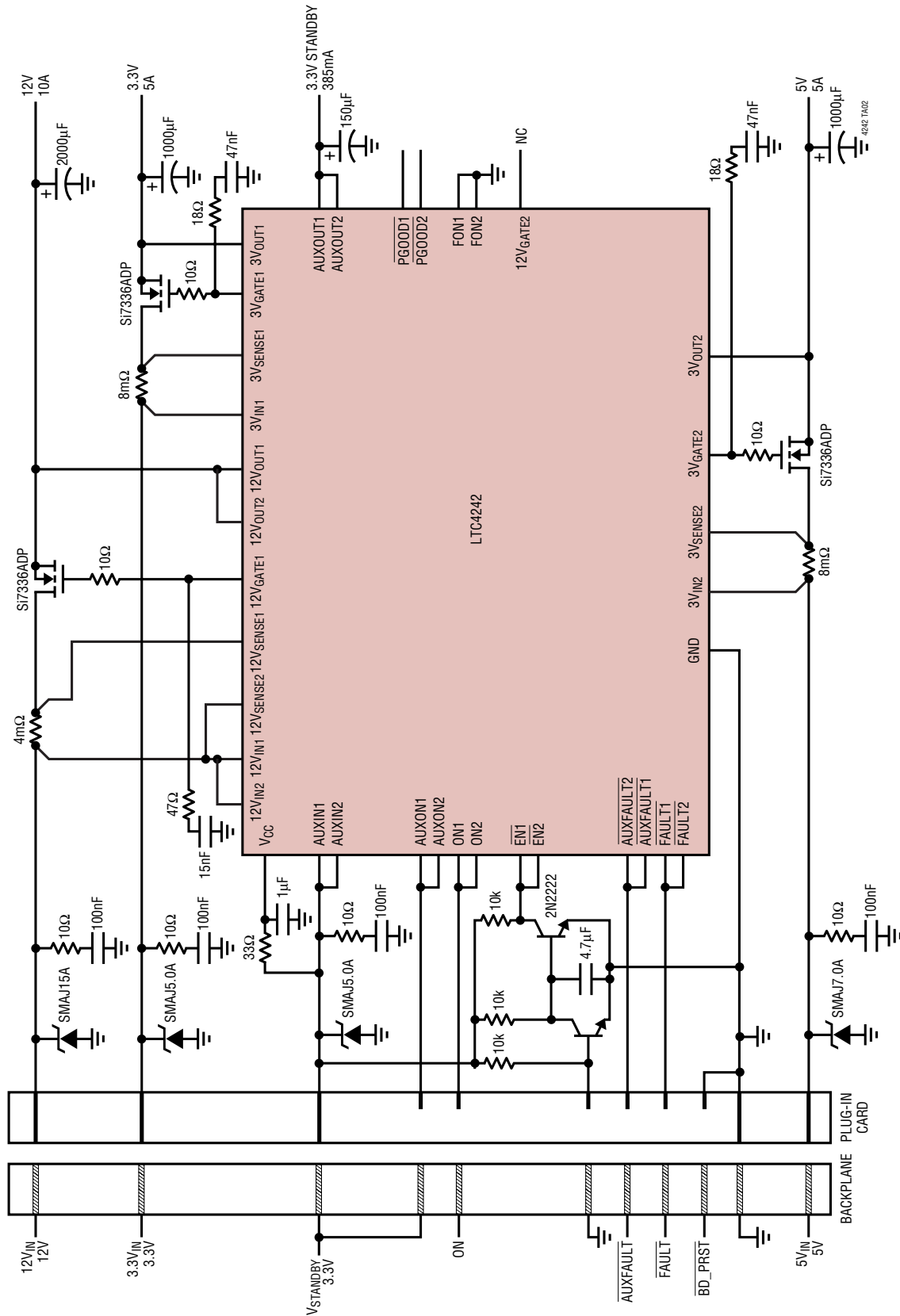
There is a 20 $\mu$ s filter time when large current of 2x circuit breaker's threshold can flow in the switches. This time is

short enough to cause minimal increase in the junction-to-ambient temperature of the MOSFETs, in the event of powering up into short circuit or short circuiting after power up. Therefore, in these events, it can be safely assumed that the MOSFETs would have minimal thermal stress on them.

If the LTC4242 operates in the diagnostic mode, user must ensure a safe joule heating limit of the external MOSFET. The internal switch will be disabled once the temperature reaches 150°C, thereby preventing overheating.

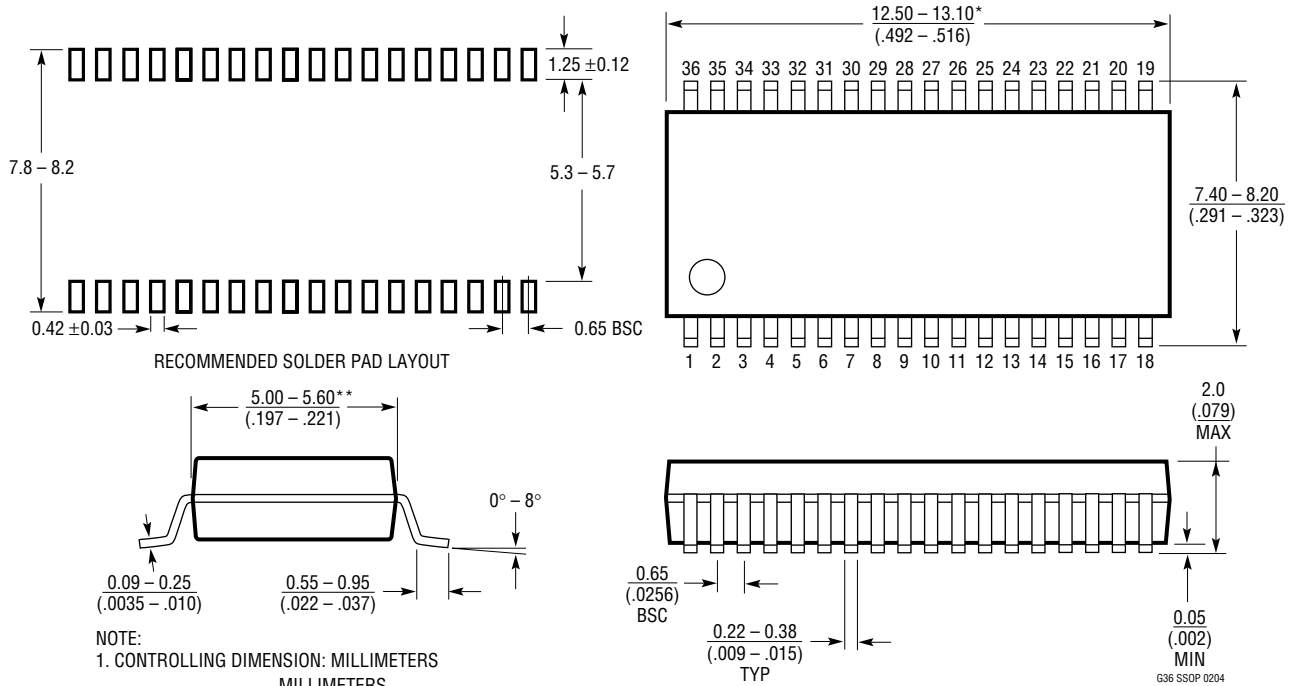
# TYPICAL APPLICATION

Standalone Hot Swap Application for Four Supplies: 12V, 5V, 3.3V and 3.3V Standby



**PACKAGE DESCRIPTION**

**G Package**  
**36-Lead Plastic SSOP (5.3mm)**  
 (Reference LTC DWG # 05-08-1640)

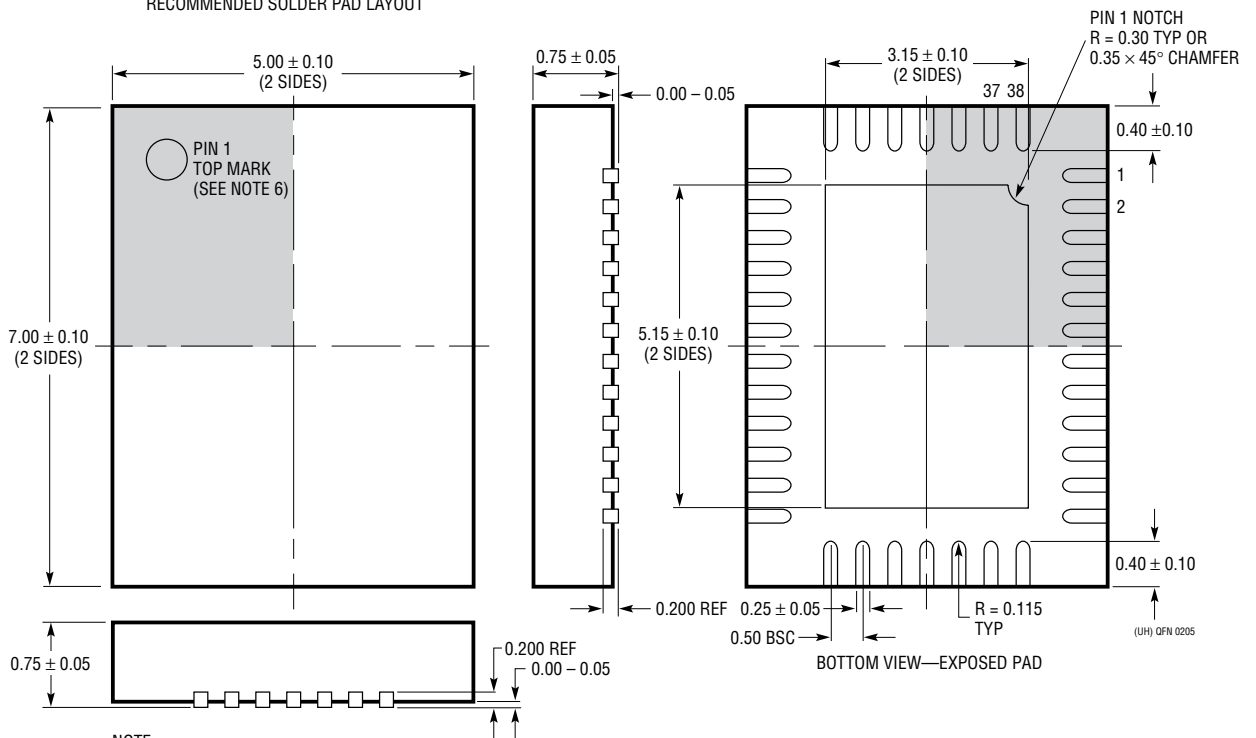
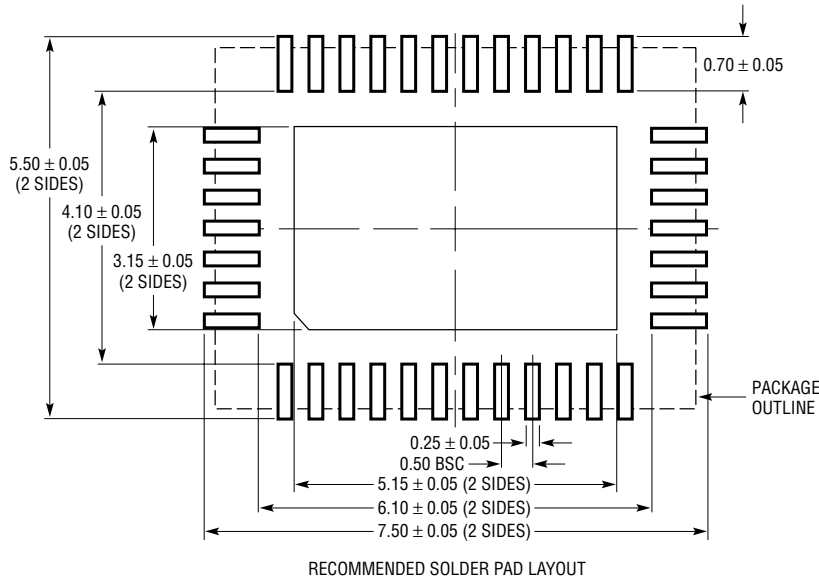


- NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
  2. DIMENSIONS ARE IN  $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
  3. DRAWING NOT TO SCALE
- \*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
- \*\*DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

G36 SSOP 0204

PACKAGE DESCRIPTION

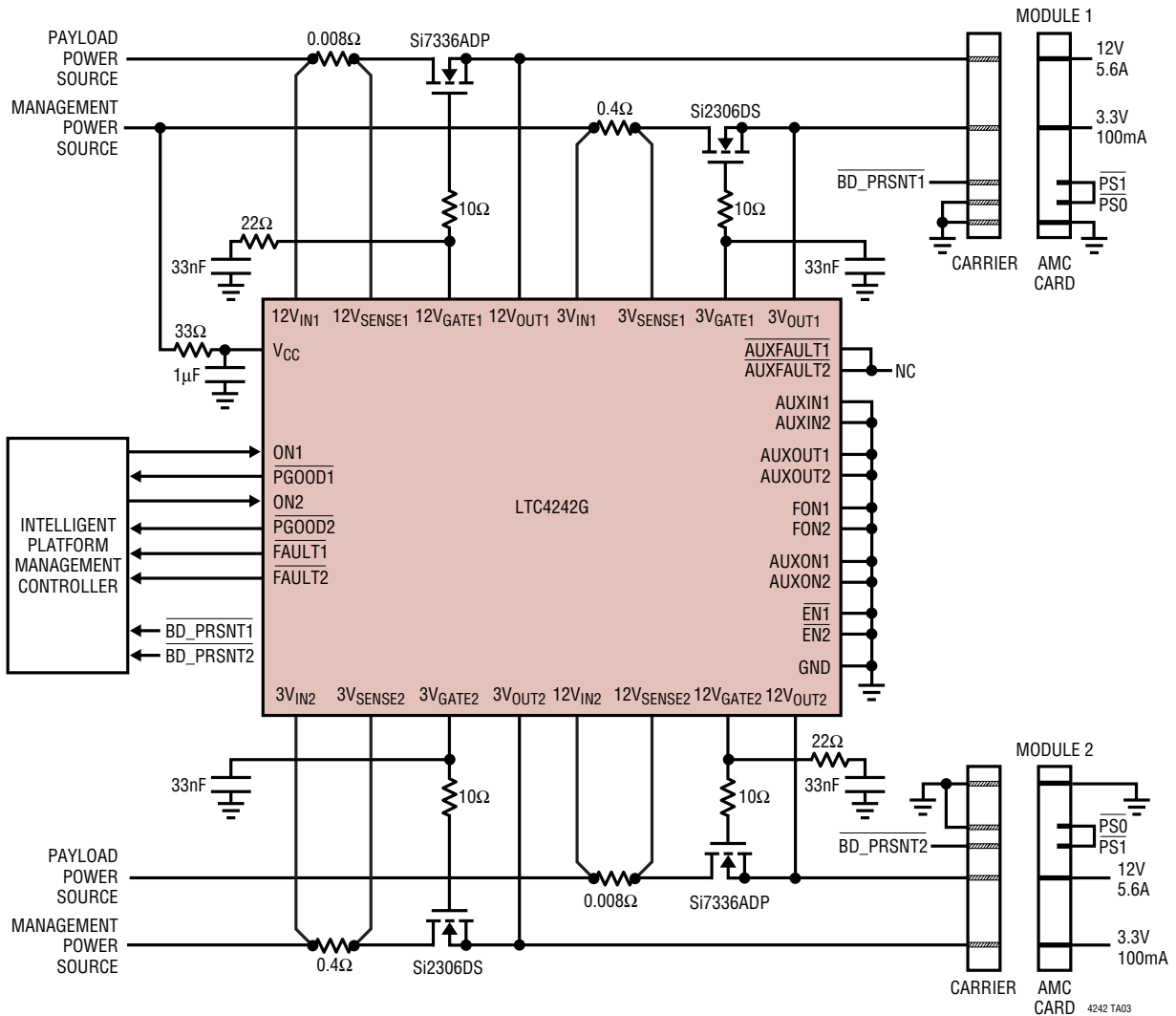
**UHF Package**  
**38-Lead Plastic QFN (5mm × 7mm)**  
 (Reference LTC DWG # 05-08-1701)



- NOTE:
- DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
  - DRAWING NOT TO SCALE
  - ALL DIMENSIONS ARE IN MILLIMETERS
  - DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
  - EXPOSED PAD SHALL BE SOLDER PLATED
  - SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## TYPICAL APPLICATION

### Hot Swap Application for Two Advanced Mezzanine Cards (AMC)



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4210	Hot Swap Contoller	6-Lead SOT-23 Package
LTC4213	No R <sub>SENSE</sub> <sup>™</sup> Electronic Circuit Breaker	Three Selectable Circuit Breaker Thresholds
LTC4214	Negative Low Voltage Hot Swap Controller	Controls Supplies from 0V to -16V
LTC4215	Hot Swap Controller with I <sup>2</sup> C Compatible Monitoring	2.9V to 15V, 8-Bit ADC Monitors Current and Voltages
LTC4216	Ultralow Voltage Hot Swap Controller	Load Voltages from 0V to 6V
LT <sup>®</sup> 4220	Dual Supply Hot Swap Controller	±2.7V to ±16V Operation
LTC4221	Dual Hot Swap Controller	Power Sequencer with Dual Speed, Dual Level Fault Protection
LTC4241	PCI-Bus Hot Swap Controller	3.3V Auxiliary Supply

No R<sub>SENSE</sub> is a trademark of Linear Technology Corporation.