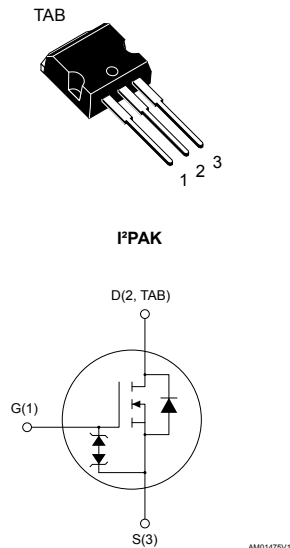


## N-channel 600 V, 0.230 $\Omega$ typ., 13 A MDmesh™ M2 EP Power MOSFET in an I<sup>2</sup>PAK package



### Features

| Order code    | V <sub>DS</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> |
|---------------|-----------------|--------------------------|----------------|
| STI20N60M2-EP | 600 V           | 0.278 $\Omega$           | 13 A           |

- Extremely low gate charge
- Excellent output capacitance (C<sub>OSS</sub>) profile
- Very low turn-off switching losses
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications
- Tailored for very high frequency converters (f > 150 kHz)

### Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 enhanced performance (EP) technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance, optimized switching characteristics with very low turn-off switching losses, rendering it suitable for the most demanding very high frequency converters.

#### Product status link

[STI20N60M2-EP](#)

#### Product summary

|            |                    |
|------------|--------------------|
| Order code | STI20N60M2-EP      |
| Marking    | 20N60M2EP          |
| Package    | I <sup>2</sup> PAK |
| Packing    | Tube               |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol         | Parameter                                                         | Value       | Unit               |
|----------------|-------------------------------------------------------------------|-------------|--------------------|
| $V_{GS}$       | Gate-source voltage                                               | $\pm 25$    | V                  |
| $I_D$          | Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$  | 13          | A                  |
| $I_D$          | Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$ | 8           | A                  |
| $I_{DM}^{(1)}$ | Drain current (pulsed)                                            | 52          | A                  |
| $P_{TOT}$      | Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$           | 110         | W                  |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope                                 | 15          | V/ns               |
| $dv/dt^{(3)}$  | MOSFET $dv/dt$ ruggedness                                         | 50          | V/ns               |
| $T_J$          | Operating junction temperature range                              | - 55 to 150 | $^{\circ}\text{C}$ |
| $T_{stg}$      | Storage temperature range                                         |             |                    |

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 13\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ;  $V_{DD} = 400\text{ V}$ .
3.  $V_{DS} \leq 480\text{ V}$

**Table 2. Thermal data**

| Symbol         | Parameter                           | Value | Unit                        |
|----------------|-------------------------------------|-------|-----------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case    | 1.14  | $^{\circ}\text{C}/\text{W}$ |
| $R_{thj-amb}$  | Thermal resistance junction-ambient | 62.5  | $^{\circ}\text{C}/\text{W}$ |

**Table 3. Avalanche characteristics**

| Symbol   | Parameter                                                                                                              | Value | Unit |
|----------|------------------------------------------------------------------------------------------------------------------------|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_{Jmax}$ )                                   | 2.7   | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AR}$ ; $V_{DD} = 50\text{ V}$ ) | 138   | mJ   |

## 2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

**Table 4. On/off states**

| Symbol        | Parameter                         | Test conditions                                                                             | Min. | Typ.  | Max.     | Unit          |
|---------------|-----------------------------------|---------------------------------------------------------------------------------------------|------|-------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$                                                 | 600  |       |          | V             |
| $I_{DSS}$     | Zero gate voltage                 | $V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$                                             |      |       | 1        | $\mu\text{A}$ |
|               | Drain current                     | $V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$ |      |       | 100      | $\mu\text{A}$ |
| $I_{GSS}$     | Gate-body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$                                          |      |       | $\pm 10$ | $\mu\text{A}$ |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                                          | 3.25 | 4     | 4.75     | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 6.5\text{ A}$                                               |      | 0.230 | 0.278    | $\Omega$      |

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

| Symbol                     | Parameter                     | Test conditions                                                                                                                              | Min. | Typ. | Max. | Unit        |
|----------------------------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|-------------|
| $C_{iss}$                  | Input capacitance             | $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$                                                                         | -    | 787  | -    | $\text{pF}$ |
| $C_{oss}$                  | Output capacitance            |                                                                                                                                              | -    | 50   | -    |             |
| $C_{rss}$                  | Reverse transfer capacitance  |                                                                                                                                              | -    | 1.2  | -    |             |
| $C_{oss\text{ eq.}}^{(1)}$ | Equivalent output capacitance | $V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$                                                                                  | -    | 89   | -    | $\text{pF}$ |
| $R_G$                      | Intrinsic gate resistance     | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$                                                                                                      | -    | 5.9  | -    | $\Omega$    |
| $Q_g$                      | Total gate charge             | $V_{DD} = 480\text{ V}$ , $I_D = 13\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$<br>(see Figure 15. Test circuit for gate charge behavior) | -    | 22   | -    | $\text{nC}$ |
| $Q_{gs}$                   | Gate-source charge            |                                                                                                                                              | -    | 3.5  | -    |             |
| $Q_{gd}$                   | Gate-drain charge             |                                                                                                                                              | -    | 10.5 | -    |             |

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching energy**

| Symbol    | Parameter                                        | Test conditions                                                                                      | Min. | Typ. | Max. | Unit          |
|-----------|--------------------------------------------------|------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $E_{off}$ | Turn-off energy (from 90% $V_{GS}$ to 0% $I_D$ ) | $V_{DD} = 400\text{ V}$ , $I_D = 2\text{ A}$ , $R_G = 4.7\text{ }\Omega$ ,<br>$V_{GS} = 10\text{ V}$ | -    | 7.2  | -    | $\mu\text{J}$ |
|           |                                                  | $V_{DD} = 400\text{ V}$ , $I_D = 5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ ,<br>$V_{GS} = 10\text{ V}$ | -    | 20.4 | -    | $\mu\text{J}$ |

**Table 7. Switching times**

| Symbol       | Parameter           | Test conditions                                                                                                                                                                                          | Min. | Typ. | Max. | Unit |
|--------------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 300\text{ V}$ , $I_D = 6.5\text{ A}$ , $R_G = 4.7\ \Omega$ ,<br>$V_{GS} = 10\text{ V}$ (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform) | -    | 10.5 | -    | ns   |
| $t_r$        | Rise time           |                                                                                                                                                                                                          | -    | 5.2  | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time |                                                                                                                                                                                                          | -    | 41   | -    | ns   |
| $t_f$        | Fall time           |                                                                                                                                                                                                          | -    | 8    | -    | ns   |

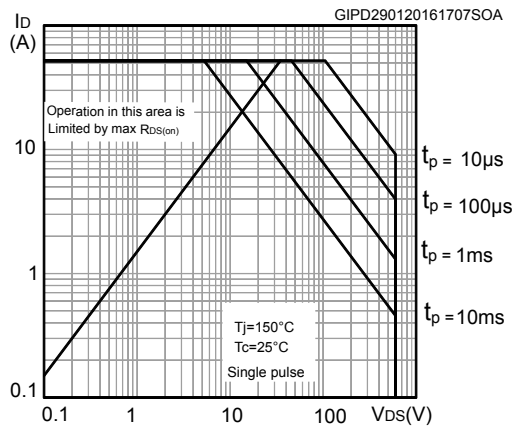
**Table 8. Source-drain diode**

| Symbol          | Parameter                     | Test conditions                                                                                                                                                                                                 | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                                                                                                 | -    |      | 13   | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                                                                                                 | -    |      | 52   | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $V_{GS} = 0\text{ V}$ , $I_{SD} = 13\text{ A}$                                                                                                                                                                  | -    |      | 1.6  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 13\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$<br>(see Figure 16. Test circuit for inductive load switching and diode recovery times )                                    | -    | 230  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                 | -    | 2.3  |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                 | -    | 20   |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 13\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ ,<br>$T_j = 150\text{ }^\circ\text{C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times) | -    | 287  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                 | -    | 2.9  |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                 | -    | 20.2 |      | A             |

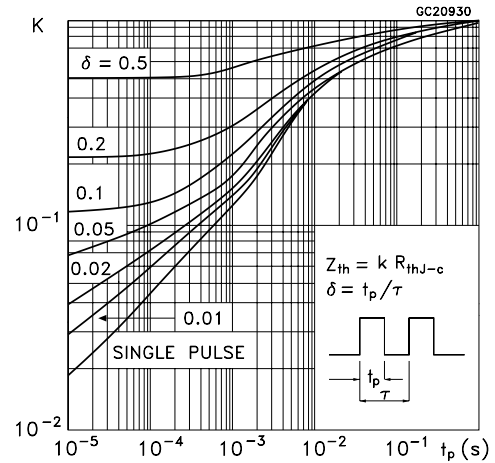
1. Pulse width is limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

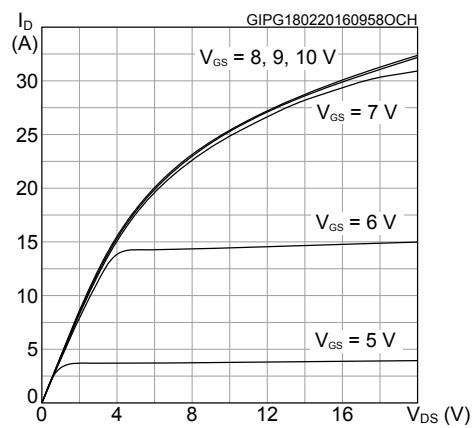
**Figure 1. Safe operating area**



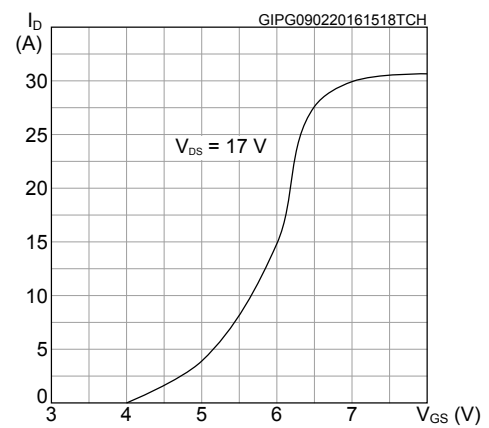
**Figure 2. Thermal impedance**



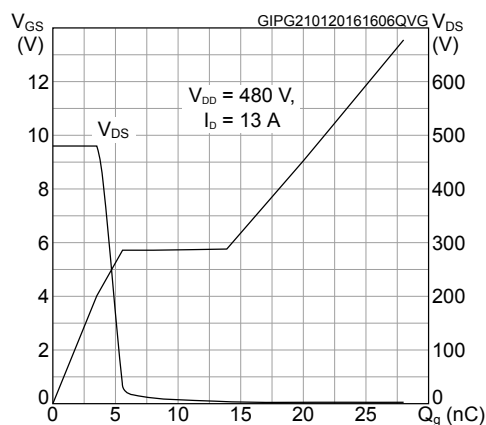
**Figure 3. Output characteristics**



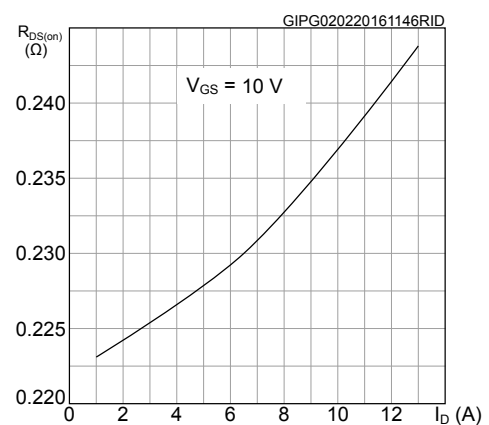
**Figure 4. Transfer characteristics**

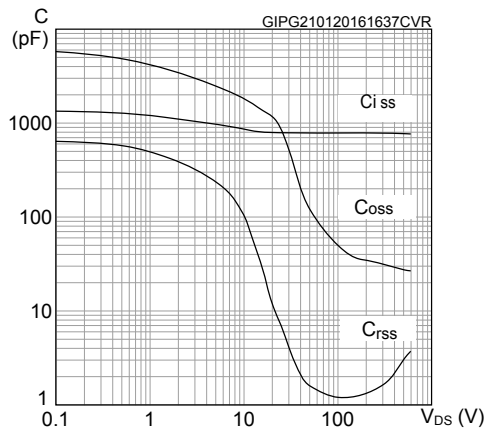
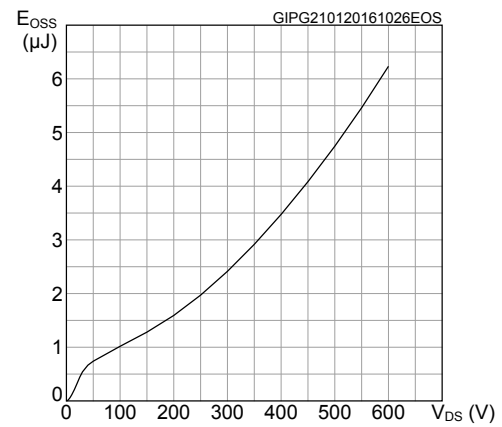
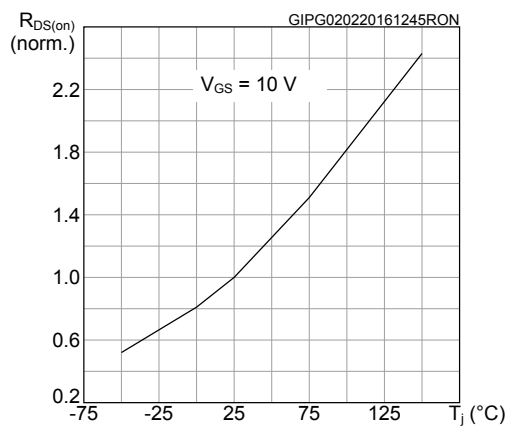
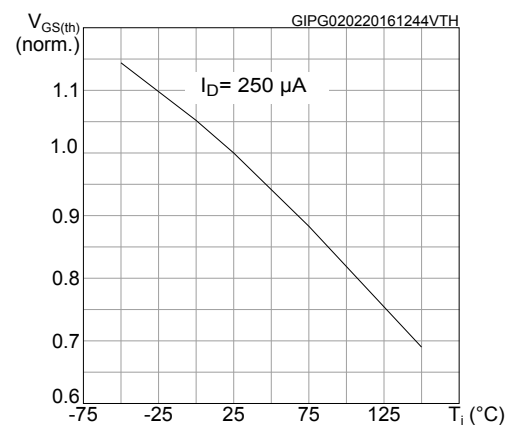
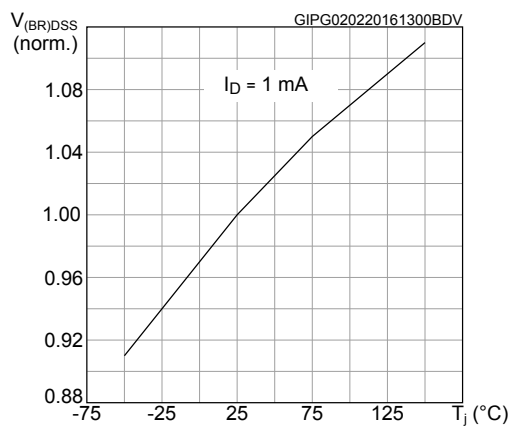
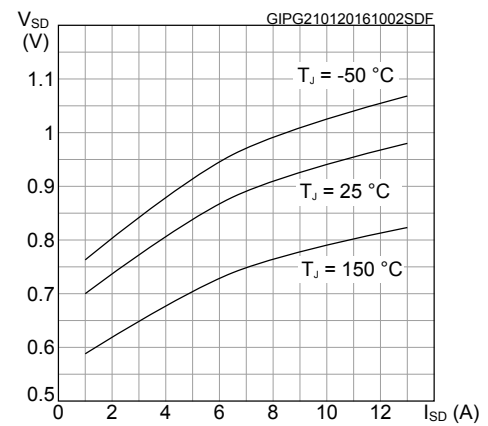


**Figure 5. Gate charge vs gate-source voltage**

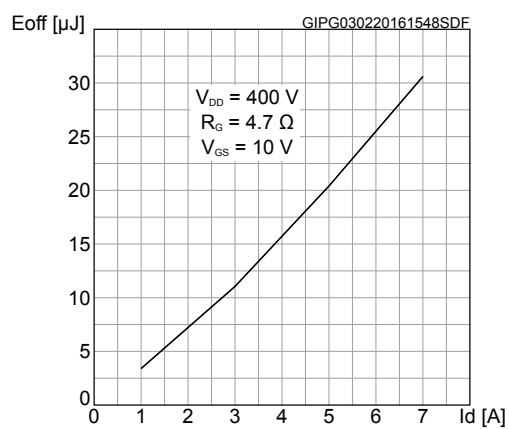


**Figure 6. Static drain-source on-resistance**

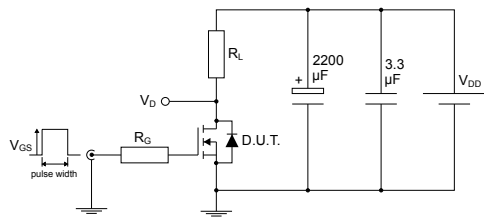


**Figure 7. Capacitance variations**

**Figure 8. Output capacitance stored energy**

**Figure 9. Normalized on-resistance vs temperature**

**Figure 10. Normalized gate threshold voltage vs temperature**

**Figure 11. Normalized  $V_{(BR)DSS}$  vs temperature**

**Figure 12. Source-drain diode forward characteristics**


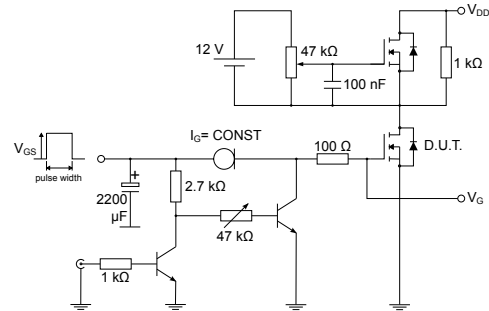
**Figure 13. Turn-off switching energy vs drain current**



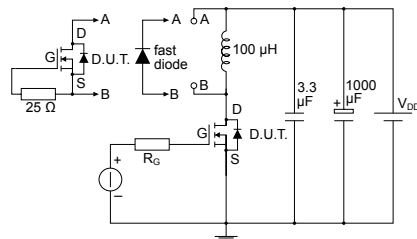
### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**


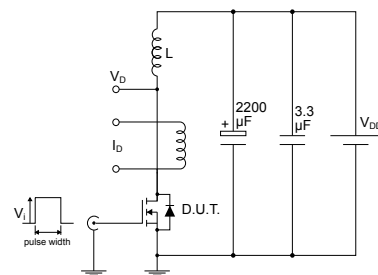
AM01468v1

**Figure 15. Test circuit for gate charge behavior**


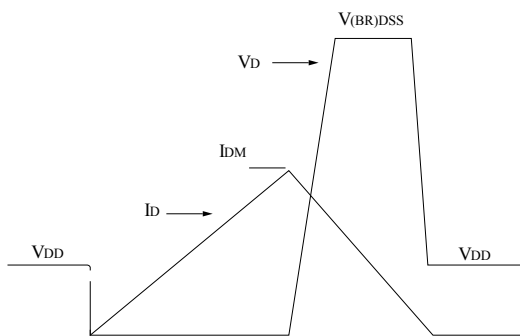
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**Figure 16. Test circuit for inductive load switching and diode recovery times**


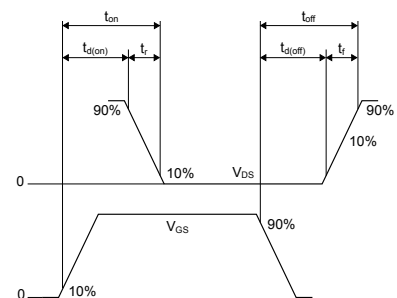
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**Figure 17. Unclamped inductive load test circuit**


AM01471v1

**Figure 18. Unclamped inductive waveform**


AM01472v1

**Figure 19. Switching time waveform**


AM01473v1

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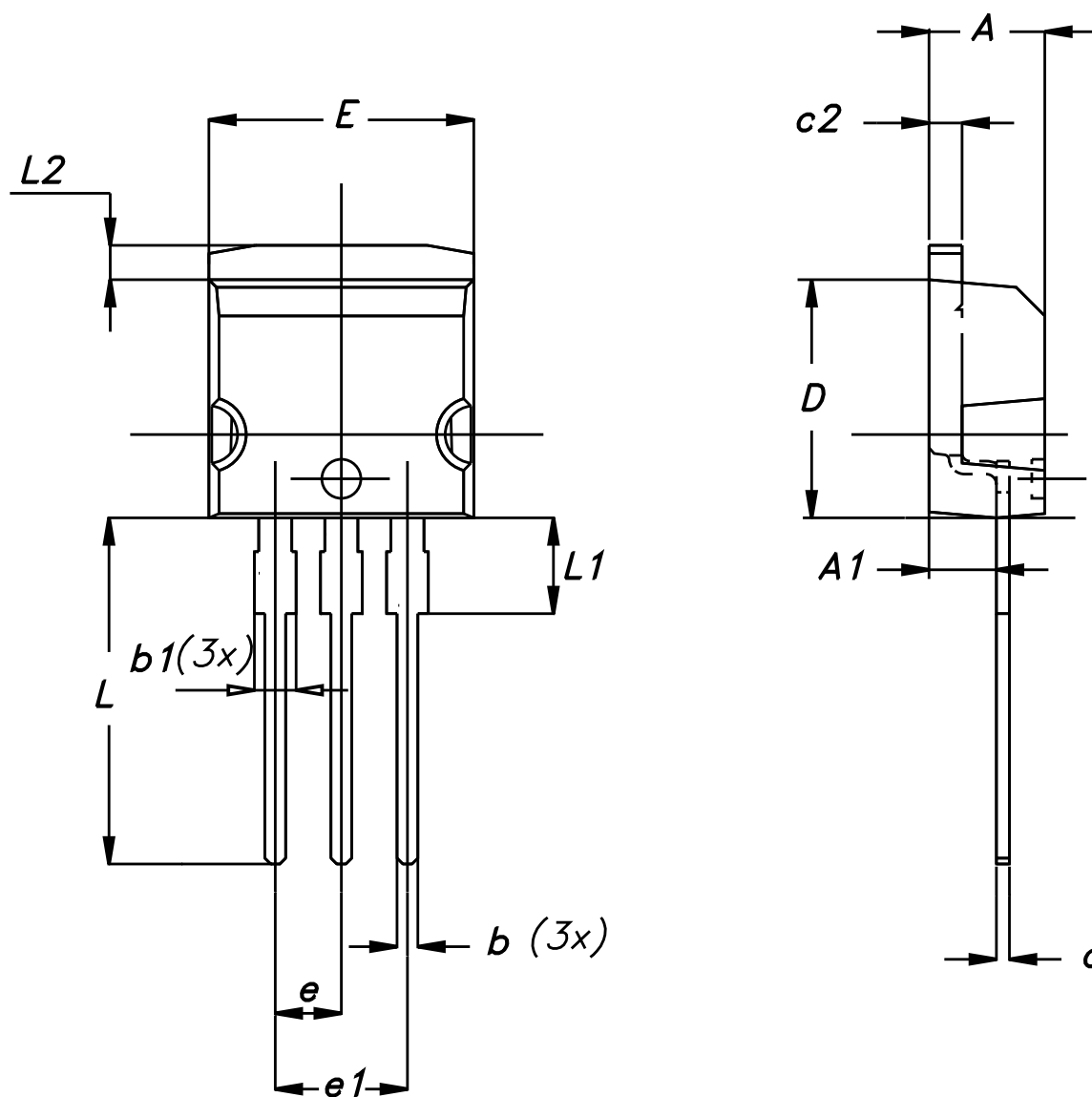
## 4 Package information

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In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

## 4.1 TO-220 package information

Figure 20. I<sup>2</sup>PAK package outline



0004982\_Rev\_H

**Table 9.** I<sup>2</sup>PAK package mechanical data

| Dim. | mm   |      |       |
|------|------|------|-------|
|      | Min. | Typ. | Max.  |
| A    | 4.40 | -    | 4.60  |
| A1   | 2.40 | -    | 2.72  |
| b    | 0.61 | -    | 0.88  |
| b1   | 1.14 | -    | 1.70  |
| c    | 0.49 | -    | 0.70  |
| c2   | 1.23 | -    | 1.32  |
| D    | 8.95 | -    | 9.35  |
| e    | 2.40 | -    | 2.70  |
| e1   | 4.95 | -    | 5.15  |
| E    | 10   | -    | 10.40 |
| L    | 13   | -    | 14    |
| L1   | 3.50 | -    | 3.93  |
| L2   | 1.27 | -    | 1.40  |

## Revision history

**Table 10. Document revision history**

| Date        | Revision | Changes                                                                                                                             |
|-------------|----------|-------------------------------------------------------------------------------------------------------------------------------------|
| 20-Mar-2018 | 1        | First release, the part number previously included in DS11505.<br>The document status is production data.                           |
| 04-Jun-2018 | 2        | Modified <a href="#">Table 1. Absolute maximum ratings</a> and <a href="#">Table 8. Source-drain diode</a> .<br>Minor text changes. |

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