# CYBLE-214015-01

# EZ-BLE™ Creator Module

## General Description

The Cypress CYBLE-214015-01 is a fully certified and qualified module supporting Bluetooth® Low Energy (BLE) wireless communication. The CYBLE-214015-01 is a turnkey solution and includes onboard crystal oscillators, trace antenna, passive components, and the Cypress PSoC 4 BLE. Refer to the PSoC 4 BLE datasheet for additional details on the capabilities of the PSoC 4 BLE device used on this module.

The EZ-BLE™ Creator module is a scalable and reconfigurable platform architecture. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. The CYBLE-214015-01 also includes digital programmable logic, high-performance analog-to-digital conversion (ADC), opamps with comparator mode, and standard communication and timing peripherals.

The CYBLE-214015-01 includes a royalty-free BLE stack compatible with Bluetooth 4.2 and provides up to 25 GPIOs in a small 11 × 11 × 1.80 mm package. The CYBLE-214015-01 is drop-in compatible with the CYBLE-014008-00 and CYBLE-214009-00 EZ-BLE Modules.

The CYBLE-214015-01 is a complete solution and an ideal fit for applications seeking a highly integrated BLE wireless solution.

### Module Description

- Module size: 11.0 mm × 11.0 mm × 1.80 mm (with shield)
- Drop-in compatible with CYBLE-014008-00 and CYBLE-214009-00
- 256-KB flash memory, 32-KB SRAM memory
- Up to 25 GPIOs configurable as open drain high/low, pull-up/pull-down, HI-Z analog, HI-Z digial, or strong output
- Bluetooth 4.2 qualified single-mode module
  - QDID: 79480
  - Declaration ID: D029646
- Certified to FCC, CE, MIC, KC, and ISED regulations
- Industrial temperature range: –40 °C to +85 °C
- 32-bit processor (0.9 DMIPS/MHz) with single-cycle 32-bit multiply, operating at up to 48 MHz
- Watchdog timer with dedicated internal low-speed oscillator (ILO)
- Two-pin SWD for programming

### Power Consumption

- TX output power: –18 dbm to +3 dbm
- Received signal strength indicator (RSSI) with 1-dB resolution
- TX current consumption of 15.6 mA (radio only, 0 dbm)
- RX current consumption of 16.4 mA (radio only)
- Low power mode support
  - Deep Sleep: 1.3 µA with watch crystal oscillator (WCO) on
  - Hibernate: 150 nA with SRAM retention
  - Stop: 60 nA with XRES wakeup

### Programmable Analog

- Four opamps with reconfigurable high-drive external and high-bandwidth internal drive, comparator modes, and ADC input buffering capability; can operate in Deep-Sleep mode
- 12-bit, 1-Msps SAR ADC with differential and single-ended modes; channel sequencer with signal averaging
- Two current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin
- One low-power comparator that operate in Deep-Sleep mode

### Programmable Digital

- Four programmable logic blocks called universal digital blocks, (UDBs), each with eight macrocells and datapath
- Cypress-provided peripheral Component library, user-defined state machines, and Verilog input

### Capacitive Sensing

- Cypress CapSense Sigma-Delta (CSD) provides best-in-class SNR (> 5:1) and liquid tolerance
- Cypress-supplied software component makes capacitive-sensing design easy
- Automatic hardware-tuning algorithm (SmartSense™)

### Segment LCD Drive

- LCD drive supported on all GPIOs (common or segment)
- Operates in Deep-Sleep mode with four bits per pin memory

### Serial Communication

- Two independent runtime reconfigurable serial communication blocks (SCBs) with $I^2C$, SPI, or UART functionality

### Timing and Pulse-Width Modulation

- Four 16-bit timer, counter, pulse-width modulator (TCPWM) blocks
- Center-aligned, Edge, and Pseudo-random modes
- Comparator-based triggering of Kill signals for motor drive and other high-reliability digital logic applications

### Up to 25 Programmable GPIOs

- Any GPIO pin can be CapSense, LCD, analog, or digital

## More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

- Overview: EZ-BLE Module Portfolio, Module Roadmap
- PSoC 4 BLE Silicon Datasheet
- Application notes: Cypress offers a number of BLE application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with EZ-BLE modules are:
  - AN96841 - Getting Started with EZ-BLE Module
  - AN91267 - Getting Started with PSoC® 4 BLE
  - AN97060 - PSoC® 4 BLE and PRoC™ BLE - Over-The-Air (OTA) Device Firmware Upgrade (DFU) Guide
  - AN91162 - Creating a BLE Custom Profile
  - AN91184 - PSoC 4 BLE - Designing BLE Applications
  - AN92584 - Designing for Low Power and Estimating Battery Life for BLE Applications
  - AN85951 - PSoC® 4 CapSense® Design Guide
  - AN95089 - PSoC® 4/PRoC™ BLE Crystal Oscillator Selection and Tuning Techniques
  - AN91445 - Antenna Design and RF Layout Guidelines
- Technical Reference Manual (TRM):
  - PSoC® 4 BLE Technical Reference Manual
  - PSOC(R) 4 BLE Registers Technical Reference Manual
- Knowledge Base Articles
  - KBA210574 - RF Regulatory Certifications for CY-BLE-014008-00, CYBLE-214009-00, and CY-BLE-214015-01 EZ-BLE™ Creator Modules
  - KBA216236 - Pin Mapping Differences Between the EZ-BLE™ Creator Evaluation Board (CYBLE-214015-EVAL) and the BLE Pioneer Kit (CY8CKIT-042-BLE)
  - KBA97095 - EZ-BLE™ Module Placement
  - KBA213976 - FAQ for BLE and Regulatory Certifications with EZ-BLE modules
  - KBA210802 - Queries on BLE Qualification and Declaration Processes
  - KBA2108122 - 3D Model Files for EZ-BLE/EZ-BT Modules
- Development Kits:
  - CYBLE-214015-EVAL, CYBLE-214015-01 Evaluation Board
  - CY8CKIT-042-BLE, Bluetooth® Low Energy (BLE) Pioneer Kit
  - CY8CKIT-002, PSoC® MiniProg3 Program and Debug Kit
- Test and Debug Tools:
  - CYSmart, Bluetooth® LE Test and Debug Tool (Windows)
  - CYSmart Mobile, Bluetooth® LE Test and Debug Tool (Android/iOS Mobile App)

## Two Easy-To-Use Design Environments to Get You Started Quickly

### PSoC® Creator™ Integrated Design Environment (IDE)

PSoC Creator is an Integrated Design Environment (IDE) that enables concurrent hardware and firmware editing, compiling and debugging of PSoC 3, PSoC 4, PSoC 5LP, PSoC 4 BLE, and EZ-BLE module systems with no code size limitations. PSoC peripherals are designed using schematic capture and simple graphical user interface (GUI) with over 120 pre-verified, production-ready PSoC Components™.

PSoC Components are analog and digital “virtual chips,” represented by an icon that users can drag-and-drop into a design and configure to suit a broad array of application requirements.

*Bluetooth Low Energy Component*

The Bluetooth Low Energy Component inside PSoC Creator provides a comprehensive GUI-based configuration window that lets you quickly design BLE applications. The Component incorporates a Bluetooth Core Specification v4.2 compliant BLE protocol stack and provides API functions to enable user applications to interface with the underlying Bluetooth Low Energy Sub-System (BLESS) hardware via the stack.

### EZ-Serial™ BLE Firmware Platform

The EZ-Serial Firmware Platform provides a simple way to access the most common hardware and communication features needed in BLE applications. EZ-Serial implements an intuitive API protocol over the UART interface and exposes various status and control signals through the module’s GPIOs, making it easy to add BLE functionality quickly to existing designs.

Use a simple serial terminal and evaluation kit to begin development without requiring an IDE. Refer to the EZ-Serial web page for User Manuals and instructions for getting started as well as detailed reference materials.

EZ-BLE modules are pre-flashed with the EZ-Serial Firmware Platform. If you do not have EZ-Serial pre-loaded on your module, you can download each EZ-BLE module’s firmware images on the EZ-Serial web page.

## Technical Support

- Frequently Asked Questions (FAQs): Learn more about our BLE ECO System.
- Forum: See if your question is already answered by fellow developers on the PSoC 4 BLE.
- Visit our support page and create a technical support case or contact a local sales representatives. If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 2 at the prompt.

## Contents

# Overview

## Module Description

The CYBLE-214015-01 module is a complete module designed to be soldered to the main host board.

*Module Dimensions and Drawing*

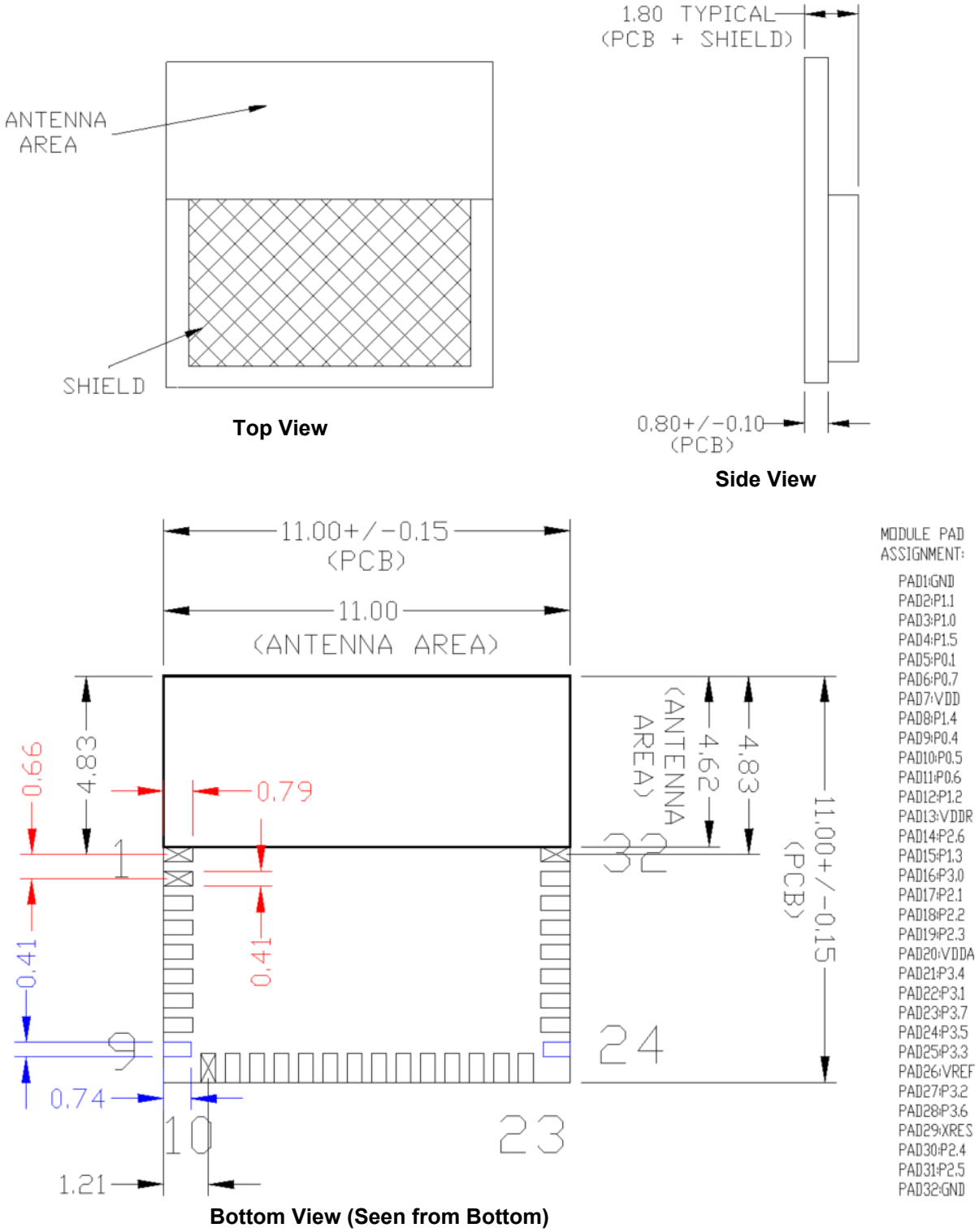
Cypress reserves the right to select components (including the appropriate BLE device) from various vendors to achieve the BLE module functionality. Such selections will guarantee that all height restrictions of the component area are maintained. Designs should be completed with the physical dimensions shown in the mechanical drawings in Figure 1. All dimensions are in millimeters (mm).

**Table 1. Module Design Dimensions**

| Dimension Item | | Specification |
|---|---|---|
| Module dimensions | Length (X) | 11.00 ± 0.15 mm |
| | Width (Y) | 11.00 ± 0.15 mm |
| Antenna location dimensions | Length (X) | 11.00 ± 0.15 mm |
| | Width (Y) | 4.62 ± 0.15 mm |
| PCB thickness | Height (H) | 0.80 ± 0.10 mm |
| Shield height | Height (H) | 1.00 ± 0.10 mm |
| Maximum component height | Height (H) | 1.00 mm typical (shield) |
| Total module thickness (bottom of module to highest component) | Height (H) | 1.80 mm typical |

See Figure 1 on page 5 for the mechanical reference drawing for CYBLE-214015-01.

**Figure 1. Module Mechanical Drawing**




**Top View**

**Side View**

**Bottom View (Seen from Bottom)**

**Note**

1. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see Figure 3 on page 6, Figure 4 and Figure 5 on page 7, and Figure 6 and Table 3 on page 8.

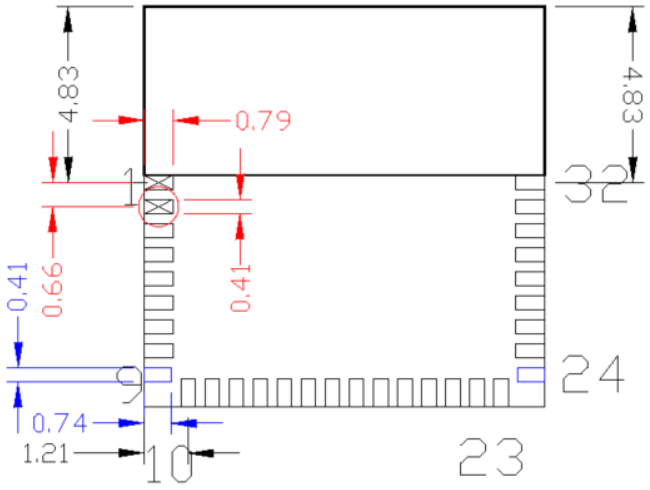
## Pad Connection Interface

As shown in the bottom view of Figure 1 on page 5, the CYBLE-214015-01 connects to the host board via solder pads on the back of the module. Table 2 and Figure 2 detail the solder pad length, width, and pitch dimensions of the CYBLE-214015-01 module.

**Table 2. Solder Pad Connection Description**

| Name | Connections | Connection Type | Pad Length Dimension | Pad Width Dimension | Pad Pitch |
|---|---|---|---|---|---|
| SP | 32 | Solder Pads | Pad9/Pad24: 0.74 mm<br>All Others: 0.79 mm | 0.41 mm | 0.66 mm |

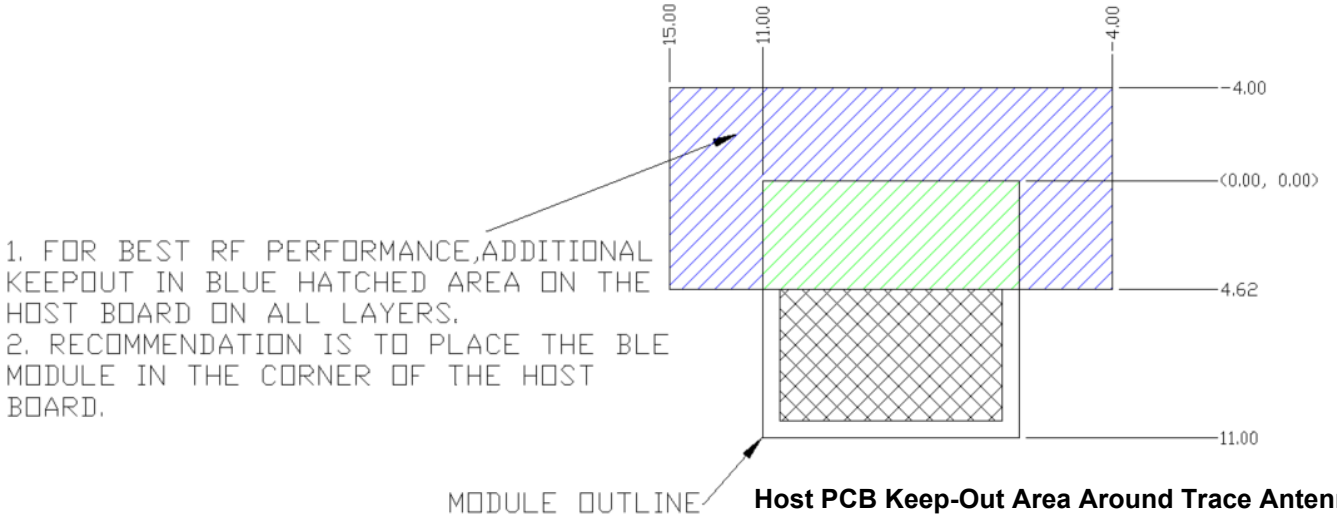
**Figure 2. Solder Pad Dimensions (Seen from Bottom)**




To maximize RF performance, the host layout should follow these recommendations:

1. The ideal placement of the Cypress BLE module is in a corner of the host board with the antenna located on the edge of the host board. This placement minimizes the additional recommended keep-out area stated in item 2. Refer to AN96841 for module placement best practices.
2. To maximize RF performance, the area immediately around the Cypress BLE module trace antenna should contain an additional keep-out area, where no grounding or signal traces are contained. The keep-out area applies to all layers of the host board. The recommended dimensions of the host PCB keep-out area are shown in Figure 3 (dimensions are in mm).

**Figure 3. Recommended Host PCB Keep-Out Area Around the CYBLE-214015-01 Trace Antenna**

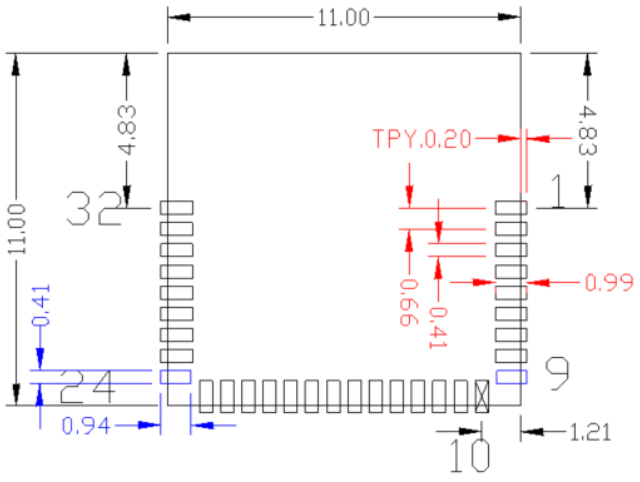



**Host PCB Keep-Out Area Around Trace Antenna**

## Recommended Host PCB Layout

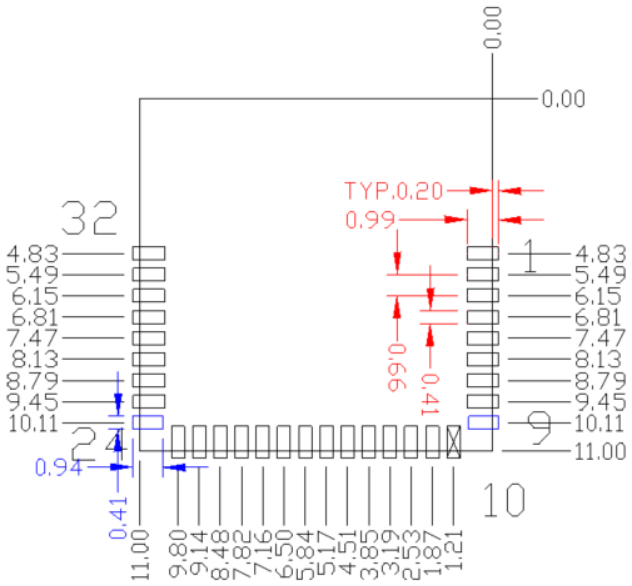
Figure 4 through Figure 6 and Table 3 provide details that can be used for the recommended host PCB layout pattern for the CYBLE-214015-01. Dimensions are in millimeters unless otherwise noted. Pad length of 0.99 mm (0.494 mm from center of the pad on either side) shown in Figure 6 is the minimum recommended host pad length. The host PCB layout pattern can be completed using either Figure 4, Figure 5, or Figure 6. It is not necessary to use all figures to complete the host PCB layout pattern.

**Figure 4. Host Layout Pattern for CYBLE-214015-01**




**Top View (Seen on Host PCB)**

**Figure 5. Module Pad Location from Origin**



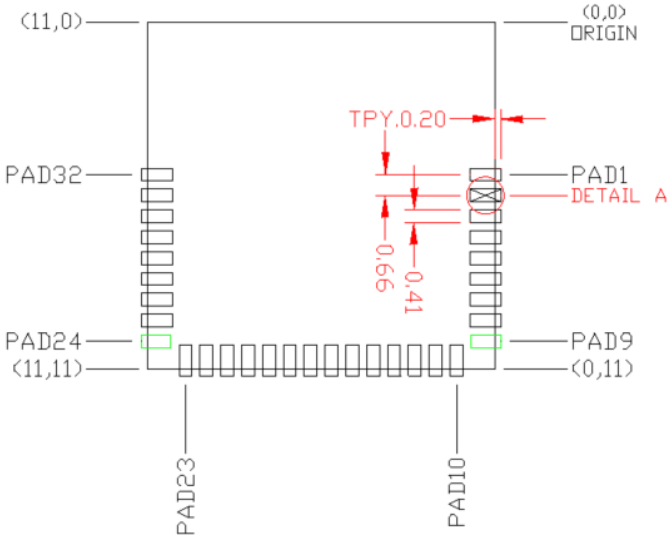

**Top View (Seen on Host PCB)**

Table 3 provides the center location for each solder pad on the CYBLE-214015-01. All dimensions are referenced to the center of the solder pad. Refer to Figure 6 for the location of each module solder pad.

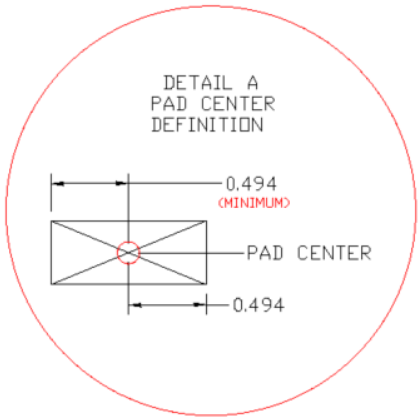
**Table 3. Module Solder Pad Location**

| Solder Pad (Center of Pad) | Location (X,Y) from Origin (mm) | Dimension from Origin (mils) |
|---|---|---|
| 1 | (0.30, 4.83) | (11.81, 190.16) |
| 2 | (0.30, 5.49) | (11.81, 216.14) |
| 3 | (0.30, 6.15) | (11.81, 242.13) |
| 4 | (0.30, 6.81) | (11.81, 268.11) |
| 5 | (0.30, 7.47) | (11.81, 294.09) |
| 6 | (0.30, 8.13) | (11.81, 320.08) |
| 7 | (0.30, 8.79) | (11.81, 346.06) |
| 8 | (0.30, 9.45) | (11.81, 372.05) |
| 9 | (0.27, 10.11) | (10.63, 398.03) |
| 10 | (1.21, 10.70) | (47.64, 421.26) |
| 11 | (1.87, 10.70) | (73.62, 421.26) |
| 12 | (2.53, 10.70) | (99.61, 421.26) |
| 13 | (3.19, 10.70) | (125.59, 421.26) |
| 14 | (3.85, 10.70) | (151.57, 421.26) |
| 15 | (4.51, 10.70) | (177.56, 421.26) |
| 16 | (5.17, 10.70) | (203.54, 421.26) |
| 17 | (5.84, 10.70) | (229.92, 421.26) |
| 18 | (6.50, 10.70) | (255.91, 421.26) |
| 19 | (7.16, 10.70) | (281.89, 421.26) |
| 20 | (7.82, 10.70) | (307.87, 421.26) |
| 21 | (8.48, 10.70) | (333.86, 421.26) |
| 22 | (9.14, 10.70) | (359.84, 421.26) |
| 23 | (9.80, 10.70) | (385.83, 421.26) |
| 24 | (10.73, 10.11) | (422.44, 398.03) |
| 25 | (10.70, 9.45) | (421.26, 372.05) |
| 26 | (10.70, 8.79) | (421.26, 346.06) |
| 27 | (10.70, 8.13) | (421.26, 320.08) |
| 28 | (10.70, 7.47) | (421.26, 294.09) |
| 29 | (10.70, 6.81) | (421.26, 268.11) |
| 30 | (10.70, 6.15) | (421.26, 242.13) |
| 31 | (10.70, 5.49) | (421.26, 216.14) |
| 32 | (10.70, 4.83) | (421.26, 190.16) |

**Figure 6. Solder Pad Reference Location**




**Top View (Seen on Host PCB)**



## Digital and Analog Capabilities and Connections

Table 4 and Table 5 detail the solder pad connection definitions and available functions for each connection pad. Table 4 lists the solder pads on CYBLE-214015-01, the BLE device port-pin, and denotes whether the digital function shown is available for each solder pad. Table 5 denotes whether the analog function shown is available for each solder pad. Each connection is configurable for a single option shown with a ✓.

**Table 4. Digital Peripheral Capabilities**

| Pad Number | Device Port Pin | UART | SPI | $I^2C$ | TCPWM[2,3] | Cap Sense | WCO Out | ECO OUT | LCD | SWD | GPIO |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | GND[4] | Ground Connection | | | | | | | | | |
| 2 | P1.1 | | ✓(SCB1_SS1) | | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 3 | P1.0 | | | | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 4 | P1.5 | ✓(SCB0_TX) | ✓(SCB0_MISO) | ✓(SCB0_SCL) | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 5 | P0.1 | ✓(SCB1_TX) | ✓(SCB1_MISO) | ✓(SCB1_SCL) | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 6 | P0.7 | ✓(SCB0_CTS) | ✓(SCB0_SCLK) | | ✓(TCPWM) | ✓ | | | ✓ | ✓ (SWDCLK) | ✓ |
| 7 | VDD | Digital Power Supply Input (1.71 to 5.5V) | | | | | | | | | |
| 8 | P1.4 | ✓(SCB0_RX) | ✓(SCB0_MOSI) | ✓(SCB0_SDA) | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 9 | P0.4 | ✓(SCB0_RX) | ✓(SCB0_MOSI) | ✓(SCB0_SDA) | ✓(TCPWM) | ✓ | | ✓ | ✓ | | ✓ |
| 10 | P0.5 | ✓(SCB0_TX) | ✓(SCB0_MISO) | ✓(SCB0_SCL) | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 11 | P0.6 | ✓(SCB0_RTS) | ✓(SCB0_SS0) | | ✓(TCPWM) | ✓ | | | ✓ | ✓ (SWDIO) | ✓ |
| 12 | P1.2 | | ✓(SCB1_SS2) | | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 13 | $V_{DDR}$ | Radio Power Supply (1.9V to 5.5V) | | | | | | | | | |
| 14 | P2.6 | | | | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 15 | P1.3 | | ✓(SCB1_SS3) | | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 16 | P3.0 | ✓(SCB0_RX) | | ✓(SCB0_SDA) | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 17 | P2.1 | | ✓(SCB0_SS2) | | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 18 | P2.2 | | ✓(SCB0_SS3) | | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 19 | P2.3 | | | | ✓(TCPWM) | ✓ | ✓ | | ✓ | | ✓ |
| 20 | VDDA | Analog Power Supply Input (1.71 to 5.5V) | | | | | | | | | |
| 21 | P3.4 | ✓(SCB1_RX) | | ✓(SCB1_SDA) | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 22 | P3.1 | ✓(SCB0_TX) | | ✓(SCB0_SCL) | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 23 | P3.7 | ✓(SCB1_CTS) | | | ✓(TCPWM) | ✓ | ✓ | | ✓ | | ✓ |
| 24 | P3.5 | ✓(SCB1_TX) | | ✓(SCB1_SCL) | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 25 | P3.3 | ✓(SCB0_CTS) | | | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 26 | VREF | Reference Voltage Input | | | | | | | | | |
| 27 | P3.2 | ✓(SCB0_RTS) | | | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 28 | P3.6 | ✓(SCB1_RTS) | | | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 29 | XRES | External Reset Hardware Connection Input | | | | | | | | | |
| 30 | P2.4 | | | | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 31 | P2.5 | | | | ✓(TCPWM) | ✓ | | | ✓ | | ✓ |
| 32 | GND[4] | Ground Connection | | | | | | | | | |

**Notes**
2. TCPWM stands for timer, counter, and PWM. If supported, the pad can be configured to any of these peripheral functions.
3. TCPWM connections on ports 0, 1, 2, and 3 can be routed through the Digital Signal Interconnect (DSI) to any of the TCPWM blocks and can be either positive or negative polarity.
4. The main board needs to connect both GND connections (Pad 1 and Pad 32) on the module to the common ground of the system.

**Table 5. Analog Peripheral Capabilities**

| Pad Number | Device Port Pin | SARMUX | OPAMP | LPCOMP |
|---|---|---|---|---|
| 1 | GND[4] | Ground Connection | | |
| 2 | P1.1 | | ✓(CTBm1_OA0_INN) | |
| 3 | P1.0 | | ✓(CTBm1_OA0_INP) | |
| 4 | P1.5 | | ✓(CTBm1_OA1_INP) | |
| 5 | P0.1 | | | |
| 6 | P0.7 | | | |
| 7 | VDD | Digital Power Supply Input (1.71 to 5.5V) | | |
| 8 | P1.4 | | ✓(CTBm1_OA1_INN) | |
| 9 | P0.4 | | | ✓(COMP1_INP) |
| 10 | P0.5 | | | ✓(COMP1_INN) |
| 11 | P0.6 | | | |
| 12 | P1.2 | | ✓(CTBm1_OA0_OUT) | |
| 13 | $V_{DDR}$ | Radio Power Supply (1.9V to 5.5V) | | |
| 14 | P2.6 | | ✓(CTBm0_OA0_INP) | |
| 15 | P1.3 | | ✓(CTBm1_OA1_OUT) | |
| 16 | P3.0 | ✓ | | |
| 17 | P2.1 | | ✓(CTBm0_OA0_INN) | |
| 18 | P2.2 | | ✓(CTBm0_OA0_OUT) | |
| 19 | P2.3 | | ✓(CTBm0_OA1_OUT) | |
| 20 | VDDA | Analog Power Supply Input (1.71 to 5.5V) | | |
| 21 | P3.4 | ✓ | | |
| 22 | P3.1 | ✓ | | |
| 23 | P3.7 | ✓ | | |
| 24 | P3.5 | ✓ | | |
| 25 | P3.3 | ✓ | | |
| 26 | VREF | Reference Voltage Input (Optional) | | |
| 27 | P3.2 | ✓ | | |
| 28 | P3.6 | ✓ | | |
| 29 | XRES | External Reset Hardware Connection Input | | |
| 30 | P2.4 | | ✓(CTBm0_OA1_INN) | |
| 31 | P2.5 | | ✓(CTBm0_OA1_INP) | |
| 32 | GND | Ground Connection | | |

# Power Supply Connections and Recommended External Components

## Power Connections

The CYBLE-214015-01 contains three power supply connections, VDD, VDDA, and VDDR. The VDD and VDDA connections supply power for the digital and analog device operation respectively. VDDR supplies power for the device radio.

VDD and VDDA accept a supply range of 1.71 V to 5.5 V. VDDR accepts a supply range of 1.9 V to 5.5 V. These specifications can be found in Table 10. The maximum power supply ripple for both power connections on the module is 100 mV, as shown in Table 8.

The power supply ramp rate of VDD and VDDA must be equal to or greater than that of VDDR when the radio is used.

## Connection Options

Two connection options are available for any application:

1. Single supply: Connect VDD, VDDA, and VDDR to the same supply.
2. Independent supply: Power VDD, VDDA, and VDDR separately.

## External Component Recommendation

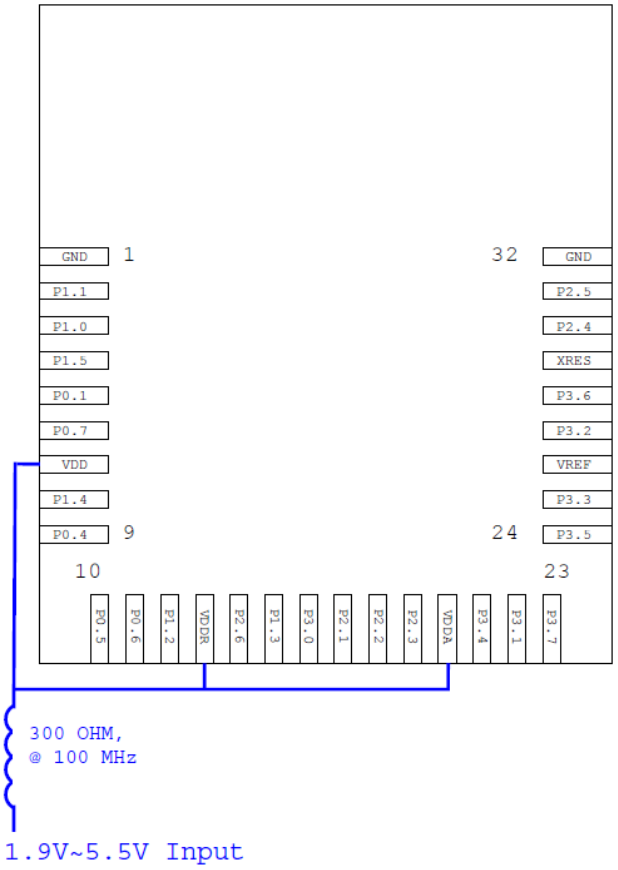
In either connection scenario, it is recommended to place an external ferrite bead between the supply and the module connection. The ferrite bead should be positioned as close as possible to the module pin connection.

Figure 7 details the recommended host schematic options for a single supply scenario. The use of one or three ferrite beads will depend on the specific application and configuration of the CYBLE-214015-01.

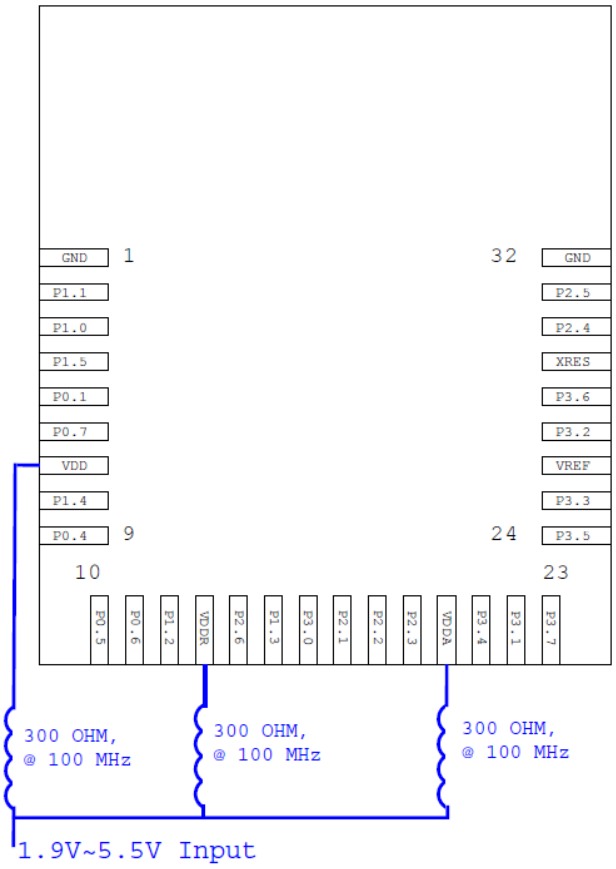
Figure 8 details the recommended host schematic for an independent supply scenario.

The recommended ferrite bead value is 330 Ω, 100 MHz (Murata BLM21PG331SN1D).

**Figure 7. Recommended Host Schematic Options for Single Supply Option**

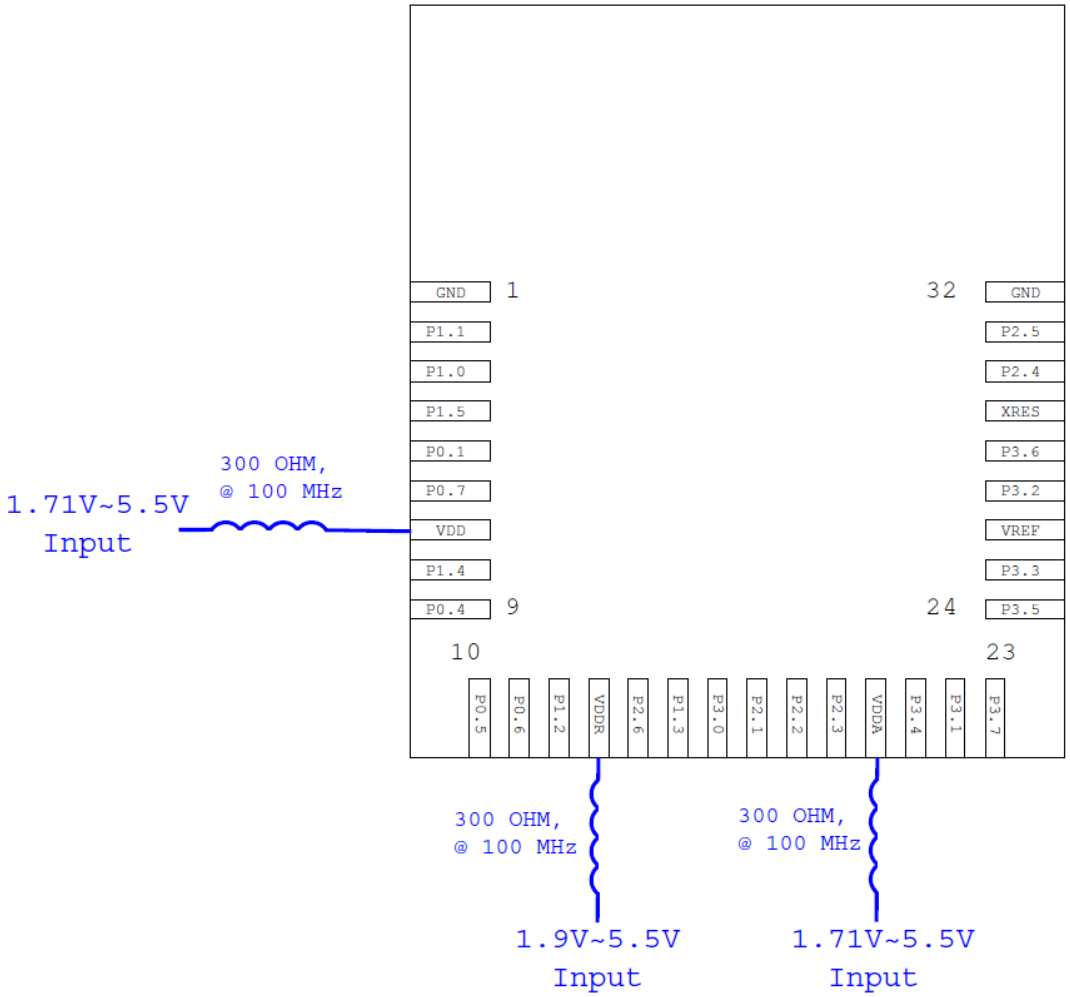



**Single Ferrite Bead Option (Seen from Bottom)**




**Three Ferrite Bead Option (Seen from Bottom)**

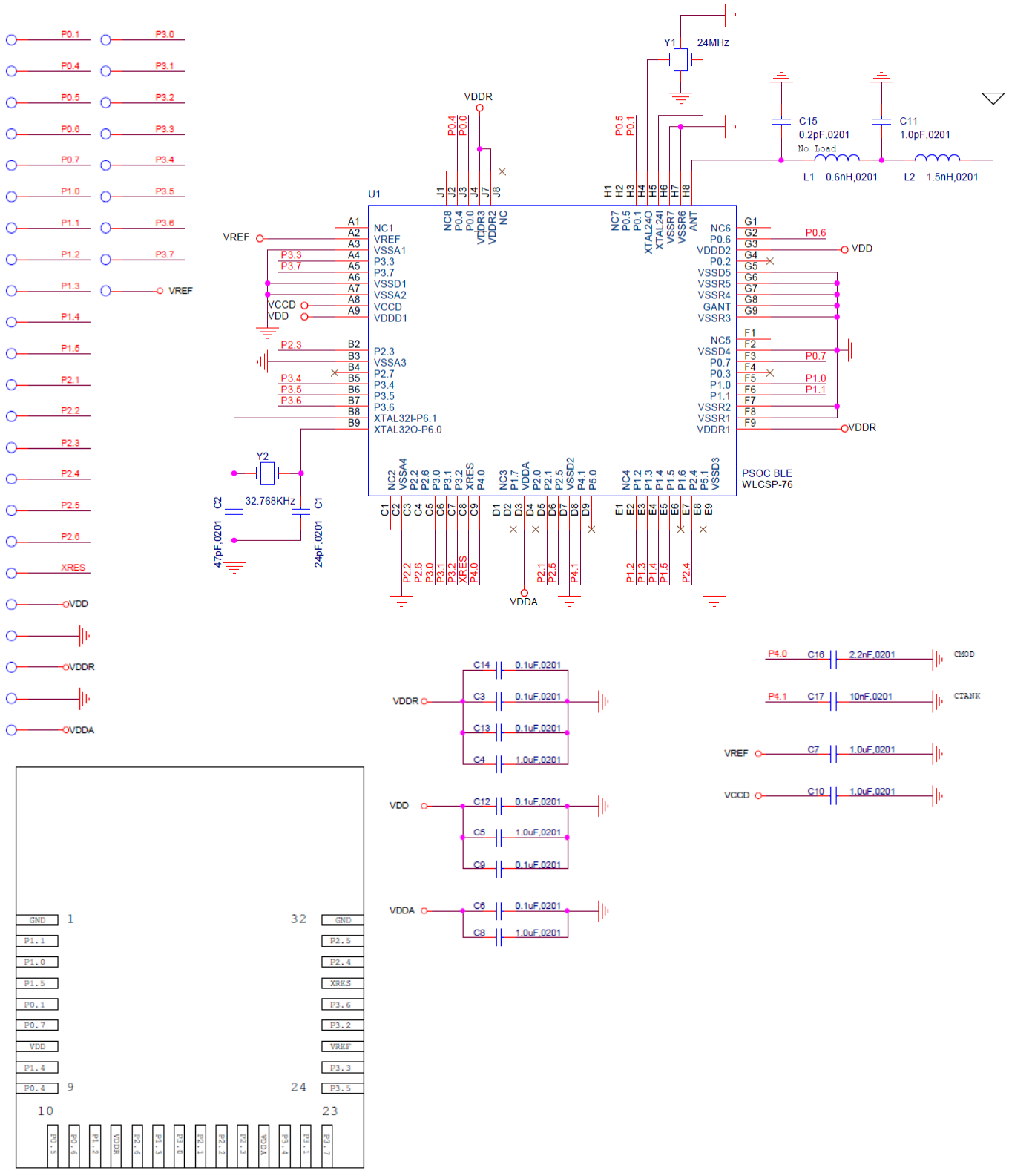
**Figure 8. Recommended Host Schematic for Independent Supply Option**




**Independent Power Supply Option (Seen from Bottom)**

The CYBLE-214015-01 schematic is shown in Figure 9.

**Figure 9. CYBLE-214015-01 Schematic Diagram**



## Critical Components List

Table 6 details the critical components used in the CYBLE-214015-01 module.

**Table 6. Critical Component List**

| Component | Reference Designator | Description |
|---|---|---|
| Silicon | U1 | 76-pin WLCSP Programmable System-on-Chip (PSoC) with BLE |
| Crystal | Y1 | 24.000 MHz, 10PF |
| Crystal | Y2 | 32.768 kHz, 12.5PF |

## Antenna Design

Table 7 details antenna used on the CYBLE-214015-01 module. The Cypress module performance improves many of these characteristics. For more information, see Table 9 on page 15.

**Table 7. Trace Antenna Specifications**

| Item | Description |
|---|---|
| Frequency Range | 2400 – 2500 MHz |
| Peak Gain | 0.5 dBi typical |
| Average Gain | –0.5 dBi typical |
| Return Loss | 10 dB minimum |

## Electrical Specification

Table 8 details the absolute maximum electrical characteristics for the Cypress BLE module.

**Table 8. CYBLE-214015-01 Absolute Maximum Ratings**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $V_{DDD\_ABS}$ | $V_{DD}$, $V_{DDA}$ or $V_{DDR}$ supply relative to $V_{SS}$ ($V_{SSD}$ = $V_{SSA}$) | –0.5 | – | 6 | V | Absolute maximum |
| $V_{CCD\_ABS}$ | Direct digital core voltage input relative to $V_{SSD}$ | –0.5 | – | 1.95 | V | Absolute maximum |
| $V_{DDD\_RIPPLE}$ | Maximum power supply ripple for $V_{DD}$, $V_{DDA}$ and $V_{DDR}$ input voltage | – | – | 100 | mV | 3.0V supply<br>Ripple frequency of 100 kHz to 750 kHz |
| $V_{GPIO\_ABS}$ | GPIO voltage | –0.5 | – | $V_{DD}$ +0.5 | V | Absolute maximum |
| $I_{GPIO\_ABS}$ | Maximum current per GPIO | –25 | – | 25 | mA | Absolute maximum |
| $I_{GPIO\_injection}$ | GPIO injection current: Maximum for $V_{IH}$ > $V_{DD}$ and minimum for $V_{IL}$ < $V_{SS}$ | –0.5 | – | 0.5 | mA | Absolute maximum current injected per pin |
| LU | Pin current for latch up | –200 | | 200 | mA | – |

Table 9 details the RF characteristics for the Cypress BLE module.

**Table 9. CYBLE-214015-01 RF Performance Characteristics**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $RF_O$ | RF output power on ANT | –18 | 0 | 3 | dBm | Configurable via register settings |
| $RX_S$ | RF receive sensitivity on ANT | – | –87 | – | dBm | Guaranteed by design simulation |
| $F_R$ | Module frequency range | 2400 | – | 2480 | MHz | – |
| $G_P$ | Peak gain | – | 0.5 | – | dBi | – |
| $G_{Avg}$ | Average gain | – | –0.5 | – | dBi | – |
| RL | Return loss | – | –10 | – | dB | – |

Table 10 through Table 51 list the module level electrical characteristics for the CYBLE-214015-01. All specifications are valid for –40 °C ≤ TA ≤ 85 °C and TJ ≤ 100 °C, except where noted. Specifications are valid for 1.71V to 5.5V, except where noted.

**Table 10. CYBLE-214015-01 DC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $V_{DD1}$ | Power supply input voltage ($V_{DD}$ = $V_{DDA}$ = $V_{DDR}$) | 1.71 | – | 5.5 | V | With regulator enabled |
| $V_{DD2}$ | Power supply input voltage unregulated ($V_{DD}$ = $V_{DDA}$ = $V_{DDR}$) | 1.71 | 1.8 | 1.89 | V | Internally unregulated supply |
| $V_{DDR1}$ | Radio supply voltage (radio on) | 1.9 | – | 5.5 | V | – |
| $V_{DDR2}$ | Radio supply voltage (radio off) | 1.71 | – | 5.5 | V | – |
| **Active Mode, $V_{DD}$ = 1.71 V to 5.5 V** | | | | | | |
| $I_{DD3}$ | Execute from flash; CPU at 3 MHz | – | 1.7 | – | mA | T = 25 °C,<br>$V_{DD}$ = 3.3V |
| $I_{DD4}$ | Execute from flash; CPU at 3 MHz | – | – | – | mA | T = –40 °C to 85 °C |
| $I_{DD5}$ | Execute from flash; CPU at 6 MHz | – | 2.5 | – | mA | T = 25 °C,<br>$V_{DD}$ = 3.3V |
| $I_{DD6}$ | Execute from flash; CPU at 6 MHz | – | – | – | mA | T = –40 °C to 85 °C |
| $I_{DD7}$ | Execute from flash; CPU at 12 MHz | – | 4 | – | mA | T = 25 °C,<br>$V_{DD}$ = 3.3V |

**Table 10. CYBLE-214015-01 DC Specifications** (continued)

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $I_{DD8}$ | Execute from flash; CPU at 12 MHz | – | – | – | mA | T = –40 °C to 85 °C |
| $I_{DD9}$ | Execute from flash; CPU at 24 MHz | – | 7.1 | – | mA | T = 25 °C, $V_{DD}$ = 3.3 V |
| $I_{DD10}$ | Execute from flash; CPU at 24 MHz | – | – | – | mA | T = –40 °C to 85 °C |
| $I_{DD11}$ | Execute from flash; CPU at 48 MHz | – | 13.4 | – | mA | T = 25 °C, $V_{DD}$ = 3.3 V |
| $I_{DD12}$ | Execute from flash; CPU at 48 MHz | – | – | – | mA | T = –40 °C to 85 °C |
| **Sleep Mode, $V_{DD}$ = 1.71 V to 5.5 V** | | | | | | |
| $I_{DD13}$ | IMO on | – | – | – | mA | T = 25 °C, $V_{DD}$ = 3.3 V, SYSCLK = 3 MHz |
| **Sleep Mode, $V_{DD}$ and $V_{DDR}$ = 1.9 V to 5.5 V** | | | | | | |
| $I_{DD14}$ | ECO on | – | – | – | mA | T = 25 °C, $V_{DD}$ = 3.3 V, SYSCLK = 3 MHz |
| **Deep-Sleep Mode, $V_{DD}$ = 1.71 V to 3.6 V** | | | | | | |
| $I_{DD15}$ | WDT with WCO on | – | 1.3 | – | µA | T = 25 °C, $V_{DD}$ = 3.3 V |
| $I_{DD16}$ | WDT with WCO on | – | – | – | µA | T = –40 °C to 85 °C |
| $I_{DD17}$ | WDT with WCO on | – | – | – | µA | T = 25 °C, $V_{DD}$ = 5 V |
| $I_{DD18}$ | WDT with WCO on | – | – | – | µA | T = –40 °C to 85 °C |
| **Deep-Sleep Mode, $V_{DD}$ = 1.71 V to 1.89 V (Regulator Bypassed)** | | | | | | |
| $I_{DD19}$ | WDT with WCO on | – | – | – | µA | T = 25 °C |
| $I_{DD20}$ | WDT with WCO on | – | – | – | µA | T = –40 °C to 85 °C |
| **Hibernate Mode, $V_{DD}$ = 1.71 V to 3.6 V** | | | | | | |
| $I_{DD27}$ | GPIO and reset active | – | 150 | – | nA | T = 25 °C, $V_{DD}$ = 3.3 V |
| $I_{DD28}$ | GPIO and reset active | – | – | – | nA | T = –40 °C to 85 °C |
| **Hibernate Mode, $V_{DD}$ = 3.6 V to 5.5 V** | | | | | | |
| $I_{DD29}$ | GPIO and reset active | – | – | – | nA | T = 25 °C, $V_{DD}$ = 5 V |
| $I_{DD30}$ | GPIO and reset active | – | – | – | nA | T = –40 °C to 85 °C |
| **Stop Mode, $V_{DD}$ = 1.71 V to 3.6 V** | | | | | | |
| $I_{DD33}$ | Stop-mode current ($V_{DD}$) | – | 20 | – | nA | T = 25 °C, $V_{DD}$ = 3.3 V |
| $I_{DD34}$ | Stop-mode current ($V_{DDR}$) | – | 40 | –- | nA | T = 25 °C, $V_{DDR}$ = 3.3 V |
| $I_{DD35}$ | Stop-mode current ($V_{DD}$) | – | – | – | nA | T = –40 °C to 85 °C |
| $I_{DD36}$ | Stop-mode current ($V_{DDR}$) | – | – | – | nA | T = –40 °C to 85 °C, $V_{DDR}$ = 1.9 V to 3.6 V |
| **Stop Mode, $V_{DD}$ = 3.6 V to 5.5 V** | | | | | | |
| $I_{DD37}$ | Stop-mode current ($V_{DD}$) | – | – | – | nA | T = 25 °C, $V_{DD}$ = 5 V |
| $I_{DD38}$ | Stop-mode current ($V_{DDR}$) | – | – | – | nA | T = 25 °C, $V_{DDR}$ = 5 V |
| $I_{DD39}$ | Stop-mode current ($V_{DD}$) | – | – | – | nA | T = –40 °C to 85 °C |
| $I_{DD40}$ | Stop-mode current ($V_{DDR}$) | – | – | – | nA | T = –40 °C to 85 °C |

**Table 11. AC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $F_{CPU}$ | CPU frequency | DC | – | 48 | MHz | 1.71 V ≤ $V_{DD}$ ≤ 5.5 V |
| $T_{SLEEP}$ | Wakeup from Sleep mode | – | 0 | – | µs | Guaranteed by characterization |
| $T_{DEEPSLEEP}$ | Wakeup from Deep-Sleep mode | – | – | 25 | µs | 24-MHz IMO. Guaranteed by characterization |
| $T_{HIBERNATE}$ | Wakeup from Hibernate mode | – | – | 800 | µs | Guaranteed by characterization |
| $T_{STOP}$ | Wakeup from Stop mode | – | – | 2 | ms | XRES wakeup |

## GPIO

**Table 12. GPIO DC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$[5] | Input voltage HIGH threshold | 0.7 × $V_{DD}$ | – | – | V | CMOS input |
| | LVTTL input, $V_{DD}$ < 2.7V | 0.7 × $V_{DD}$ | – | – | V | – |
| | LVTTL input, $V_{DD}$ ≥ 2.7V | 2.0 | – | – | V | – |
| $V_{IL}$ | Input voltage LOW threshold | – | – | 0.3 × $V_{DD}$ | V | CMOS input |
| | LVTTL input, $V_{DD}$ < 2.7V | – | – | 0.3 × $V_{DD}$ | V | – |
| | LVTTL input, $V_{DD}$ ≥ 2.7V | – | – | 0.8 | V | – |
| $V_{OH}$ | Output voltage HIGH level | $V_{DD}$ – 0.6 | – | – | V | $I_{OH}$ = 4 mA at 3.3-V $V_{DD}$ |
| | Output voltage HIGH level | $V_{DD}$ – 0.5 | – | – | V | $I_{OH}$ = 1 mA at 1.8-V $V_{DD}$ |
| $V_{OL}$ | Output voltage LOW level | – | – | 0.6 | V | $I_{OL}$ = 8 mA at 3.3-V $V_{DD}$ |
| | Output voltage LOW level | – | – | 0.6 | V | $I_{OL}$ = 4 mA at 1.8-V $V_{DD}$ |
| | Output voltage LOW level | – | – | 0.4 | V | $I_{OL}$ = 3 mA at 3.3-V $V_{DD}$ |
| $R_{PULLUP}$ | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | – |
| $R_{PULLDOWN}$ | Pull-down resistor | 3.5 | 5.6 | 8.5 | kΩ | – |
| $I_{IL}$ | Input leakage current (absolute value) | – | – | 2 | nA | 25 °C, $V_{DD}$ = 3.3 V |
| $I_{IL\_CTBM}$ | Input leakage on CTBm input pins | – | – | 4 | nA | – |
| $C_{IN}$ | Input capacitance | – | – | 7 | pF | – |
| $V_{HYSTTL}$ | Input hysteresis LVTTL | 25 | 40 | – | mV | $V_{DD}$ > 2.7 V |
| $V_{HYSCMOS}$ | Input hysteresis CMOS | 0.05 × $V_{DD}$ | – | – | 1 | – |
| $I_{DIODE}$ | Current through protection diode to $V_{DD}$/$V_{SS}$ | – | – | 100 | µA | – |
| $I_{TOT\_GPIO}$ | Maximum total source or sink chip current | – | – | 200 | mA | – |

**Note**
5. $V_{IH}$ must not exceed $V_{DD}$ + 0.2 V.

**Table 13. GPIO AC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $T_{RISEF}$ | Rise time in Fast-Strong mode | 2 | – | 12 | ns | 3.3-V $V_{DDD}$, $C_{LOAD}$ = 25 pF |
| $T_{FALLF}$ | Fall time in Fast-Strong mode | 2 | – | 12 | ns | 3.3-V $V_{DDD}$, $C_{LOAD}$ = 25 pF |
| $T_{RISES}$ | Rise time in Slow-Strong mode | 10 | – | 60 | ns | 3.3-V $V_{DDD}$, $C_{LOAD}$ = 25 pF |
| $T_{FALLS}$ | Fall time in Slow-Strong mode | 10 | – | 60 | ns | 3.3-V $V_{DDD}$, $C_{LOAD}$ = 25 pF |
| $F_{GPIOUT1}$ | GPIO $F_{OUT}$; 3.3 V ≤ $V_{DD}$ ≤ 5.5 V Fast-Strong mode | – | – | 33 | MHz | 90/10%, 25-pF load, 60/40 duty cycle |
| $F_{GPIOUT2}$ | GPIO $F_{OUT}$; 1.7 V≤ $V_{DD}$ ≤ 3.3 V Fast-Strong mode | – | – | 16.7 | MHz | 90/10%, 25-pF load, 60/40 duty cycle |
| $F_{GPIOUT3}$ | GPIO $F_{OUT}$; 3.3 V ≤ $V_{DD}$ ≤ 5.5 V Slow-Strong mode | – | – | 7 | MHz | 90/10%, 25-pF load, 60/40 duty cycle |
| $F_{GPIOUT4}$ | GPIO $F_{OUT}$; 1.7 V ≤ $V_{DD}$ ≤ 3.3 V Slow-Strong mode | – | – | 3.5 | MHz | 90/10%, 25-pF load, 60/40 duty cycle |
| $F_{GPIOIN}$ | GPIO input operating frequency 1.71 V ≤ $V_{DD}$ ≤ 5.5 V | – | – | 48 | MHz | 90/10% $V_{IO}$ |

## XRES

**Table 14. XRES DC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input voltage HIGH threshold | 0.7 × $V_{DDD}$ | – | – | V | CMOS input |
| $V_{IL}$ | Input voltage LOW threshold | – | – | 0.3 × $V_{DDD}$ | V | CMOS input |
| $R_{PULLUP}$ | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | – |
| $C_{IN}$ | Input capacitance | – | 3 | – | pF | – |
| $V_{HYSXRES}$ | Input voltage hysteresis | – | 100 | – | mV | – |
| $I_{DIODE}$ | Current through protection diode to $V_{DD}$/$V_{SS}$ | – | – | 100 | µA | – |

**Table 15. XRES AC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $T_{RESETWIDTH}$ | Reset pulse width | 1 | – | – | µs | – |

## Analog Peripherals

*Opamp*

**Table 16. Opamp Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| **$I_{DD}$ (Opamp Block Current. $V_{DD}$ = 1.8 V. No Load)** | | | | | | |
| $I_{DD\_HI}$ | Power = high | – | 1000 | 1300 | µA | – |
| $I_{DD\_MED}$ | Power = medium | – | 500 | – | µA | – |
| $I_{DD\_LOW}$ | Power = low | – | 250 | 350 | µA | – |
| **GBW (Load = 20 pF, 0.1 mA. $V_{DDA}$ = 2.7 V)** | | | | | | |
| GBW_HI | Power = high | 6 | – | – | MHz | – |
| GBW_MED | Power = medium | 4 | – | – | MHz | – |
| GBW_LO | Power = low | – | 1 | – | MHz | – |
| **$I_{OUT\_MAX}$ ($V_{DDA}$ ≥ 2.7 V, 500 mV from Rail)** | | | | | | |
| $I_{OUT\_MAX\_HI}$ | Power = high | 10 | – | – | mA | – |

**Table 16. Opamp Specifications** (continued)

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $I_{OUT\_MAX\_MID}$ | Power = medium | 10 | – | – | mA | – |
| $I_{OUT\_MAX\_LO}$ | Power = low | – | 5 | – | mA | – |
| **$I_{OUT}$ ($V_{DDA}$ = 1.71 V, 500 mV from Rail)** | | | | | | |
| $I_{OUT\_MAX\_HI}$ | Power = high | 4 | – | – | mA | – |
| $I_{OUT\_MAX\_MID}$ | Power = medium | 4 | – | – | mA | – |
| $I_{OUT\_MAX\_LO}$ | Power = low | – | 2 | – | mA | – |
| $V_{IN}$ | Charge pump on, $V_{DDA} \geq 2.7V$ | –0.05 | – | $V_{DDA}$ – 0.2 | V | – |
| $V_{CM}$ | Charge pump on, $V_{DDA} \geq 2.7V$ | –0.05 | – | $V_{DDA}$ – 0.2 | V | – |
| **$V_{OUT}$ ($V_{DDA} \geq 2.7$ V)** | | | | | | |
| $V_{OUT\_1}$ | Power = high, $I_{LOAD}$ = 10 mA | 0.5 | – | $V_{DDA}$ – 0.5 | V | – |
| $V_{OUT\_2}$ | Power = high, $I_{LOAD}$ = 1 mA | 0.2 | – | $V_{DDA}$ – 0.2 | V | – |
| $V_{OUT\_3}$ | Power = medium, $I_{LOAD}$ = 1 mA | 0.2 | – | $V_{DDA}$ – 0.2 | V | – |
| $V_{OUT\_4}$ | Power = low, $I_{LOAD}$ = 0.1 mA | 0.2 | – | $V_{DDA}$ – 0.2 | V | – |
| $V_{OS\_TR}$ | Offset voltage, trimmed | 1 | ±0.5 | 1 | mV | High mode |
| $V_{OS\_TR}$ | Offset voltage, trimmed | – | ±1 | – | mV | Medium mode |
| $V_{OS\_TR}$ | Offset voltage, trimmed | – | ±2 | – | mV | Low mode |
| $V_{OS\_DR\_TR}$ | Offset voltage drift, trimmed | –10 | ±3 | 10 | µV/°C | High mode |
| $V_{OS\_DR\_TR}$ | Offset voltage drift, trimmed | – | ±10 | – | µV/°C | Medium mode |
| $V_{OS\_DR\_TR}$ | Offset voltage drift, trimmed | – | ±10 | – | µV/°C | Low mode |
| CMRR | DC | 65 | 70 | – | dB | $V_{DDD}$ = 3.6V, High-power mode |
| PSRR | At 1 kHz, 100-mV ripple | 70 | 85 | – | dB | $V_{DDD}$ = 3.6V |
| **Noise** | | | | | | |
| $V_{N1}$ | Input referred, 1 Hz–1 GHz, power = high | – | 94 | – | µVrms | – |
| $V_{N2}$ | Input referred, 1 kHz, power = high | – | 72 | – | nV/rtHz | – |
| $V_{N3}$ | Input referred, 10 kHz, power = high | – | 28 | – | nV/rtHz | – |
| $V_{N4}$ | Input referred, 100 kHz, power = high | – | 15 | – | nV/rtHz | – |
| $C_{LOAD}$ | Stable up to maximum load. Performance specs at 50 pF | – | – | 125 | pF | _ |
| Slew_rate | Cload = 50 pF, Power = High, $V_{DDA} \geq 2.7V$ | 6 | – | – | V/µs | _ |
| T_op_wake | From disable to enable, no external RC dominating | – | 300 | – | µs | _ |
| **Comp_mode (Comparator Mode; 50-mV Drive, $T_{RISE}$ = $T_{FALL}$ (Approx.)** | | | | | | |
| $T_{PD1}$ | Response time; power = high | – | 150 | – | ns | – |
| $T_{PD2}$ | Response time; power = medium | – | 400 | – | ns | – |
| $T_{PD3}$ | Response time; power = low | – | 2000 | – | ns | – |
| Vhyst_op | Hysteresis | – | 10 | – | mV | – |
| **Deep-Sleep Mode (Deep-Sleep mode operation is only guaranteed for $V_{DDA}$ > 2.5 V)** | | | | | | |
| GBW_DS | Gain bandwidth product | – | 50 | – | kHz | – |
| IDD_DS | Current | – | 15 | – | µA | – |
| Vos_DS | Offset voltage | – | 5 | – | mV | – |
| Vos_dr_DS | Offset voltage drift | – | 20 | – | µV/°C | – |
| Vout_DS | Output voltage | 0.2 | – | $V_{DD}$–0.2 | V | – |
| Vcm_DS | Common mode voltage | 0.2 | – | $V_{DD}$ – 1.8 | V | – |

**Table 17. Comparator DC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $V_{OFFSET1}$ | Input offset voltage, Factory trim | – | – | ±10 | mV | – |
| $V_{OFFSET2}$ | Input offset voltage, Custom trim | – | – | ±6 | mV | – |
| $V_{OFFSET3}$ | Input offset voltage, ultra-low-power mode | – | ±12 | – | mV | – |
| $V_{HYST}$ | Hysteresis when enabled | – | 10 | 35 | mV | – |
| $V_{ICM1}$ | Input common mode voltage in normal mode | 0 | – | $V_{DDD}$ – 0.1 | V | Modes 1 and 2 |
| $V_{ICM2}$ | Input common mode voltage in low-power mode | 0 | – | $V_{DDD}$ | V | – |
| $V_{ICM3}$ | Input common mode voltage in ultra low-power mode | 0 | – | $V_{DDD}$ – 1.15 | V | – |
| CMRR | Common mode rejection ratio | 50 | – | – | dB | $V_{DDD} \geq 2.7$ V |
| CMRR | Common mode rejection ratio | 42 | – | – | dB | $V_{DDD} \leq 2.7$ V |
| $I_{CMP1}$ | Block current, normal mode | – | – | 400 | µA | – |
| $I_{CMP2}$ | Block current, low-power mode | – | – | 100 | µA | – |
| $I_{CMP3}$ | Block current in ultra-low-power mode | – | 6 | – | µA | – |
| $Z_{CMP}$ | DC input impedance of comparator | 35 | – | – | MΩ | – |

**Table 18. Comparator AC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $T_{RESP1}$ | Response time, normal mode, 50-mV overdrive | – | 38 | – | ns | 50-mV overdrive |
| $T_{RESP2}$ | Response time, low-power mode, 50-mV overdrive | – | 70 | – | ns | 50-mV overdrive |
| $T_{RESP3}$ | Response time, ultra-low-power mode, 50-mV overdrive | – | 2.3 | – | µs | 200-mV overdrive |

*Temperature Sensor*

**Table 19. Temperature Sensor Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $T_{SENSACC}$ | Temperature-sensor accuracy | –5 | ±1 | 5 | °C | –40 to +85 °C |

*SAR ADC*

**Table 20. SAR ADC DC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| A_RES | Resolution | – | – | 12 | bits | – |
| A_CHNIS_S | Number of channels - single-ended | – | – | 8 | – | 8 full-speed |
| A-CHNKS_D | Number of channels - differential | – | – | 4 | – | Diff inputs use neighboring I/O |
| A-MONO | Monotonicity | – | – | – | – | Yes |
| A_GAINERR | Gain error | – | – | ±0.1 | % | With external reference |
| A_OFFSET | Input offset voltage | – | – | 2 | mV | Measured with 1-V $V_{REF}$ |
| A_ISAR | Current consumption | – | – | 1 | mA | – |
| A_VINS | Input voltage range - single-ended | $V_{SS}$ | – | $V_{DDA}$ | V | – |

**Table 20. SAR ADC DC Specifications** (continued)

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| A_VIND | Input voltage range - differential | $V_{SS}$ | – | $V_{DDA}$ | V | – |
| A_INRES | Input resistance | – | – | 2.2 | kΩ | – |
| A_INCAP | Input capacitance | – | – | 10 | pF | – |
| VREFSAR | Trimmed internal reference to SAR | –1 | – | 1 | % | Percentage of Vbg (1.024 V) |

**Table 21. SAR ADC AC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| A_PSRR | Power-supply rejection ratio | 70 | – | – | dB | Measured at 1-V reference |
| A_CMRR | Common-mode rejection ratio | 66 | – | – | dB | – |
| A_SAMP | Sample rate | – | – | 1 | Msps | – |
| Fsarintref | SAR operating speed without external ref. bypass | – | – | 100 | Ksps | 12-bit resolution |
| A_SNR | Signal-to-noise ratio (SNR) | 65 | – | – | dB | $F_{IN}$ = 10 kHz |
| A_BW | Input bandwidth without aliasing | – | – | A_SAMP/2 | kHz | – |
| A_INL | Integral nonlinearity. $V_{DD}$ = 1.71 V to 5.5 V, 1 Msps | –1.7 | – | 2 | LSB | $V_{REF}$ = 1 V to $V_{DD}$ |
| A_INL | Integral nonlinearity. $V_{DDD}$ = 1.71 V to 3.6 V, 1 Msps | –1.5 | – | 1.7 | LSB | $V_{REF}$ = 1.71 V to $V_{DD}$ |
| A_INL | Integral nonlinearity. $V_{DD}$ = 1.71 V to 5.5 V, 500 Ksps | –1.5 | – | 1.7 | LSB | $V_{REF}$ = 1 V to $V_{DD}$ |
| A_dnl | Differential nonlinearity. $V_{DD}$ = 1.71 V to 5.5 V, 1 Msps | –1 | – | 2.2 | LSB | $V_{REF}$ = 1 V to $V_{DD}$ |
| A_DNL | Differential nonlinearity. $V_{DD}$ = 1.71 V to 3.6 V, 1 Msps | –1 | – | 2 | LSB | $V_{REF}$ = 1.71 V to $V_{DD}$ |
| A_DNL | Differential nonlinearity. $V_{DD}$ = 1.71 V to 5.5 V, 500 Ksps | –1 | – | 2.2 | LSB | $V_{REF}$ = 1 V to $V_{DD}$ |
| A_THD | Total harmonic distortion | – | – | –65 | dB | $F_{IN}$ = 10 kHz |

*CSD*

**Table 22. CSD Block Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $V_{CSD}$ | Voltage range of operation | 1.71 | – | 5.5 | V | – |
| IDAC1 | DNL for 8-bit resolution | –1 | – | 1 | LSB | – |
| IDAC1 | INL for 8-bit resolution | –3 | – | 3 | LSB | – |
| IDAC2 | DNL for 7-bit resolution | –1 | – | 1 | LSB | – |
| IDAC2 | INL for 7-bit resolution | –3 | – | 3 | LSB | – |
| SNR | Ratio of counts of finger to noise | 5 | – | – | Ratio | Capacitance range of 9 pF to 35 pF, 0.1-pF sensitivity. Radio is not operating during the scan |
| $I_{DAC1\_CRT1}$ | Output current of IDAC1 (8 bits) in High range | – | 612 | – | µA | – |

**Table 22. CSD Block Specifications** (continued)

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $I_{DAC1\_CRT2}$ | Output current of IDAC1 (8 bits) in Low range | – | 306 | – | µA | – |
| $I_{DAC2\_CRT1}$ | Output current of IDAC2 (7 bits) in High range | – | 305 | – | µA | – |
| $I_{DAC2\_CRT2}$ | Output current of IDAC2 (7 bits) in Low range | – | 153 | – | µA | – |

## Digital Peripherals

*Timer*

**Table 23. Timer DC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $I_{TIM1}$ | Block current consumption at 3 MHz | – | – | 42 | µA | 16-bit timer |
| $I_{TIM2}$ | Block current consumption at 12 MHz | – | – | 130 | µA | 16-bit timer |
| $I_{TIM3}$ | Block current consumption at 48 MHz | – | – | 535 | µA | 16-bit timer |

**Table 24. Timer AC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $T_{TIMFREQ}$ | Operating frequency | $F_{CLK}$ | – | 48 | MHz | – |
| $T_{CAPWINT}$ | Capture pulse width (internal) | $2 \times T_{CLK}$ | – | – | ns | – |
| $T_{CAPWEXT}$ | Capture pulse width (external) | $2 \times T_{CLK}$ | – | – | ns | – |
| $T_{TIMRES}$ | Timer resolution | $T_{CLK}$ | – | – | ns | – |
| $T_{TENWIDINT}$ | Enable pulse width (internal) | $2 \times T_{CLK}$ | – | – | ns | – |
| $T_{TENWIDEXT}$ | Enable pulse width (external) | $2 \times T_{CLK}$ | – | – | ns | – |
| $T_{TIMRESWINT}$ | Reset pulse width (internal) | $2 \times T_{CLK}$ | – | – | ns | – |
| $T_{TIMRESEXT}$ | Reset pulse width (external) | $2 \times T_{CLK}$ | – | – | ns | – |

*Counter*

**Table 25. Counter DC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $I_{CTR1}$ | Block current consumption at 3 MHz | – | – | 42 | µA | 16-bit counter |
| $I_{CTR2}$ | Block current consumption at 12 MHz | – | – | 130 | µA | 16-bit counter |
| $I_{CTR3}$ | Block current consumption at 48 MHz | – | – | 535 | µA | 16-bit counter |

**Table 26. Counter AC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $T_{CTRFREQ}$ | Operating frequency | $F_{CLK}$ | – | 48 | MHz | – |
| $T_{CTRPWINT}$ | Capture pulse width (internal) | $2 \times T_{CLK}$ | – | – | ns | – |
| $T_{CTRPWEXT}$ | Capture pulse width (external) | $2 \times T_{CLK}$ | – | – | ns | – |
| $T_{CTRES}$ | Counter Resolution | $T_{CLK}$ | – | – | ns | – |
| $T_{CENWIDINT}$ | Enable pulse width (internal) | $2 \times T_{CLK}$ | – | – | ns | – |
| $T_{CENWIDEXT}$ | Enable pulse width (external) | $2 \times T_{CLK}$ | – | – | ns | – |
| $T_{CTRRESWINT}$ | Reset pulse width (internal) | $2 \times T_{CLK}$ | – | – | ns | – |
| $T_{CTRRESWEXT}$ | Reset pulse width (external) | $2 \times T_{CLK}$ | – | – | ns | – |

*Pulse Width Modulation (PWM)*

**Table 27. PWM DC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $I_{PWM1}$ | Block current consumption at 3 MHz | – | – | 42 | µA | 16-bit PWM |
| $I_{PWM2}$ | Block current consumption at 12 MHz | – | – | 130 | µA | 16-bit PWM |
| $I_{PWM3}$ | Block current consumption at 48 MHz | – | – | 535 | µA | 16-bit PWM |

**Table 28. PWM AC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $T_{PWMFREQ}$ | Operating frequency | $F_{CLK}$ | – | 48 | MHz | – |
| $T_{PWMPWINT}$ | Pulse width (internal) | $2 \times T_{CLK}$ | – | – | ns | – |
| $T_{PWMEXT}$ | Pulse width (external) | $2 \times T_{CLK}$ | – | – | ns | – |
| $T_{PWMKILLINT}$ | Kill pulse width (internal) | $2 \times T_{CLK}$ | – | – | ns | – |
| $T_{PWMKILLEXT}$ | Kill pulse width (external) | $2 \times T_{CLK}$ | – | – | ns | – |
| $T_{PWMEINT}$ | Enable pulse width (internal) | $2 \times T_{CLK}$ | – | – | ns | – |
| $T_{PWMENEXT}$ | Enable pulse width (external) | $2 \times T_{CLK}$ | – | – | ns | – |
| $T_{PWMRESWINT}$ | Reset pulse width (internal) | $2 \times T_{CLK}$ | – | – | ns | – |
| $T_{PWMRESWEXT}$ | Reset pulse width (external) | $2 \times T_{CLK}$ | – | – | ns | – |

*LCD Direct Drive*

**Table 29. LCD Direct Drive DC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID228 | $I_{LCDLOW}$ | Operating current in low-power mode | – | 17.5 | – | µA | 16 × 4 small segment display at 50 Hz |
| SID229 | $C_{LCDCAP}$ | LCD capacitance per segment/common driver | – | 500 | 5000 | pF | – |
| SID230 | $LCD_{OFFSET}$ | Long-term segment offset | – | 20 | – | mV | – |
| SID231 | $I_{LCDOP1}$ | LCD system operating current $V_{BIAS}$ = 5 V | – | 2 | – | mA | 32 × 4 segments. 50 Hz at 25 °C |
| SID232 | $I_{LCDOP2}$ | LCD system operating current $V_{BIAS}$ = 3.3 V | – | 2 | – | mA | 32 × 4 segments 50 Hz at 25 °C |

**Table 30. LCD Direct Drive AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID233 | $F_{LCD}$ | LCD frame rate | 10 | 50 | 150 | Hz | – |

## Serial Communication

### Table 31. Fixed I²C DC Specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $I_{I2C1}$ | Block current consumption at 100 kHz | – | – | 50 | µA | – |
| $I_{I2C2}$ | Block current consumption at 400 kHz | – | – | 155 | µA | – |
| $I_{I2C3}$ | Block current consumption at 1 Mbps | – | – | 390 | µA | – |
| $I_{I2C4}$ | I²C enabled in Deep-Sleep mode | – | – | 1.4 | µA | – |

### Table 32. Fixed I²C AC Specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $F_{I2C1}$ | Bit rate | – | – | 400 | kHz | – |

### Table 33. Fixed UART DC Specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $I_{UART1}$ | Block current consumption at 100 kbps | – | – | 55 | µA | – |
| $I_{UART2}$ | Block current consumption at 1000 kbps | – | – | 312 | µA | – |

### Table 34. Fixed UART AC Specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $F_{UART}$ | Bit rate | – | – | 1 | Mbps | – |

### Table 35. Fixed SPI DC Specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $I_{SPI1}$ | Block current consumption at 1 Mbps | – | – | 360 | µA | – |
| $I_{SPI2}$ | Block current consumption at 4 Mbps | – | – | 560 | µA | – |
| $I_{SPI3}$ | Block current consumption at 8 Mbps | – | – | 600 | µA | – |

### Table 36. Fixed SPI AC Specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $F_{SPI}$ | SPI operating frequency (master; 6x over sampling) | – | – | 8 | MHz | – |

### Table 37. Fixed SPI Master Mode AC Specifications

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $T_{DMO}$ | MOSI valid after SCLK driving edge | – | – | 18 | ns | – |
| $T_{DSI}$ | MISO valid before SCLK capturing edge Full clock, late MISO sampling used | 20 | – | – | ns | Full clock, late MISO sampling |
| $T_{HMO}$ | Previous MOSI data hold time | 0 | – | – | ns | Referred to Slave capturing edge |

### Table 38. Fixed SPI Slave Mode AC Specifications

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{DMI}$ | MOSI valid before SCLK capturing edge | 40 | – | – | ns |
| $T_{DSO}$ | MISO valid after SCLK driving edge | – | – | $42 + 3 \times T_{CPU}$ | ns |
| $T_{DSO\_ext}$ | MISO Valid after SCLK driving edge in external clock mode. $V_{DD} < 3.0V$ | – | – | 50 | ns |
| $T_{HSO}$ | Previous MISO data hold time | 0 | – | – | ns |
| $T_{SSELSCK}$ | SSEL valid to first SCK valid edge | 100 | – | – | ns |

## Memory

**Table 39. Flash DC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $V_{PE}$ | Erase and program voltage | 1.71 | – | 5.5 | V | – |
| $T_{WS48}$ | Number of Wait states at 32–48 MHz | 2 | – | – | _ | CPU execution from flash |
| $T_{WS32}$ | Number of Wait states at 16–32 MHz | 1 | – | – | _ | CPU execution from flash |
| $T_{WS16}$ | Number of Wait states for 0–16 MHz | 0 | – | – | _ | CPU execution from flash |

**Table 40. Flash AC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $T_{ROWWRITE}$[6] | Row (block) write time (erase and program) | – | – | 20 | ms | Row (block) = 256 bytes |
| $T_{ROWERASE}$[6] | Row erase time | – | – | 13 | ms | – |
| $T_{ROWPROGRAM}$[6] | Row program time after erase | – | – | 7 | ms | – |
| $T_{BULKERASE}$[6] | Bulk erase time (256 KB) | – | – | 35 | ms | – |
| $T_{DEVPROG}$[6] | Total device program time | – | – | 25 | seconds | – |
| $F_{END}$ | Flash endurance | 100 K | – | – | cycles | – |
| $F_{RET}$ | Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles. | 20 | – | – | years | – |
| $F_{RET2}$ | Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles. | 10 | – | – | years | – |

## System Resources

*Power-on-Reset (POR)*

**Table 41. POR DC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $V_{RISEIPOR}$ | Rising trip voltage | 0.80 | – | 1.45 | V | – |
| $V_{FALLIPOR}$ | Falling trip voltage | 0.75 | – | 1.40 | V | – |
| $V_{IPORHYST}$ | Hysteresis | 15 | – | 200 | mV | – |

**Table 42. POR AC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $T_{PPOR\_TR}$ | Precision power-on reset (PPOR) response time in Active and Sleep modes | – | – | 1 | µs | – |

**Table 43. Brown-Out Detect**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $V_{FALLPPOR}$ | BOD trip voltage in Active and Sleep modes | 1.64 | – | – | V | – |
| $V_{FALLDPSLP}$ | BOD trip voltage in Deep Sleep | 1.4 | – | – | V | – |

**Table 44. Hibernate Reset**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $V_{HBRTRIP}$ | BOD trip voltage in Hibernate | 1.1 | – | – | V | – |

**Note**

6. It can take as much as 20 ms to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

*Voltage Monitors (LVD)*

**Table 45. Voltage Monitor DC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $V_{LVI1}$ | LVI_A/D_SEL[3:0] = 0000b | 1.71 | 1.75 | 1.79 | V | – |
| $V_{LVI2}$ | LVI_A/D_SEL[3:0] = 0001b | 1.76 | 1.80 | 1.85 | V | – |
| $V_{LVI3}$ | LVI_A/D_SEL[3:0] = 0010b | 1.85 | 1.90 | 1.95 | V | – |
| $V_{LVI4}$ | LVI_A/D_SEL[3:0] = 0011b | 1.95 | 2.00 | 2.05 | V | – |
| $V_{LVI5}$ | LVI_A/D_SEL[3:0] = 0100b | 2.05 | 2.10 | 2.15 | V | – |
| $V_{LVI6}$ | LVI_A/D_SEL[3:0] = 0101b | 2.15 | 2.20 | 2.26 | V | – |
| $V_{LVI7}$ | LVI_A/D_SEL[3:0] = 0110b | 2.24 | 2.30 | 2.36 | V | – |
| $V_{LVI8}$ | LVI_A/D_SEL[3:0] = 0111b | 2.34 | 2.40 | 2.46 | V | – |
| $V_{LVI9}$ | LVI_A/D_SEL[3:0] = 1000b | 2.44 | 2.50 | 2.56 | V | – |
| $V_{LVI10}$ | LVI_A/D_SEL[3:0] = 1001b | 2.54 | 2.60 | 2.67 | V | – |
| $V_{LVI11}$ | LVI_A/D_SEL[3:0] = 1010b | 2.63 | 2.70 | 2.77 | V | – |
| $V_{LVI12}$ | LVI_A/D_SEL[3:0] = 1011b | 2.73 | 2.80 | 2.87 | V | – |
| $V_{LVI13}$ | LVI_A/D_SEL[3:0] = 1100b | 2.83 | 2.90 | 2.97 | V | – |
| $V_{LVI14}$ | LVI_A/D_SEL[3:0] = 1101b | 2.93 | 3.00 | 3.08 | V | – |
| $V_{LVI15}$ | LVI_A/D_SEL[3:0] = 1110b | 3.12 | 3.20 | 3.28 | V | – |
| $V_{LVI16}$ | LVI_A/D_SEL[3:0] = 1111b | 4.39 | 4.50 | 4.61 | V | – |
| LVI_IDD | Block current | – | – | 100 | µA | – |

**Table 46. Voltage Monitor AC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $T_{MONTRIP}$ | Voltage monitor trip time | – | – | 1 | µs | – |

*SWD Interface*

**Table 47. SWD Interface Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| F_SWDCLK1 | 3.3 V ≤ $V_{DD}$ ≤ 5.5 V | – | – | 14 | MHz | SWDCLK ≤ 1/3 CPU clock frequency |
| F_SWDCLK2 | 1.71 V ≤ $V_{DD}$ ≤ 3.3 V | – | – | 7 | MHz | SWDCLK ≤ 1/3 CPU clock frequency |
| T_SWDI_SETUP | T = 1/f SWDCLK | 0.25 × T | – | – | ns | – |
| T_SWDI_HOLD | T = 1/f SWDCLK | 0.25 × T | – | – | ns | – |
| T_SWDO_VALID | T = 1/f SWDCLK | – | – | 0.5 × T | ns | – |
| T_SWDO_HOLD | T = 1/f SWDCLK | 1 | – | – | ns | – |

*Internal Main Oscillator*

**Table 48. IMO DC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $I_{IMO1}$ | IMO operating current at 48 MHz | – | – | 1000 | µA | – |
| $I_{IMO2}$ | IMO operating current at 24 MHz | – | – | 325 | µA | – |
| $I_{IMO3}$ | IMO operating current at 12 MHz | – | – | 225 | µA | – |
| $I_{IMO4}$ | IMO operating current at 6 MHz | – | – | 180 | µA | – |
| $I_{IMO5}$ | IMO operating current at 3 MHz | – | – | 150 | µA | – |

**Table 49. IMO AC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $F_{IMOTOL3}$ | Frequency variation from 3 to 48 MHz | – | – | ±2 | % | With API-called calibration |
| $F_{IMOTOL3}$ | IMO startup time | – | 12 | – | µs | – |

*Internal Low-Speed Oscillator*

**Table 50. ILO DC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $I_{ILO2}$ | ILO operating current at 32 kHz | – | 0.3 | 1.05 | µA | – |

**Table 51. ILO AC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| $T_{STARTILO1}$ | ILO startup time | – | – | 2 | ms | – |
| $F_{ILOTRIM1}$ | 32-kHz trimmed frequency | 15 | 32 | 50 | kHz | – |

**Table 52. Recommended ECO Trim Value**

| Parameter | Description | Value | Details/Conditions |
|---|---|---|---|
| $ECO_{TRIM}$ | 24-MHz trim value (firmware configuration) | 0x00009595 | Recommended trim value that needs to be loaded to register CY_SYS_XTAL_BLERD_BB_XO_CAPTRIM_REG |

**Table 53. UDB AC Specifications**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| **Data Path performance** | | | | | | |
| $F_{MAX-TIMER}$ | Max frequency of 16-bit timer in a UDB pair | – | – | 48 | MHz | – |
| $F_{MAX-ADDER}$ | Max frequency of 16-bit adder in a UDB pair | – | – | 48 | MHz | – |
| $F_{MAX\_CRC}$ | Max frequency of 16-bit CRC/PRS in a UDB pair | – | – | 48 | MHz | – |
| **PLD Performance in UDB** | | | | | | |
| $F_{MAX\_PLD}$ | Max frequency of 2-pass PLD function in a UDB pair | – | – | 48 | MHz | – |
| **Clock to Output Performance** | | | | | | |
| $T_{CLK\_OUT\_UDB1}$ | Prop. delay for clock in to data out at 25 °C, Typical | – | 15 | – | ns | – |
| $T_{CLK\_OUT\_UDB2}$ | Prop. delay for clock in to data out, Worst case | – | 25 | – | ns | – |

**Table 54. BLE Subsystem**

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| **RF Receiver Specification** | | | | | | |
| RXS, IDLE | RX sensitivity with idle transmitter | – | –89 | – | dBm | – |
| | RX sensitivity with idle transmitter excluding Balun loss | – | –91 | – | dBm | Guaranteed by design simulation |
| RXS, DIRTY | RX sensitivity with dirty transmitter | – | –87 | –70 | dBm | RF-PHY Specification (RCV-LE/CA/01/C) |
| RXS, HIGHGAIN | RX sensitivity in high-gain mode with idle transmitter | – | –91 | – | dBm | – |
| PRXMAX | Maximum input power | –10 | –1 | – | dBm | RF-PHY Specification (RCV-LE/CA/06/C) |
| CI1 | Cochannel interference, Wanted signal at –67 dBm and Interferer at FRX | – | 9 | 21 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| CI2 | Adjacent channel interference Wanted signal at –67 dBm and Interferer at FRX ±1 MHz | – | 3 | 15 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| CI3 | Adjacent channel interference Wanted signal at –67 dBm and Interferer at FRX ±2 MHz | – | –29 | – | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| CI4 | Adjacent channel interference Wanted signal at –67 dBm and Interferer at ≥FRX ±3 MHz | – | –39 | – | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| CI5 | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at Image frequency ($F_{IMAGE}$) | – | –20 | – | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| CI3 | Adjacent channel interference Wanted signal at –67 dBm and Interferer at Image frequency ($F_{IMAGE}$ ± 1 MHz) | – | –30 | – | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| OBB1 | Out-of-band blocking, Wanted signal at –67 dBm and Interferer at F = 30–2000 MHz | –30 | –27 | – | dBm | RF-PHY Specification (RCV-LE/CA/04/C) |
| OBB2 | Out-of-band blocking, Wanted signal at –67 dBm and Interferer at F = 2003–2399 MHz | –35 | –27 | – | dBm | RF-PHY Specification (RCV-LE/CA/04/C) |
| OBB3 | Out-of-band blocking, Wanted signal at –67 dBm and Interferer at F = 2484–2997 MHz | –35 | –27 | – | dBm | RF-PHY Specification (RCV-LE/CA/04/C) |
| OBB4 | Out-of-band blocking, Wanted signal a –67 dBm and Interferer at F = 3000–12750 MHz | –30 | –27 | – | dBm | RF-PHY Specification (RCV-LE/CA/04/C) |
| IMD | Intermodulation performance Wanted signal at –64 dBm and 1-Mbps BLE, third, fourth, and fifth offset channel | –50 | – | – | dBm | RF-PHY Specification (RCV-LE/CA/05/C) |
| RXSE1 | Receiver spurious emission 30 MHz to 1.0 GHz | – | – | –57 | dBm | 100-kHz measurement bandwidth ETSI EN300 328 V1.8.1 |
| RXSE2 | Receiver spurious emission 1.0 GHz to 12.75 GHz | – | – | –47 | dBm | 1-MHz measurement bandwidth ETSI EN300 328 V1.8.1 |

**Table 54. BLE Subsystem** (continued)

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| **RF Transmitter Specifications** | | | | | | |
| TXP, ACC | RF power accuracy | – | ±1 | – | dB | – |
| TXP, RANGE | RF power control range | – | 20 | – | dB | – |
| TXP, 0dBm | Output power, 0-dB Gain setting (PA7) | – | 0 | – | dBm | – |
| TXP, MAX | Output power, maximum power setting (PA10) | – | 3 | – | dBm | – |
| TXP, MIN | Output power, minimum power setting (PA1) | – | –18 | – | dBm | – |
| F2AVG | Average frequency deviation for 10101010 pattern | 185 | – | – | kHz | RF-PHY Specification (TRM-LE/CA/05/C) |
| F1AVG | Average frequency deviation for 11110000 pattern | 225 | 250 | 275 | kHz | RF-PHY Specification (TRM-LE/CA/05/C) |
| EO | Eye opening = ΔF2AVG/ΔF1AVG | 0.8 | – | – | | RF-PHY Specification (TRM-LE/CA/05/C) |
| FTX, ACC | Frequency accuracy | –150 | – | 150 | kHz | RF-PHY Specification (TRM-LE/CA/06/C) |
| FTX, MAXDR | Maximum frequency drift | –50 | – | 50 | kHz | RF-PHY Specification (TRM-LE/CA/06/C) |
| FTX, INITDR | Initial frequency drift | –20 | – | 20 | kHz | RF-PHY Specification (TRM-LE/CA/06/C) |
| FTX, DR | Maximum drift rate | –20 | – | 20 | kHz/ 50 µs | RF-PHY Specification (TRM-LE/CA/06/C) |
| IBSE1 | In-band spurious emission at 2-MHz offset | – | – | –20 | dBm | RF-PHY Specification (TRM-LE/CA/03/C) |
| IBSE2 | In-band spurious emission at ≥3-MHz offset | – | – | –30 | dBm | RF-PHY Specification (TRM-LE/CA/03/C) |
| TXSE1 | Transmitter spurious emissions (average), <1.0 GHz | – | – | –55.5 | dBm | FCC-15.247 |
| TXSE2 | Transmitter spurious emissions (average), >1.0 GHz | – | – | –41.5 | dBm | FCC-15.247 |
| **RF Current Specifications** | | | | | | |
| IRX | Receive current in normal mode | – | 18.7 | – | mA | – |
| IRX_RF | Radio receive current in normal mode | – | 16.4 | – | mA | Measured at $V_{DDR}$ |
| IRX, HIGHGAIN | Receive current in high-gain mode | – | 21.5 | – | mA | – |
| ITX, 3dBm | TX current at 3-dBm setting (PA10) | – | 20 | – | mA | – |
| ITX, 0dBm | TX current at 0-dBm setting (PA7) | – | 16.5 | – | mA | – |
| ITX_RF, 0dBm | Radio TX current at 0 dBm setting (PA7) | – | 15.6 | – | mA | Measured at $V_{DDR}$ |
| ITX_RF, 0dBm | Radio TX current at 0 dBm excluding Balun loss | – | 14.2 | – | mA | Guaranteed by design simulation |
| ITX,-3dBm | TX current at –3-dBm setting (PA4) | – | 15.5 | – | mA | – |
| ITX,-6dBm | TX current at –6-dBm setting (PA3) | – | 14.5 | – | mA | – |
| ITX,-12dBm | TX current at –12-dBm setting (PA2) | – | 13.2 | – | mA | – |
| ITX,-18dBm | TX current at –18-dBm setting (PA1) | – | 12.5 | – | mA | – |

**Table 54. BLE Subsystem** (continued)

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---|---|---|---|---|---|---|
| Iavg_1sec, 0dBm | Average current at 1-second BLE connection interval | – | 17.1 | – | µA | TXP: 0 dBm; ±20-ppm master and slave clock accuracy. For empty PDU exchange. |
| Iavg_4sec, 0dBm | Average current at 4-second BLE connection interval | – | 6.1 | – | µA | TXP: 0 dBm; ±20-ppm master and slave clock accuracy. For empty PDU exchange. |
| **General RF Specifications** | | | | | | |
| FREQ | RF operating frequency | 2400 | – | 2482 | MHz | – |
| CHBW | Channel spacing | – | 2 | – | MHz | – |
| DR | On-air data rate | – | 1000 | – | kbps | – |
| IDLE2TX | BLE.IDLE to BLE. TX transition time | – | 120 | 140 | µs | – |
| IDLE2RX | BLE.IDLE to BLE. RX transition time | – | 75 | 120 | µs | – |
| **RSSI Specifications** | | | | | | |
| RSSI, ACC | RSSI accuracy | – | ±5 | – | dB | – |
| RSSI, RES | RSSI resolution | – | 1 | – | dB | – |
| RSSI, PER | RSSI sample period | – | 6 | – | µs | – |

# Environmental Specifications

## Environmental Compliance

This Cypress BLE module is built in compliance with the Restriction of Hazardous Substances (RoHS) and Halogen Free (HF) directives. The Cypress module and components used to produce this module are RoHS and HF compliant.

## RF Certification

The CYBLE-214015-01 module is certified under the following RF certification standards:

- FCC ID: WAP4008
- CE
- IC: 7922A-4008
- MIC: 203-JN0505
- KC: MSIP-CRM-Cyp-4008

## Environmental Conditions

Table 55 describes the operating and storage conditions for the Cypress BLE module.

**Table 55. Environmental Conditions for CYBLE-214015-01**

| Description | Minimum Specification | Maximum Specification |
|---|---|---|
| Operating temperature | –40 °C | 85 °C |
| Operating humidity (relative, non-condensation) | 5% | 85% |
| Thermal ramp rate | – | 3 °C/minute |
| Storage temperature | –40 °C | 85 °C |
| Storage temperature and humidity | – | 85 ° C at 85% |
| ESD: Module integrated into system Components[7] | – | 15 kV Air<br>2.2 kV Contact |

## ESD and EMI Protection

Exposed components require special attention to ESD and electromagnetic interference (EMI).

A grounded conductive layer inside the device enclosure is suggested for EMI and ESD performance. Any openings in the enclosure near the module should be surrounded by a grounded conductive layer to provide ESD protection and a low-impedance path to ground.

**Device Handling**: Proper ESD protocol must be followed in manufacturing to ensure component reliability.

**Note**
7. This does not apply to the RF pins (ANT, XTALI, and XTALO). RF pins (ANT, XTALI, and XTALO) are tested for 500-V HBM.

# Regulatory Information

## FCC

FCC NOTICE:

The device CYBLE-214015-01 complies with Part 15 of the FCC Rules. The device meets the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407. Transmitter Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

CAUTION:

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Cypress Semiconductor may void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates and can radiate radio frequency energy and, if not installed and used in accordance with the instructions,ê may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that FCC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor FCC identifier for this product as well as the FCC Notice above. The FCC identifier is FCC ID: WAP4008.

In any case the end product must be labeled exterior with "Contains FCC ID: WAP4008"

ANTENNA WARNING:

This device is tested with a standard SMA connector and with the antennas listed in Table 7 on page 14. When integrated in the OEMs product, these fixed antennas require installation preventing end-users from replacing them with non-approved antennas. Any antenna not in the following table must be tested to comply with FCC Section 15.203 for unique antenna connectors and Section 15.247 for emissions.

RF EXPOSURE:

To comply with FCC RF Exposure requirements, the Original Equipment Manufacturer (OEM) must ensure to install the approved antenna in the previous.

The preceding statement must be included as a CAUTION statement in manuals, for products operating with the approved antennas in Table 7 on page 14, to alert users on FCC RF Exposure compliance. Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of CYBLE-214015-01 is far below the FCC radio frequency exposure limits. Nevertheless, use CYBLE-214015-01 in such a manner that minimizes the potential for human contact during normal operation.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

## ISED

**Innovation, Science and Economic Development (ISED) Canada Certification**

CYBLE-214015-01 is licensed to meet the regulatory requirements of Innovation, Science and Economic Development (ISED) Canada.

License: IC: 7922A-4008

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from www.ic.gc.ca.

This device has been designed to operate with the antennas listed in Table 7 on page 14, having a maximum gain of 0.5 dBi. Antennas not included in this list or having a gain greater than 0.5 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

ISED NOTICE:

The device CYBLE-214015-01 complies with Canada RSS-GEN Rules. The device meets the requirements for modular transmitter approval as detailed in RSS-GEN. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

ISED RADIATION EXPOSURE STATEMENT FOR CANADA

This device complies with Innovation, Science and Economic Development (ISED) Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil est conforme à la norme sur l'innovation, la science et le développement économique (ISED) norme RSS exempte de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that ISED labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor IC identifier for this product as well as the ISED Notice above. The IC identifier is 7922A-4008. In any case, the end product must be labeled in its exterior with "Contains IC: 7922A-4008".

## European R&TTE Declaration of Conformity

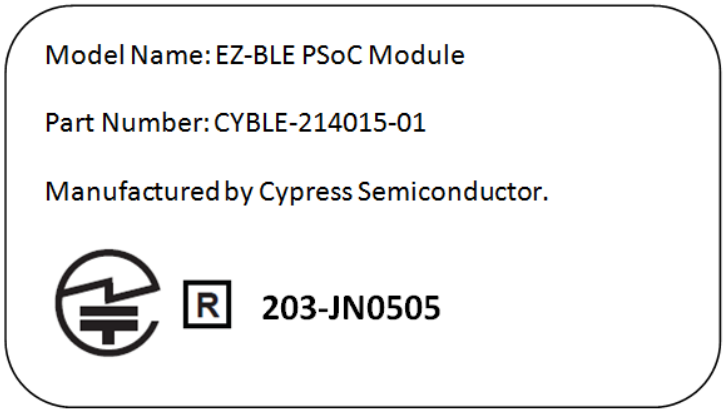
Hereby, Cypress Semiconductor declares that the Bluetooth module CYBLE-214015-01 complies with the essential requirements and other relevant provisions of Directive 1999/5/EC. As a result of the conformity assessment procedure described in Annex III of the Directive 1999/5/EC, the end-customer equipment should be labeled as follows:

All versions of the CYBLE-214015-01 in the specified reference design can be used in the following countries: Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

### MIC Japan

CYBLE-214015-01 is certified as a module with type certification number 203-JN0505. End products that integrate CYBLE-214015-01 do not need additional MIC Japan certification for the end product.

End product can display the certification label of the embedded module.




### KC Korea

CYBLE-214015-01 is certified for use in Korea with certificate number MSIP-CRM-Cyp-4008.

한국 인증 세부정보:

1. 제품명(모델명): 특정소출력무선기기(무선데이터통신시스템용 무선기기), CYBLE-214015-01
2. 인증 번호: MSIP-CRM-Cyp-4008
3. 라이선스 소유자: Cypress Semiconductor Corporation
4. 제조일자: 2015.12
5. 제조업체/국가명: Cypress Semiconductor Corporation/ 중국

해당 무선설비는 전파혼신 가능성이 있으므로 인명안전과 관련된 서비스는 할 수 없습니다.

## Packaging

**Table 56. Solder Reflow Peak Temperature**

| Module Part Number | Package | Maximum Peak Temperature | Maximum Time at PeakTemperature | No. of Cycles |
|---|---|---|---|---|
| CYBLE-214015-01 | 32-pad SMT | 260 °C | 30 seconds | 2 |

**Table 57. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

| Module Part Number | Package | MSL |
|---|---|---|
| CYBLE-214015-01 | 32-pad SMT | MSL 3 |

The CYBLE-214015-01 is offered in tape and reel packaging. Figure 10 details the tape dimensions used for the CYBLE-214015-01.

**Figure 10. CYBLE-214015-01 Tape Dimensions**

| Item | W | $A_0$ | $B_0$ | $K_0$ | $P_1$ | F | E | $D_0$ | $D_1$ | $P_0$ | $P_2$ | T |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Measurement | 24.0 | 11.30 | 11.30 | 2.30 | 16.0 | 11.5 | 1.75 | 1.50 | 1.50 | 4.00 | 2.00 | 0.30 |

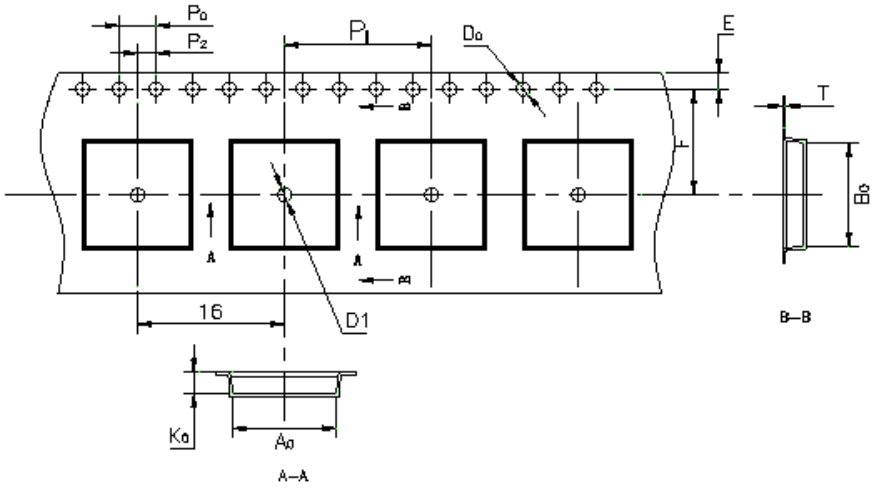



Figure 11 details the orientation of the CYBLE-214015-01 in the tape as well as the direction for unreeling.

**Figure 11. Component Orientation in Tape and Unreeling Direction**

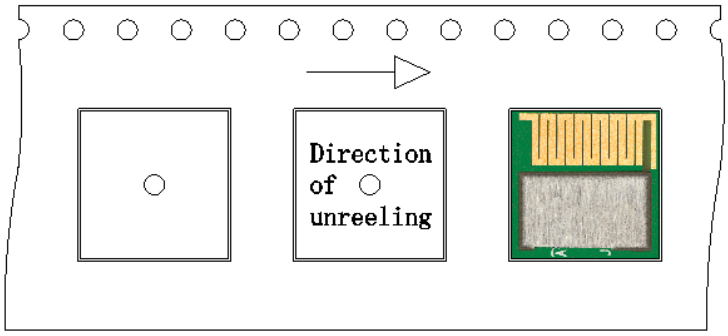
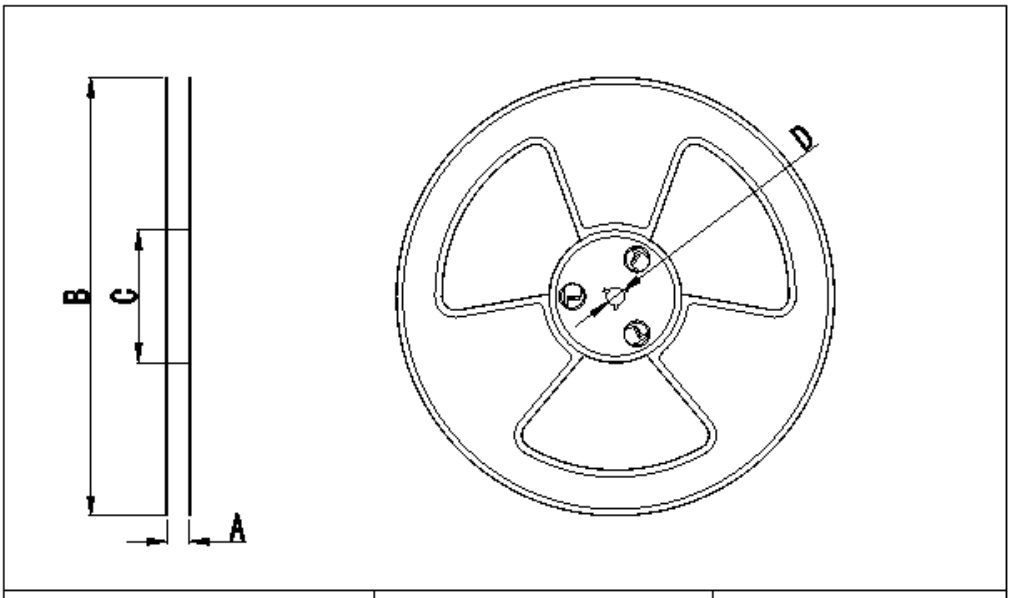


Figure 12 details reel dimensions used for the CYBLE-214015-01.

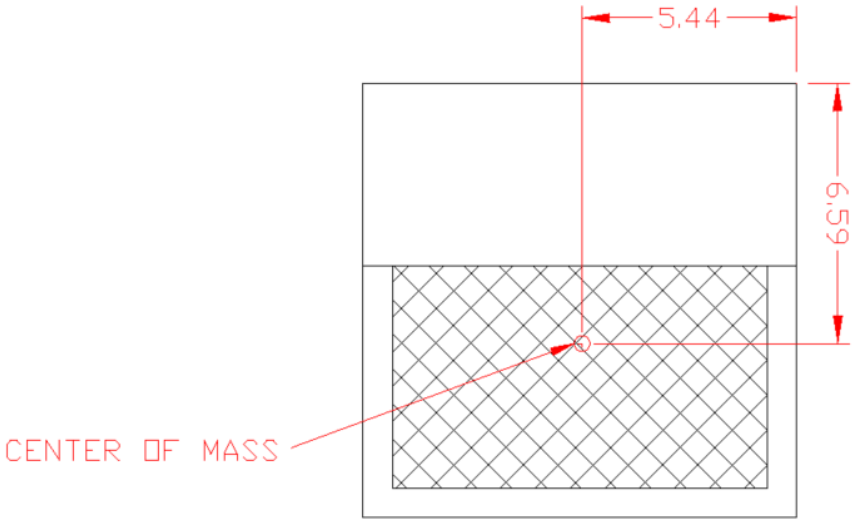
**Figure 12. Reel Dimensions**




| Index | NOTE | Dimension | Tolerance | |
|---|---|---|---|---|
| A | Inside Width | 24.4 | +2.0mm | -0.0mm |
| B | Reel Diameter | 254.00 | +2.0mm | -2.0mm |
| C | Outer Axis Diameter | 100.00 | +2.0mm | -2.0mm |
| D | Inner Axis Diameter | 13.20 | +0.3mm | -0.2mm |

The CYBLE-214015-01 is designed to be used with pick-and-place equipment in an SMT manufacturing environment. The center-of-mass for the CYBLE-214015-01 is detailed in Figure 13.

**Figure 13. CYBLE-214015-01 Center of Mass**



## Ordering Information

Table 58 lists the CYBLE-214015-01 part number and features. Table 59 lists the reel shipment quantities for the CYBLE-214015-01.

**Table 58. Ordering Information**

| MPN | Features | | | | | | | | | | | | | | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Max CPU Speed (MHz) | Flash (KB) | SRAM (KB) | UDB | Opamp (CTBm) | CapSense | Direct LCD Drive | 12-bit SAR ADC | LP Comparators | TCPWM Blocks | SCB Blocks | PWMs (using UDBs) | I2S (using UDB) | GPIO | |
| CYBLE-214015-01 | 48 | 256 | 32 | 4 | 4 | ✓ | ✓ | 1 Msps | 1 | 4 | 2 | 4 | ✓ | 25 | 32-SMT |

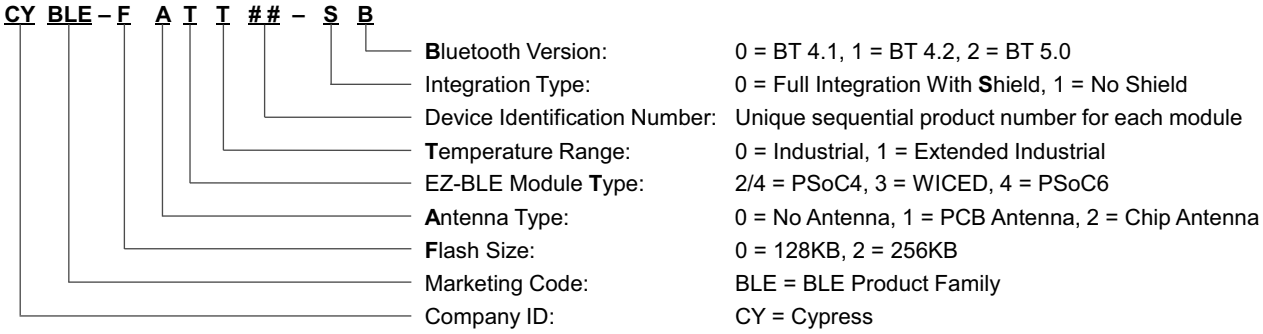
**Table 59. Tape and Reel Package Quantity and Minimum Order Amount**

| Description | Minimum Reel Quantity | Maximum Reel Quantity | Comments |
|---|---|---|---|
| Reel Quantity | 500 | 500 | Ships in 500 unit reel quantities. |
| Minimum Order Quantity (MOQ) | 500 | – | |
| Order Increment (OI) | 500 | – | |

The CYBLE-214015-01 is offered in tape and reel packaging. The CYBLE-214015-01 ships with a maximum of 500 units/reel.

### Part Numbering Convention

The part numbers are of the form CYBLE-FATT##-SB where the fields are defined as follows.




For additional information and a complete list of Cypress Semiconductor BLE products, contact your local Cypress sales representative. To locate the nearest Cypress office, visit our website.

| | |
|---|---|
| U.S. Cypress Headquarters Address | 198 Champion Court, San Jose, CA 95134 |
| U.S. Cypress Headquarter Contact Info | (408) 943-2600 |
| Cypress website address | http://www.cypress.com |

## Acronyms

**Table 60. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| ABUS | analog local bus |
| ADC | analog-to-digital converter |
| AG | analog global |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus |
| ALU | arithmetic logic unit |
| AMUXBUS | analog multiplexer bus |
| API | application programming interface |
| APSR | application program status register |
| ARM® | advanced RISC machine, a CPU architecture |
| ATM | automatic thump mode |
| BLE | Bluetooth Low Energy |
| Bluetooth SIG | Bluetooth Special Interest Group |
| BW | bandwidth |
| CAN | Controller Area Network, a communications protocol |
| CE | European Conformity |
| CSA | Canadian Standards Association |
| CMRR | common-mode rejection ratio |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| DAC | digital-to-analog converter, see also IDAC, VDAC |
| DFB | digital filter block |
| DIO | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DMIPS | Dhrystone million instructions per second |
| DMA | direct memory access, see also TD |
| DNL | differential nonlinearity, see also INL |
| DNU | do not use |
| DR | port write data registers |
| DSI | digital system interconnect |
| DWT | data watchpoint and trace |
| ECC | error correcting code |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| EMI | electromagnetic interference |

**Table 60. Acronyms Used in this Document** (continued)

| Acronym | Description |
|---|---|
| EMIF | external memory interface |
| EOC | end of conversion |
| EOF | end of frame |
| EPSR | execution program status register |
| ESD | electrostatic discharge |
| ETM | embedded trace macrocell |
| FCC | Federal Communications Commission |
| FET | field-effect transistor |
| FIR | finite impulse response, see also IIR |
| FPB | flash patch and breakpoint |
| FS | full-speed |
| GPIO | general-purpose input/output, applies to a PSoC pin |
| HCI | host controller interface |
| HVI | high-voltage interrupt, see also LVI, LVD |
| IC | integrated circuit |
| IDAC | current DAC, see also DAC, VDAC |
| IDE | integrated development environment |
| $I^2C$, or IIC | Inter-Integrated Circuit, a communications protocol |
| IC | Industry Canada |
| IIR | infinite impulse response, see also FIR |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| INL | integral nonlinearity, see also DNL |
| I/O | input/output, see also GPIO, DIO, SIO, USBIO |
| IPOR | initial power-on reset |
| IPSR | interrupt program status register |
| IRQ | interrupt request |
| ITM | instrumentation trace macrocell |
| KC | Korea Certification |
| LCD | liquid crystal display |
| LIN | Local Interconnect Network, a communications protocol. |
| LR | link register |
| LUT | lookup table |
| LVD | low-voltage detect, see also LVI |
| LVI | low-voltage interrupt, see also HVI |
| LVTTL | low-voltage transistor-transistor logic |

**Table 60. Acronyms Used in this Document** (continued)

| Acronym | Description |
|---|---|
| MAC | multiply-accumulate |
| MCU | microcontroller unit |
| MIC | Ministry of Internal Affairs and Communications (Japan) |
| MISO | master-in slave-out |
| NC | no connect |
| NMI | nonmaskable interrupt |
| NRZ | non-return-to-zero |
| NVIC | nested vectored interrupt controller |
| NVL | nonvolatile latch, see also WOL |
| Opamp | operational amplifier |
| PAL | programmable array logic, see also PLD |
| PC | program counter |
| PCB | printed circuit board |
| PGA | programmable gain amplifier |
| PHUB | peripheral hub |
| PHY | physical layer |
| PICU | port interrupt control unit |
| PLA | programmable logic array |
| PLD | programmable logic device, see also PAL |
| PLL | phase-locked loop |
| PMDD | package material declaration data sheet |
| POR | power-on reset |
| PRES | precise power-on reset |
| PRS | pseudo random sequence |
| PS | port read data register |
| PSoC® | Programmable System-on-Chip™ |
| PSRR | power supply rejection ratio |
| PWM | pulse-width modulator |
| QDID | qualification design ID |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| RTC | real-time clock |
| RTL | register transfer language |
| RTR | remote transmission request |
| RX | receive |
| SAR | successive approximation register |
| SC/CT | switched capacitor/continuous time |
| SCL | $I^2C$ serial clock |

**Table 60. Acronyms Used in this Document** (continued)

| Acronym | Description |
|---|---|
| SDA | $I^2C$ serial data |
| S/H | sample and hold |
| SINAD | signal to noise and distortion ratio |
| SIO | special input/output, GPIO with advanced features. See GPIO. |
| SMT | surface-mount technology; a method for producing electronic circuitry in which the components are placed directly onto the surface of PCBs |
| SOC | start of conversion |
| SOF | start of frame |
| SPI | Serial Peripheral Interface, a communications protocol |
| SR | slew rate |
| SRAM | static random access memory |
| SRES | software reset |
| STN | super twisted nematic |
| SWD | serial wire debug, a test protocol |
| SWV | single-wire viewer |
| TD | transaction descriptor, see also DMA |
| THD | total harmonic distortion |
| TIA | transimpedance amplifier |
| TN | twisted nematic |
| TRM | technical reference manual |
| TTL | transistor-transistor logic |
| TUV | Germany: Technischer Überwachungs-Verein (Technical Inspection Association) |
| TX | transmit |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UDB | universal digital block |
| USB | Universal Serial Bus |
| USBIO | USB input/output, PSoC pins used to connect to a USB port |
| VDAC | voltage DAC, see also DAC, IDAC |
| WDT | watchdog timer |
| WOL | write once latch, see also NVL |
| WRES | watchdog timer reset |
| XRES | external reset I/O pin |
| XTAL | crystal |

# Document Conventions

## Units of Measure

**Table 61. Units of Measure**

| Symbol | Unit of Measure |
|---|---|
| °C | degrees Celsius |
| dB | decibel |
| dBm | decibel-milliwatts |
| fF | femtofarads |
| Hz | hertz |
| KB | 1024 bytes |
| kbps | kilobits per second |
| Khr | kilohour |
| kHz | kilohertz |
| kΩ | kilo ohm |
| ksps | kilosamples per second |
| LSB | least significant bit |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msps | megasamples per second |
| µA | microampere |
| µF | microfarad |
| µH | microhenry |
| µs | microsecond |
| µV | microvolt |
| µW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| nV | nanovolt |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |
| sqrtHz | square root of hertz |
| V | volt |

## Document History Page

| Document Title: CYBLE-214015-01 EZ-BLE™ Creator Module<br>Document Number: 002-15923 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 5428716 | DSO | 09/07/2016 | Preliminary datasheet for CYBLE-214015-01 module. |
| *A | 5536076 | DSO | 11/29/2016 | Updated More Information:<br>Added EZ-Serial™ BLE Firmware Platform section.<br>Updated Overview:<br>Updated Figure 1 to specify that Bottom View is “Seen from Bottom”.<br>Updated Recommended Host PCB Layout:<br>Updated Figure 4, Figure 5, and Figure 6 captions to specify that these as “Seen on Host PCB”.<br>Updated Power Supply Connections and Recommended External Components:<br>Updated Figure 7 and Figure 8 to specify that these are “Seen from Bottom”.<br>Updated Digital and Analog Capabilities and Connections:<br>Updated Table 4:<br>Updated TCPWM column to add TCPWM capability on Port 2 pins.<br>Added Footnote 3.<br>Updated Document History Page:<br>Remove “,” from Document Title. |
| *B | 5554670 | DSO | 12/15/2016 | Updated Table 5:<br>Port 2.x OPAMP definitions changed to CTBm0 instead of CTBm1.<br>Updated Power Supply Connections and Recommended External Components:<br>Updated typo to state that the use of one to three ferrite beads will depend on the application configuration. |
| *C | 5965469 | AESATMP8 | 11/13/2017 | Updated logo and Copyright. |
| *D | 6006702 | DSO | 12/27/2017 | Updated reel dimensions in Figure 10 and Figure 12. |
| *E | 6091378 | DSO | 03/12/2018 | Updated the title as “EZ-BLE™ Creator Module**”.**<br>Updated the links of QDID and Declaration ID in Module Description section as “**https://launchstudio.bluetooth.com/ListingDetails/2183**”<br>Updated “PSoC 4” to “Creator” throughout the document.<br>Updated More Information section.<br>Updated the term “IC” to “ISED”.<br>Changed the Heading “Industry Canada (IC) Certification” to “ISED” and added a subtitle “Innovation, Science and Economic Development Canada (ISED) Certification”.<br>Updated Part Numbering Convention.<br>Added “Cet appareil est conforme à la norme sur l'innovation, la science et le développement économique (ISED) norme RSS exempte de licence. L'exploitation est autorisée aux deux conditions suivantes:” in ISED RADIATION EXPOSURE STATEMENT FOR CANADA.<br>Updated the Copyright year. |

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