

P-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
- 60	0.155 at $V_{GS} = - 10$ V	- 8.4	12.5
	0.280 at $V_{GS} = - 4.5$ V	- 7.4	

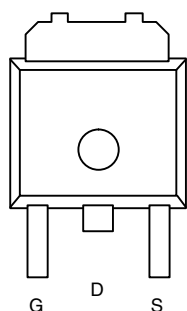
FEATURES

- TrenchFET® Power MOSFETS
- Material categorization:
For definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

TO-252

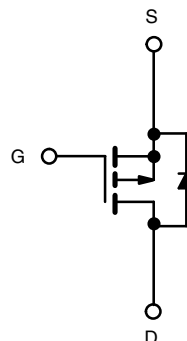


Top View

Drain Connected to Tab

Ordering Information:

SUD08P06-155L-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_J = 150$ °C)	I_D	- 8.2	A
		- 5.2	
Pulsed Drain Current	I_{DM}	- 18	
Continuing Source Current (Diode Conduction)	I_S	- 8.4	
Avalanche Current	I_{AS}	- 12	
Single Pulse Avalanche Energy	E_{AS}	7.2	mJ
Maximum Power Dissipation	P_D	20.8 ^a	W
		1.7 ^b	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient ^b	R_{thJA}	20	25	°C/W
		62	75	
Junction-to-Case	R_{thJC}	5	6	

Notes:

a. See SOA curve for voltage derating.

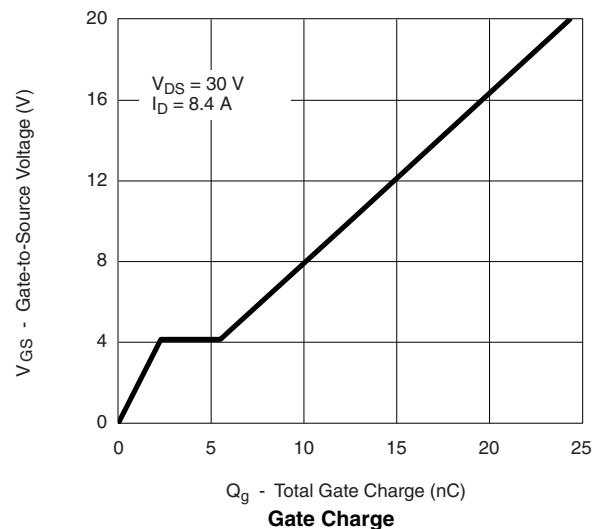
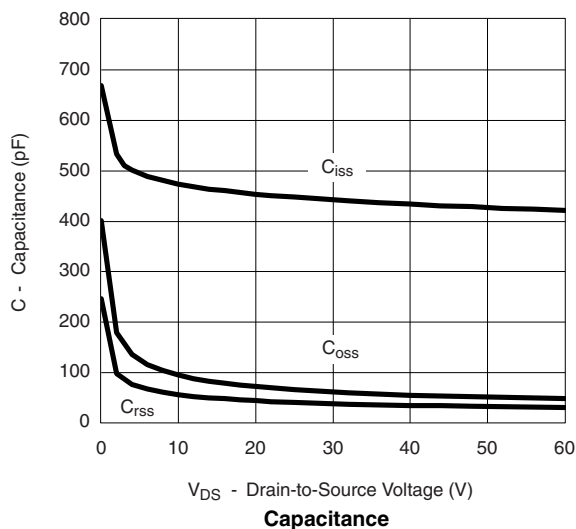
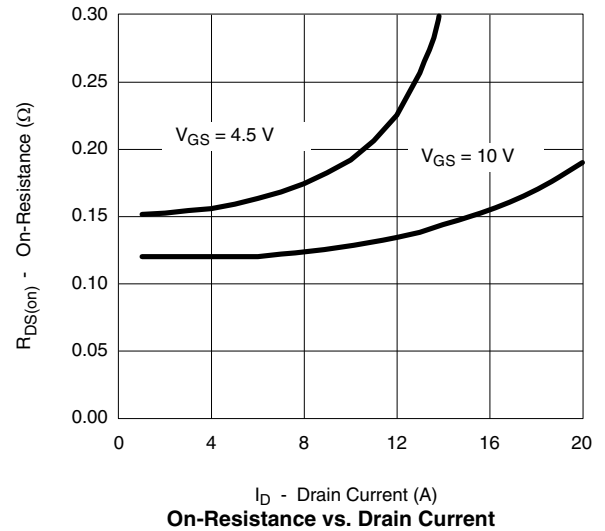
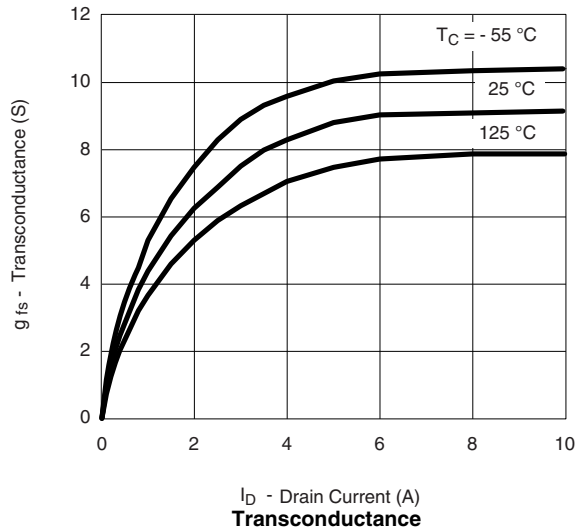
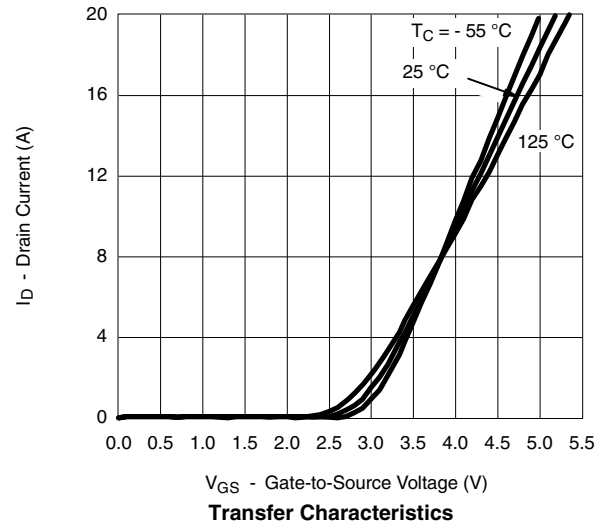
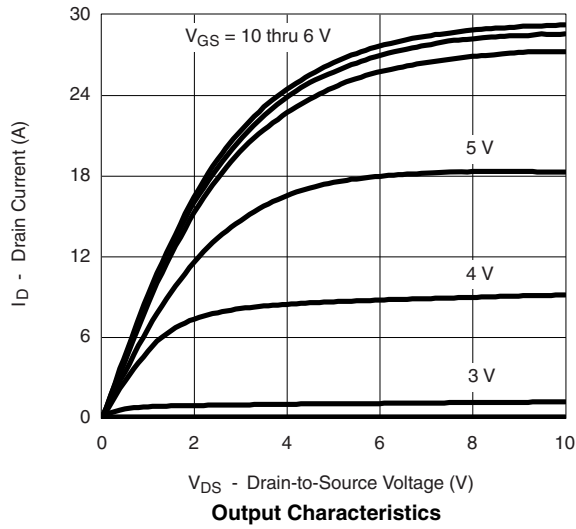
b. Surface mounted on 1" x 1" FR-4 board.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 60			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 1	- 2	- 3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 60 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 60 V, V _{GS} = 0 V, T _J = 125 °C			- 50	
		V _{DS} = - 60 V, V _{GS} = 0 V, T _J = 150 °C			- 150	
On-State Drain Current ^b	I _{D(on)}	V _{DS} = - 5 V, V _{GS} = - 10 V	- 10			A
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = - 10 V, I _D = - 5 A		0.125	0.155	Ω
		V _{GS} = - 10 V, I _D = - 5 A, T _J = 125 °C			0.280	
		V _{GS} = - 10 V, I _D = - 5 A, T _J = 150 °C			0.350	
		V _{GS} = - 4.5 V, I _D = - 2 A		0.158	0.280	
Forward Transconductance ^b	g _{fs}	V _{DS} = - 15 V, I _D = - 5 A		8		S
Dynamic						
Input Capacitance	C _{iss}	V _{DS} = - 25 V, V _{GS} = 0 V, f = 1 MHz		450		pF
Output Capacitance	C _{oss}			65		
Reverse Transfer Capacitance	C _{rss}			40		
Total Gate Charge	Q _g	V _{DS} = - 30 V, V _{GS} = - 10 V, I _D = - 8.4 A		12.5	19	nC
Gate-Source Charge	Q _{gs}			2.3		
Gate-Drain Charge	Q _{gd}			3.2		
Gate Resistance	R _g	f = 1 MHz		8		Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = - 30 V, R _L = 3.57 Ω I _D ≡ - 8.4 A, V _{GEN} = - 10 V, R _G = 2.5 Ω		5	10	ns
Rise Time ^c	t _r			14	25	
Turn-Off Delay Time ^c	t _{d(off)}			15	25	
Fall Time ^c	t _f			7	12	
Source-Drain Diode Ratings and Characteristics (T _C = 25 °C) ^b						
Pulsed Current	I _{SM}				- 20	A
Forward Voltage ^b	V _{SD}	I _F = - 2 A, V _{GS} = 0 V		- 0.9	- 1.3	V
Reverse Recovery Time	t _{rr}	I _F = - 8 A, dI/dt = 100 A/μs		50	80	ns
Reverse Recovery Time	Q _{rr}			80	120	nC

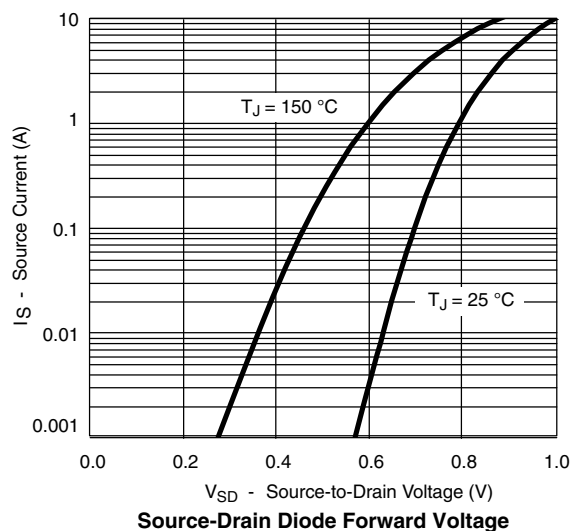
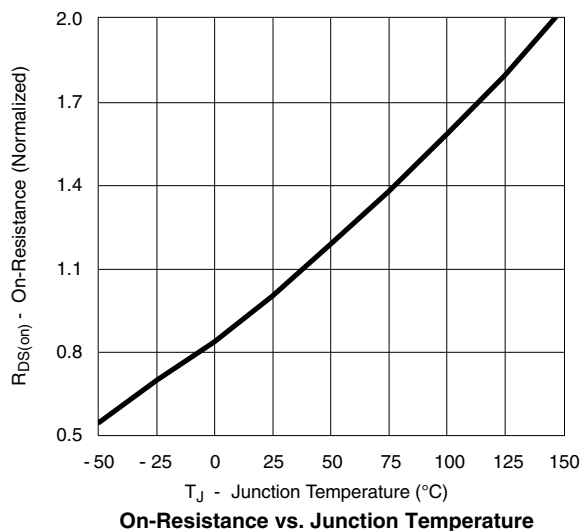
Notes:

- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
c. Independent of operating temperature.

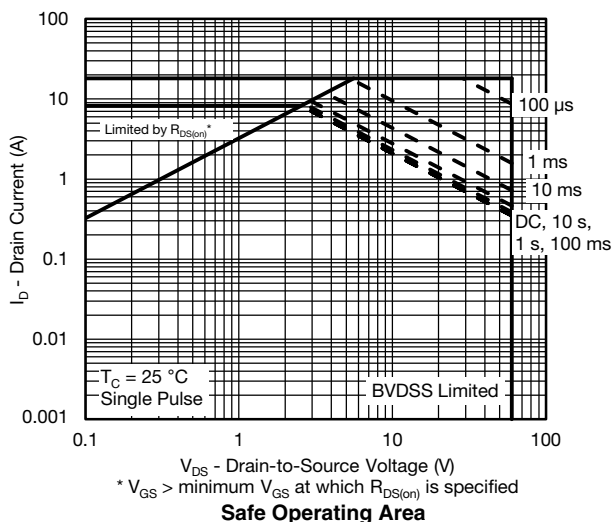
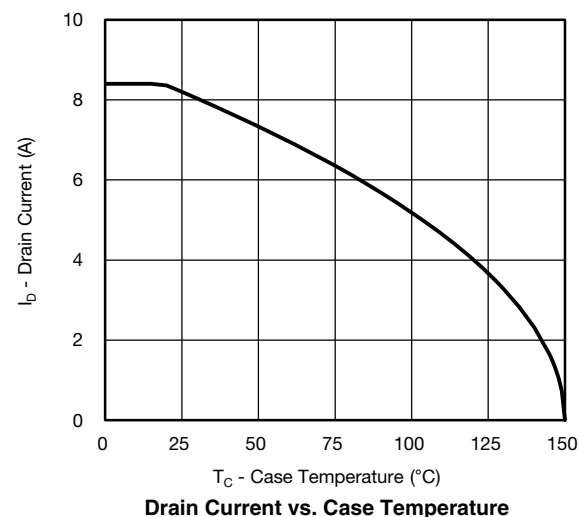
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

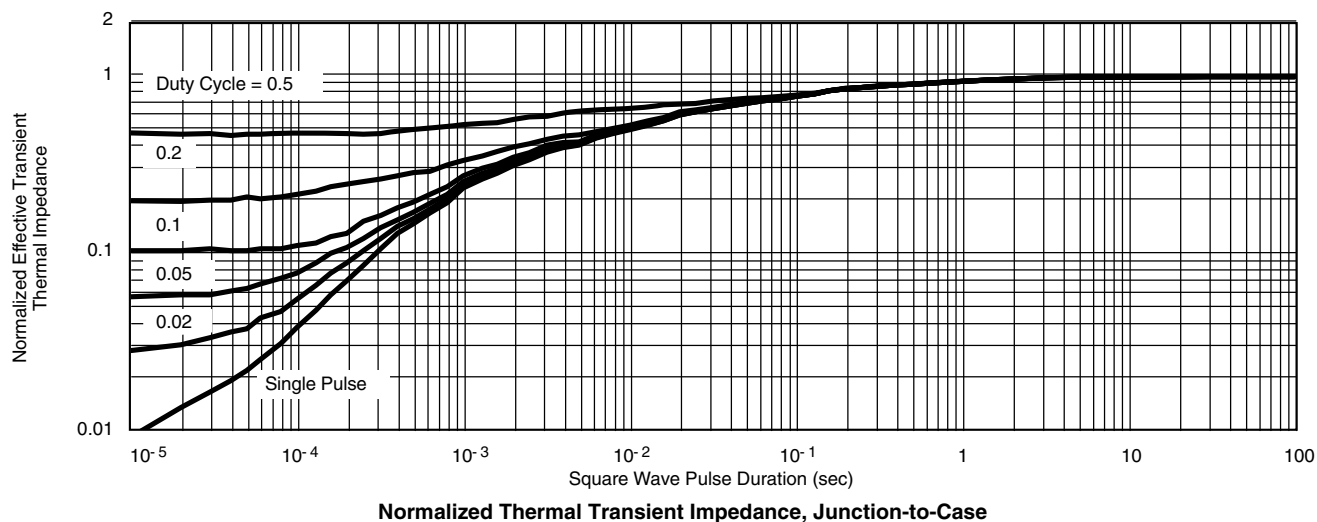
TYPICAL CHARACTERISTICS (25 °C unless noted)


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THERMAL RATINGS

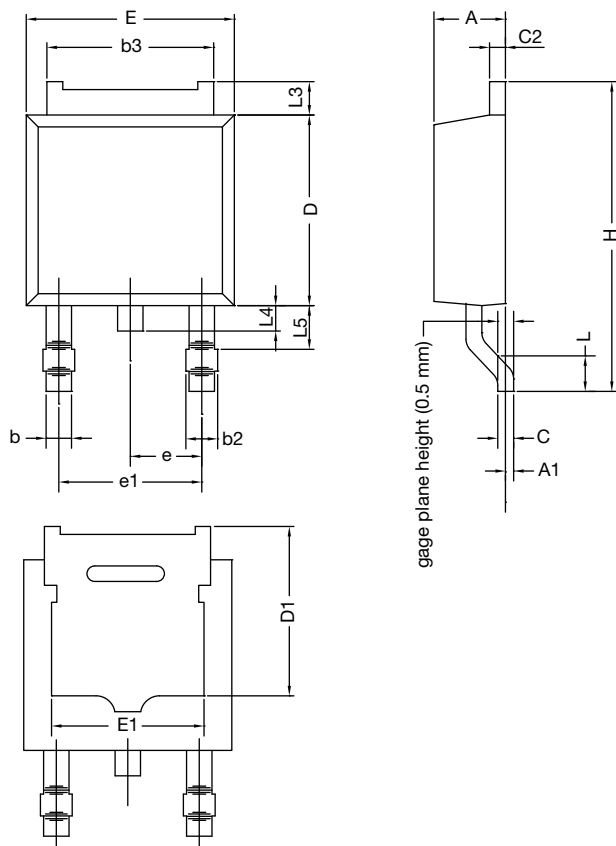


THERMAL RATINGS


Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62843.



TO-252AA Case Outline

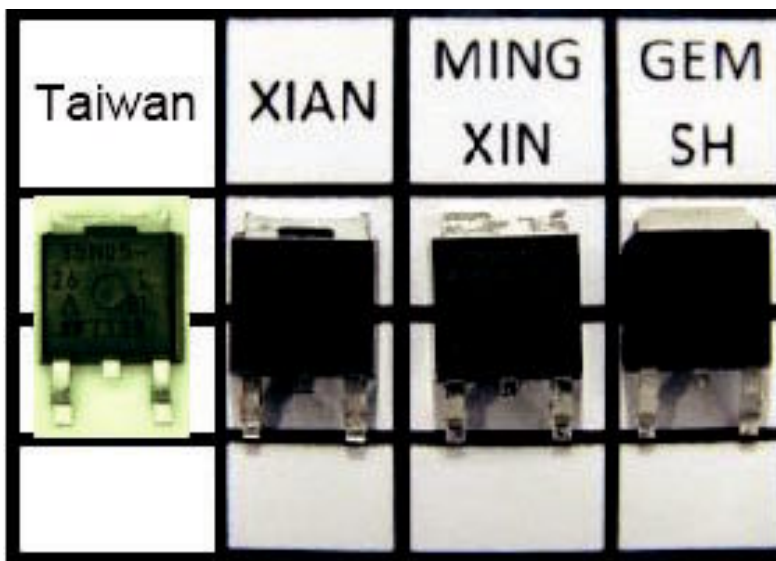


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

ECN: T13-0359-Rev. O, 03-Jun-13
DWG: 5347

Notes

- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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