

# 74ALVC164245-Q100

16-bit dual supply translating transceiver; 3-state

Rev. 3 — 9 April 2019

Product data sheet

## 1. General description

The 74ALVC164245-Q100 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74ALVC164245-Q100 is a 16-bit (dual octal) dual supply translating transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. It is designed to interface between a 3 V and 5 V bus in a mixed 3 V and 5 V supply environment.

This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The direction control inputs (1DIR and 2DIR) determine the direction of the data flow. nDIR (active HIGH) enables data from nAn ports to nBn ports. nDIR (active LOW) enables data from nBn ports to nAn ports. The output enable inputs (1 $\overline{OE}$  and 2 $\overline{OE}$ ), when HIGH, disable both nAn and nBn ports by placing them in a high-impedance OFF-state. Pins nAn, n $\overline{OE}$  and nDIR are referenced to  $V_{CC(A)}$  and pins nBn are referenced to  $V_{CC(B)}$ .

In suspend mode, when one of the supply voltages is zero, there is no current flow from the non-zero supply towards the zero supply. The nAn outputs must be set 3-state and the voltage on the A-bus must be smaller than  $V_{diode}$  (typical 0.7 V).  $V_{CC(B)} \geq V_{CC(A)}$  (except in suspend mode).

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

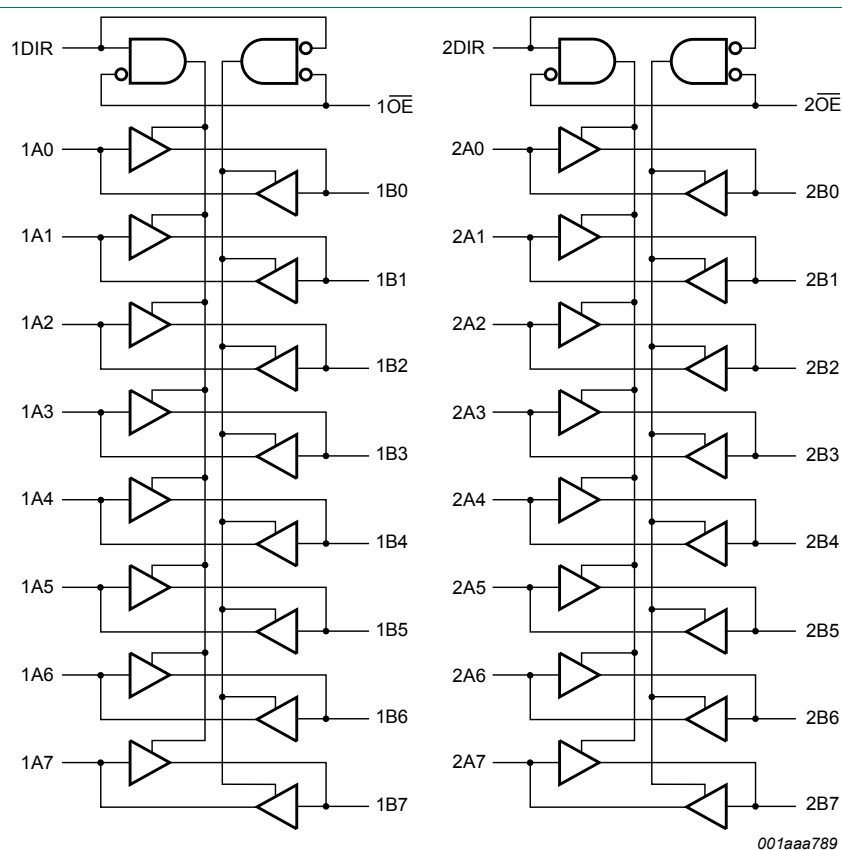
- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range:
  - 3 V port ( $V_{CC(A)}$ ): 1.5 V to 3.6 V
  - 5 V port ( $V_{CC(B)}$ ): 1.5 V to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Control inputs voltage range from 2.7 V to 5.5 V
- Inputs accept voltages up to 5.5 V
- High-impedance outputs when  $V_{CC(A)}$  or  $V_{CC(B)} = 0$  V
- Complies with JEDEC standard JESD8-B/JESD36
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0  $\Omega$ )

### 3. Ordering information

### Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVC164245DGG-Q100	-40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

#### 4. Functional diagram



**Fig. 1. Logic symbol**

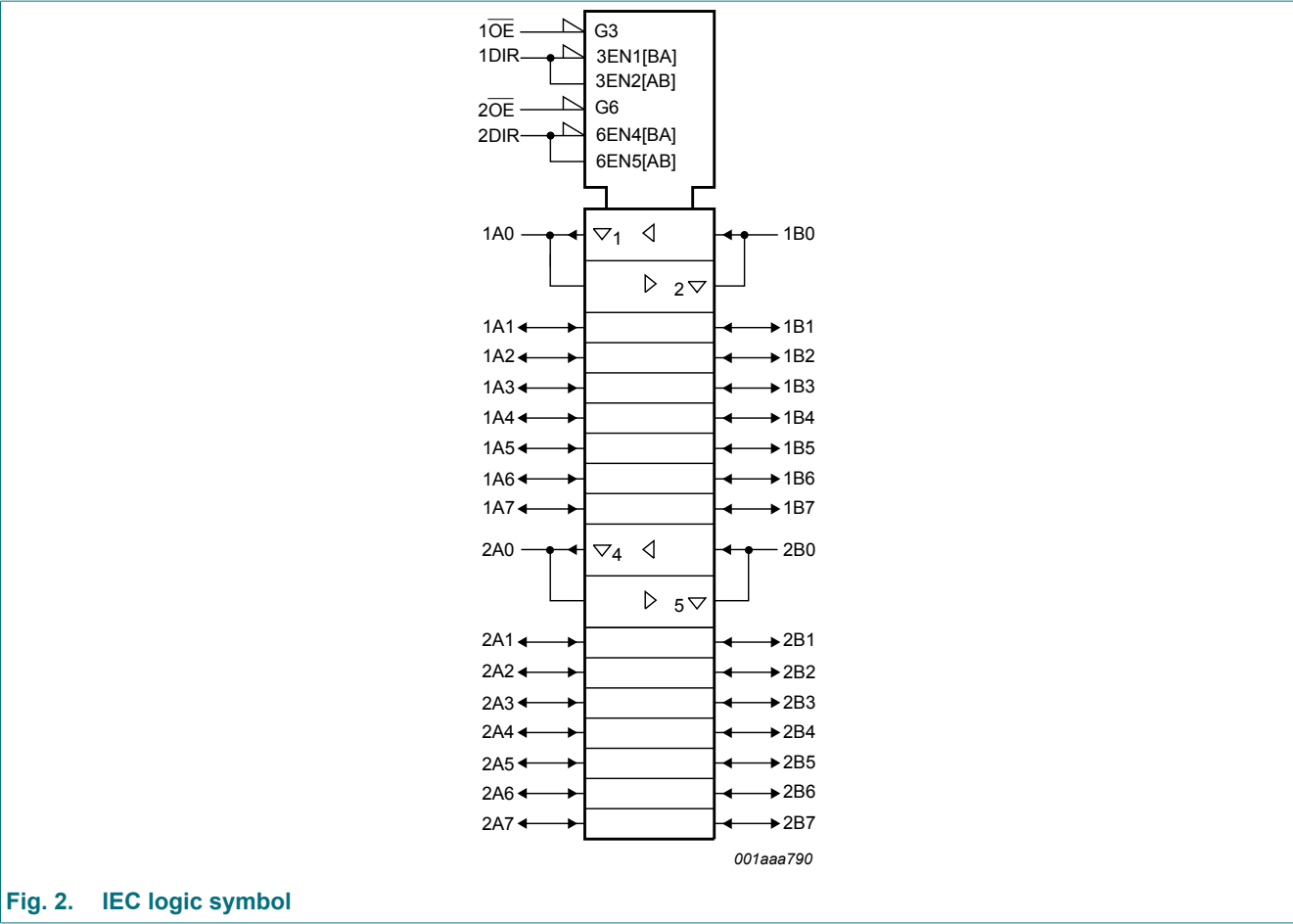


Fig. 2. IEC logic symbol

5. Pinning information

5.1. Pinning

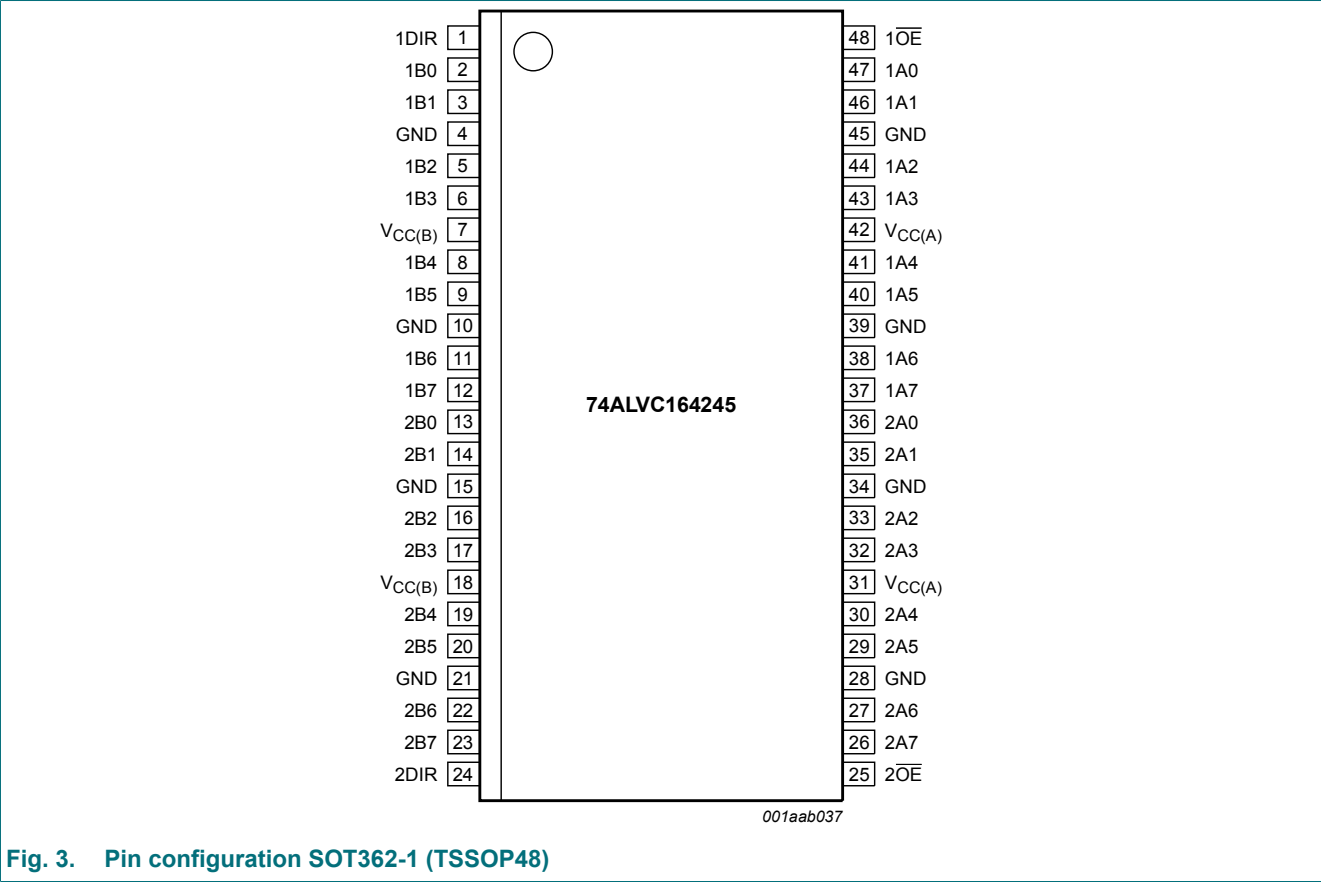


Fig. 3. Pin configuration SOT362-1 (TSSOP48)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1DIR, 2DIR	1, 24	direction control input
1B0, 1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7	2, 3, 5, 6, 8, 9, 11, 12	data input/output
2B0, 2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7	13, 14, 16, 17, 19, 20, 22, 23	data input/output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V <sub>CC(B)</sub>	7, 18	supply voltage B (5 V bus)
1OE, 2OE	48, 25	output enable input (active LOW)
1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7	47, 46, 44, 43, 41, 40, 38, 37	data input/output
2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7	36, 35, 33, 32, 30, 29, 27, 26	data input/output
V <sub>CC(A)</sub>	31, 42	supply voltage A (3 V bus)

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.*

Inputs		Outputs	
nOE	nDIR	nAn	nBn
L	L	nAn = nBn	inputs
L	H	inputs	nBn = nAn
H	X	Z	Z

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(B)}$	supply voltage B	$V_{CC(B)} \geq V_{CC(A)}$	-0.5	+6.0	V
$V_{CC(A)}$	supply voltage A	$V_{CC(B)} \geq V_{CC(A)}$	-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage	[1]	-0.5	+6.0	V
$V_{I/O}$	input/output voltage		-0.5	$V_{CC} + 0.5$	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	$\pm 50$	mA
$V_O$	output voltage	output HIGH or LOW [1]	-0.5	$V_{CC} + 0.5$	V
		output 3-state [1]	-0.5	+6.0	V
$I_{O(sink/source)}$	output sink or source current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature	[2]	-	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C [3]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] Above 60 °C the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(B)}$	supply voltage B	$V_{CC(B)} \geq V_{CC(A)}$				
		maximum speed performance	2.7	-	5.5	V
		low-voltage applications	1.5	-	5.5	V
$V_{CC(A)}$	supply voltage A	$V_{CC(B)} \geq V_{CC(A)}$				
		maximum speed performance	2.7	-	3.6	V
		low-voltage applications	1.5	-	3.6	V
$V_I$	input voltage	control inputs: $\overline{nOE}$ and $nDIR$	0	-	5.5	V
$V_{I/O}$	input/output voltage	nAn port	0	-	$V_{CC(A)}$	V
		nBn port	0	-	$V_{CC(B)}$	V
$V_O$	output voltage	nAn port	0	-	$V_{CC(A)}$	V
		nBn port	0	-	$V_{CC(B)}$	V
$T_{amb}$	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC(A)} = 2.7 \text{ V to } 3.0 \text{ V}$	0	-	20	ns/V
		$V_{CC(A)} = 3.0 \text{ V to } 3.6 \text{ V}$	0	-	10	ns/V
		$V_{CC(B)} = 3.0 \text{ V to } 4.5 \text{ V}$	0	-	20	ns/V
		$V_{CC(B)} = 4.5 \text{ V to } 5.5 \text{ V}$	0	-	10	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	nBn port						
		$V_{CC(B)} = 3.0 \text{ V to } 5.5 \text{ V}$ [2]	2.0	-	-	2.0	-	V
		nAn port, $\overline{nOE}$ and $nDIR$						
		$V_{CC(A)} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	-	-	2.0	-	V
		$V_{CC(A)} = 2.3 \text{ V to } 2.7 \text{ V}$ [2]	1.7	-	-	1.7	-	V
$V_{IL}$	LOW-level input voltage	nBn port						
		$V_{CC(B)} = 4.5 \text{ V to } 5.5 \text{ V}$ [2]	-	-	0.8	-	0.8	V
		$V_{CC(B)} = 3.0 \text{ V to } 3.6 \text{ V}$ [2]	-	-	0.7	-	0.7	V
		nAn port, $\overline{nOE}$ and $nDIR$						
		$V_{CC(A)} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	0.8	-	0.8	V
		$V_{CC(A)} = 2.3 \text{ V to } 2.7 \text{ V}$ [2]	-	-	0.7	-	0.7	V

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V <sub>OH</sub>	HIGH-level output voltage	nBn port; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -24 mA; V <sub>CC(B)</sub> = 4.5 V	V <sub>CC(B)</sub> - 0.8	-	-	V <sub>CC(B)</sub> - 1.2	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC(B)</sub> = 4.5 V	V <sub>CC(B)</sub> - 0.5	-	-	V <sub>CC(B)</sub> - 0.8	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC(B)</sub> = 3.0 V	V <sub>CC(B)</sub> - 0.8	-	-	V <sub>CC(B)</sub> - 1.0	-	V
		I <sub>O</sub> = -100 µA; V <sub>CC(B)</sub> = 3.0 V	V <sub>CC(B)</sub> - 0.2	V <sub>CC(B)</sub>	-	V <sub>CC(B)</sub> - 0.3	-	V
		nAn port; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -24 mA; V <sub>CC(A)</sub> = 3.0 V	V <sub>CC(A)</sub> - 0.7	-	-	V <sub>CC(A)</sub> - 1.0	-	V
		I <sub>O</sub> = -100 µA; V <sub>CC(A)</sub> = 3.0 V	V <sub>CC(A)</sub> - 0.2	-	-	V <sub>CC(A)</sub> - 0.3	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC(A)</sub> = 2.7 V	V <sub>CC(A)</sub> - 0.5	-	-	V <sub>CC(A)</sub> - 0.8	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC(A)</sub> = 2.3 V	V <sub>CC(A)</sub> - 0.6	-	-	V <sub>CC(A)</sub> - 0.6	-	V
		I <sub>O</sub> = -100 µA; V <sub>CC(A)</sub> = 2.3 V	V <sub>CC(A)</sub> - 0.2	V <sub>CC(A)</sub>	-	V <sub>CC(A)</sub> - 0.3	-	V
V <sub>OL</sub>	LOW-level output voltage	nBn port; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 24 mA; V <sub>CC(B)</sub> = 4.5 V	-	-	0.55	-	0.80	V
		I <sub>O</sub> = 12 mA; V <sub>CC(B)</sub> = 4.5 V	-	-	0.40	-	0.60	V
		I <sub>O</sub> = 100 µA; V <sub>CC(B)</sub> = 4.5 V	-	-	0.20	-	0.30	V
		I <sub>O</sub> = 18 mA; V <sub>CC(B)</sub> = 3.0 V	-	-	0.55	-	0.80	V
		I <sub>O</sub> = 100 µA; V <sub>CC(B)</sub> = 3.0 V	-	-	0.20	-	0.30	V
		nAn port; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 24 mA; V <sub>CC(A)</sub> = 3.0 V	-	-	0.55	-	0.80	V
		I <sub>O</sub> = 100 µA; V <sub>CC(A)</sub> = 3.0 V	-	-	0.20	-	0.30	V
		I <sub>O</sub> = 12 mA; V <sub>CC(A)</sub> = 2.7 V	-	-	0.40	-	0.60	V
		I <sub>O</sub> = 12 mA; V <sub>CC(A)</sub> = 2.3 V	-	-	0.60	-	0.60	V
		I <sub>O</sub> = 100 µA; V <sub>CC(A)</sub> = 2.3 V	-	-	0.20	-	0.20	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	-	±0.1	±5	-	±10	µA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND [3]	-	±0.1	±10	-	±20	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.1	40	-	80	µA
ΔI <sub>CC</sub>	additional supply current	per control pin; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A [4]	-	5	500	-	5000	µA
C <sub>I</sub>	input capacitance		-	4.0	-	-	-	pF
C <sub>I/O</sub>	input/output capacitance	nAn and nBn port	-	5.0	-	-	-	pF

[1] All typical values are measured at V<sub>CC(B)</sub> = 5.0 V, V<sub>CC(A)</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

[2] If V<sub>CC(A)</sub> < 2.7 V, the switching levels at all inputs are not TTL compatible.

[3] For transceivers, the parameter I<sub>OZ</sub> includes the input leakage current.

[4] V<sub>CC(A)</sub> = 2.7 V to 3.6 V: other inputs at V<sub>CC(A)</sub> or GND; V<sub>CC(B)</sub> = 4.5 V to 5.5 V: other inputs at V<sub>CC(B)</sub> or GND.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

$GND = 0\text{ V}$ ;  $t_r = t_f \leq 2.5\text{ ns}$ ;  $C_L = 50\text{ pF}$ ; for test circuit see Fig. 6.

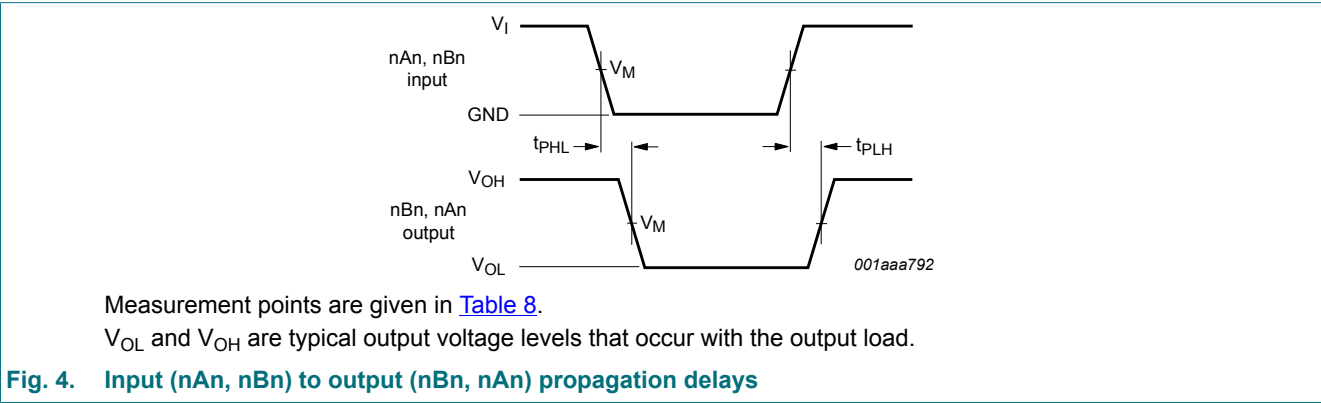
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$t_{pd}$	propagation delay	nAn to nBn; see Fig. 4 [2]						
		$V_{CC(A)} = 2.3\text{ V to }2.7\text{ V};$ $V_{CC(B)} = 3.0\text{ V to }3.6\text{ V}$	1.5	3.3	7.6	1.5	9.5	ns
		$V_{CC(A)} = 2.7\text{ V};$ $V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$	1.0	3.0	5.9	1.0	7.5	ns
		$V_{CC(A)} = 3.0\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$	1.0	2.9	5.8	1.0	7.5	ns
		nBn to nAn; see Fig. 4 [2]						
		$V_{CC(A)} = 2.3\text{ V to }2.7\text{ V};$ $V_{CC(B)} = 3.0\text{ V to }3.6\text{ V}$	1.0	3.0	7.6	1.0	9.5	ns
		$V_{CC(A)} = 2.7\text{ V};$ $V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$	1.0	4.3	6.7	1.0	8.5	ns
		$V_{CC(A)} = 3.0\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$	1.2	2.5	5.8	1.2	7.5	ns
$t_{en}$	enable time	nOE to nBn; see Fig. 5 [3]						
		$V_{CC(A)} = 2.3\text{ V to }2.7\text{ V};$ $V_{CC(B)} = 3.0\text{ V to }3.6\text{ V}$	1.5	4.1	11.5	1.5	14.5	ns
		$V_{CC(A)} = 2.7\text{ V};$ $V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$	1.5	3.6	9.2	1.5	11.5	ns
		$V_{CC(A)} = 3.0\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$	1.0	3.2	8.9	1.0	12.0	ns
		nOE to nAn; see Fig. 5 [3]						
		$V_{CC(A)} = 2.3\text{ V to }2.7\text{ V};$ $V_{CC(B)} = 3.0\text{ V to }3.6\text{ V}$	1.5	4.6	12.3	1.5	15.5	ns
		$V_{CC(A)} = 2.7\text{ V};$ $V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$	1.5	4.3	9.3	1.5	12.0	ns
		$V_{CC(A)} = 3.0\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$	1.0	3.2	8.9	1.0	11.5	ns
$t_{dis}$	disable time	nOE to nBn; see Fig. 5 [4]						
		$V_{CC(A)} = 2.3\text{ V to }2.7\text{ V};$ $V_{CC(B)} = 3.0\text{ V to }3.6\text{ V}$	2.0	2.7	10.5	2.0	13.5	ns
		$V_{CC(A)} = 2.7\text{ V};$ $V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$	2.5	4.6	9.0	2.5	11.5	ns
		$V_{CC(A)} = 3.0\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$	2.1	4.9	8.6	2.1	11.0	ns
		nOE to nAn; see Fig. 5 [4]						
		$V_{CC(A)} = 2.3\text{ V to }2.7\text{ V};$ $V_{CC(B)} = 3.0\text{ V to }3.6\text{ V}$	1.0	2.7	9.3	1.0	12.0	ns
		$V_{CC(A)} = 2.7\text{ V};$ $V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$	1.5	3.5	9.0	1.5	11.5	ns
		$V_{CC(A)} = 3.0\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 4.5\text{ V to }5.5\text{ V}$	2.0	3.2	8.6	2.0	11.0	ns

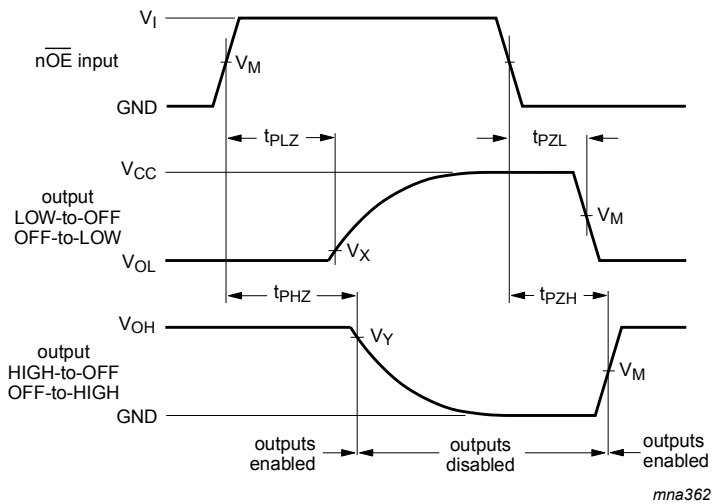


Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
C <sub>PD</sub>	power dissipation capacitance	5 V port: nAn to nBn; V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC(B)</sub> = 5 V; V <sub>CC(A)</sub> = 3.3 V [5]						
		outputs enabled	-	30	-	-	-	pF
		outputs disabled	-	15	-	-	-	pF
		3 V port: nBn to nAn; V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC(B)</sub> = 5 V; V <sub>CC(A)</sub> = 3.3 V [5]						
		outputs enabled	-	40	-	-	-	pF
		outputs disabled	-	5	-	-	-	pF

- [1] All typical values are measured at nominal voltage for V<sub>CC(B)</sub> and V<sub>CC(A)</sub> and at T<sub>amb</sub> = 25 °C.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.
- [3] t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.
- [4] t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.
- [5] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
f<sub>i</sub> = input frequency in MHz;  
f<sub>o</sub> = output frequency in MHz;  
C<sub>L</sub> = output load capacitance in pF;  
V<sub>CC</sub> = supply voltage in V;  
N = number of inputs switching;  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

10.1. Waveforms and test circuit



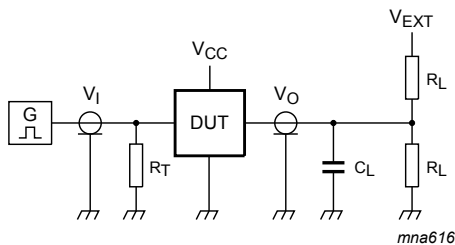


Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with output load.

Fig. 5. 3-state enable and disable times

Table 8. Measurement points

Direction	Supply voltage		Input		Output		
	$V_{CC(A)}$	$V_{CC(B)}$	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
nAn port to nBn port	2.3 V to 2.7 V	2.7 V to 3.6 V	$V_{CC(A)}$	$0.5 \times V_{CC(A)}$	1.5 V	$V_{OL(B)} + 0.3 \text{ V}$	$V_{OH(B)} - 0.3 \text{ V}$
nBn port to nAn port	2.3 V to 2.7 V	2.7 V to 3.6 V	2.7 V	1.5 V	$0.5 \times V_{CC(A)}$	$V_{OL(A)} + 0.15 \text{ V}$	$V_{OH(A)} - 0.15 \text{ V}$
nAn port to nBn port	2.7 V to 3.6 V	4.5 V to 5.5 V	2.7 V	1.5 V	$0.5 \times V_{CC(B)}$	$0.2 \times V_{CC(B)}$	$0.8 \times V_{CC(B)}$
nBn port to nAn port	2.7 V to 3.6 V	4.5 V to 5.5 V	3.0 V	1.5 V	1.5 V	$V_{OL(A)} + 0.3 \text{ V}$	$V_{OH(A)} - 0.3 \text{ V}$



Test data is given in [Table 9](#).  
Definitions for test circuit:  
 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.  
 $C_L$  = Load capacitance including jig and probe capacitance.  
 $R_L$  = Load resistance.  
 $V_{EXT}$  = External voltage for measuring switching times.

Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Direction	Supply voltage		Load		$V_{EXT}$		
	$V_{CC(A)}$	$V_{CC(B)}$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
nAn port to nBn port	2.3 V to 2.7 V	2.7 V to 3.6 V	50 pF	500 $\Omega$	open	GND	$2 \times V_{CC}$
nBn port to nAn port	2.3 V to 2.7 V	2.7 V to 3.6 V	50 pF	500 $\Omega$	open	GND	6.0 V
nAn port to nBn port	2.7 V to 3.6 V	4.5 V to 5.5 V	50 pF	500 $\Omega$	open	GND	$2 \times V_{CC}$
nBn port to nAn port	2.7 V to 3.6 V	4.5 V to 5.5 V	50 pF	500 $\Omega$	open	GND	6.0 V

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm SOT362-1

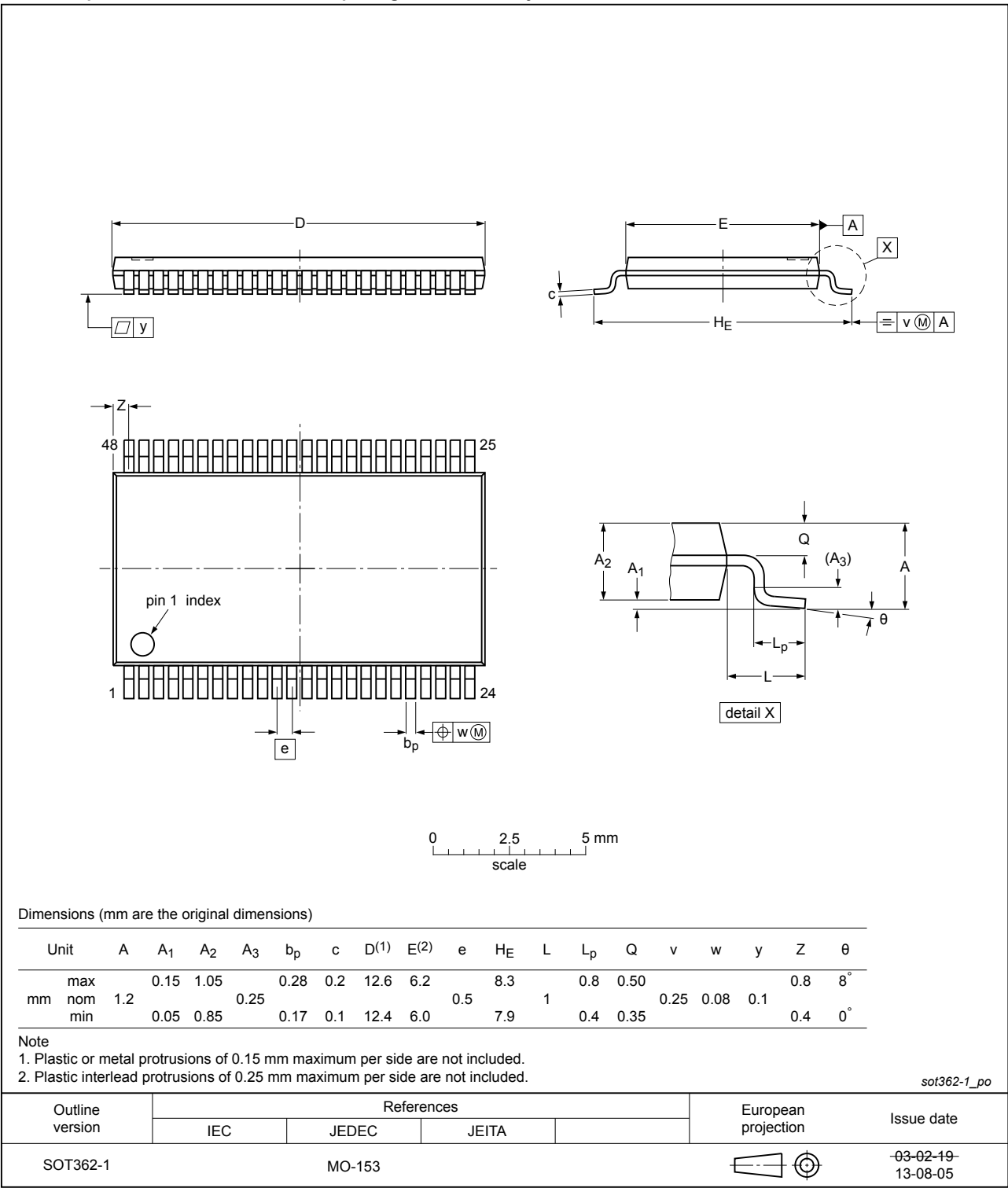


Fig. 7. Package outline SOT362-1 (TSSOP48)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC164245_Q100 v.3	20190409	Product data sheet	-	74ALVC164245_Q100 v.2
Modifications:	<ul style="list-style-type: none"><li><a href="#">Table 6</a>: Typo corrected for <math>V_{OL(max)}</math> at <math>V_{CC(B)} = 4.5\text{ V}</math>.</li></ul>			
74ALVC164245_Q100 v.2	20181112	Product data sheet	-	74ALVC164245_Q100 v.1
Modifications:	<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li><li>Legal texts have been adapted to the new company name where appropriate.</li><li>Package outline drawing <a href="#">SOT362-1</a> updated.</li></ul>			
74ALVC164245_Q100 v.1	20130514	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

### Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

**Right to make changes** — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use in automotive applications** — This Nexperia product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or

equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nexperia.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

### Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## Contents

1. General description.....	1
2. Features and benefits.....	1
3. Ordering information.....	2
4. Functional diagram.....	2
5. Pinning information.....	4
5.1. Pinning.....	4
5.2. Pin description.....	4
6. Functional description.....	5
7. Limiting values.....	5
8. Recommended operating conditions.....	6
9. Static characteristics.....	6
10. Dynamic characteristics.....	8
10.1. Waveforms and test circuit.....	9
11. Package outline.....	11
12. Abbreviations.....	12
13. Revision history.....	12
14. Legal information.....	13

© Nexperia B.V. 2019. All rights reserved

For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)

Date of release: 9 April 2019