VT505 Evaluation Kit Manual

Integrated Protection IC On 12V Bus With An Integrated Mosfet, Lossless Current Sensing And Pmbus Interface

General Description

This evaluation kit (EV kit) serves as a reference for evaluating Maxim's VT505 integrated protection IC on a 12V bus. The VT505 is a circuit breaker protection IC with an integrated low resistance MOSFET and lossless current sense circuitry featuring PMBus control and reporting. The VT505 monitors the current and the voltage of the 12V system power rail and provides multiple levels of protection. The IC is designed to provide the optimum solution for distribution, control, monitoring and protection of the system's 12V power supply. An internal LDO provides the supply voltage for the protection IC. The VT505 monitors the current and the voltage of the 12V system power rail and provides multiple levels of protection with fast turn off if a fault is detected.

Three methods of overcurrent protection are provided. Programmable "moderate" OCP level allows surge currents for a limited time. User selectable "severe" OCP level provides a fast disconnect if a current exceeding the "severe" OCP threshold is detected. An additional, fixed high shutdown OCP level provides instantaneous disconnect to further protect the device. User programmable "Startup OCP" is available to protect the device during soft-start.

Maxim's patented lossless current sense provides high accuracy current sensing over load and temperature, improving overall system energy efficiency, and reducing dissipation. A signal proportional to the load current is reported through an analog output and extensive reporting is provided using a PMBus.

Output voltage is monitored at all times. If at any time the output voltage falls below the programmable output undervoltage lockout threshold, the PWRGD signal is asserted low. If at any time the input voltage falls below the programmable input undervoltage lockout threshold, the PWRGD signal is asserted low. If the input voltage exceeds a programmable overvoltage threshold, the MOSFET is latched off and a fault indicated. During startup, the PWRGD signal is deasserted low. The VT505 has been designed to provide controlled, monotonic startup. Programmable soft-start is implemented to limit the inrush current during startup. The VT505 performs the following check procedures at every startup: pass FET short detection, the soft-start capacitor discharge ROCP resistor value check and pass FET, V_{GS}, and UVLO check. The VT505 also provides overtemperature protection and pass FET, V_{GS}, and UVLO during normal operation. If any fault (other than input or output UVLO) is detected, the VT505 latches the pass FET off and reports the fault by asserting the $\overline{FAULT}$ signal low. Restarting the system requires $12V_{IN}$ supply cycling, EN/UVLO toggling, or PMBus commands. The EV kit consists of an assembled and tested printed circuit board implementation of a 12V power distribution network with circuit-breaker protection using the VT505 protection IC. All the VT505 features can be verified using this EV kit. More thorough explanations of topics discussed in this manual can be found in the VT505 data sheet.

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- High Density (6.5mm x 4mm for 60A): Less than 25% of the Board Area of Conventional Solutions
  - Monolithic Integration of Power, Control and Monitoring
    - Integrated Power MOSFET with 0.9mW Total Resistance in 12V Power Path (RDSON), Including Package
    - Integrated Lossless, Precise Current Sensing
    - Integrated LDO Provides V_{DD} Supply (1.8V Bias Supply)
- Enables Advanced System Power Management
  - PMBus/SMBus Telemetry with Extensive Status Monitoring and Reporting
  - Load Current Indicator (ILOAD) Pin Provides Analog Output Current Reporting with High Accuracy
  - Programmable Soft-Start for Inrush Current Limiting
- Increases Power Supply Reliability with IC Self-Protection Features
  - Very Fast Fault Detection and Isolation
    - Detection and Isolation of Severe Overcurrent in Less Than 5µs
    - Fail-Safe Overcurrent (Safe-OCP) Detection and Isolation in Less Than 250ns
  - Three Levels of Programmable Overcurrent Protection
  - V_{IN} to V_{OUT} Short Protection During Startup

Systems and Applications

Servers, Networking, Storage, Communication Equipment and AC/DC Power Supplies

- 12V Power Distribution and Protection IC: Circuit Breaker/E-Fuse, Hot Swap

19-7254; Rev 3; 2/17

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System Configuration

Table 1. System Configuration

PARAMETER	COMPONENT/SETTING
Integrated Protection IC on 12V Bus	VT505
Input Capacitors	1x 180µF (OS-CON) 1x 10µF 1x 2.2µF
Output Capacitors	2 x 330µF (OS-CON) 1x 10µF 1x 2.2µF 1x 0.1µF
SMBus Address Programming Resistor (R23)	1.78kΩ
SMBus Address	40h
Input Transient Voltage Suppressor	1 x 14V, 400W
Output Schottky Diode	1 x 30V, 80A
R_{OCP} (R9 + R10/R11). Moderate OCP Threshold Programming Resistor	1 x 301kΩ 1 x 137kΩ 1 x 330kΩ
Moderate OCP Threshold	68A / 41A
R_{ILOAD} (R13). Current Reporting Resistor	1 x 4.42kΩ 0402, 0.1%
ILOAD Reporting Range	0 - 61A
Pullup resistors ($\overline{FAULT}$, PWRGD, SMBUS_DATA, SMBUS_CLK, $\overline{SMBUS\_ALERT}$)	5 x 10kΩ (0402)
EN/UVLO Voltage Divider (R15, R16)	1 x 20kΩ 1 x 2.26kΩ
Input UVLO Threshold	10.3V
Bootstrap Capacitor	1x 0.22µF
Soft-Start Capacitor C_{SS} (C2)	1x 47nF (0402, 25V)
Soft-Start Time	19ms
Severe OCP Threshold (PMBus)	130% of Moderate OCP
Moderate OCP Timeout (PMBus)	100µs
Input OVP Protection (PMBus)	14V (Disabled by default)
Startup Delay (PMBus)	0µs
Output PWRGD Threshold (PMBus)	11V
Self-Test Threshold (PMBus)	9V
Overtemperature Warning/ Fault Thresholds (PMBus)	Disabled / 135°C
Input Overpower Warning Threshold (PMBus)	Disabled
Reporting and Warning Averaging Size (PMBus)	1 Sample
Output Overcurrent Warning (PMBus)	Disabled
Input/Output Undervoltage Warning (PMBus)	Disabled
Current Hysteresis	Disabled
Startup OCP	16A

Note 1. *For Hot Swap operation C_{IN} should be removed and additional C_{OUT} might be required.*

Additional Components

- 1 x 180µF (OS-CON) + 1 x 10µF additional input capacitors to increase input voltage filtering (not loaded by default).
- 2A, 30V Schottky diode to protect VT505 from damage in case of high-inductive short on output (> 400nH).
- 100mA LDO to provide 3.3V pullup voltage for PMBus and LEDs.
- A transient voltage suppressor to protect VT505 from damage in case of high inductance input connection.

EV kit provides additional circuitry for measurements and testing:

- PMBus interface for telemetry and programming;
- fast output short to ground;
- “on-the-fly” moderate OCP threshold change
- soft-start capacitor C_{SS} discharge fail
- pass FET short protection
- wrong ROCP or SMBUS_ID resistor fault detection

Additional components like sense/test jumpers and connectors could be loaded on the board.

Getting Started

The following steps explain how to verify the board operation:

1) There are four board standoffs provided with the EV kit. These standoffs should be installed on holes located on each edge of the board.
2) Check that the J14 jumper is not loaded for initial board operation. This jumper is used to perform FET short protection tests. See chapter “Using the evaluation board”, section “VT505 protection against faults validation” for details.
3) Check that all the following switches are in the correct position:
   a) SW2: This switch is used to control EN/UVLO signal. EN/UVLO should be set low before startup (SW2 pointing away from the edge of the board).
   b) SW4: This switch enables circuitry for V_{OUT} to GND short testing. Set SW4 to off position at startup (switch pointing towards the USB connector). See chapter “Using the Evaluation Board” section “VT505 protection against fault validation” for details.
4) Monitoring
   a) Output voltage can be monitored at J10.
   b) Input voltage on the VT505 V_{IN} pins can be monitored by connecting a voltmeter across J12 or placing a differential oscilloscope probe in J12.
   c) Load current as reported by the VT505 can be monitored by connecting a voltmeter across J9 pins 13 and 14. See chapter “Using the Evaluation Board,” section “Analog Load Current Reporting” for details.
   d) The soft-start voltage (SS pin) across soft-start capacitor can be monitored using J13.
   e) The PWRGD reporting pin can be monitored on J9_4. LED D5 should illuminate when the PWRGD is asserted high.
   f) The $\overline{\text{FAULT}}$ reporting pin can be monitored on J9_6. LED D3 should illuminate when the $\overline{\text{FAULT}}$ is asserted low.
   g) EN/UVLO signal at the IC pin can be monitored on J9_2.
   h) Use J19 connector (pins 1 and 3) to accurately measure voltage across device (V_{OUT} - V_{IN}).
5) Connect a powered off 12V power source to terminal blocks J2 (+12V) and J3 (GND).
6) Turn on the 12V input power source. Make sure that the power source is not current limited. Note that 3.3V voltage is provided by LDO (loaded by default). This LDO is powered by a 12V input supply. Therefore, if accurate 12V input current measurement is desired, disable the LDO by removing R30 and R31. If LDO is disabled, a 3.3V should be supplied to J4.
7) Verify that there is no fault reported: $\overline{\text{FAULT}}$ is not asserted low; LED D3 is not illuminating.
8) Verify that PWRGD is asserted low. LED D5 is not illuminating.
9) Enable output voltage by toggling SW2. Output voltage should ramp up to 12V within programmed soft-start time. $\overline{\text{FAULT}}$ should stay deasserted (LED D3 should not illuminate) and PWRGD signal should be asserted high (LED D5 should illuminate)

Using the Evaluation Board

Detailed product and applications information for the VT505 integrated protection IC can be found in the VT505 preliminary data sheet. The evaluation board’s top and bottom silkscreen layers and assembly drawing for the board are illustrated in Figure 1 and Figure 2, respectively. The evaluation board schematics is shown in Figure 3 and Figure 4.

PMBus Communication

VT505 supports a wide range of PMBus features as described in the data sheet. The EV kit supports PMBus communication through a USB interface and custom software, which is available upon request. Simply connect USB cable to J16 to enable communication with VT505. J18 can be used to bypass the USB and control the PMBus data and clock lines directly. Note that R58 and R59 should be removed in this case.

Programmable Soft-Start

The VT505 implements soft-start with externally programmable soft-start time (through soft-start capacitor C2). Default soft-start time is described in Table 1. A different soft-start time t_{SS} can be obtained by changing the value of C2.

Use Equation 1 to calculate the soft-start capacitance value for obtaining desired t_{SS} time.

Equation 1

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{12}$$

where:

t_{SS} = Ramp duration (ms)

I_{SS} = Soft-start current (µA)

C_{SS} = C2 value (nF)

Soft-Start Time Limitation

- t_{SS} Upper Limit: t_{SS} should be < 30ms to guarantee the device stays within SOA at all times.
- t_{SS} Lower Limit: During startup, output bypass capacitance is charged up by a constant current I = C_{OUT} x V_{IN}/ t_{SS}, the inrush current during the start-up should be small enough (i.e., t_{SS} should be long enough) to insure proper startup without OCP fault trip and meeting SOA limitations. More detailed information can be found in the VT505 data sheet.

Configuration

The VT505 is configured using both analog programming resistors and PMBus. See Table 1 for default EV kit configuration.

Overcurrent Protection Thresholds

Moderate overcurrent protection (OCP) threshold is on-the-fly analog programmable by selecting the value of the ROCP resistor connected to the ROCP pin. This EV kit provides options to program the moderate OCP threshold on-the-fly by toggling SW1 to choose between “high” or “low” settings (SW1 pointed towards “L” label selects “low” setting and if pointed towards “H” label selects “high”). Severe OCP threshold is programmed using PMBus Reg_D0h bit [7], default value is 130% of moderate OCP (Reg_D0h[7] = 0).

Analog Load Current Reporting

The VT505 provides a dedicated pin (ILOAD) to report analog current representation of a load current. Current representation of a load current should be measured across resistor R13. The voltage across R13 can be measured by connecting a voltmeter across J9 (pins 13 and 14). VREP (V), as reported by the voltmeter, represents the reported output current that can be calculated using Equation 2.

Equation 2

$$I_{OUT} = 1000 \times \frac{V_{REP}}{G_{ILOAD} \times R_{ILOAD}}$$

where:

VREP = Voltage reported on the ILOAD pin (V)

GILOAD = Current reporting gain (= 5µA/A)

RILOAD = Value of RILOAD resistor (kΩ)

IOUT = Output current value (A)

Output Enable

The output voltage can be enabled or disabled by using the EN/UVLO switch (SW2). At restart, the VT505 performs a pass FET short test, C_{SS} discharge and resistors check tests.

Fault Reporting

The board provides options to monitor $\overline{FAULT}$ and PWRGD fault-reporting signals. PWRGD and $\overline{FAULT}$ can be monitored on J9 (pins 4 and 6, respectively). In addition, two LEDs (D5 and D3) are loaded by default to indicate fault status. D5 illuminates if PWRGD is asserted high. D3 illuminates if $\overline{FAULT}$ is asserted low. Refer to the VT505 data sheet for the tables to interpret fault and status conditions reported by $\overline{FAULT}$ and PWRGD pins.

Fault Testing and Validation Protection

This evaluation board enables verification of the VT505 protection against fault conditions that could cause system failure. Required board modification for specific tests and test guidelines are provided in subsequent chapters.

Moderate Overcurrent Protection

Test procedure to verify the moderate overcurrent protection (OCP) feature is provided below:

1) Power up the board: follow the instructions provided in the *Getting Started* section. Make sure that a load is connected to the output.
2) Select Moderate_OCP threshold = “high”
3) Apply a load current to achieve Moderate_OCP threshold < IOUT < Severe_OCP threshold (Severe_OCP threshold is set to 130% of Moderate_OCP threshold by default). Keep the load for longer than Moderate OCP timeout. After the timer expiration, the VT505 should turn off the pass FET and assert the $\overline{FAULT}$ signal low. This is a latching fault that can be removed by cycling the $12V_{IN}$ supply, PMBus commands or EN/UVLO toggling. PWRGD is expected to be asserted low after a fault condition.

To monitor system behavior and the VT505 protection response, it is suggested to sense:

- Output Voltage
- Load current
- FAULT
- PWRGD
- Voltage across soft-start capacitor C2

Moderate Overcurrent Protection - "On-the-Fly" Threshold Validation

Test procedure to verify the moderate OCP feature is provided below:

1) Power up the board: follow the instructions provided in the *Getting Started* session. Make sure that a load is connected to the output.
2) Select Moderate_OCP threshold = "high" (SW1 pointing towards J3).
3) Apply a load current: square waveform: 0 - (0.8 × Moderate_OCP), 1Hz, 50% duty cycle. Verify that the VT505 stays in normal operation (no overcurrent fault is detected).
4) Toggle SW1 to select Moderate_OCP threshold "low." The VT505 should turn off the pass FET and assert the $\overline{FAULT}$ signal low. This is a latching fault that can be removed by cycling the $12V_{IN}$ supply, toggling EN/UVLO or through PMBus commands. PWRGD is expected to be deasserted low and $\overline{FAULT}$ asserted low.

Severe OCP Protection

Test procedure to verify the circuit-breaker protection feature is provided below:

1) Power up the board: follow the instructions provided in the *Getting Started* section. Make sure that a load is connected to the output.
2) Apply a load current to achieve output current I_{OUT} > Severe_OCP threshold (Severe_OCP threshold is set to 130% of Moderate_OCP threshold by default). The VT505 should turn off the pass FET and assert the $\overline{FAULT}$ signal low. This is a latching fault that can be removed by cycling the $12V_{IN}$ supply, toggling EN/UVLO or through PMBus commands. PWRGD is expected to be asserted low and $\overline{FAULT}$ asserted low.

V_{OUT} to GND Short Fault Protection

The board provides options to test V_{OUT} to GND short fault protection. The VT505 should turn off the pass FET and assert $\overline{FAULT}$ signal low. This is a latching fault that can be removed by cycling the $12V_{IN}$ supply, cycling EN/UVLO or through PMBus commands.

1) Option 1: Testing V_{OUT} to GND short during normal operation:
   a) Power up the board: follow the instructions provided in the *Getting Started* section.
   b) Toggle SW4 to EN (switch pointing towards J1).

This test could be performed in any operating condition (i.e., any load condition including no load and full load).

2) Option 2: Testing the system starting into shorted output:
   a) Get ready to power up the board: follow the instructions provided in the *Getting Started* section but do not enable the VT505 (i.e., keep EN/UVLO signal deasserted (do not toggle SW2)).
   b) Before testing the system starting into shorted output, it is required to toggle SW4 into the off position (switch pointing towards the USB connector).
   c) Short output connectors by shorting top and bottom sides of output edge connector (J1).
   d) Complete turning on the VT505 by toggling EN/UVLO switch to EN.

Overtemperature Fault Protection

Test procedure to verify overtemperature protection (OTP) is provided below:

1) Power up the board: follow the instructions provided in the *Getting Started* section.
2) Increase the device temperature beyond the OTP threshold (135°C).

Note: Maxim recommends placement of a thermocouple on the IC to monitor IC temperature. The thermocouple should be placed on the bottom-side of the IC and above the FET section as it allows more precise temperature monitoring.

A heat gun, in addition to soldering heater, placed under the evaluation board could be used. To improve temperature reporting it's recommended not to aim the heat gun directly at the IC: the thermocouple reports temperature higher than the actual IC temperature.

VT505 Faults Protection

C_{SS} Discharge Fail Fault

The VT505 performs a C_{SS} discharge test at restart to insure correct and repeatable soft-start.

1) Power up the board: Follow the instructions provided in the *Getting Started* section.
2) Connect 1V power supply to J13_2 header.
3) Disable the VT505 by deasserting EN/UVLO signal low (toggle the SW2), forcing the system to shut-down, and then re-enable the VT505 by asserting EN/UVLO signal high (toggle the SW2).

As a response to a C_{SS} discharge fail fault, the VT505 does not turn the pass FET on and does report the fault by asserting the $\overline{FAULT}$ signal low. This is a latching fault state. The PWRGD signal remains asserted low.

To restart the part, deassert the EN/UVLO low (toggle the SW2), open J13, cycle the 12V power supply and assert EN/UVLO high (toggle SW2).

V_{IN} to V_{OUT} Short Detection and Protection

The VT505 performs V_{IN} to V_{OUT} short test at restart to avoid startup in severe failure condition. If the VT505 detects the V_{IN} to V_{OUT} short during startup, it reports it by asserting both $\overline{FAULT}$ and PWRGD signals low. This is a latching fault.

1) Power up the board: Follow the instructions provided in the *Getting Started* section.
2) Short the VT505 input and output pins by shorting J14 (placing jumper).
3) Toggle EN/UVLO to low and then again to high, forcing the VT505 to shut down and restart with V_{IN} to V_{OUT} short fault condition present.

The VT505 does not start and assert $\overline{FAULT}$ pin low, PWRGD signal stays deasserted low.

Wrong ROCP Fault

Programming resistor for moderate OCP (ROCP) threshold is monitored at all times, including startup. If ROCP value is detected to be outside the range specified in the VT505 data sheet, the VT505 turns off the pass FET and reports a fault by asserting the $\overline{FAULT}$ signal low. This is a latching fault that can be removed by cycling the $12V_{IN}$ supply, toggling EN/ UVLO or through PMBus command. Board modification is required to perform this test:

Option 1: Wrong ROCP fault response testing during normal operation:

1) Mount R10 = 0W.
2) Select OCP_M threshold = “low” (SW1 pointing towards to L).
3) Power up the board: Follow the instructions provided in the *Getting Started* section.
4) Select OCP_M threshold = “high”: the IC latches the FET off and reports $\overline{FAULT}$ low.

Option 2: Wrong ROCP fault response testing during startup:

1) Mount R10 = 0W.
2) Select OCP_M threshold = “high.”
3) Power up the board: follow the instructions provided in the *Getting Started* section.
4) The IC does not start and reports $\overline{FAULT}$ low.

MOSFET V_{GS} UVLO Fault

The VT505 performs pass FET, V_{GS}, and UVLO test at restart to avoid startup in fault condition. If the pass FET V_{GS} does not exceed its UVLO thresholds within 110ms (max) after startup is initiated, the VT505 does not turn the pass FET ON and reports a fault by asserting the $\overline{FAULT}$ signal low (latching fault). The following board modifications are required to perform this test:

1) Preparing the board for power-up: Follow the instructions provided in the *Getting Started* section, but do not enable the VT505, (i.e., keep EN/UVLO signal deasserted; do not toggle SW2).
2) Short VT505 SS pin to GND (use J13).
3) Complete the VT505 turn-on by toggling EN/UVLO switch SW2.
4) VT505 should report $\overline{FAULT}$ 110ms (max) after enabling ($\overline{FAULT}$ asserted low). PWRGD remains deasserted low.

Special Notes

1) If a fast load transient resulting in fast and large transient output voltage deviation is possible in the application, an additional capacitor (100nF) between the SS pin and $12V_{OUT}$ is recommended to keep pass FET and V_{GS} above its UVLO threshold during the transients (C47 not stuffed by default).
2) Circuitry provided on board is designed to be used for testing protection against V_{OUT} short to GND during normal operation only. This circuitry is not to be used for V_{OUT} to GND short test during startup. Use edge connector J1 to perform start into short circuit tests (it can be also used for V_{OUT} short to GND during normal operation).

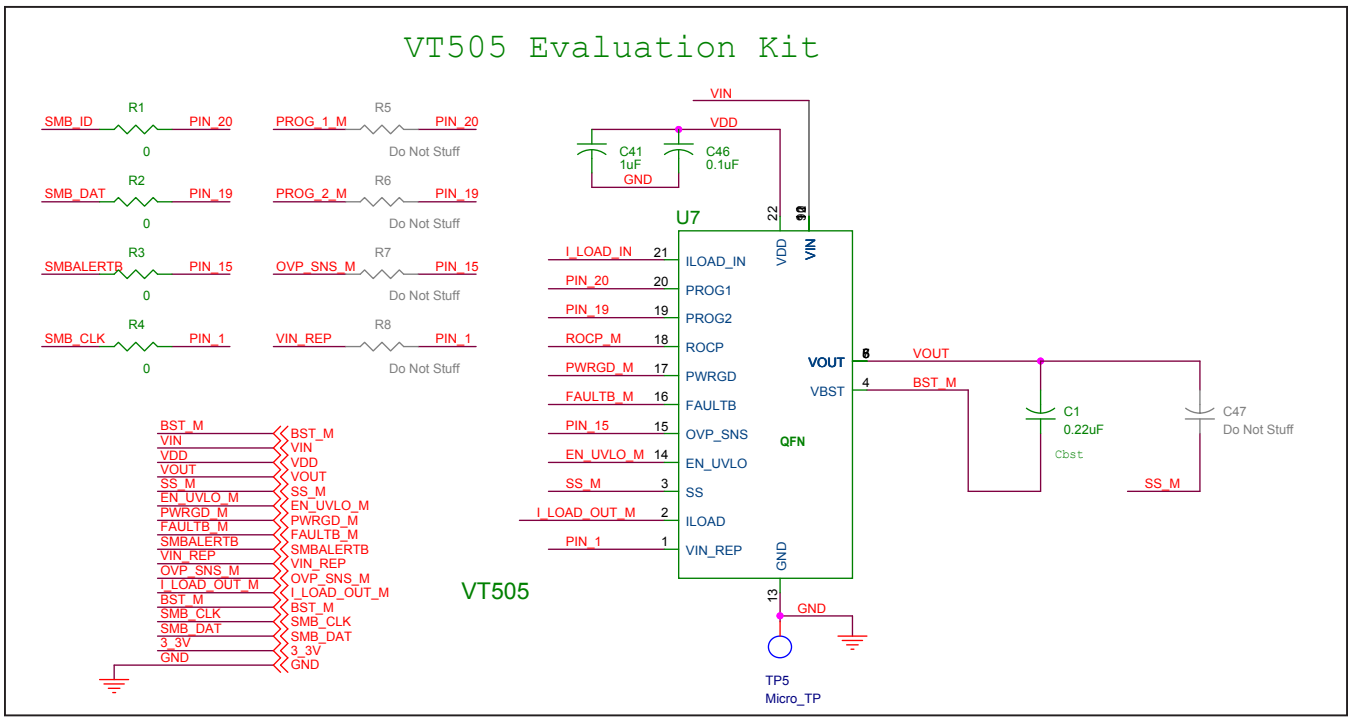
VT505 EV Kit Bill of Materials

REFERENCE	QTY	DESCRIPTION
C3, C19, C44	3	16V, X7R, 10%, 0.1µF
C1	1	25V, X6S, 25V, 0.22µF
C2	1	25V, X7R, 10%, 47nF
C4, C5	2	16V, OS-CON, 20%, 330µF
C21	1	20V, TANTALUM, 20%, 180µF
C16, C22	2	16V, X5R, 10%, 10µF
C18, C24	2	25V, X7R, 10%, 2.2µF
C25	1	25V, X7R, 10%, 22µF
C26, C27, C41	3	16V, Y5V, +80/20%, 1µF
C28, C29, C33	3	16V, X7R, 10%, 0.1µF
C34	1	25V, X5R, 10%, 1.0µF
C36	1	10V, X5R, 10%, .22µF
C37	1	25V, X7R, 10%, 0.47µF
C38	1	16V, Y5V, +80/20%, 1µF
C39, C40	2	50V, NPO, 5%, 22pF
C45	1	50V, X7R, 10%, 1000pF
C46	1	10V, X5R, 10%, 0.1µF
D1	1	20BQ030
D2	1	SMBJ14A
D3	1	HSMH-C650
D4	1	CMD15-21VYC
D5, D7, D8	3	HSMG-C650
D6	1	BZT52C5V6
J1, J5, MTG1, MTG2, TP1, TP2, TP3, TP4, TP5	9	Edge Fingers
J2	1	Banana Jack Kit, Red
J3	1	Banana Jack Kit, Black
J4	1	2 Pin, Terminal Block w/ Screws, Blue
J9	1	2 x 7 Straight
J10, J11, J12, J13, J15, J20, J22	7	1 x 2 Straight
J14	1	2 x 2 Straight
J16	1	4 Pin, USB B type, Receptacle, Right Angle, Horizontal
J17	1	1 x 5 Straight
J18	1	1 x 4 Straight
J19	1	1 x 3 Straight
Q1	1	BSS138
Q4, Q5, Q6	3	FDS6699S
R1, R2, R3, R4, R45, R46, R57, R58, R59	9	1/16W, 5%, 0
R9	1	1/10W, 1%, 301K
R10	1	1/10W, 1%, 137K
R11	1	1/10W, 1%, 330K
R13	1	1/16W, 0.1%, 4.42K
R14	1	1/16W, .5%, 1020
R15	1	1/16W, 1%, 20.0K
R16	1	1/16W, 1%, 2.26K
R12, R19, R20, R24, R25, R26, R43, R44, R65	9	1/16W, 1%, 10K
R23	1	1/16W, 1%, 1.78K
R30, R31	2	1/8W, 5%, 0
R32, R33	2	1/16W, 1%, 280
R34	1	1/16W, 5%, 10K
R35, R36	2	1/16W, 1%, 100
R47, R48, R49, R50	4	1/16W, 5%, 0
R51	1	1/10W, 1%, 1K
R54	1	1/10W, 5%, 470
R55, R56	2	1/16W, 1%, 750
SW1, SW2, SW4	3	DPDT, 6pins, 1switch
U2	1	LM3480IM3-3.3
U5	1	MIC4420BM
U6	1	PIC18F2455
U7	1	VT505
X1	1	20.0Mhz crystal 4.3mm height
		PCB# 35-900257-02-00-11

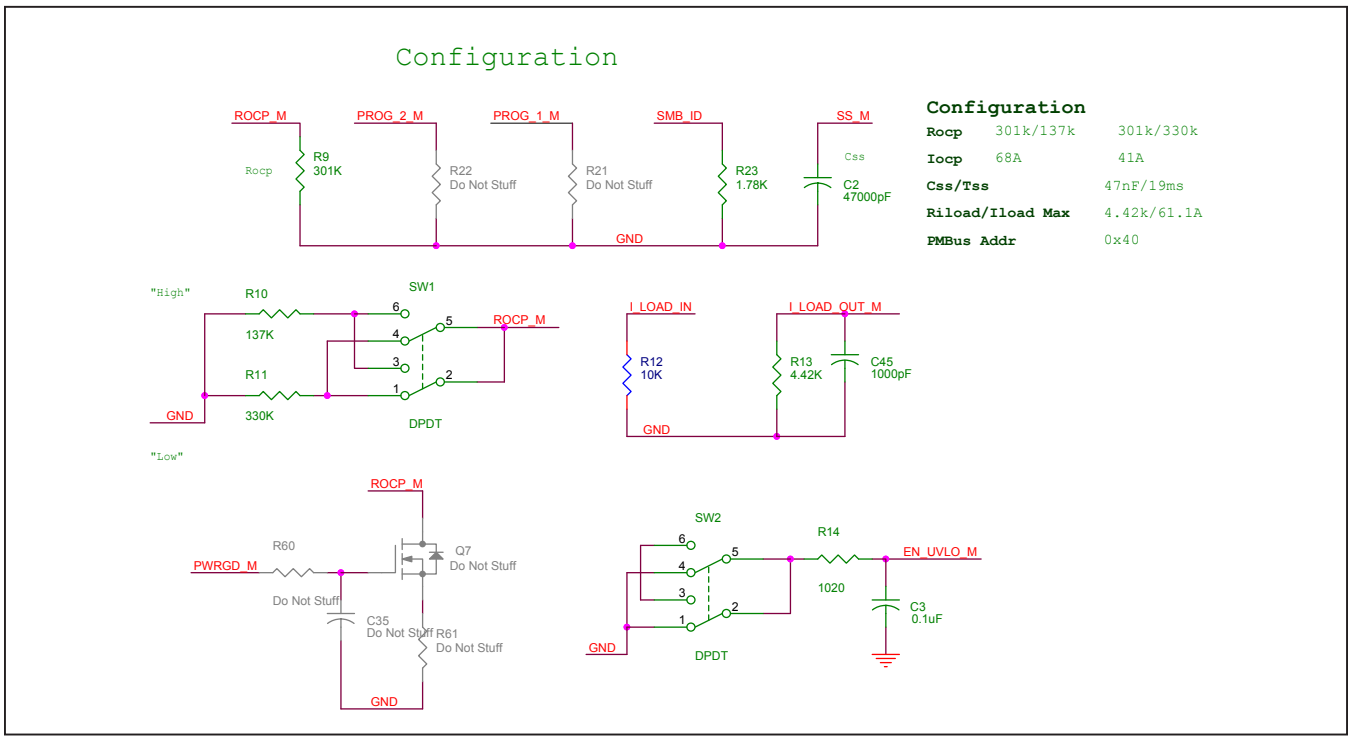
Ordering Information

PART	TYPE
VT505EVKIT#	VT505 Evaluation Kit

VT505 EV System Schematic

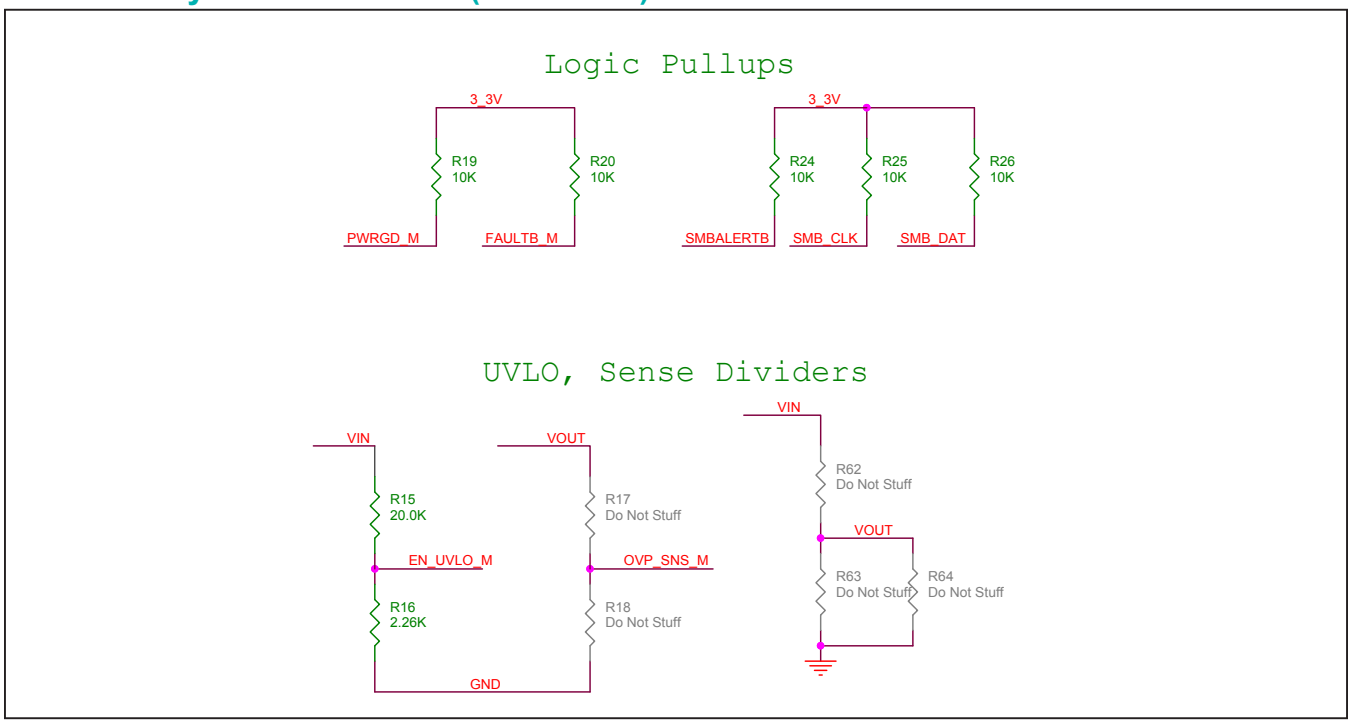


VT505 EV Kit Schematic (1 of 10)

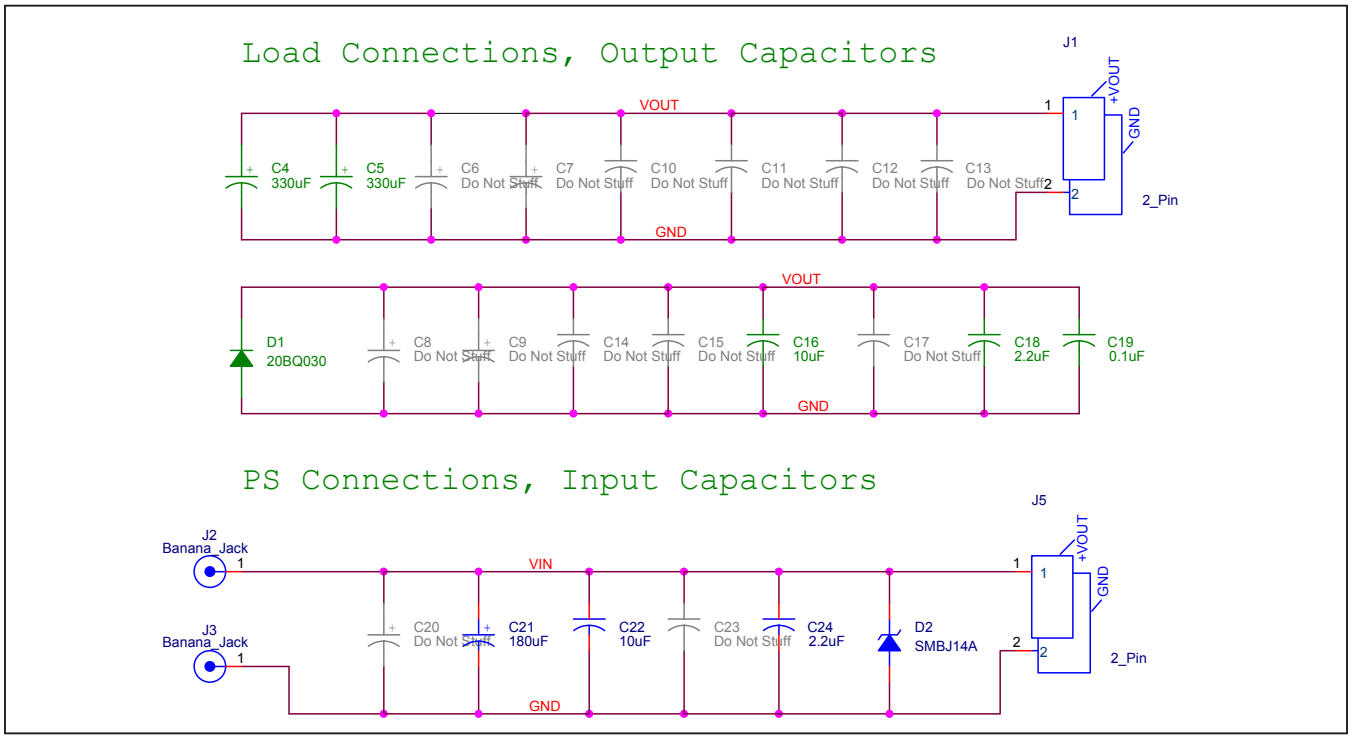


VT505 EV Kit Schematic (2 of 10)

VT505 EV System Schematic (continued)

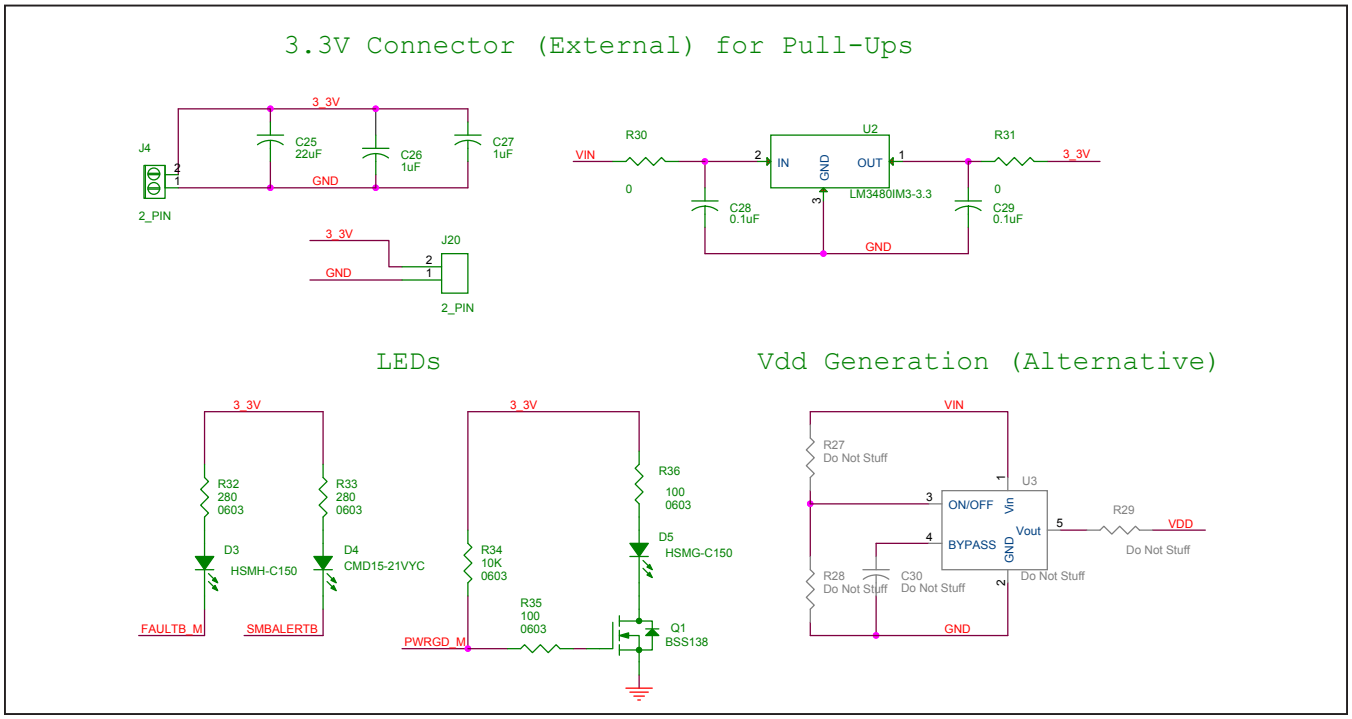


VT505 EV Kit Schematic (3 of 10)

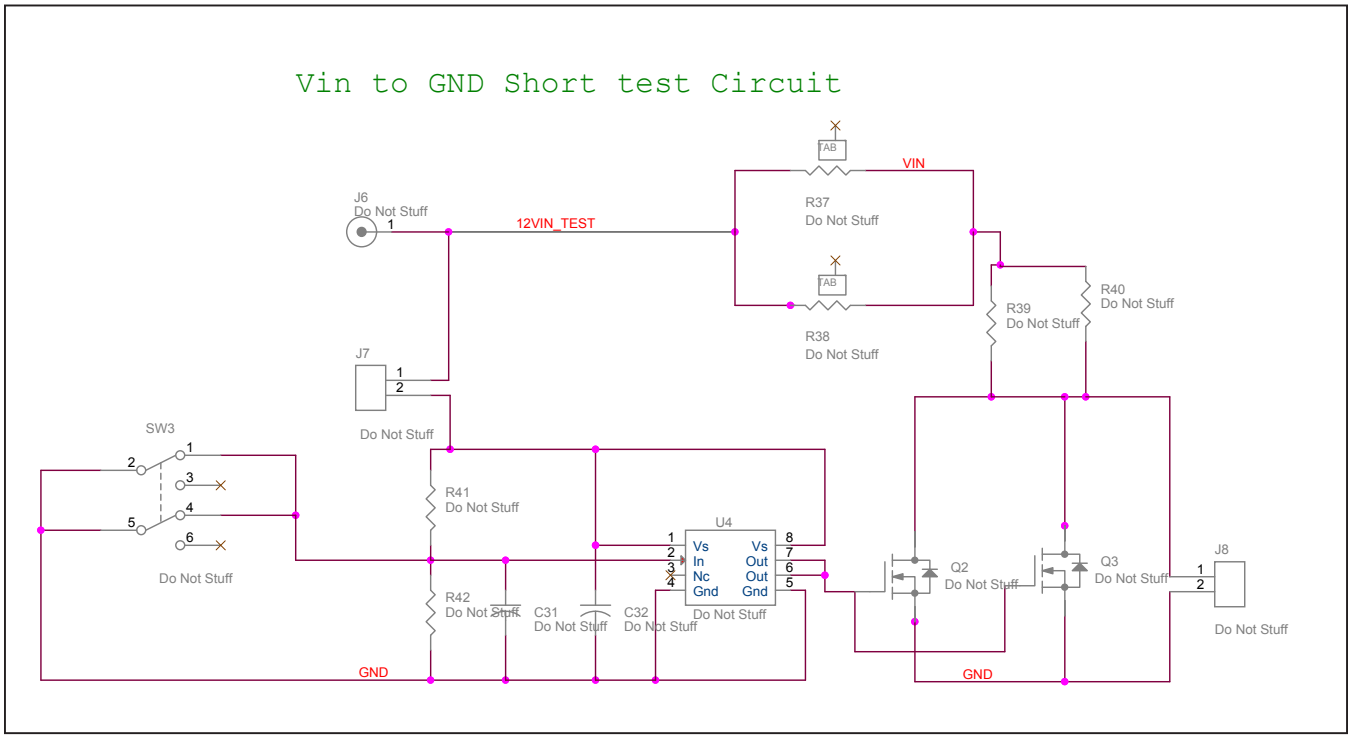


VT505 EV Kit Schematic (4 of 10)

VT505 EV System Schematic (continued)

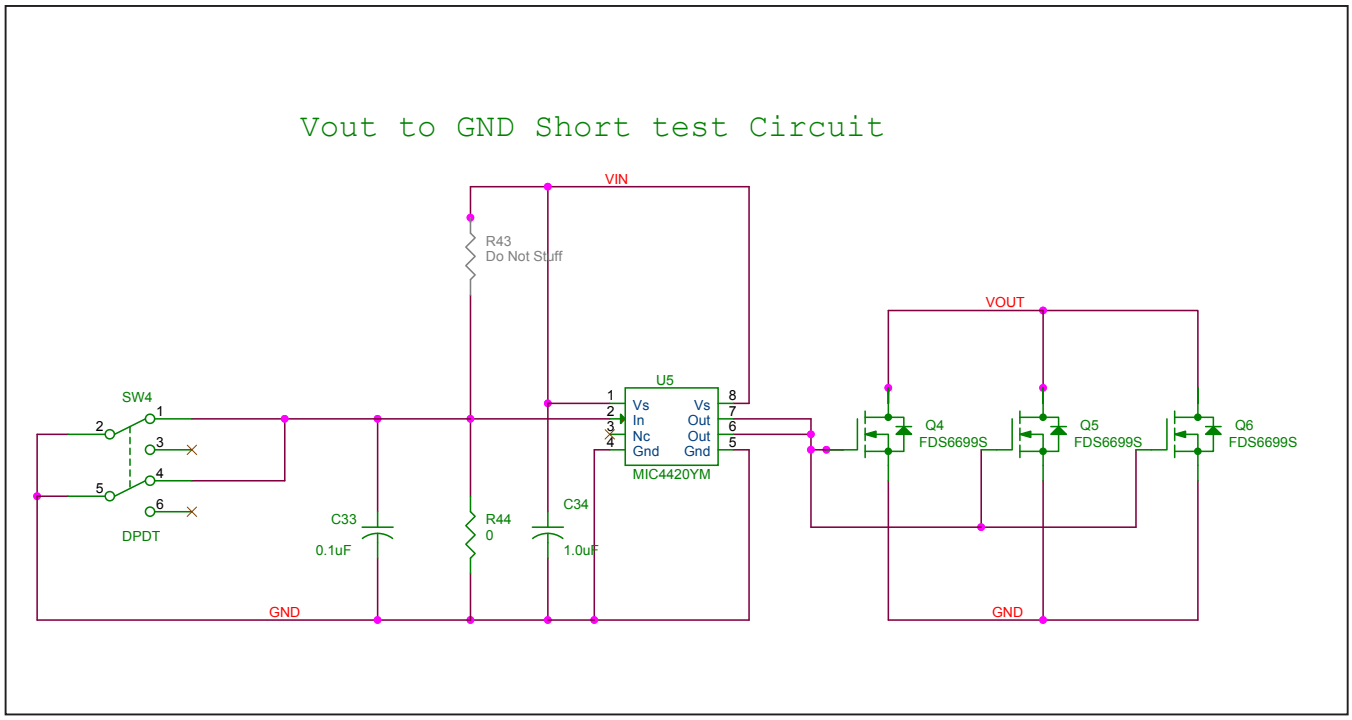


VT505 EV Kit Schematic (5 of 10)

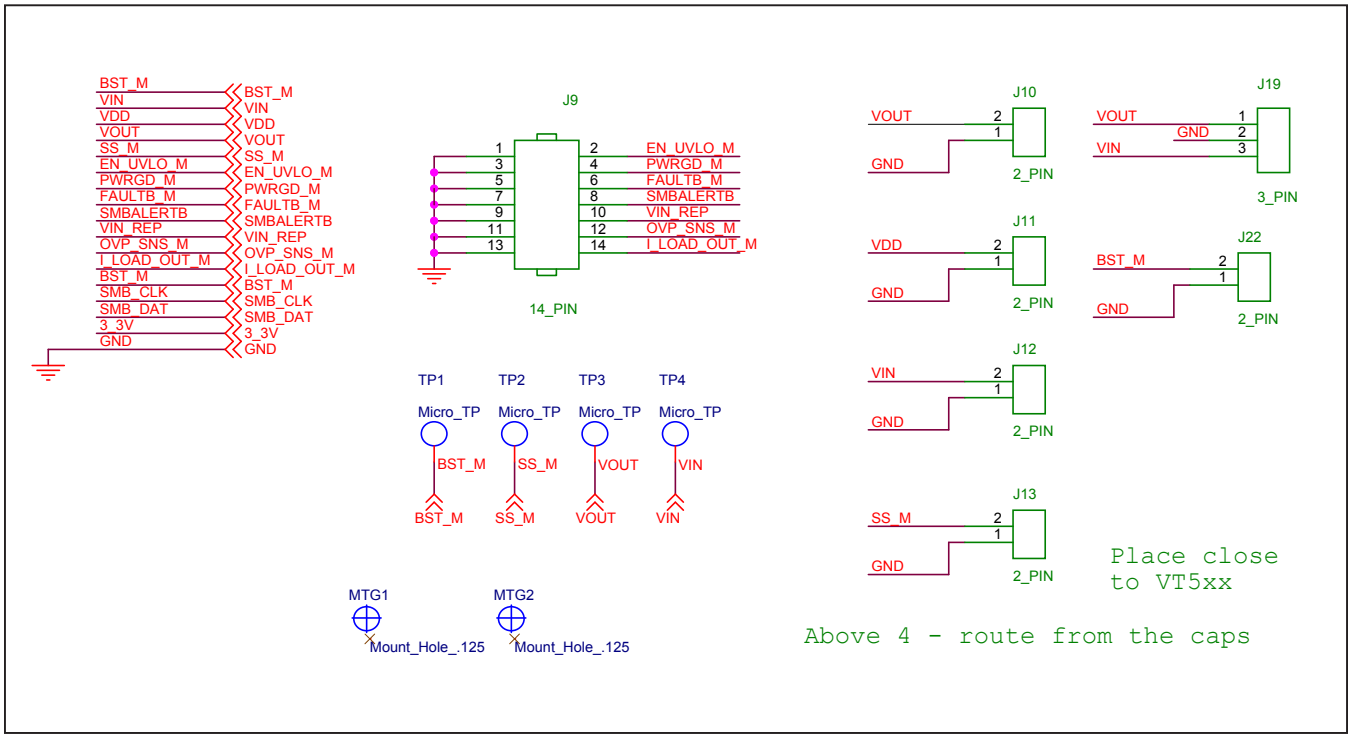


VT505 EV Kit Schematic (6 of 10)

VT505 EV System Schematic (continued)

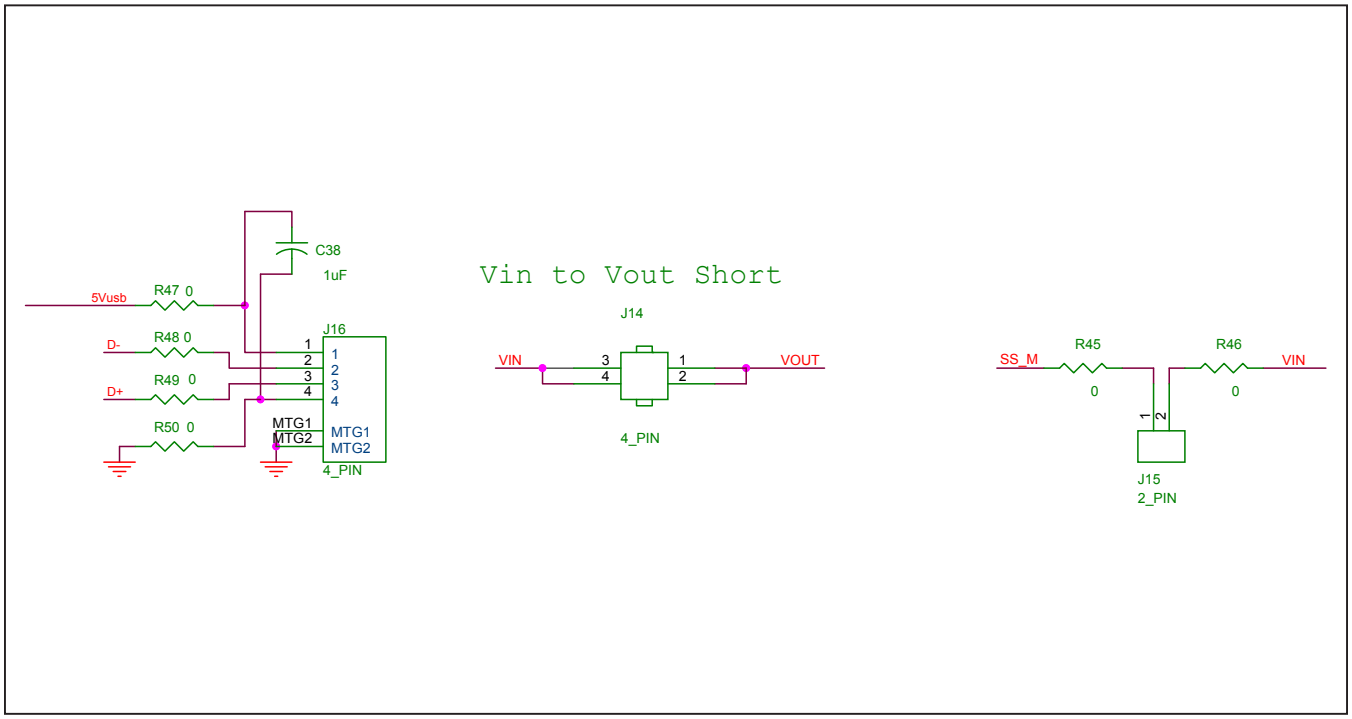


VT505 EV Kit Schematic (7 of 10)

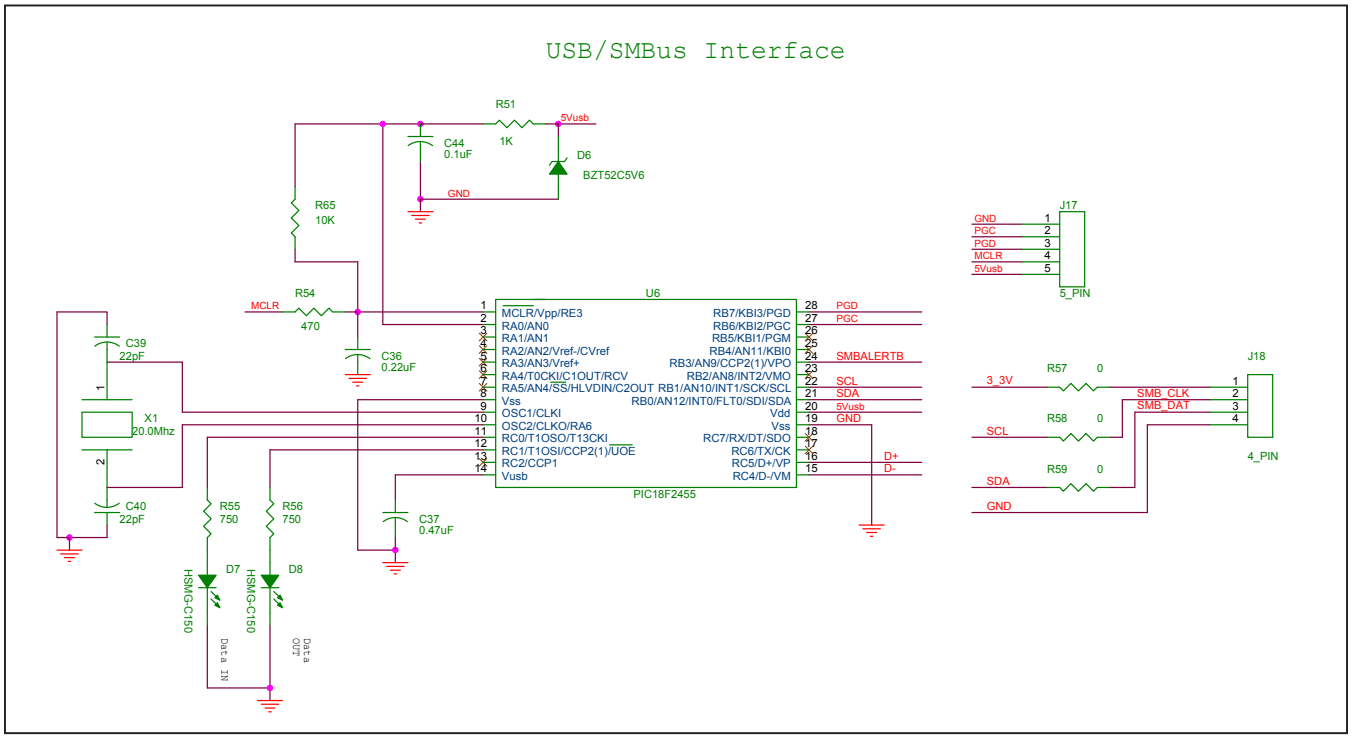


VT505 EV Kit Schematic (8 of 10)

VT505 EV System Schematic (continued)

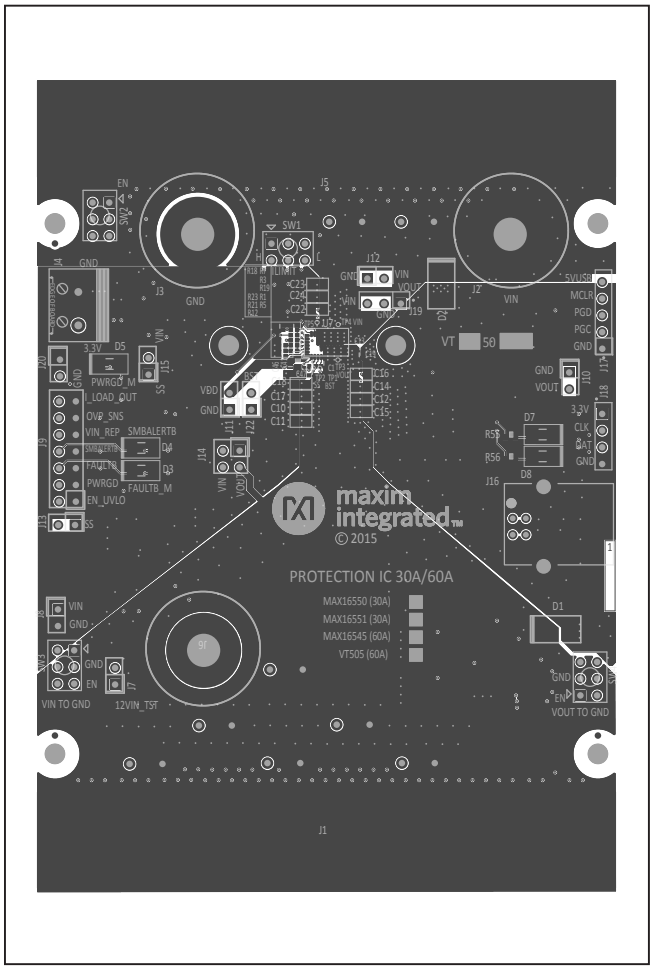


VT505 EV Kit Schematic (9 of 10)

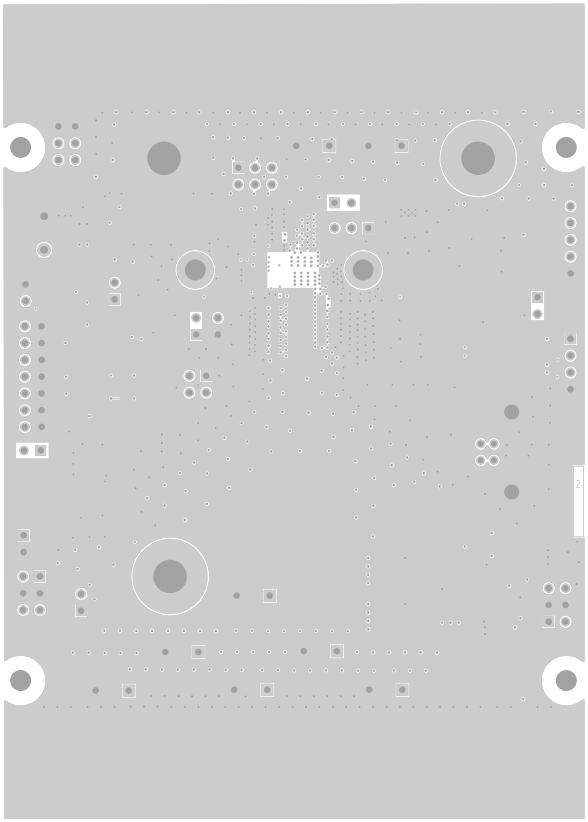


VT505 EV Kit Schematic (10 of 10)

VT505 EV PCB Layouts

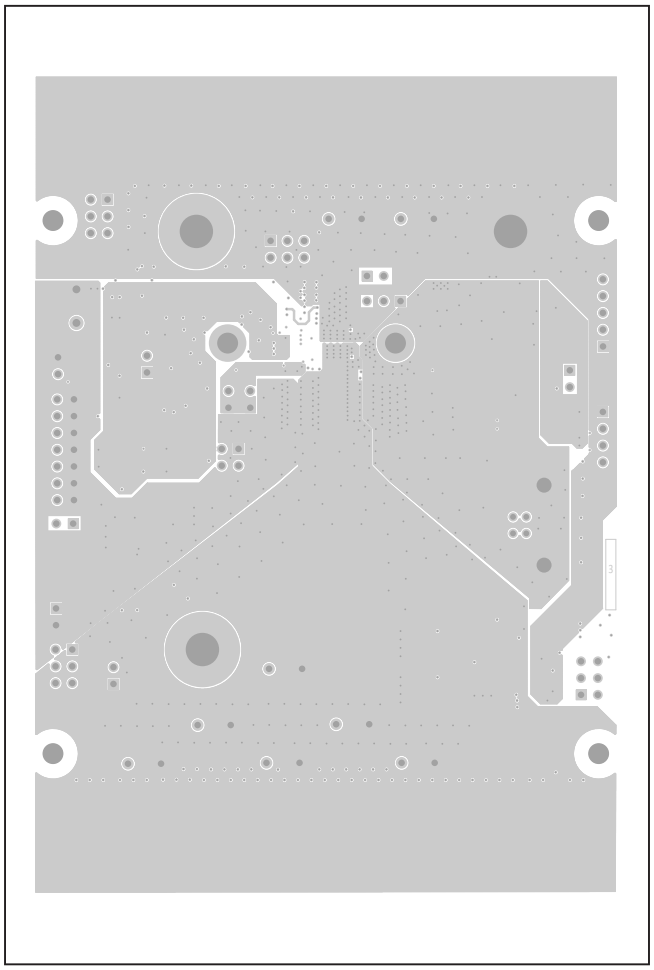


Top Silkscreen Layer

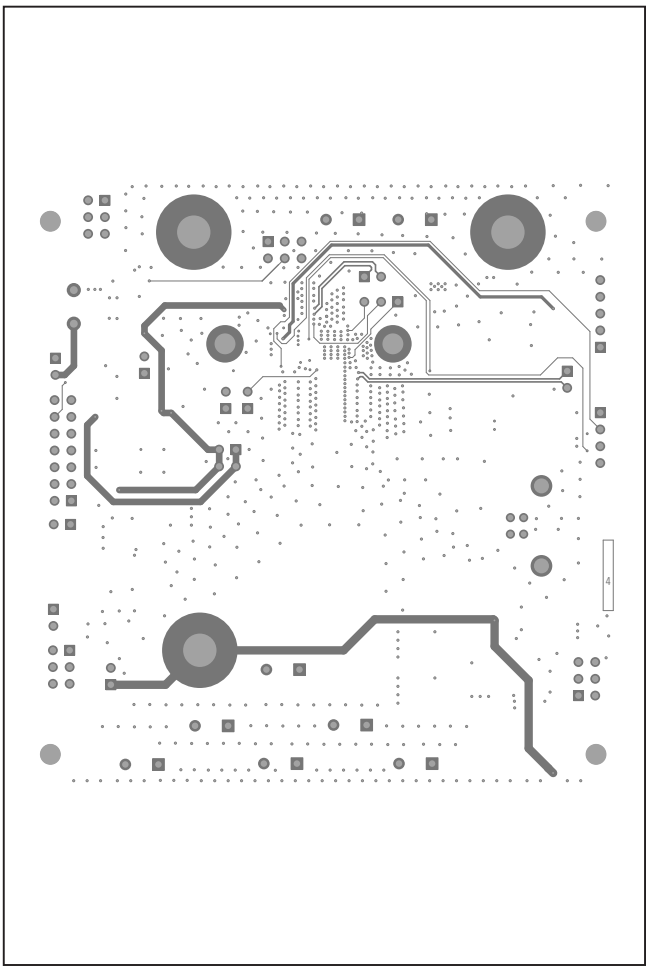


Layer 2

VT505 EV PCB Layouts (continued)

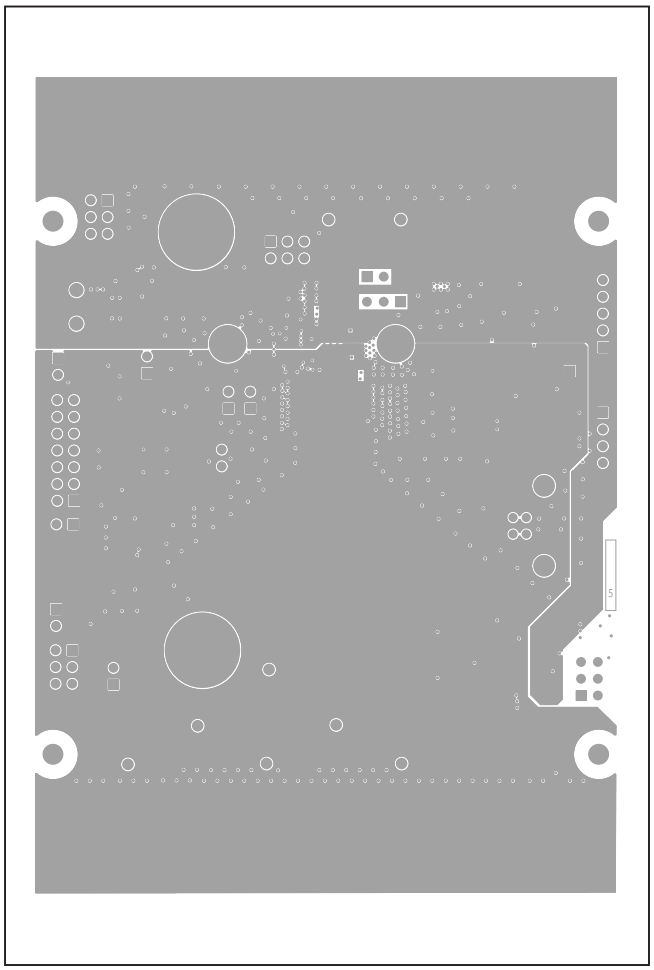


Layer 3

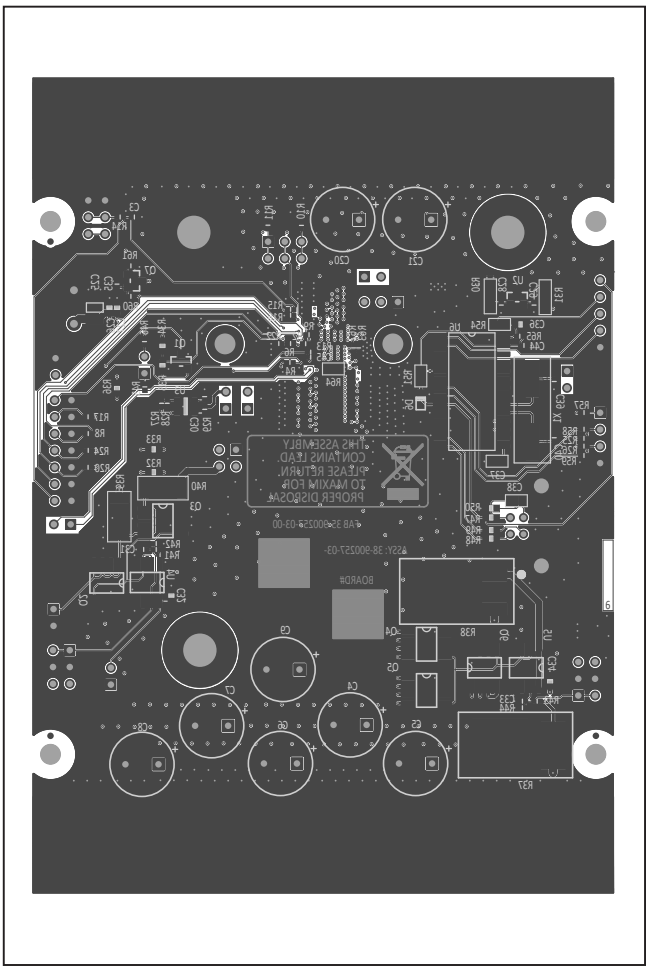


Layer 4

VT505 EV PCB Layouts (continued)



Layer 5



Bottom Silkscreen Layer

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/14	Initial Release	—
1	5/14	Updated to match latest IC	1–13
2	10/14	Updated to match current BOM	8
3	2/17	Updated the *General Description, Additional Components, Bill of Materials, Schematics, PCB Layout,* and *Ordering Information* sections.	1–2, 7, 8-15

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