

FEATURES

- ±2 V to ±6 V dual supply
- 2 V to 12 V single supply
- Automotive temperature range –40°C to +125°C
- <0.1 nA leakage currents
- 45 Ω on resistance over full signal range
- Rail-to-rail switching operation
- Single 8-to-1 multiplexer **ADG658**
- Differential 4-to-1 multiplexer **ADG659**
- 16-lead LFCSP/TSSOP/QSOP packages
- Typical power consumption <0.1 μW
- TTL/CMOS compatible inputs
- Package upgrades to 74HC4051/74HC4052 and
MAX4051/MAX4052/MAX4581/MAX4582

APPLICATIONS

- Automotive applications
- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Communication systems
- Audio and video signal routing
- Relay replacement
- Sample-and-hold systems
- Industrial control systems

GENERAL DESCRIPTION

The **ADG658** and **ADG659** are low voltage, CMOS analog multiplexers comprised of eight single channels and four differential channels, respectively. The **ADG658** switches one of eight inputs (S1–S8) to a common output, D, as determined by the 3-bit binary address lines A0, A1, and A2. The **ADG659** switches one of four differential inputs to a common differential output, as determined by the 2-bit binary address lines A0 and A1. An $\overline{\text{EN}}$ input on both devices enables or disables the device. When disabled, all channels are switched off.

These devices are designed on an enhanced process that provides lower power dissipation yet gives high switching speeds. These devices can operate equally well as either multiplexers or demultiplexers and have an input range that extends to the supplies. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels. All digital inputs have 0.8 V to 2.4 V logic thresholds, ensuring TTL/CMOS logic compatibility when using single +5 V or dual ±5 V supplies.

FUNCTIONAL BLOCK DIAGRAM

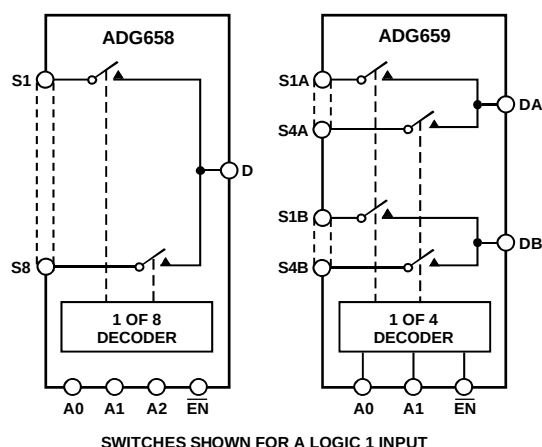


Figure 1.

The **ADG658** and **ADG659** are available in 16-lead TSSOP/QSOP packages and 16-lead 4 mm × 4 mm LFCSP packages.

PRODUCT HIGHLIGHTS

1. Single- and dual-supply operation. The **ADG658** and **ADG659** offer high performance and are fully specified and guaranteed with ±5 V, +5 V, and +3 V supply rails.
2. Automotive temperature range –40°C to +125°C.
3. Low power consumption, typically <0.1 μW.
4. 16-lead 4 mm × 4 mm LFCSP packages, 16-lead TSSOP package and 16-lead QSOP package.

Rev. D

Document Feedback

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 ©2004–2016 Analog Devices, Inc. All rights reserved.
Technical Support www.analog.com

TABLE OF CONTENTS

Features	1	Absolute Maximum Ratings	9
Applications	1	ESD Caution	9
Functional Block Diagram	1	Pin Configurations and Function Descriptions	11
General Description	1	Typical Performance Characteristics	12
Product Highlights	1	Terminology	15
Revision History	2	Test Circuits	16
Specifications	3	Outline Dimensions	19
Dual Supply	3	Ordering Guide	20
5 V Single Supply	5	Automotive Products	20
2.7 V to 3.6 V Single Supply	7		

REVISION HISTORY

11/2016—Rev. C to Rev. D

Changes to Figure 3 and Table 7	11
Updated Outline Dimensions	19
Changes to Ordering Guide	20

9/2014—Rev. B to Rev. C

Moved Terminology Section	15
Updated Outline Dimensions	19
Changes to Ordering Guide	20

2/2009—Rev. A to Rev. B

Changes to Ordering Guide	20
---------------------------------	----

7/2004—Rev. 0 to Rev. A

Updated Format	Universal
Added QSOP Package Outline	20
Changes to Ordering Guide	20
3/03—Rev. 0: Initial Version	

SPECIFICATIONS

DUAL SUPPLY

$V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	+25°C	B Version –40°C to +85°C	Y Version –40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	$V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$
On Resistance (R_{ON})	45 75	90	100	Ω typ Ω max	$V_S = \pm 4.5\text{ V}$, $I_S = 1\text{ mA}$; see Figure 21
On Resistance Match between Channels (ΔR_{ON})	1.3 3	3.2	3.5	Ω typ Ω max	$V_S = 3.5\text{ V}$, $I_S = 1\text{ mA}$
On Resistance Flatness ($R_{FLAT(ON)}$)	10 16	17	18	Ω typ Ω max	$V_{DD} = +5\text{ V}$, $V_{SS} = -5\text{ V}$; $V_S = \pm 3\text{ V}$, $I_S = 1\text{ mA}$
LEAKAGE CURRENTS					
Source OFF Leakage I_S (OFF)	± 0.005 ± 0.2		± 5	nA typ nA max	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ $V_D = \pm 4.5\text{ V}$, $V_S = \mp 4.5\text{ V}$; see Figure 22
Drain OFF Leakage I_D (OFF)	± 0.005 ± 0.2		± 5	nA typ nA max	$V_D = \pm 4.5\text{ V}$, $V_S = \mp 4.5\text{ V}$; see Figure 23
Channel ON Leakage I_D , I_S (ON)	± 0.005 ± 0.2 ± 0.1		± 5 ± 2.5	nA typ nA max nA max	$V_D = V_S = \pm 4.5\text{ V}$; see Figure 24
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current I_{INL} or I_{INH}	0.005		± 1	μA typ μA max	$V_{IN} = V_{INL}$ or V_{INH}
C_{IN} , Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS ¹					
$t_{TRANSITION}$	80 115	140	165	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$; see Figure 25
$t_{ON}(\overline{EN})$	80 115	140	165	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$; see Figure 27
$t_{OFF}(\overline{EN})$	30 45	50	55	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$; see Figure 27
Break-Before-Make Time Delay, t_{BBM}	50		10	ns typ ns min	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 3\text{ V}$; see Figure 26
Charge Injection	2 4			pC typ pC max	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 28
Off Isolation	–90			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 29
Total Harmonic Distortion, THD + N	0.025			% typ	$R_L = 600\ \Omega$, 2 V p-p, $f = 20\text{ Hz}$ to 20 kHz
Channel-to-Channel Crosstalk (ADG659)	–90			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 31
–3 dB Bandwidth	210 400			MHz typ MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 30

Parameter	+25°C	B Version –40°C to +85°C	Y Version –40°C to +125°C	Unit	Test Conditions/Comments
C _S (OFF)	4			pF typ	f = 1 MHz
C _D (OFF)					
ADG658	23			pF typ	f = 1 MHz
ADG659	12			pF typ	f = 1 MHz
C _D , C _S (ON)					
ADG658	28			pF typ	f = 1 MHz
ADG659	16			pF typ	f = 1 MHz
POWER REQUIREMENTS					V _{DD} = +5.5 V, V _{SS} = –5.5 V
I _{DD}	0.01			μA typ	Digital Inputs = 0 V or 5.5 V
			1	μA max	
I _{SS}	0.01			μA typ	Digital Inputs = 0 V or 5.5 V
			1	μA max	

¹ Guaranteed by design; not subject to production test.

5 V SINGLE SUPPLY

$V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	+25°C	B Version –40°C to +85°C	Y Version –40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	$V_{DD} = 4.5\text{ V}$, $V_{SS} = 0\text{ V}$
On Resistance (R_{ON})	85			Ω typ	$V_S = 0\text{ V}$ to 4.5 V , $I_S = 1\text{ mA}$; see Figure 21
	150	160	200	Ω max	
On Resistance Match between Channels (ΔR_{ON})	4.5			Ω typ	$V_S = 3.5\text{ V}$, $I_S = 1\text{ mA}$
	8	9	10	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	13	14	16	Ω typ	$V_{DD} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $V_S = 1.5\text{ V}$ to 4 V , $I_S = 1\text{ mA}$
LEAKAGE CURRENTS					
Source OFF Leakage I_S (OFF)	± 0.005			nA typ	$V_{DD} = 5.5\text{ V}$
	± 0.2		± 5	nA max	$V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$; see Figure 22
Drain OFF Leakage I_D (OFF)	± 0.005			nA typ	$V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$; see Figure 23
ADG658	± 0.2		± 5	nA max	
ADG659	± 0.1		± 2.5	nA max	
Channel ON Leakage I_D , I_S (ON)	± 0.005			nA typ	$V_S = V_D = 1\text{ V}$ or 4.5 V , see Figure 24
ADG658	± 0.2		± 5	nA max	
ADG659	± 0.1		± 2.5	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	$V_{IN} = V_{INL}$ or V_{INH}
			± 1	μA max	
C_{IN} , Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS¹					
$t_{TRANSITION}$	120			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	200	270	300	ns max	$V_S = 3\text{ V}$; see Figure 25
$t_{ON}(\overline{EN})$	120			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	190	245	280	ns max	$V_S = 3\text{ V}$; see Figure 27
$t_{OFF}(\overline{EN})$	35			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	50	60	70	ns max	$V_S = 3\text{ V}$; see Figure 27
Break-Before-Make Time Delay, t_{BBM}	100			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			10	ns min	$V_{S1} = V_{S2} = 3\text{ V}$; see Figure 26
Charge Injection	0.5			pC typ	$V_S = 2.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 28
	1			pC max	
Off Isolation	–90			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 29
Channel-to-Channel Crosstalk	–90			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; $f = 1\text{ MHz}$; see Figure 31
(ADG659)					
–3 dB Bandwidth					
ADG658	180			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 30
ADG659	330			MHz typ	
C_S (OFF)	5			pF typ	$f = 1\text{ MHz}$
C_D (OFF)					
ADG658	29			pF typ	$f = 1\text{ MHz}$
ADG659	15			pF typ	$f = 1\text{ MHz}$

Parameter	B Version		Y Version	Unit	Test Conditions/Comments
	+25°C	–40°C to +85°C	–40°C to +125°C		
C _D , C _S (ON)					
ADG658	30			pF typ	f = 1 MHz
ADG659	16			pF typ	f = 1 MHz
POWER REQUIREMENTS					
I _{DD}	0.01		1	μA typ μA max	V _{DD} = 5.5 V Digital Inputs = 0 V or 5.5 V

¹ Guaranteed by design; not subject to production test.

2.7 V TO 3.6 V SINGLE SUPPLY

$V_{DD} = 2.7$ to 3.6 V, $V_{SS} = 0$ V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	+25°C	B Version –40°C to +85°C	Y Version –40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	$V_{DD} = 2.7$ V, $V_{SS} = 0$ V
On Resistance (R_{ON})	185			Ω typ	$V_S = 0$ V to 2.7 V, $I_S = 0.1$ mA; see Figure 21
	300	350	400	Ω max	
On Resistance Match between	2			Ω typ	$V_S = 1.5$ V, $I_S = 0.1$ mA
Channels (ΔR_{ON})	4.5	6	7	Ω max	
LEAKAGE CURRENTS					
Source OFF Leakage I_S (OFF)	± 0.005			nA typ	$V_{DD} = 3.3$ V
	± 0.2		± 5	nA max	$V_S = 1$ V/3 V, $V_D = 3$ V/1 V; see Figure 22
Drain OFF Leakage I_D (OFF)	± 0.005			nA typ	$V_S = 1$ V/3 V, $V_D = 3$ V/1 V; see Figure 23
ADG658	± 0.2		± 5	nA max	
ADG659	± 0.1		± 2.5	nA max	
Channel ON Leakage I_D, I_S (ON)	± 0.005			nA typ	$V_S = V_D = 1$ V or 3 V, see Figure 24
ADG658	± 0.2		± 5	nA max	
ADG659	± 0.1		± 2.5	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.5	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μ A typ	$V_{IN} = V_{INL}$ or V_{INH}
			± 1	μ A max	
C_{IN} , Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS¹					
$t_{TRANSITION}$	200			ns typ	$R_L = 300 \Omega$, $C_L = 35$ pF
	370	440	490	ns max	$V_S = 1.5$ V; see Figure 25
$t_{ON}(\overline{EN})$	230			ns typ	$R_L = 300 \Omega$, $C_L = 35$ pF
	370	440	490	ns max	$V_S = 1.5$ V; see Figure 27
$t_{OFF}(\overline{EN})$	50			ns typ	$R_L = 300 \Omega$, $C_L = 35$ pF
	80	90	110	ns max	$V_S = 1.5$ V; see Figure 27
Break-Before-Make Time Delay, t_{BBM}	200			ns typ	$R_L = 300 \Omega$, $C_L = 35$ pF
			10	ns min	$V_{S1} = V_{S2} = 1.5$ V; see Figure 26
Charge Injection	1			pC typ	$V_S = 1.5$ V, $R_S = 0 \Omega$, $C_L = 1$ nF; see Figure 28
	2			pC max	
Off Isolation	–90			dB typ	$R_L = 50 \Omega$, $C_L = 5$ pF, $f = 1$ MHz; see Figure 29
Channel-to-Channel Crosstalk	–90			dB typ	$R_L = 50 \Omega$, $C_L = 5$ pF; $f = 1$ MHz; see Figure 31
(ADG659)					
–3 dB Bandwidth					
ADG658	160			MHz typ	$R_L = 50 \Omega$, $C_L = 5$ pF; see Figure 30
ADG659	300			MHz typ	
C_S (OFF)	5			pF typ	$f = 1$ MHz
C_D (OFF)					
ADG658	29			pF typ	$f = 1$ MHz
ADG659	15			pF typ	$f = 1$ MHz

Parameter	+25°C	B Version –40°C to +85°C	Y Version –40°C to +125°C	Unit	Test Conditions/Comments
C _D , C _S (ON)					
ADG658	30			pF typ	f = 1 MHz
ADG659	16			pF typ	f = 1 MHz
POWER REQUIREMENTS					V _{DD} = 3.6 V
I _{DD}	0.01		1	μA typ μA max	Digital Inputs = 0 V or 3.6 V

¹ Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to V_{SS}	13 V
V_{DD} to GND	−0.3 V to +13 V
V_{SS} to GND	+0.3 V to −6.5 V
Analog Inputs ¹	$V_{SS} - 0.3 \text{ V}$ to $V_{DD} + 0.3 \text{ V}$
Digital Inputs ¹	GND − 0.3 V to $V_{DD} + 0.3 \text{ V}$ or 10 mA, whichever occurs first
Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max)	40 mA
Continuous Current, S or D	20 mA
Operating Temperature Range	
Automotive (Y Version)	−40°C to +125°C
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
16-Lead QSOP	104°C/W
16-Lead TSSOP	150.4°C/W
16-Lead LFCSP (4-Layer Board)	70°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	5.5 kV

¹ Over voltages at A_x , $\overline{EN}$, S, or D are clamped by internal diodes. Current must be limited to the maximum ratings.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 5. ADG658 Truth Table

A2	A1	A0	$\overline{\text{EN}}$	Switch Condition
X ¹	X ¹	X ¹	1	None
0	0	0	0	1
0	0	1	0	2
0	1	0	0	3
0	1	1	0	4
1	0	0	0	5
1	0	1	0	6
1	1	0	0	7
1	1	1	0	8

¹ X = Don't Care

Table 6. ADG659 Truth Table

A1	A0	$\overline{\text{EN}}$	On Switch Pair
X ¹	X ¹	1	None
0	0	0	1
0	1	0	2
1	0	0	3
1	1	0	4

¹ X = Don't Care

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

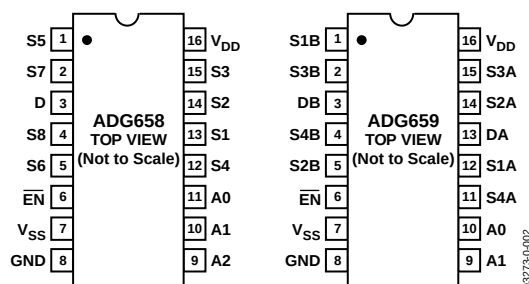
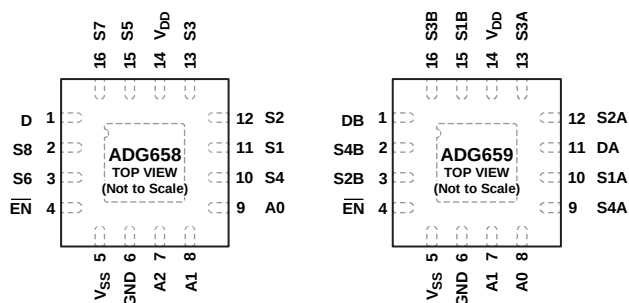


Figure 2. 16-Lead TSSOP/QSOP Pin Configuration



NOTES

1. EXPOSED PAD. THE EXPOSED PAD MUST BE LEFT FLOATING.

Figure 3. 16-Lead, 4 mm × 4 mm LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Parameter	Description
V_{DD}	Most Positive Power Supply Potential.
V_{SS}	Most Negative Power Supply Potential.
I_{DD}	Positive Supply Current.
I_{SS}	Negative Supply Current.
GND	Ground (0 V) Reference.
S	Source Terminal. Can be an input or output.
D	Drain Terminal. Can be an input or output.
A_X	Logic Control Input.
$\overline{EN}$	Active Low Digital Input. When high, device is disabled and all switches are OFF. When low, A_X logic inputs determine ON switch.
EPAD (LFCSP Only)	Exposed Pad. The exposed pad must be left floating.

TYPICAL PERFORMANCE CHARACTERISTICS

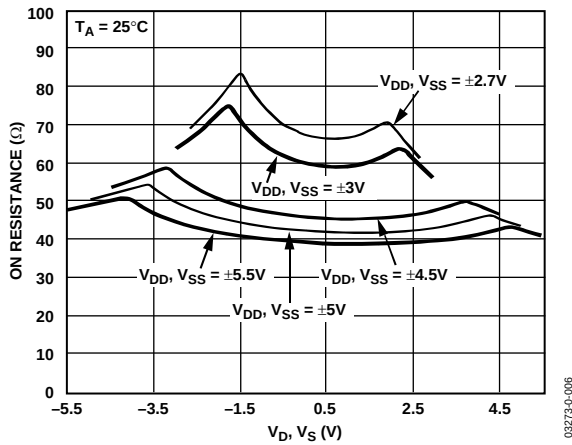
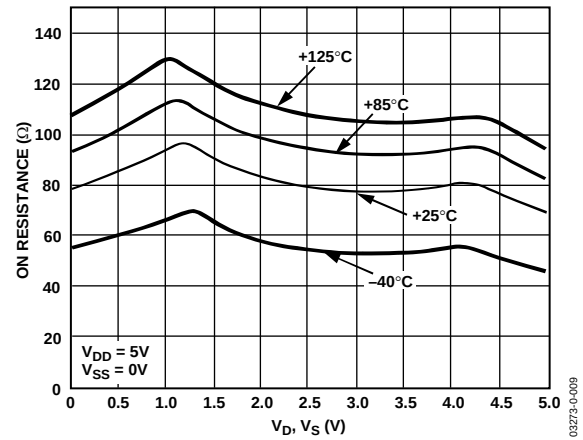
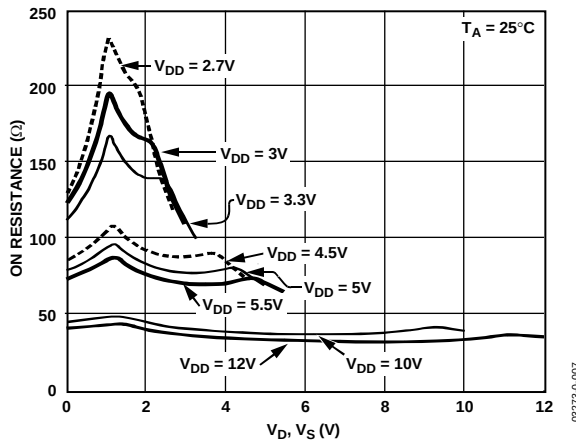
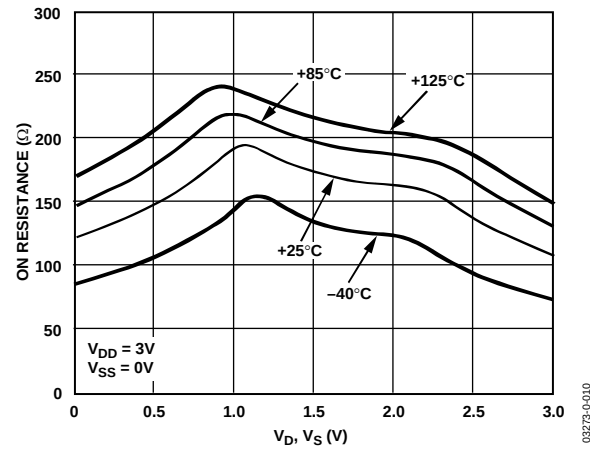
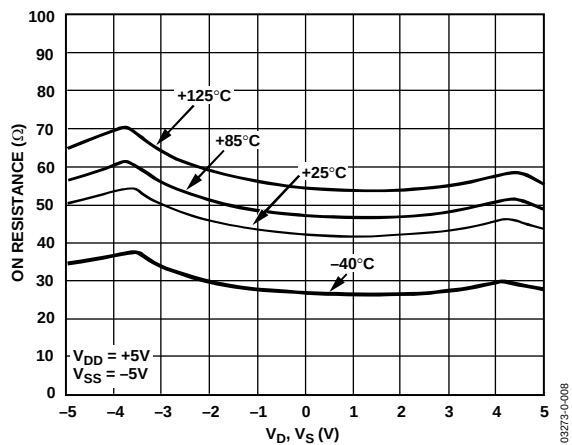
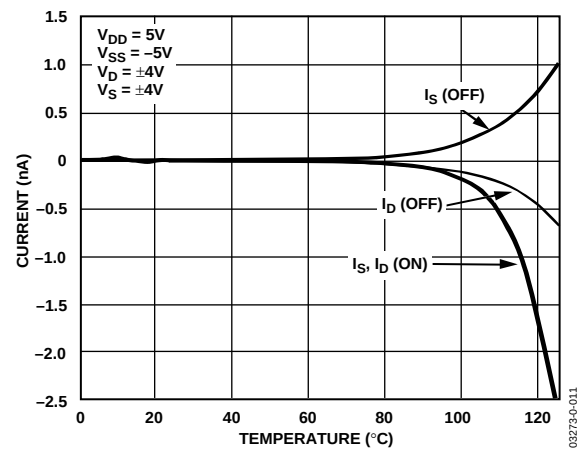
Figure 4. On Resistance vs. V_D (V_S) for Dual SupplyFigure 7. On Resistance vs. V_D (V_S) for Different Temperatures (Single Supply)Figure 5. On Resistance vs. V_D (V_S) for Single SupplyFigure 8. On Resistance vs. V_D (V_S) for Different Temperatures (Single Supply)Figure 6. On Resistance vs. V_D (V_S) for Different Temperatures (Dual Supply)

Figure 9. Leakage Current vs. Temperature (Dual Supply)

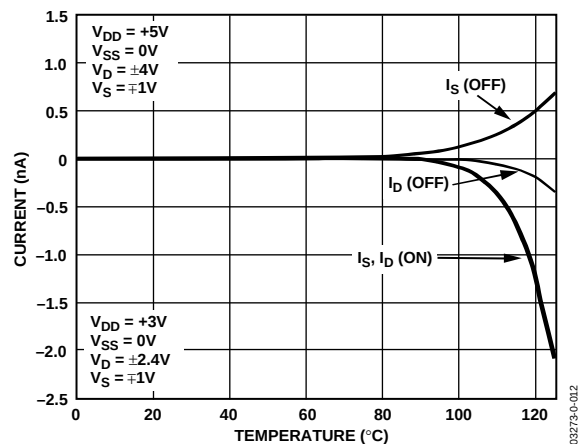


Figure 10. Leakage Current vs. Temperature (Single Supply)

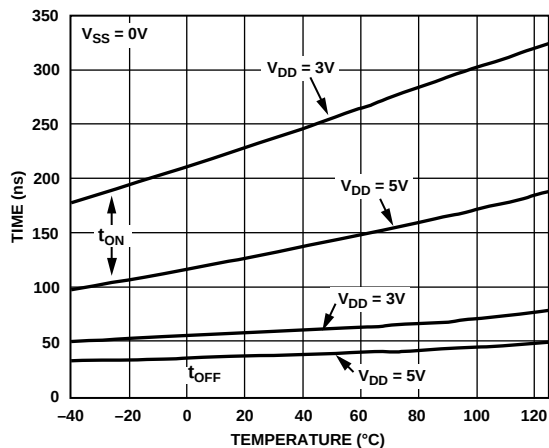
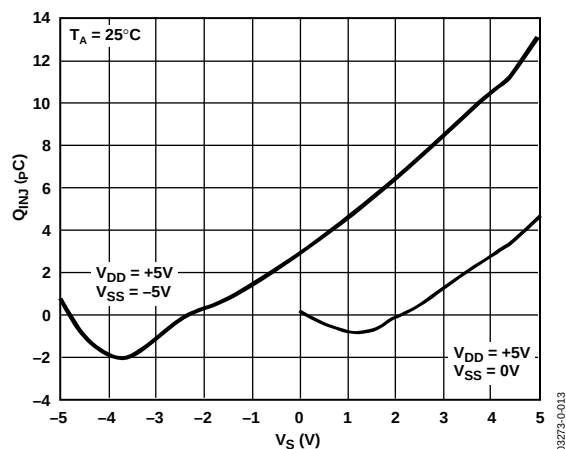
Figure 13. t_{ON}/t_{OFF} Times vs. Temperature (Single Supply)

Figure 11. Charge Injection vs. Source Voltage

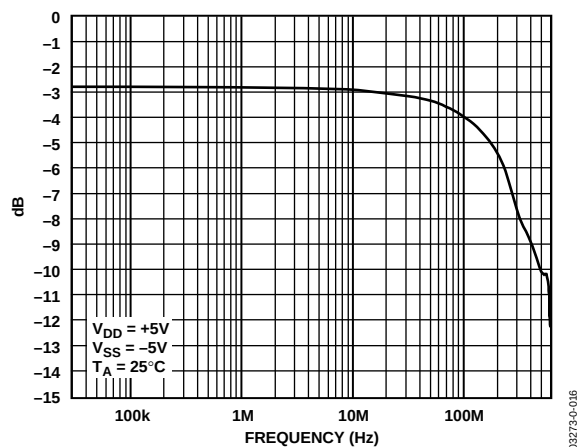


Figure 14. ON Response vs. Frequency (ADG658)

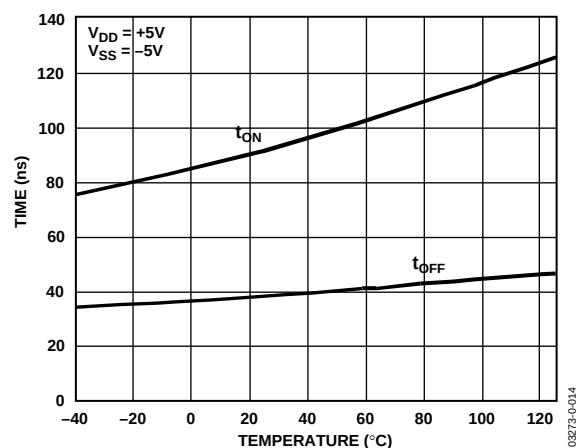
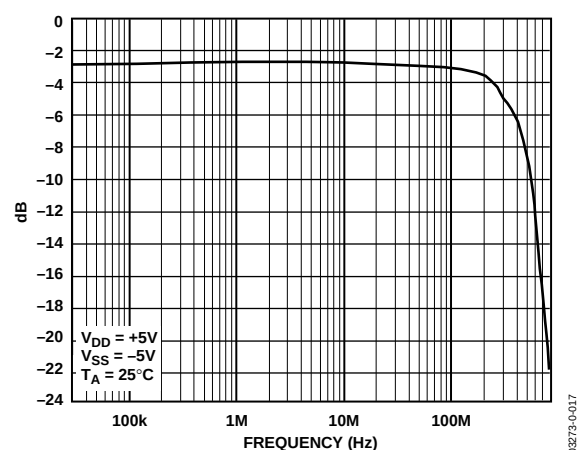
Figure 12. t_{ON}/t_{OFF} Times vs. Temperature (Dual Supply)

Figure 15. ON Response vs. Frequency (ADG659)

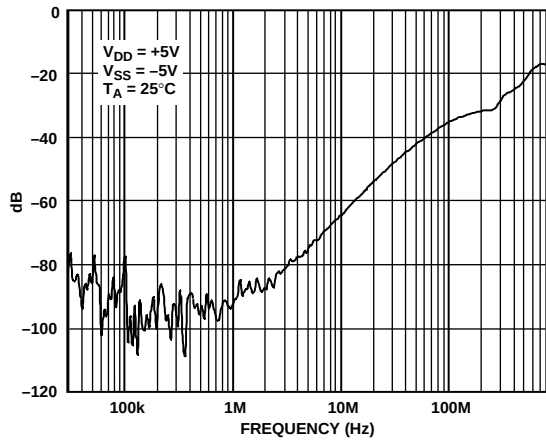


Figure 16. OFF Isolation vs. Frequency

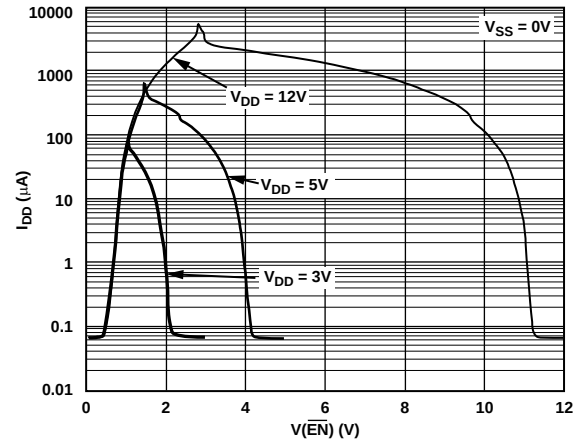


Figure 19. V_{DD} Current vs. Logic Level

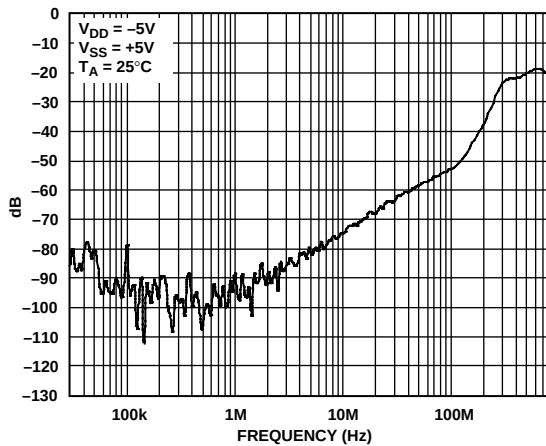


Figure 17. Crosstalk vs. Frequency

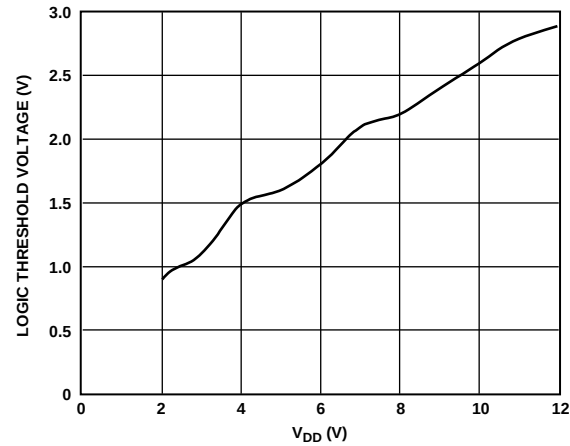


Figure 20. Logic Threshold Voltage vs. Supply Voltage

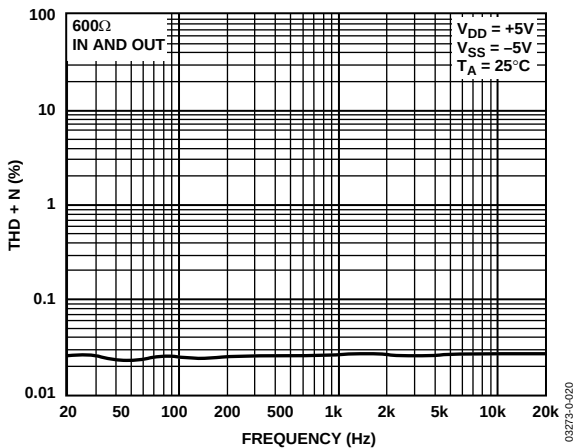


Figure 18. THD + Noise

TERMINOLOGY

V_D (V_S)

Analog Voltage on Terminals D, S.

R_{ON}

Ohmic Resistance between D and S.

ΔR_{ON}

On Resistance Match between Any Two Channels, i.e., $R_{ONmax} - R_{ONmin}$.

$R_{FLAT(ON)}$

Flatness is defined as the difference between the maximum and minimum value of ON Resistance as measured over the specified analog signal range.

I_S (OFF)

Source Leakage Current with the Switch OFF.

I_D (OFF)

Drain Leakage Current with the Switch OFF.

I_D, I_S (ON)

Channel Leakage Current with the Switch ON.

V_{INL}

Maximum Input Voltage for Logic 0.

V_{INH}

Minimum Input Voltage for Logic 1.

I_{INL} (I_{INH})

Input Current of the Digital Input.

C_S (OFF)

OFF Switch Source Capacitance. Measured with reference to ground.

C_D (OFF)

OFF Switch Drain Capacitance. Measured with reference to ground.

C_D, C_S (ON)

ON Switch Capacitance. Measured with reference to ground.

C_{IN}

Digital Input Capacitance.

t_{ON}

Delay between Applying the Digital Control Input and the Output Switching ON. See Figure 27.

t_{OFF}

Delay between Applying the Digital Control Input and the Output Switching OFF.

t_{BEM}

ON Time. Measured between 80% points of both switches when switching from one address state to another.

Charge Injection

Measure of the Glitch Impulse Transferred from the Digital Input to the Analog Output during Switching.

Off Isolation

Measure of Unwanted Signal Coupling through an OFF Switch.

Crosstalk

Measure of Unwanted Signal Coupled through from One Channel to Another as a Result of Parasitic Capacitance.

Bandwidth

The Frequency at which the Output is Attenuated by 3 dB.

On Response

The Frequency Response of the ON Switch.

Insertion Loss

The Loss Due to the ON Resistance of the Switch.

TEST CIRCUITS

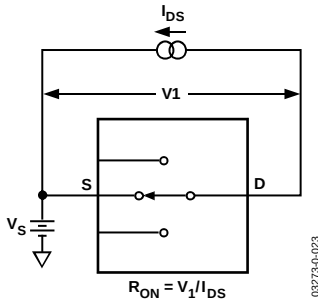


Figure 21. ON Resistance

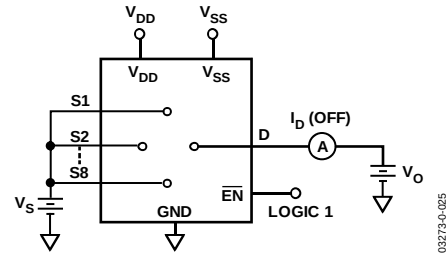


Figure 23. I_D (OFF)

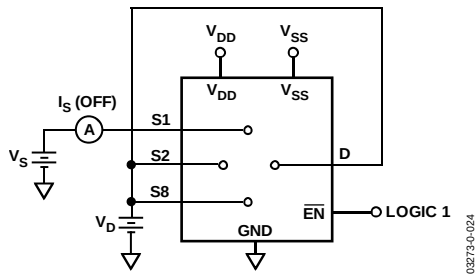


Figure 22. I_S (OFF)

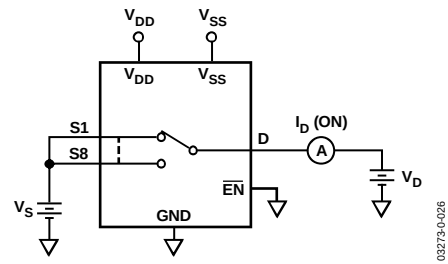


Figure 24. I_D (ON)

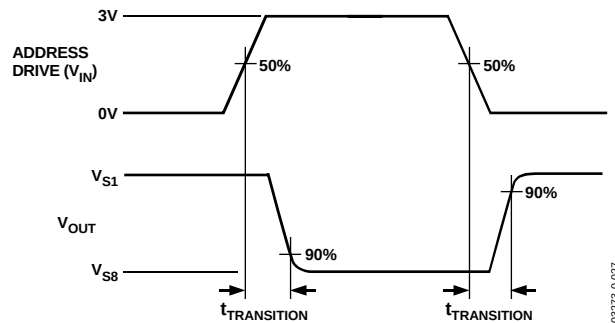
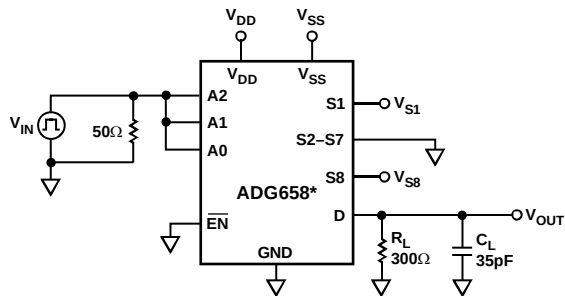


Figure 25. Switching Time of Multiplexer, $t_{\text{TRANSITION}}$

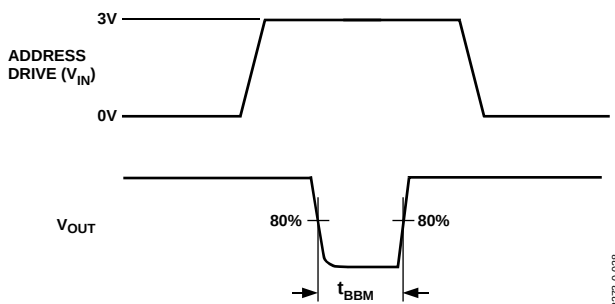
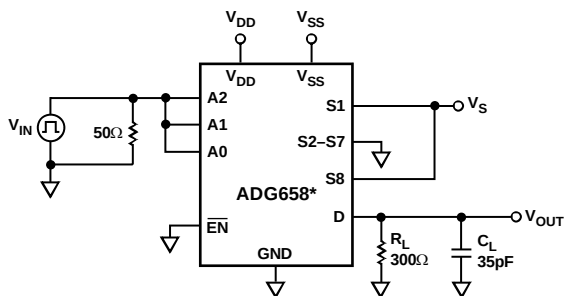
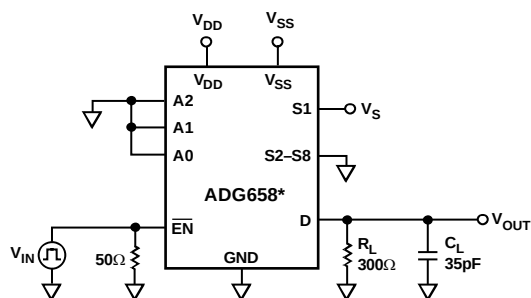
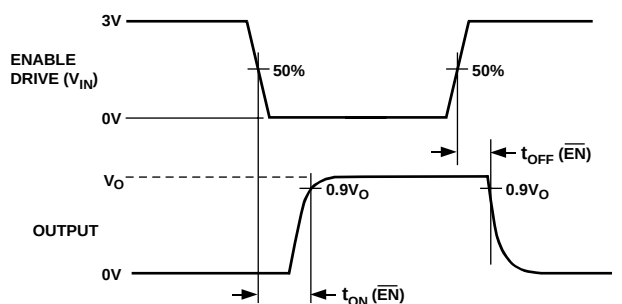


Figure 26. Break-Before-Make Delay, t_{BBM}

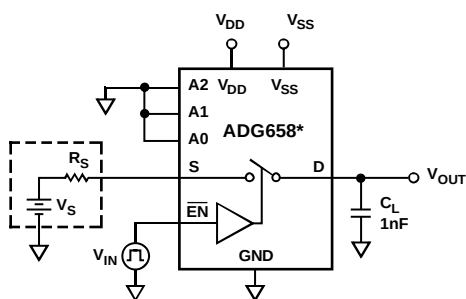


*SIMILAR CONNECTION FOR ADG659

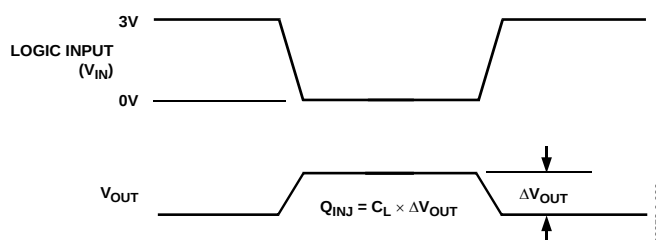


03273-0-029

Figure 27. Enable Delay, $t_{ON}(\overline{EN})$, $t_{OFF}(\overline{EN})$

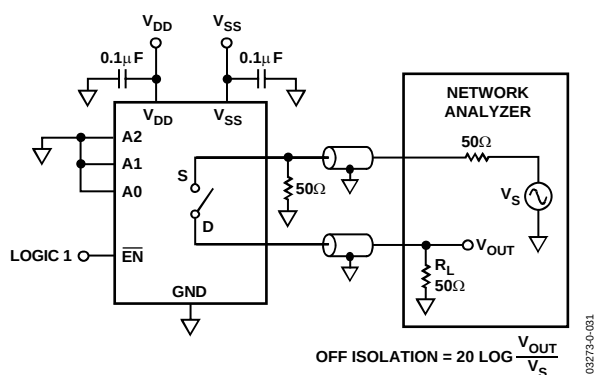


*SIMILAR CONNECTION FOR ADG659



03273-0-030

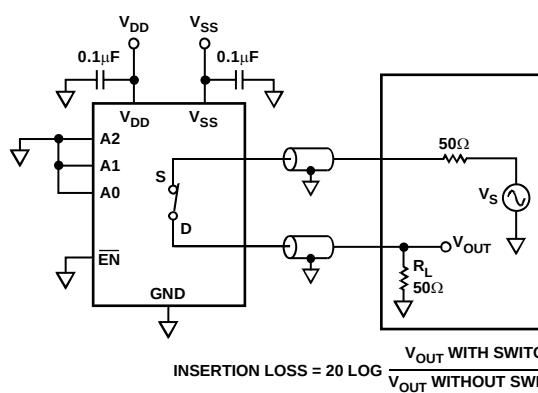
Figure 28. Charge Injection



$$\text{OFF ISOLATION} = 20 \log \frac{V_{OUT}}{V_S}$$

03273-0-031

Figure 29. Off Isolation



$$\text{INSERTION LOSS} = 20 \log \frac{V_{OUT \text{ WITH SWITCH}}}{V_{OUT \text{ WITHOUT SWITCH}}}$$

03273-0-032

Figure 30. Bandwidth

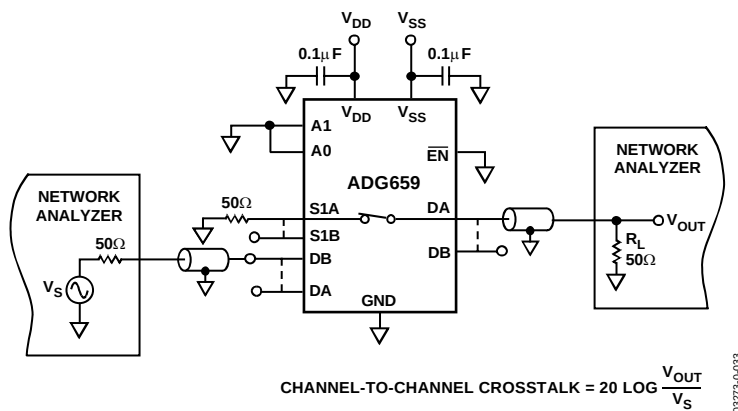


Figure 31. Channel-to-Channel Crosstalk

OUTLINE DIMENSIONS

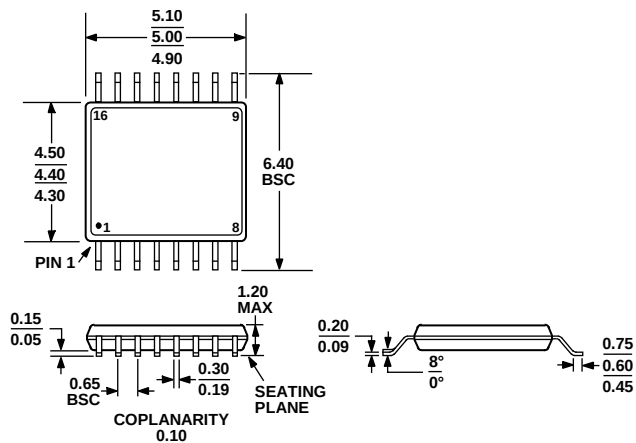
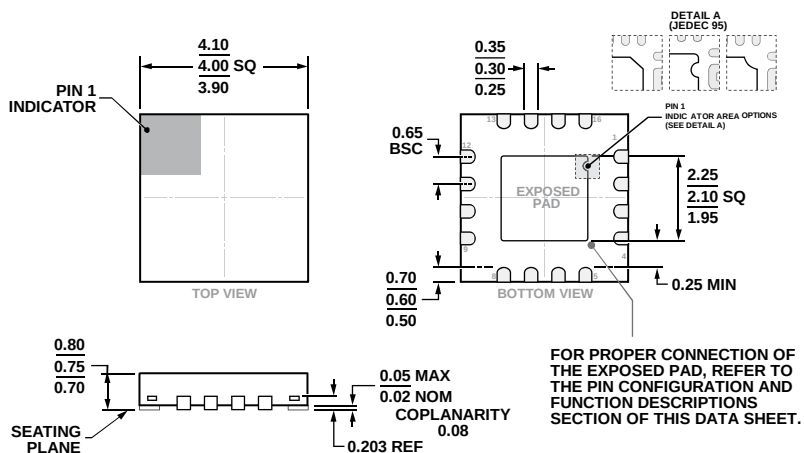


Figure 32. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)

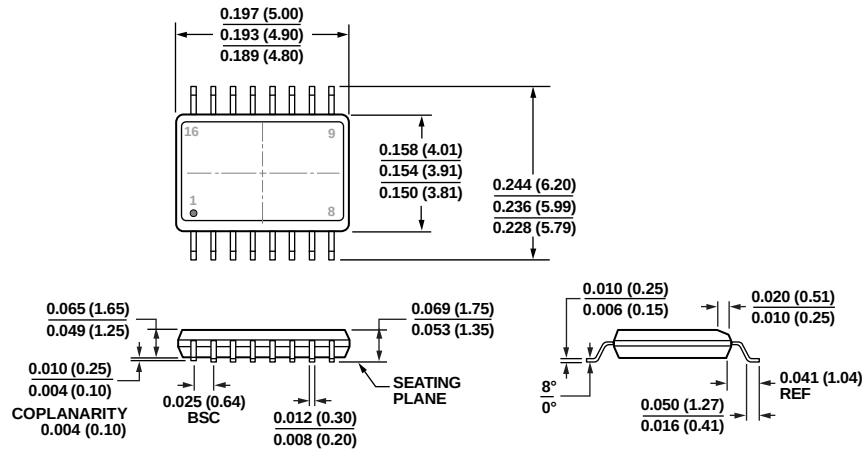
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 33. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-23)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-137-AB
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 34. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)

Dimensions shown in inches and (millimeters)

09-12-2014-A

ORDERING GUIDE

Model ^{1, 2}	Temperature Range	Package Description	Package Option
ADG658YRU	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG658YRU-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG658YRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG658YRUZ-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG658YCPZ	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-23
ADG658YCPZ-REEL7	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-23
ADG658YRQ	−40°C to +125°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADG658YRQZ	−40°C to +125°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADG658YRQZ-REEL7	−40°C to +125°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADW54003-0	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADW54003-ORL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG659YRU	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG659YRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG659YRUZ-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG659YRUZ-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG659YCPZ	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-23
ADG659YCPZ-REEL7	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-23
ADG659YRQZ	−40°C to +125°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16

¹ Z = RoHS Compliant Part.

² W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADW54003 models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.