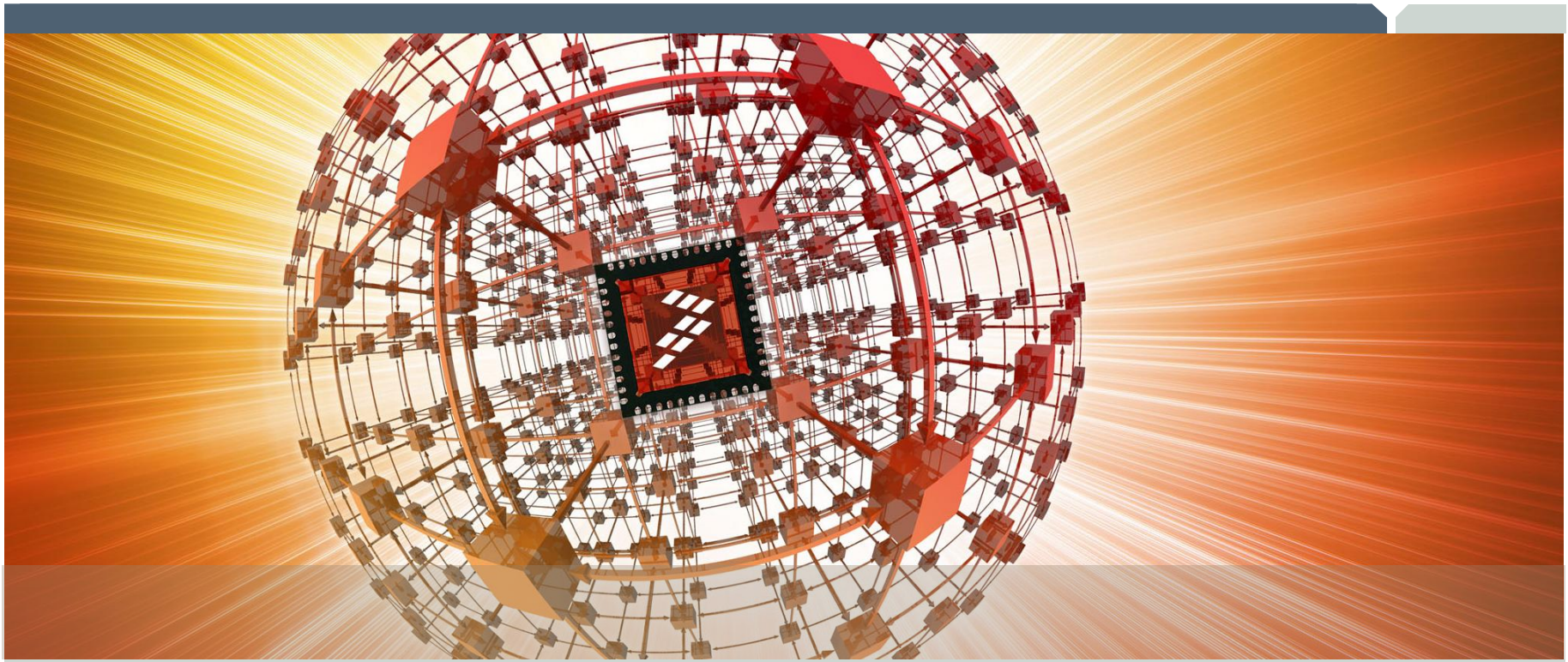

Kinetis Microcontrollers

The most scalable portfolio of low power, mixed-signal MCUs based on the ARM Cortex-M4 architecture in the industry

November 4, 2010

Eduardo Montanez – Industrial & Multi-Market Systems Engineer

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Kinetis Revolution: Cortex-M4 Microcontroller Portfolio Powered with Innovative 90nm TFS Flash Technology by Freescale

Freescale's 32-bit industrial and consumer microcontrollers are evolving into a new era with the launch of Kinetis. The first broad-market mixed signal microcontroller family based on the new ARM Cortex-M4 core and innovative 90nm thin-film storage (TFS) flash memory technology. With over 200 Kinetis MCUs, Freescale enables scalable performance, market-leading mixed-signal integration and ultra-low power consumption.

Agenda

- Portfolio Overview
- Key Differentiators
- Enablement Solutions
- Application Use Cases
- Technical Deep Dive
- Kinetis Solution Demonstration

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New Kinetis MCUs

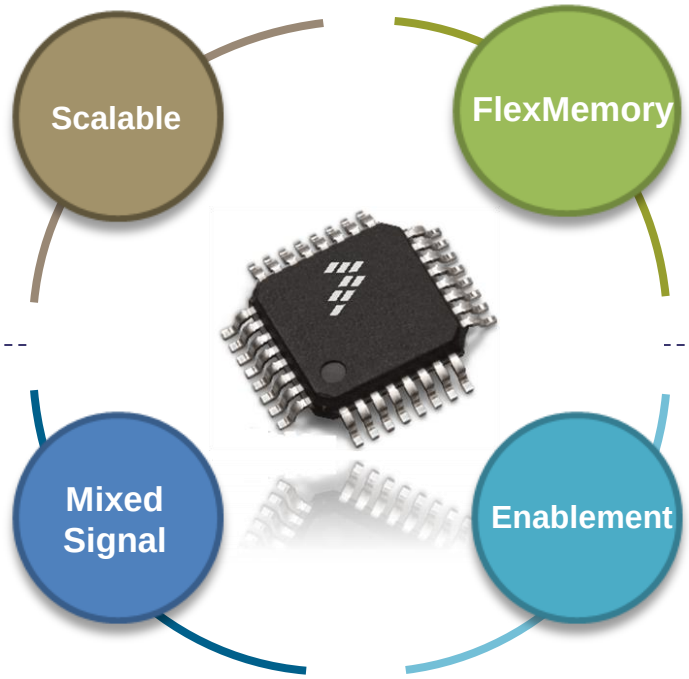
Scalable Mixed-Signal Consumer and Industrial Microcontroller Families

The most **scalable** portfolio of **low-power ARM Cortex-M4** MCUs available today

*Over **200** hardware and software compatible ARM Cortex-M4 devices with high performance **signal processing capability** and run currents of **<200uA/MHz***

Innovative Low Power **90nm Thin-Film Storage** Flash with **FlexMemory**

*Offers **EEPROM capability** with unprecedented programming speed and endurance, capable of over **10 Million cycles***



Exceptional **mixed-signal** integration

*Flexible, High-speed, high-precision 16-bit **ADCs**, 12-bit **DACs**, Programmable Gain **Amplifiers**, Voltage References, and Hardware **Touch Sensing** lower system costs.*

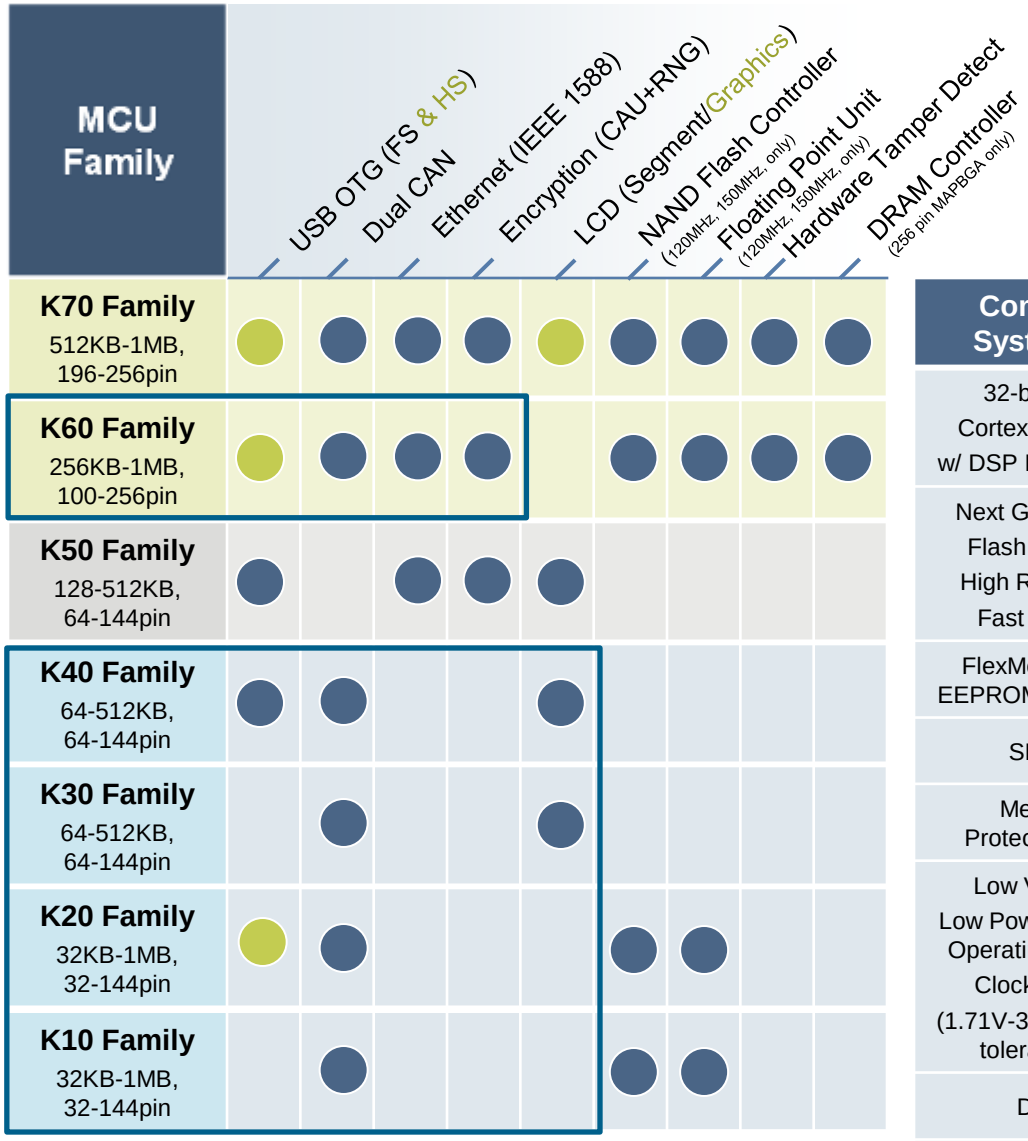
One of the most **comprehensive ARM® enablement** portfolios

***Complimentary Freescale MQX RTOS** and **Eclipse-based CodeWarrior** 10.0 IDE, as well as **IAR, KEIL** and other ARM ecosystem providers help speed time to market*

More than **200 New** Parts
7 scalable families

First available broad-market MCU samples based on ARM Cortex-M4!

Kinetis Product Family Features



Available Q4 2010

Common System IP	Common Analog IP	Common Digital IP	Development Tools
32-bit ARM Cortex-M4 Core w/ DSP Instructions	16-bit ADC	CRC	Bundled IDE w/ Processor Expert
Next Generation Flash Memory High Reliability, Fast Access	Programmable Gain Amplifiers	I^2C	Bundled OS USB, TCP/IP, Security
FlexMemory w/ EEPROM capability	12-bit DAC	SAI (I^2S)	Modular Tower H/ware Development System
SRAM	High-speed Comparators	UART/SPI	Application Software Stacks, Peripheral Drivers & App. Libraries (Motor Control, HMI, USB)
Memory Protection Unit	Low-power Touch Sensing	Programmable Delay Block	
Low Voltage, Low Power Multiple Operating Modes, Clock Gating (1.71V-3.6V with 5V tolerant I/O)		External Bus Interface	
DMA		Motor Control Timers	
-40 to 105C		eSDHC	Broad 3rd party ecosystem
		RTC	

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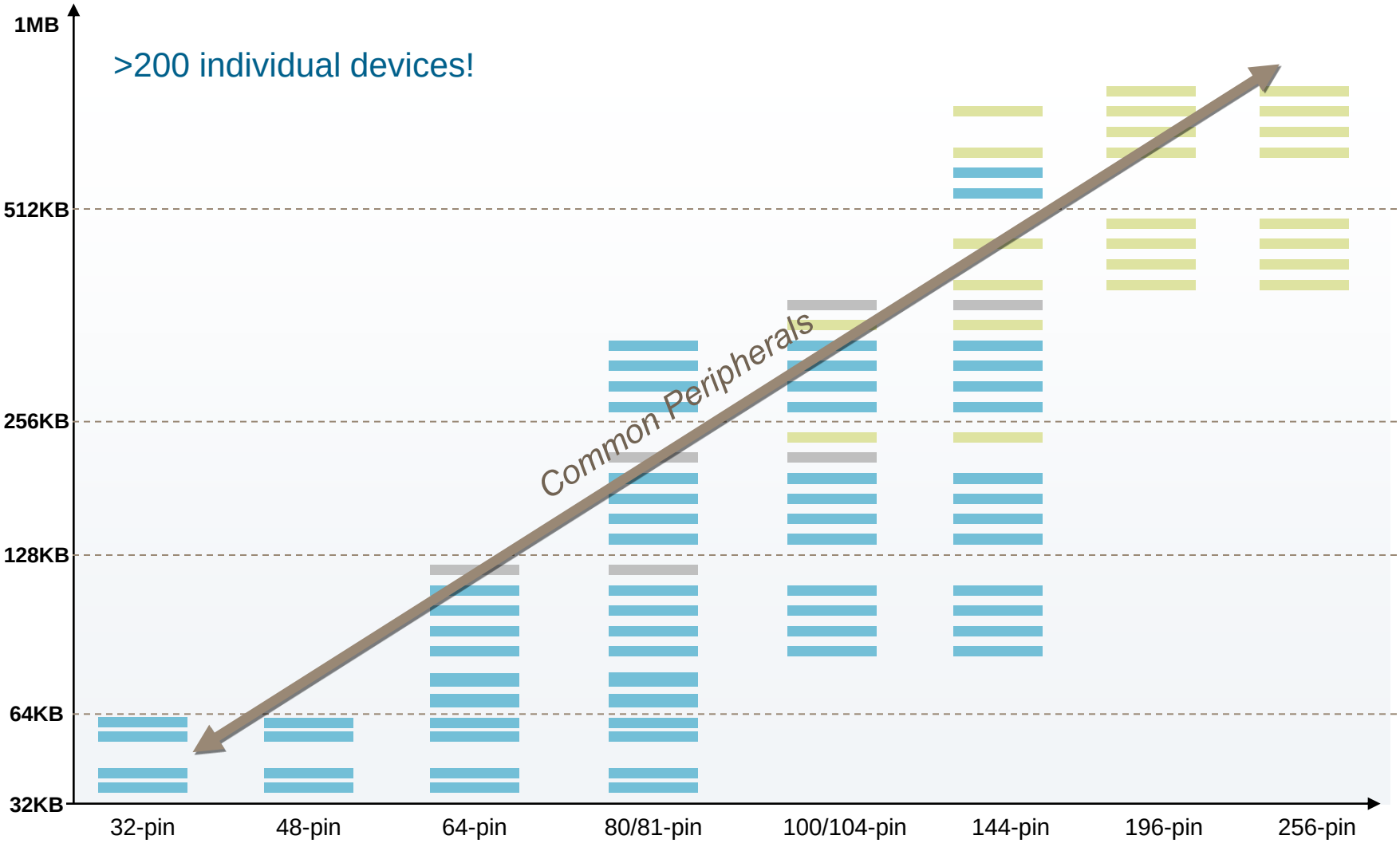
An Unmatched Range of ARM Cortex-M4 Microcontrollers



Multiple compatible families with scalable performance, memory and peripherals

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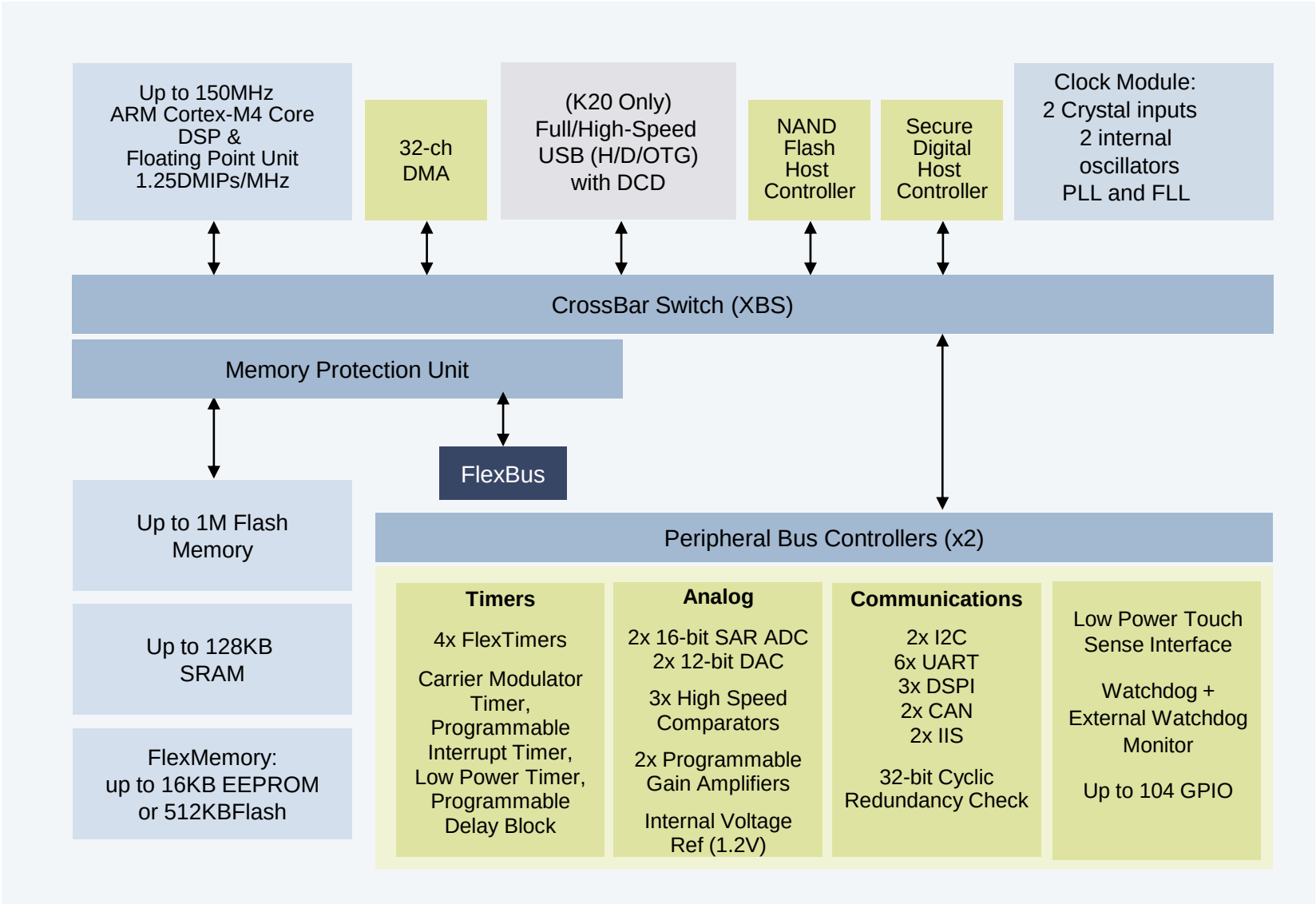
K10/K20 Family Block Diagram



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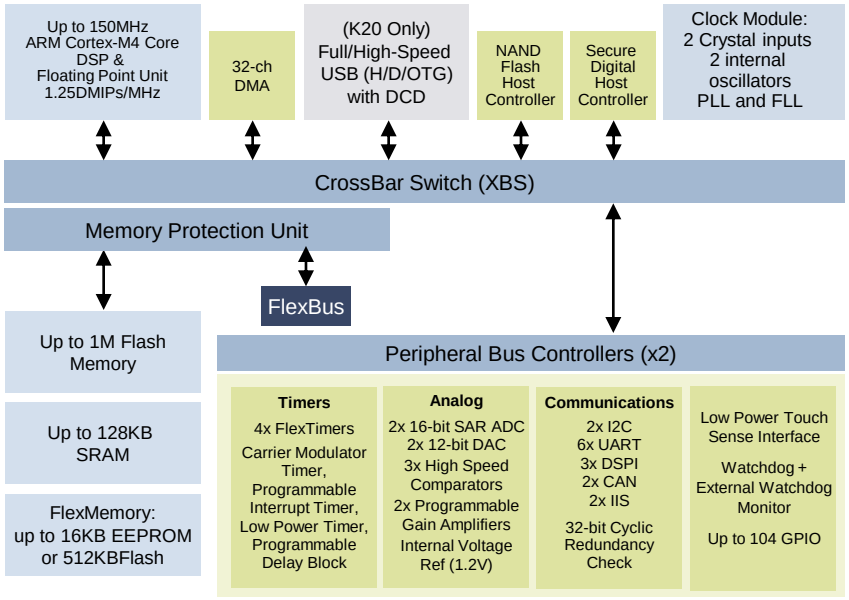
K10/K20 Family Overview

High Integration Mixed-Signal MCUs

- **Processing Performance and FlexMemory**
  - Direct Memory Access, Cross Bar Switch, and on-chip Cache maximize bus bandwidth and Flash execution
  - FlexMemory provides on-chip, high-endurance configurable EEPROM and/or additional Flash memory
- **(K20 Only) Connect via USB AND charge a battery**
  - USB 2.0 Full-Speed Device/Host/OTG Controller with integrated transceiver, HS via ULPI interface
  - Includes Device Charge Detector (DCD) and Regulator to supports battery charging via USB for Portable Devices
- **Flexible and Powerful Mixed Signal Capability**
  - 16-bit ADC enables small signal capture for medical/sensing applications, or high speed conversions for motor control.
  - 12-bit DAC, High-Speed Comparator, and Voltage Reference on-chip reduces system cost
- **Ultra-low power with 1.71V operation**
  - Multiple low power modes and Flash & analog operation down to 1.71V – power profile optimization and prolonged battery life
  - Stop Currents <500nA, run currents <200uA/MHz

32KB Flash in 32 pin package starting at $0.99 for 10K SRP



Enablement Bundle

TOWER development system
Complementary MQX RTOS with USB Stack
Eclipse-Based CodeWarrior 10.0 IDE
Processor Expert Rapid Application Development Tool
IAR, Keil and full ARM Ecosystem Support
Motor Control and DSP Libraries

Family	USB OTG + DCD
K10	-
K20	X

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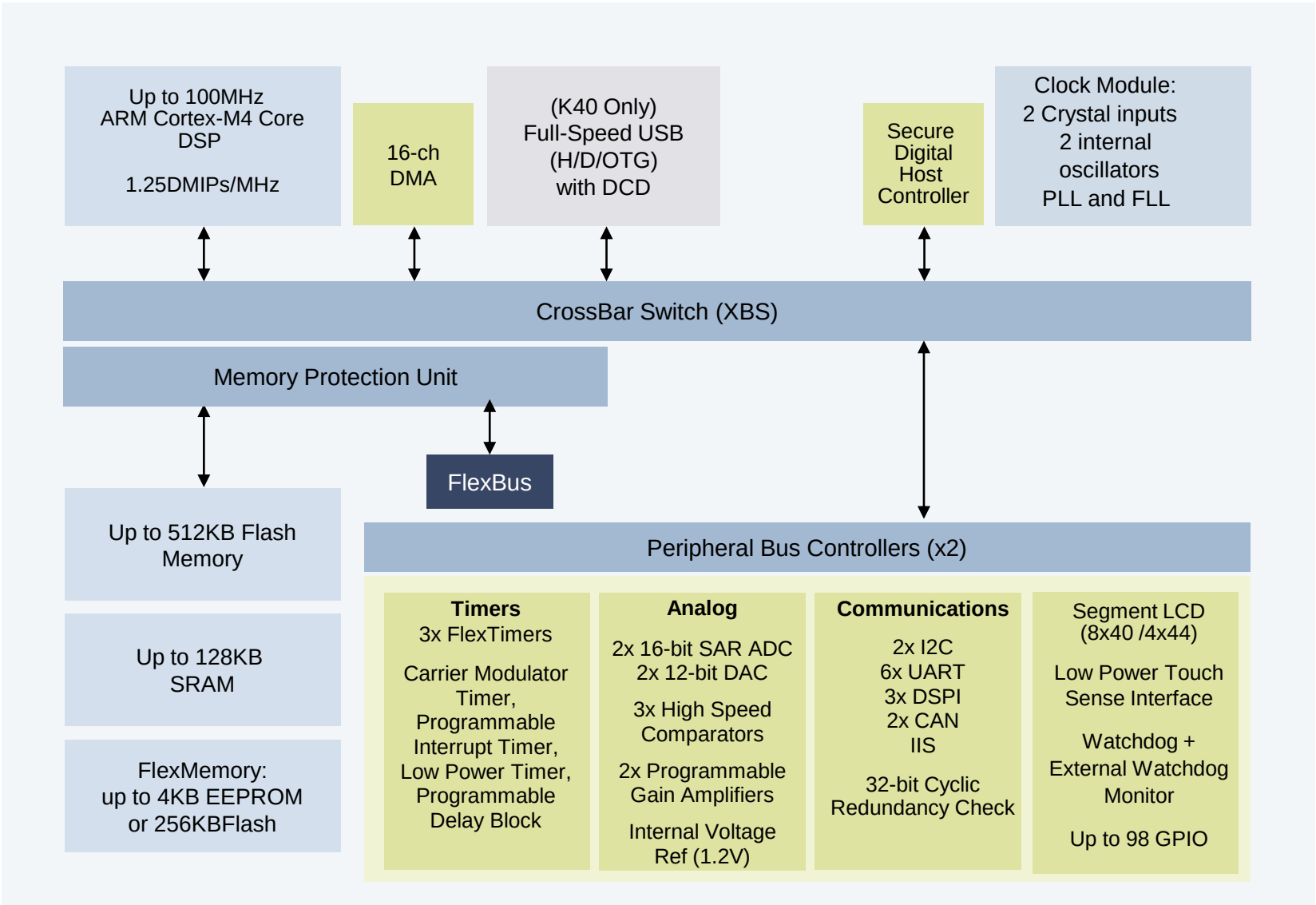
K30/K40 Family Block Diagram



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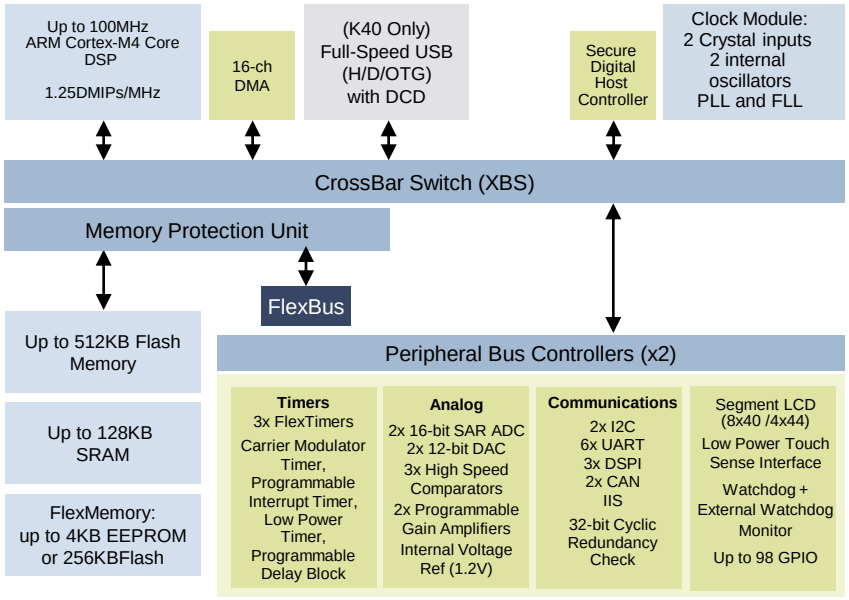
K30/K40 Family Overview

For Segment LCD HMI Applications

- **Flexible, low power LCD Interface**
  - Segment LCD Blink mode lowers average power
  - Segment Fail Detect prevents erroneous readouts and reduces LCD test cost
  - Front/back plane reassignment provides pin-out flexibility and allows configuration changes in firmware
- **Diverse communications suite**
  - A multitude of serial interfaces, with UART support for ISO7816 SIM/Smart Cards & IrDA interfaces
  - Dual CAN for industrial network bridging
- **System reliability & safety**
  - Hardware Cyclic Redundancy Check safeguards memory contents and communication data
  - Memory Protection Unit – increase SW reliability
  - Independently-clocked watchdog prevents code runaway for fail-safe applications e.g. IEC60730
- **Hardware and software compatibility**
  - Common packages & peripherals across families enable rapid feature growth with minimal hardware & software disruption



Enablement Bundle

TOWER development system
Complementary MQX RTOS with USB Stack
Eclipse-Based CodeWarrior 10.0 IDE
Processor Expert Rapid Application Development Tool
IAR, Keil and Full ARM Ecosystem Support
Motor Control Software Library, IEC60730 test routines

Family	USB OTG + DCD	Segment LCD
K30	-	X
K40	X	X

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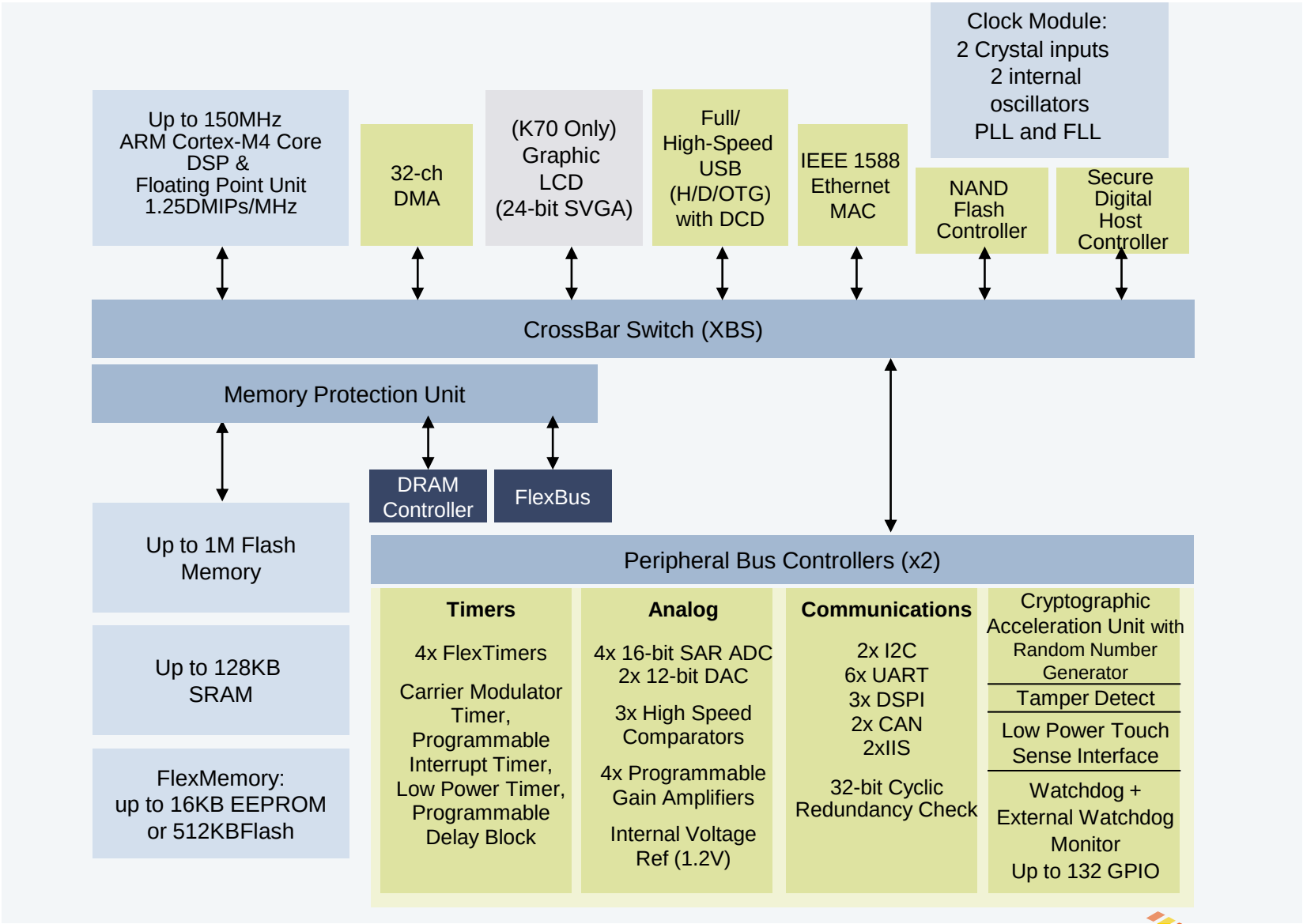
K60/K70 Family Block Diagram



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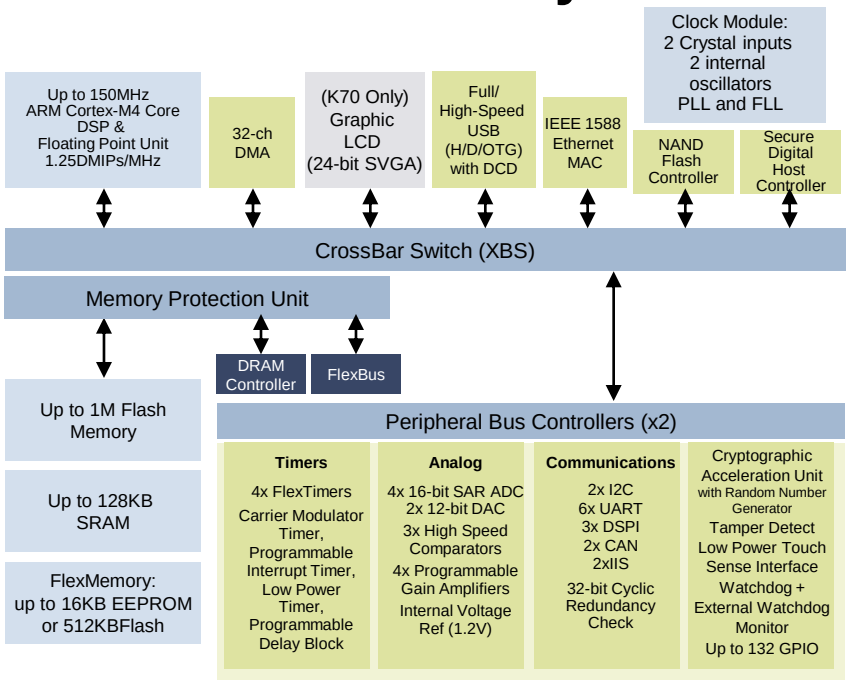
K60/K70 Family Overview

Higher Performance, Security, & Connectivity

- **Real-time Ethernet for precision automation**
  - IEEE 1588 hardware time stamping & clock synchronization enables accurate, deterministic control over Ethernet networks
- **(K70 only) Graphical LCD for advanced user interfaces**
  - Single-chip QVGA support possible, allowing use of lower-cost displays without Chip-on-Glass capability
  - Up to 24-bit SVGA with external memory support
- **Robust system security with tamper detection**
  - Tamper detection with voltage, frequency, and temperature monitoring. External sensor support for physical attack detection
- **Hardware Encryption for secure data transfer & storage**
  - Significantly faster than software implementations while consuming minimal system resources.
  - Supports numerous algorithms with hardware assisted software routines – SSH, SSL, IPSec, etc



Enablement Bundle

TOWER development system
Complementary MQX RTOS with TCP/IP & USB Stack
Eclipse-Based CodeWarrior 10.0 IDE
Processor Expert Rapid Application Development Tool
IAR, Keil and Full ARM Ecosystem Support
Graphics LCD and Encryption libraries

Family	Graphics LCD Controller	IEEE 1588 Ethernet / Encryption / Tamper Detect
K60	-	X
K70	X	X

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Key Differentiators

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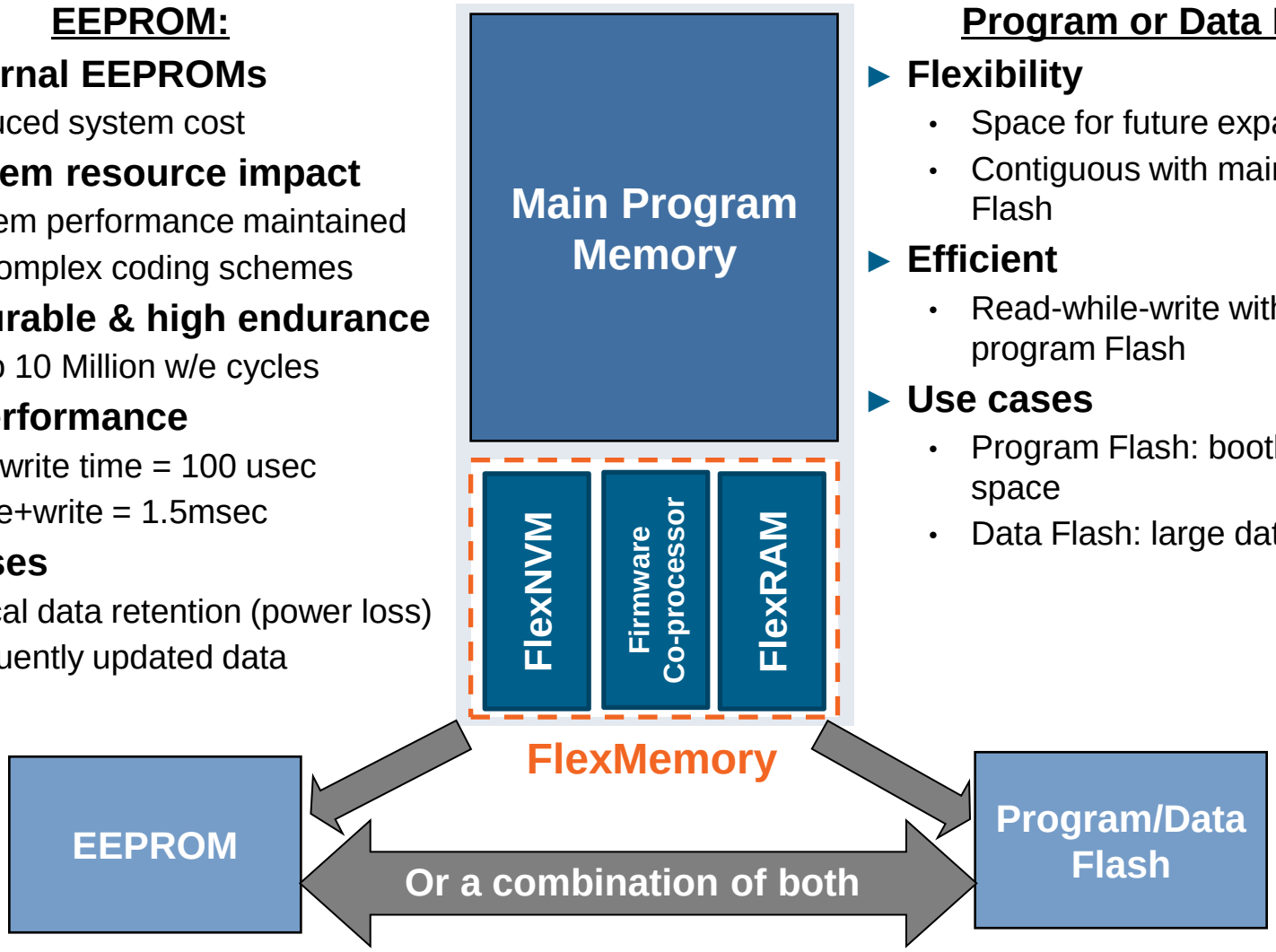
What is FlexMemory?

User Configurable As…

EEPROM:

- **No external EEPROMs**
  - Reduced system cost
- **No system resource impact**
  - System performance maintained
  - No complex coding schemes
- **Configurable & high endurance**
  - Up to 10 Million w/e cycles
- **High performance**
  - Fast write time = 100 usec
  - Erase+write = 1.5msec
- **Use cases**
  - Critical data retention (power loss)
  - Frequently updated data



Program or Data Flash:

- **Flexibility**
  - Space for future expansion needs
  - Contiguous with main program Flash
- **Efficient**
  - Read-while-write with the main program Flash
- **Use cases**
  - Program Flash: bootloader code space
  - Data Flash: large data tables

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Freescale FlexMemory vs. Traditional EEPROM

Attribute	Traditional Embedded EEPROM	FlexMemory
Read-while-write with program memory	Yes	Yes
Granularity	Byte write/erase	Byte write/erase
Write time	~1-5 msec (byte write only)	~100 µsec (byte or word program to erased location, brown-outs w/o loss or corruption of data)
Erase + write time	~5-10 msec	~1.5 msec (byte or word erase and program)
Endurance	50-300K cycles (fixed)	SoC implementation and user configurable, can exceed 10M cycles
Minimum write voltage	≥ 2.0V	1.71V
Flexibility	Fixed by part number	Programmable trade-off - quantity vs. endurance

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Mixed Signal Integration

- **16-bit SAR ADCs**
  - 1.15V minimum reference
  - Differential or Single Ended
  - Averaging by 1, 4, 8, 16, or 32
  - Automatic Compare Function
  - Triggering synchronization w/ DAC
  - Configurable resolution, sample time, speed and power (8/10/12/16-bit resolution)
  - Up to 20 input channels per converter
- **Voltage Reference (Vref)**
  - Trimmable
  - < 33ppm/ºC temp variation
- **12-bit DACs**
  - 16 word DAC FIFO
  - Hardware or software trigger
- **High Speed Comparators**
  - Programmable hysteresis control, and interrupt trigger
  - Selectable inversion on comparator output
  - Integrated 6-bit DAC for reference
- **Programmable Gain Amplifiers**
  - x64 gain

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Kinetis: Low Power Capabilities

- **Flexible power modes**
  - **10** Run, Wait & STOP modes – customise power usage to application requirements
- **Industry leading 90nm process technology**
  - **1/3** dynamic power reduction vs. existing technologies
  - Intelligent power management controller reduces dynamic and leakage currents
- **Low power design techniques**
  - Clock gating: only leakage currents are incurred
  - Power gating: shuts down un-used modules reducing leakage
- **Ultra fast wake up times**
  - **4µs** wake up from low leakage stop mode
  - New Low Leakage Wake-up Unit for leakage current reduction

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Kinetis Power Modes

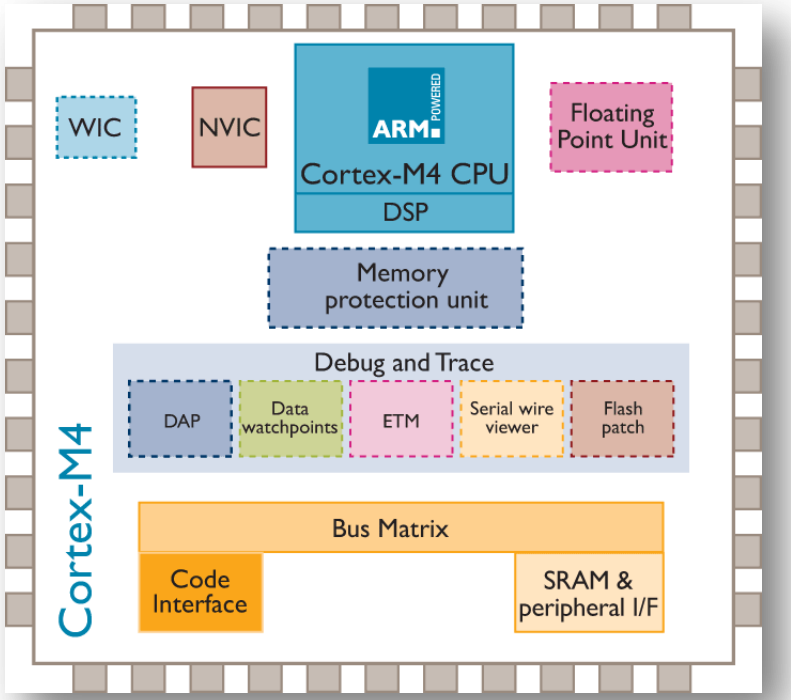
Typical Power Modes in an embedded system	Cortex M4 Power Modes	Kinetis Extended Power Modes	Recovery Time	"Typical" Idd Range
Run	Run	Run	-	Starting @ <200uA/MHz
		VLPR	-	Starting @ <200uA/MHz
Wait	Sleep	Wait	-	
		VLPW	4us	
Stop	DeepSleep	Stop	4us	
		VLPS	4us	
		LLS	4us	1.2uA - 7uA
		VLLS3	35us	1uA - 5uA
		VLLS2	35us	750nA - 2uA
		VLLS1	100us+EE restore	500nA – 1.5uA

Freescale Adds Low Leakage Wake-up Unit

- Enables complete shut-down of core logic, including WIC, further reducing leakage currents in all low power modes
- Supports 16 external input pins and 8 internal modules as wakeup sources
- Wakeup inputs are activated in LLS or VLLS modes

ARM Cortex-M4 Processor Microarchitecture

- **Backwards compatible with ARM Cortex-M3**
- **New features**
  - Single cycle MAC (Up to 32 x 32, with 32-bit result)
  - DSP extensions
  - Single Precision Floating Point Unit
- **Freescale IP and Innovation**
  - On-chip cache for instructions and data
  - Cross-Bar Switch for concurrent multi-master/slave accessing
  - On-chip DMA for CPU off-load
  - Low-leakage Wake-up Unit adds flexibility for low power operation
- **Architected for Digital Signal Processing**
  - **Motor Control** - advanced algorithms, longer lifespan, power efficiency
  - **Automation** - high calculation and algorithm bandwidth at a low cost
  - **Power management** – designed for low/battery powered systems
  - **Audio and Video** – 5x performance improvement over software, making batteries last longer



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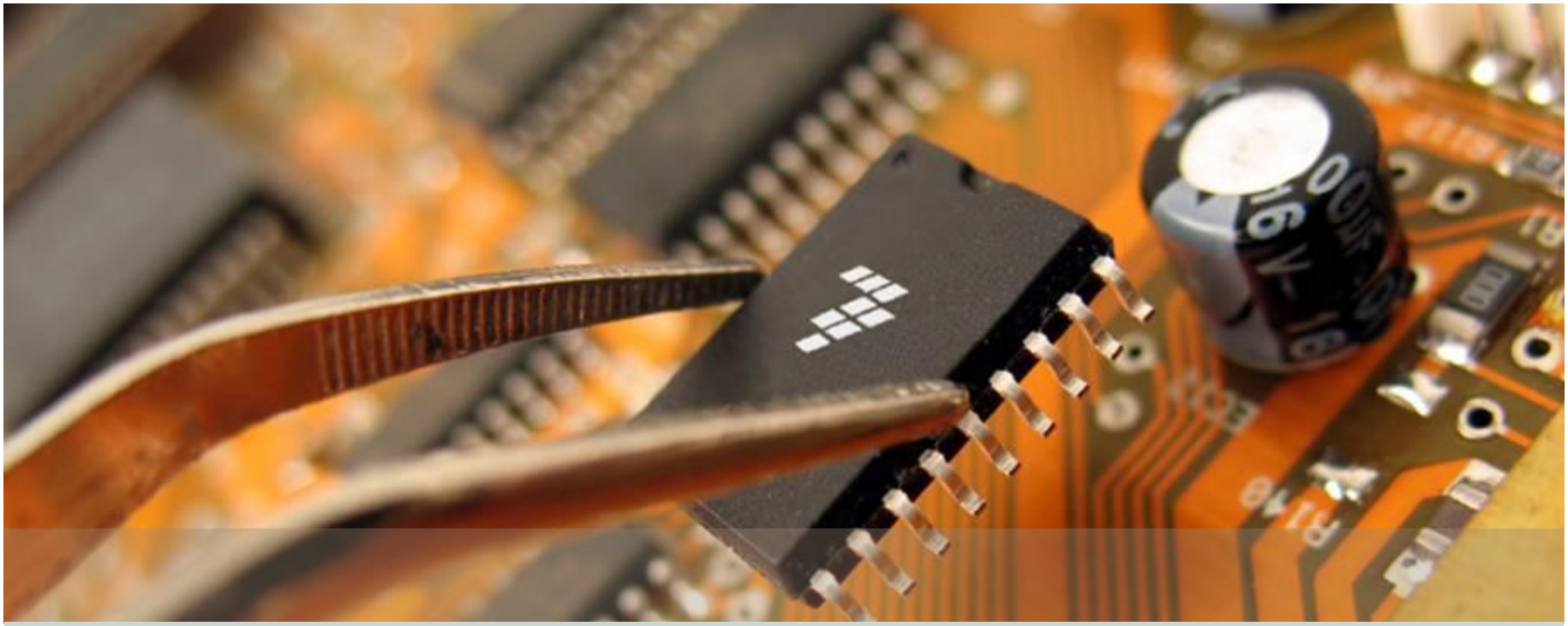

Enablement: Software and Hardware Tools

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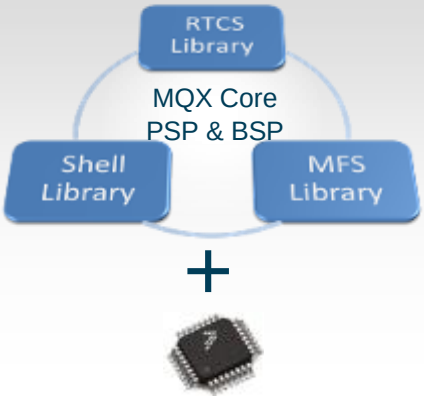
Freescale's Microcontroller Enablement Bundle

Freescale MQX + MCU

Complimentary MQX RTOS



- Full-featured, scalable, proven RTOS
- Simplifies HW management, streamlines SW development
- Reduces development costs while speeding time to market

Comprehensive solution for embedded control and connectivity

+ Tower System

- Modular, expandable and cost-effective development platform for 8/16/32-bit MCUs and MPUs
- Rapid eval and prototyping with maximum HW reuse.
- Supported by a diverse range of MCU and peripheral plug-in boards and a growing web community

Open source hardware platform for prototyping application development

+ CodeWarrior *IDE*

- Eclipse environment
- Processor Expert code generation wizard
- Build, debug and flash tools
- Software analysis
- Kernel-aware debug
- Host platform support

Visual and automated framework to accelerate development time

Save time, cost, and effort.

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Freescale MQX RTOS Solution

- Scalable, fully-featured and proven RTOS bundled with 32-bit MCUs
  - Full-featured and powerful
    - BSPs incorporate tightly integrated RTOS, Middleware (USB, TCP/IP stacks), file system, and I/O drivers
    - Designed for speed and size efficiency
  - Market proven
    - MQX has been available on Freescale processors for > 15 years
    - MQX has been used in millions of products including Medical and Heavy Industrial areas
  - Simple and scalable
    - Can be as small as ~10KB for smallest implementation, or scale up to support sophisticated networking and threading
    - Intuitive API & modular architecture enables straight-forward feature fine-tuning
    - Production source code provided
  - Similar to other "pay-for" software OS

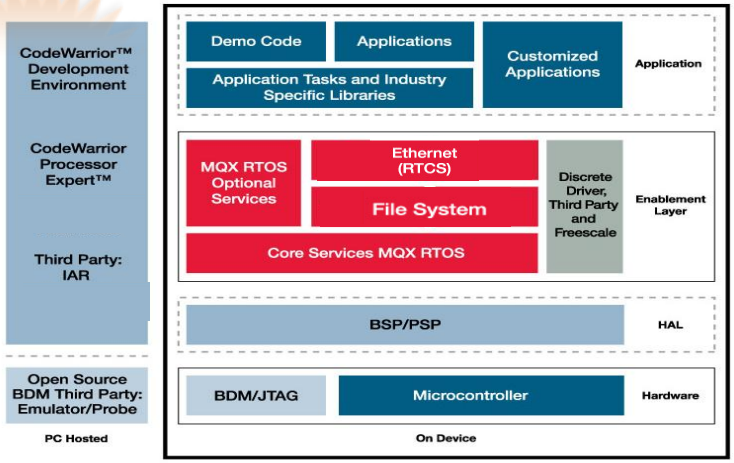
THREADX NUCLEUS Green Hills SOFTWARE INC.

MQX Software speeds time to market with support from Freescale

Software Integration headache

$95,000 of software bundled with Freescale MCUs!

Integrated MQX Solution



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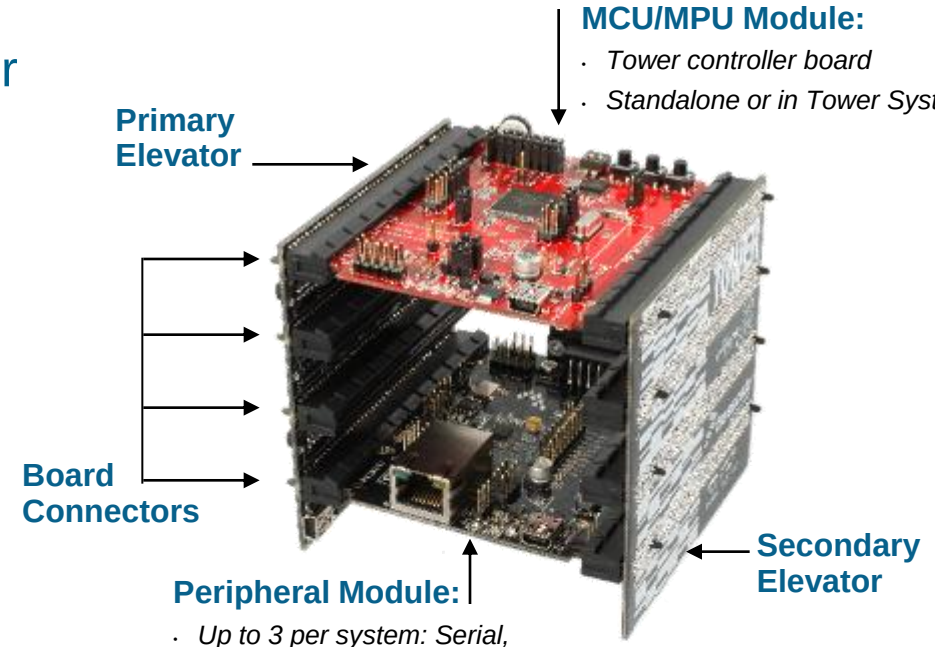
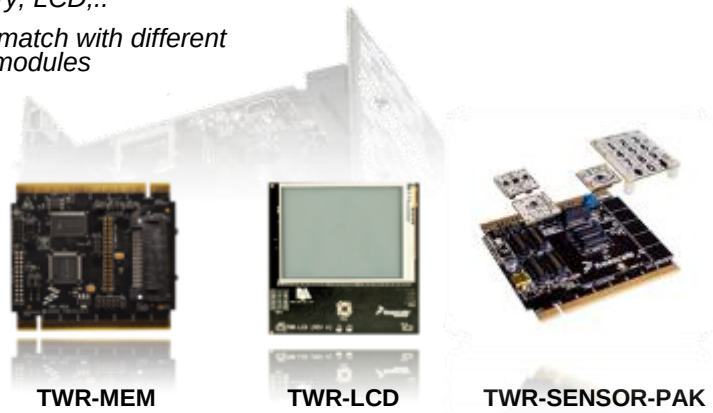
The Freescale Tower System

- A modular development platform for 8/16/32-bit MCUs & MPUs
  - Quickly combine Tower Modules to build a prototype of your application
  - Modules sold individually or in kits
  - Open Source: Build your own Tower Module to integrate your IP
  - Cost-optimized hardware
  - Software support from Freescale and Third Parties
  - Growing community of Third Party hardware support
  - On-line community: www.towergeeks.org



Rapidly build a prototype of your end application

Support for all ColdFire+ and Kinetis MCUs!



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CodeWarrior Development Studio for Microcontrollers v10.1

- **Integrated development tool suite for ColdFire, Kinetis and S08 architectures based on the Eclipse open development platform**
  - Project Wizard creates a new project in as few as 9 clicks
  - MCU Change Wizard retargets a project to a new processor in as few as 6 clicks
  - CodeWarrior optimizing C/C ++ compilers for ColdFire and Kinetis Microcontrollers included
  - Extensions to Eclipse CDT to provide sophisticated features to troubleshoot and repair embedded applications
  - Processor Expert combines easy-to-use component-based application creation with an expert knowledge system
  - Trace and profile support for on-chip trace buffers to provide emulator-like debug capability without additional hardware
  - Kernel-aware debug for MQX, Linux and OSEK
  - CodeWarrior Special Edition is a complimentary version up to 128KB code size

Accelerate the development of the most complex embedded applications

www.freescale.com/codewarrior
to download

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IAR Embedded Workbench

- The most widely used tool chain for ARM MCUs
- A consistent tool chain for ColdFire+ and Kinetis devices
- Completely integrated development environment
- Highly optimized IAR C/C++ Compiler
- Powerful IAR C-SPY Debugger
- MQX integration
- Ready-made example projects

More on www.iar.com/freescale

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Keil Software Development Tools

Microcontroller Development Kit

CMSIS COMPLIANT

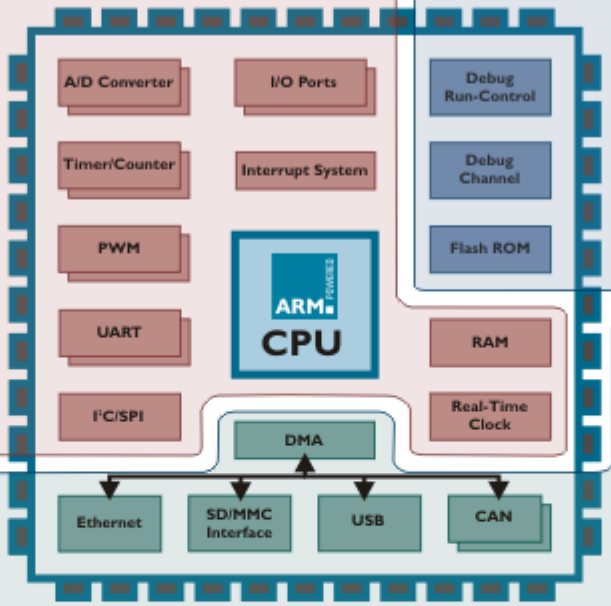
Complete software development environment for Cortex-M and ARM7/9 microcontrollers

Easy to learn and use, yet powerful enough for the most demanding embedded ARM application

MDK-ARM
Microcontroller Development Kit

- ARM C/C++ Compiler
- Royalty-Free RTX RTOS
- µVision Device Database & IDE
- µVision Debugger & Analysis Tools
- Device Peripheral Simulation

Examples and Templates



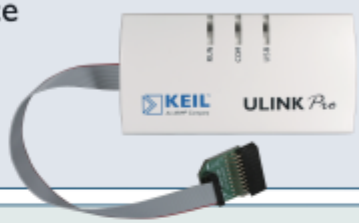
RTX and Real-Time Library

Fully featured real-time kernel

Library of middleware components to speed up software development and solve real-time and communication challenges

ULINK USB Adapters

On-the-fly debugging and Flash programming via JTAG or serial interface



RL-ARM
Real-Time Library

- RTX RTOS Source Code
- TCPnet Networking Suite
- Flash File System
- USB Device Interface
- CAN Interface

Examples and Templates

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Choose Your Partner: The Freescale Microcontroller Ecosystem

Run-Time Software: RTOS, Stacks, File System

Embedded Access Inc
SEGGER
freeRTOS
Green Hills Software, Inc.
µd Micro Digital
IXXAT
Quadros Systems Inc.
freescale semiconductor
expresslogic
Micrium
Mentor Graphics
CMX SYSTEMS
ecos
IAR SYSTEMS
CMSIS COMPLIANT

HW BDM Debugger/Emulators

PE micro

IAR SYSTEMS
SEGGER
RAISONANCE
Rowley Associates
KEIL An ARM® Company





SIGNUM SYSTEMS

IDE: Tools Compliers, Debuggers

CodeWarrior
CodeSourcery
IAR SYSTEMS
KEIL An ARM® Company

GNU Tools
Green Hills Software, Inc.

MQX Support / Design Services

EAI

Audio/Video Codecs

alvaview
AllGo embedded

GUI Graphical

SEGGER
SWELL

Security / Medical

mocana
monebo

EVBs & System Design

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AXIOM

Ind. Protocol Stacks

IXXAT

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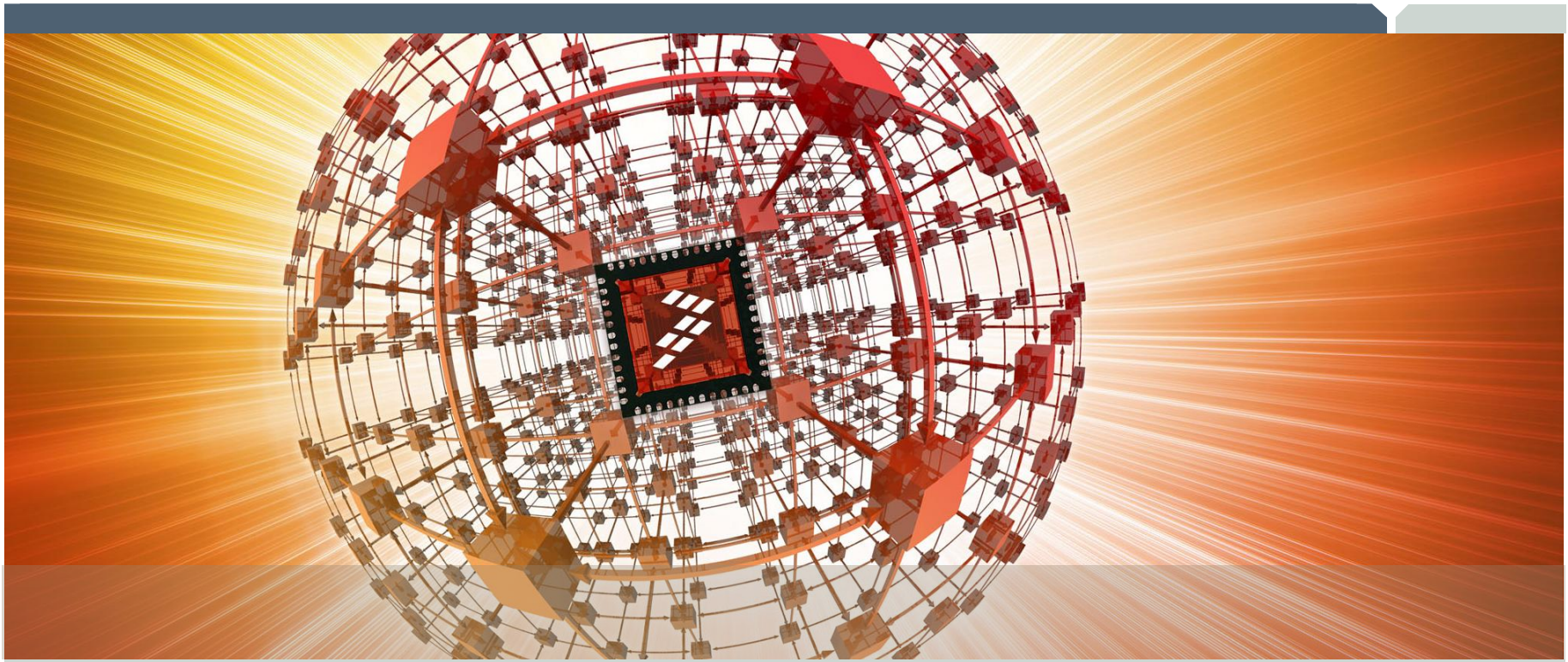

Application Use Cases

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Motor Control Use Case

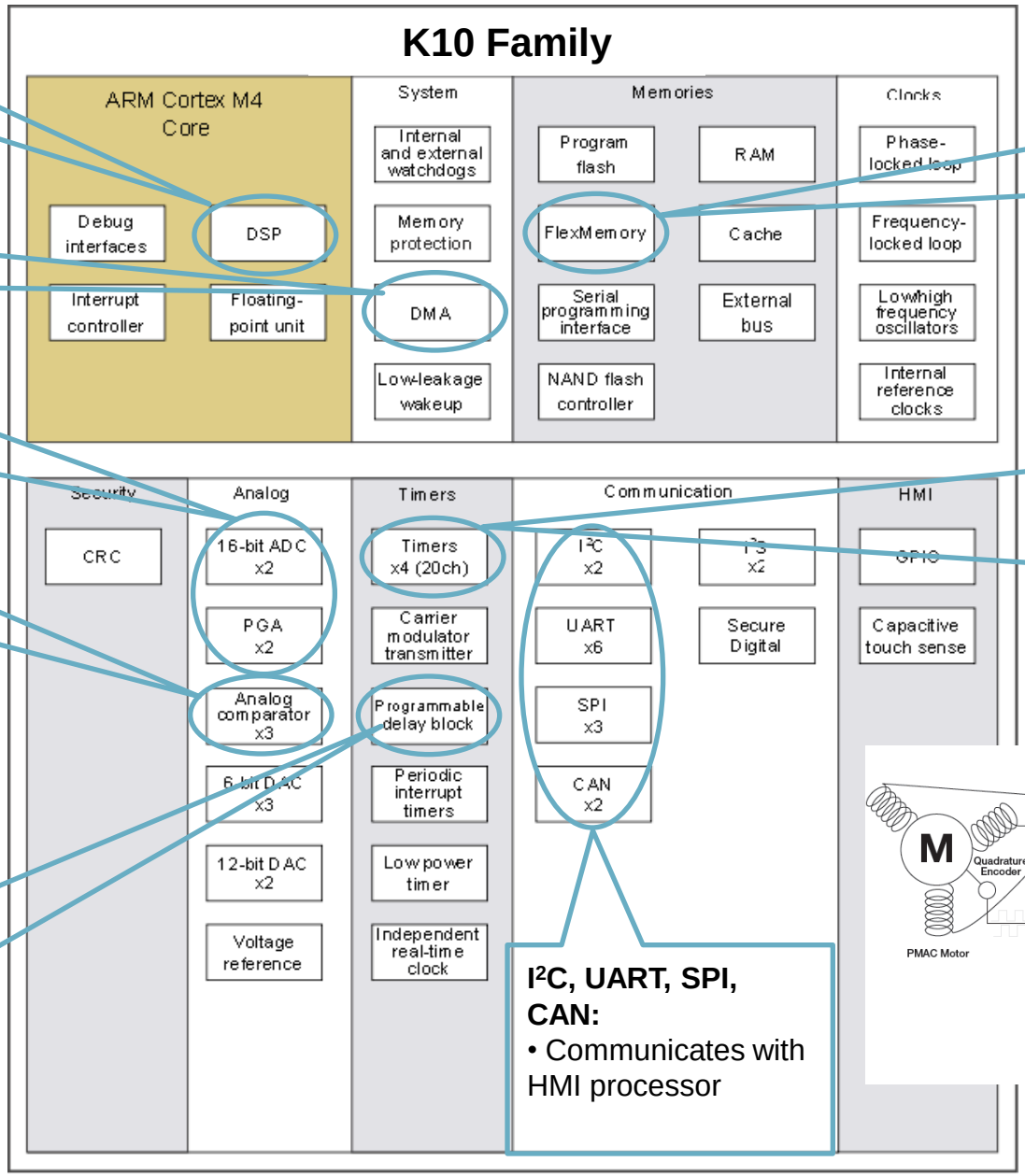
DSP hardware:
► Accelerates motor control calculations

DMA:
► Off loads CPU from repetitive data transfers

16-bit ADC & PGA:
► Measures 3 phase bridge current and voltage

Analog Comparator:
► Detects back EMF
►Monitors over current

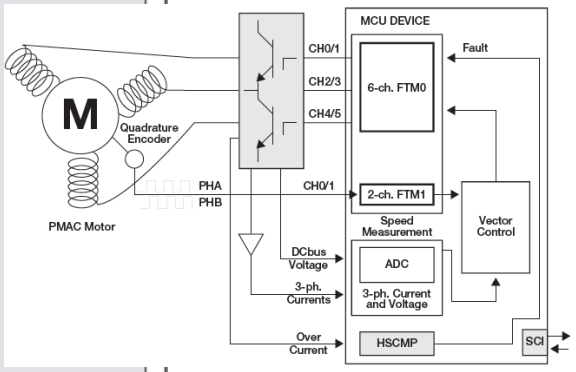
Programmable delay block:
► Schedules delayed ADC conversions relative to Timer triggers



I²C, UART, SPI, CAN:
• Communicates with HMI processor

FlexMemory:
► Saving motor calibration data
• Remote update bootloader

Timers:
► Drives various motor types including stepper, BLDC, and PMAC motors with sensor or sensorless algorithms
► Built-in quadrature decoder detects motor speed



Thermostat Use Case

FlexMemory:
► Saves user defined schedule
► Remote update bootloader
► Stores display menus and graphics
► Logs usage

Low-Leakage Wakeup:
► Deep sleep wakeup controller

16-bit ADC & PGA:
► Samples temperature sensor

Voltage reference:
► Accurate voltage reference for sensor

RTC:
► Clock source with optional independent battery supply

Periodic interrupt timers:
• Periodically triggers ADC conversion on sensor

I²S:
► Audio interface for voice

Capacitive touch sense:
► Keypad buttons
► Wake up source

Segment LCD:
► Drives up to 320 segments of 3V or 5V custom LCD glass
► Conducts segment failure self-test

USB Subsystem:
► Firmware updates

Factory Automation Use Case

Cortex-M4 core with DSP and FPU:
► Signal filtering
►Motor control
►Complex real time control algorithms

Low-Leakage Wakeup:
► Deep sleep wakeup controller

Mixed Signal:
► Sensor monitoring
►Load control
►Voltage and current measurement

System security:
► IP protection
►Communication protection
►Tamper protection

RTC:
► Clock source with optional independent battery supply

FlexMemory:
► Equipment configuration & calibration
► Remote update bootloader

External Bus:
► FPGA for custom logic

NAND flash controller:
► External storage for data logging

Capacitive touch sense:
► Robust keypad
►Robust slider input

Comprehensive Industrial Connectivity:
► 10/100 Ethernet with 1588
►UARTs with RS485 and CAN for legacy protocols
►USB otg
►SPI and I2C for peripheral systems
►SDIO for wireless adaptors

Timers:
► Motor control for up to two BLDC motors
►Signal measurement
►Load control

Universal Remote Control Use Case

FlexMemory:
►Saving user defined settings
►Remote update bootloader
►Stores display menus and graphics

Low-Leakage Wakeup:
►Deep sleep wakeup controller

16-bit ADC:
►Touch screen
►USB Vbus monitoring for smart charger

RTC:
►Clock source with optional independent battery supply

K20 Family

ARM Cortex M4 Core
Debug interfaces
DSP
Interrupt controller
Floating-point unit

System
Internal and external watchdogs
Memory protection
DMA
Low-leakage wakeup

Memories
Program flash
RAM
FlexMemory
Cache
Serial programming interface
External bus
NAND flash controller

Clocks
Phase-locked loop
Frequency-locked loop
Low/high frequency oscillators
Internal reference clocks

Security
CRC

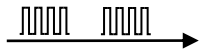
Analog
16-bit ADC x2
PGA x2
Analog comparator x3
6-bit DAC x3
12-bit DAC x2
Voltage reference

Timers
Timers x4 (20ch)
Carrier modulator transmitter
Programmable delay block
Periodic interrupt timers
Low power timer
Independent real-time clock

Communication
I²C x2
I²S x2
UART x6
Secure Digital
SPI x3
USB OTG LS/FS/HS
CAN x2
USB charger detect
USB voltage regulator

HMI
GPIO
Capacitive touch sense

CMT:
• Carrier wave for Infrared



External Bus:
►Smart Display

NAND flash controller:
►External storage for additional graphics

I²C:
►Controls smart charger IC

Capacitive touch sense:
►Keypad buttons
►Wake up source

USB Subsystem:
►Configuration & charging port to host PC
►Detects type of charger and controls battery charger IC
►Firmware updates
►Regulates 3.3V from USB Vbus

Technical Overview

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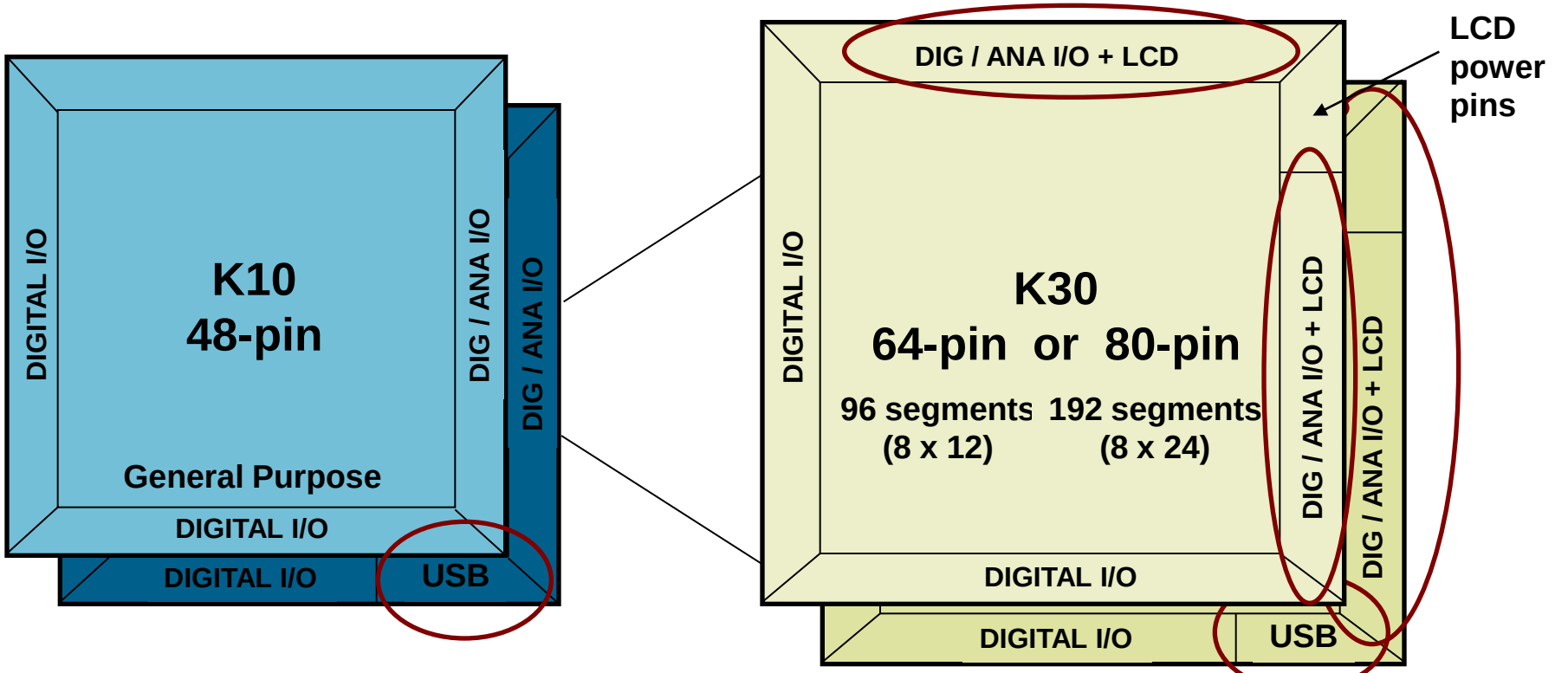
Pin Compatibility Across Families



K10 → K20 & K30 → K40 = Add USB with almost zero changes

- ✓The only difference will be 4 extra USB pins and 4 less digital I/O pins

K10 → K30 & K20 → K40 = Add Segment LCD with minimal board layout changes

- ✓Digital & Analog I/O signals maintain placement order
- ✓Segment LCD signals are muxed with existing Digital & Analog I/O signals
- ✓Most Digital I/O signals muxed with Segment LCD signals become available on added pins by larger package

K20 → K60 = Add Ethernet with NO changes

- ✓All Ethernet signals are muxed with existing Digital & Analog I/O signals

DIGITAL I/O = UART, SPI, I2C, CAN, TIMER, etc.	ANALOG I/O = OSC, ADC, CMP, etc.

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Operating Parameters

Operating Parameters	
Voltage Range (VDD)	1.71 to 3.6 V
	Flash programming across entire voltage range
Temperature Range (TA)	-40 to 105°C
Maximum CPU Frequency Tiers (Max. CPUCLK)	50 MHz
	72 MHz
	100 MHz
	120 MHz
	150 MHz

Package Options

Type	Body Size	Pitch	Families
32-pin QFN	5 x 5 mm	0.5 mm	K10, K20
48-pin QFN	7 x 7 mm	0.5 mm	K10, K20
48-pin LQFP	7 x 7 mm	0.5 mm	K10, K20
64-pin QFN	9 x 9 mm	0.5 mm	K10, K20, K30, K40
64-pin LQFP	10 x 10 mm	0.5 mm	K10, K20, K30, K40
80-pin LQFP	12 x 12 mm	0.5 mm	K10, K20, K30, K40
81-pin MAPBGA	8 x 8 mm	0.65 mm	K10, K20, K30, K40
100-pin LQFP	14 x 14 mm	0.5 mm	K10, K20, K30, K40, K60
104-pin MAPBGA	8 x 8 mm	0.65 mm	K10, K20, K30, K40, K60
144-pin LQFP	20 x 20 mm	0.5 mm	K10, K20, K30, K40, K60
144-pin MAPBGA	13 x 13 mm	1.0 mm	K10, K20, K30, K40, K60
196-pin MAPBGA	15 x 15 mm	1.0 mm	K60
256-pin MAPBGA	17 x 17 mm	1.0 mm	K60

- QFN/LQFP packages optimized for cost reduced 2 layer board designs
- MAPBGA packages optimized for cost reduced 4 layer board designs

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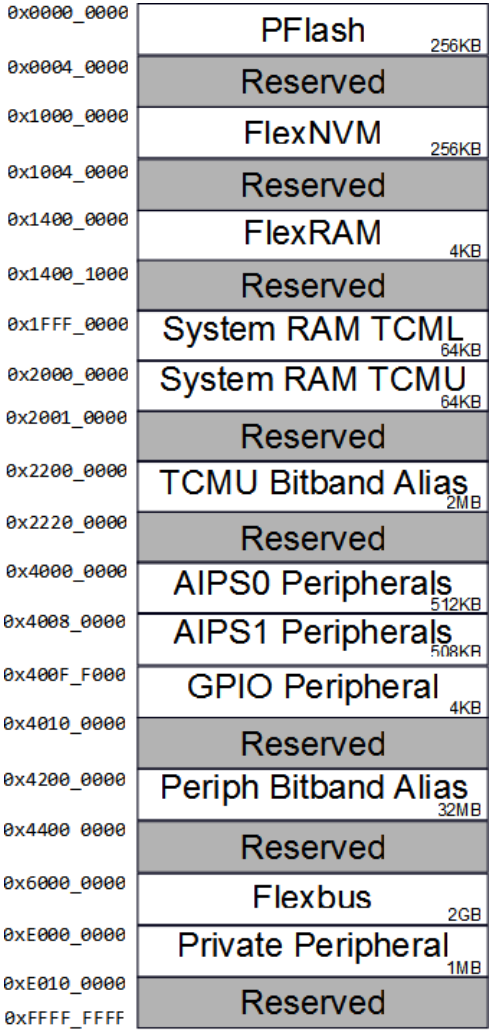
Embedded Memory Options

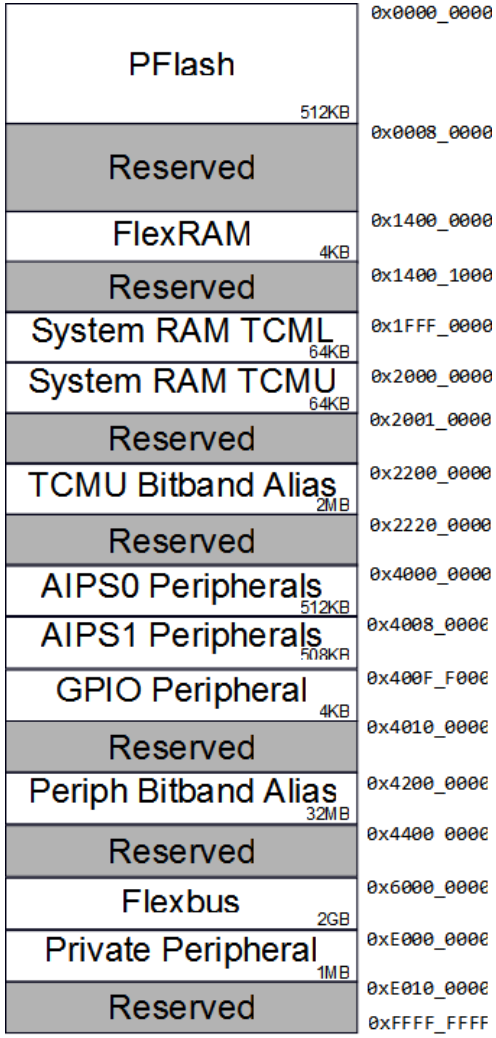
- Multiple flash arrays allowing code execution while non-volatile data or firmware are updated
- Robust update option for seamlessly switching program code execution between flash arrays
- FlexMemory option from 32 KB to 512 KB FlexNVM for additional program and data flash
  - Common uses:
    - Large data tables
    - Protected bootloader
- FlexMemory option for high-endurance, byte-writeable, embedded EEPROM from 32 bytes to 16 KB with up to 10 million read/write cycles
  - Common uses:
    - Saving frequently updated data
    - Protecting critical data during brown out conditions

Memory Map Examples

With FlexMemory



Without FlexMemory



- Identical peripherals and memory maps simplifying code reuse
- Transparent migration between devices with or without FlexMemory to quickly add additional program flash, data flash or EEPROM.

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Flash Security Options

Security State	Description
Unsecured	Debug Access: Full FSL Factory Access: Full
Secured Level I	Debug Access: Mass Erase Only FSL Factory Access: ERSALL, RD1ALL, RDREG, WRREG, and the RAM-only commands
Secured Level II	Debug Access: Mass Erase Only FSL Factory Access: Mass Erase Only
Secured Level III	Debug Access: No Access FSL Factory Access: No Access

Mechanisms for Changing Flash Security State

Mechanism	Description
Backdoor Key	Providing an 8-byte key that is compared with one stored in flash allow the SW to change the security state. Usually the key is provided through an external port.
Debug Access	Through the debug port a Flash mass erase can be performed, clearing the security state.
FSL Factory Access	In secured Level I, NVMBIST mode can only perform a Mass Erase. Other test modes have full access to change all flags, and the entire contents of the NVM memory.

System RAM Memory Map

Tightly Coupled Memory Lower (TCML) SRAM	0x1800_0000–0x1FFF_FFFF
Tightly Coupled Memory Upper (TCMU) SRAM	0x2000_0000–0x200F_FFFF

- SRAM performance for core accesses:
  - Instruction fetch from TCML has zero wait states
  - Instruction fetch from TCMU has one wait state
  - Data fetch from TCML and TCMU have zero wait states

- The on-chip SRAM is implemented with TCML:TCMU ranges forming a contiguous block of memory. TCML is anchored to 0x1FFF_FFFF and occupies the range before this base address. The TCMU is anchored to 0x2000_0000 and occupies the space after this base address.

•SRAM retained in VLLS2 mode starts at TCMU 0x2000_0000

Debug and Trace Options

Debug Interfaces
2-pin Serial Wire Debug (SWD)
4 or 5-pin IEEE 1149.1 Joint Test Access Group (JTAG)
2-pin IEEE 1149.7 Compact JTAG (cJTAG)

Debug & Trace Resources
Trace Port Interface Unit (TPIU)
Flash Patch and Breakpoint (FPB)
Data Watchpoint and Trace (DWT)
Instrumentation Trace Macrocell (ITM)
Embedded Trace Macrocell (ETM)
Embedded Trace Buffer (ETB)

- Use advanced debug & trace features in larger footprint with ETM and ETB and cost reduce in smaller package options

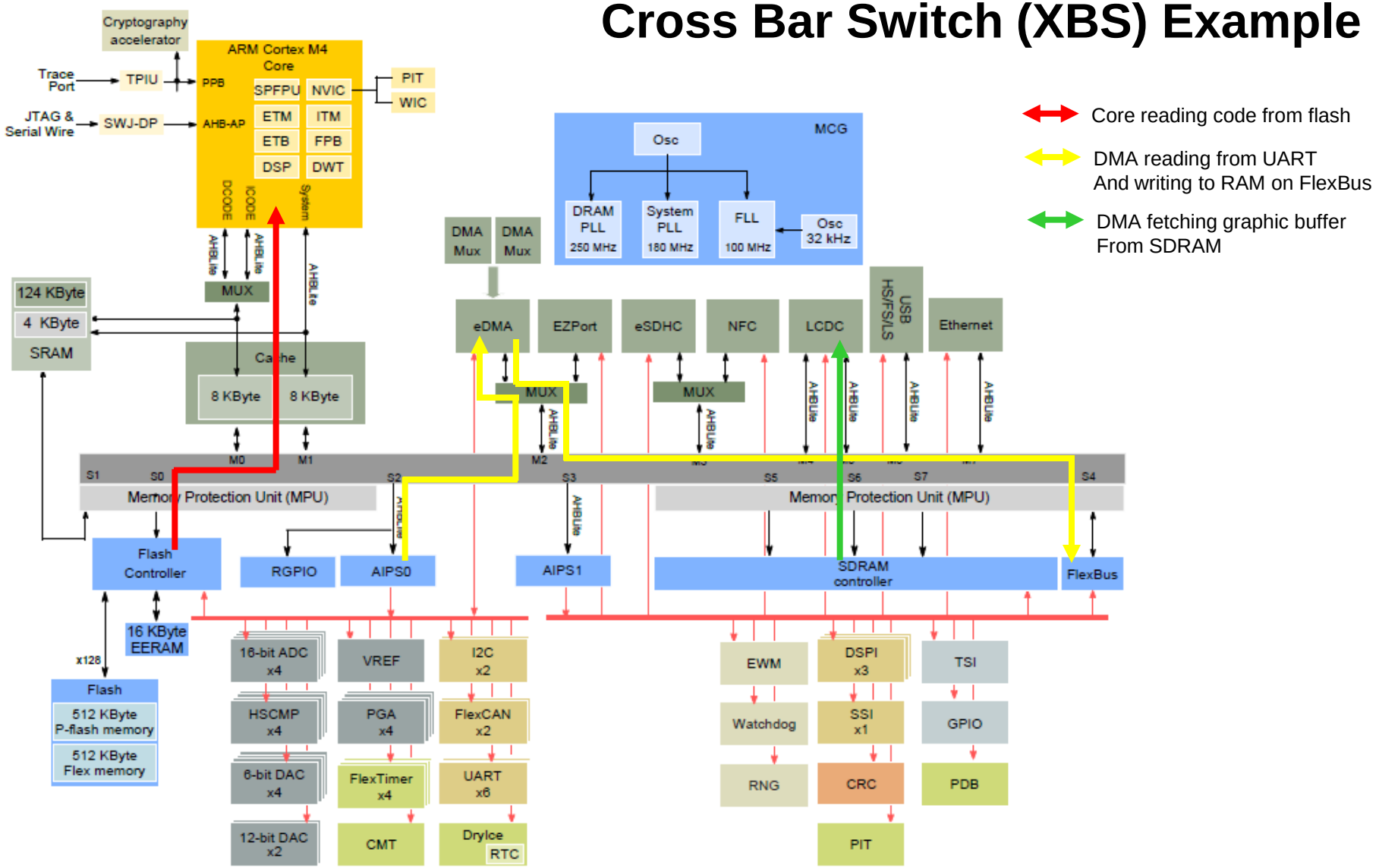
EzPort (EZP) Features

- Serial interface that is compatible with a subset of the SPI format.
- Able to read, erase and program flash memory
  - Supports section program command for most efficient programming
- Able to reset the micro-controller, allowing it to boot from the flash memory after the memory has been configured
- EzPort can be made available on the JTAG header (10-pin or 20-pin)
  - EzPort can program the flash faster than JTAG
  - Using EzPort on JTAG header allows for fast programming option without needing an additional header
  - Will be supported by CodeWarrior tool chain
- EzPort force disable option bit in flash option register
  - User programmable bit that can disable entry into EzPort mode
    - Prevents accidental entry into EzPort mode
    - Extra system security (prevents EzPort from being used as a security exploit)

Cross Bar Switch (XBS) Features

- **Symmetric crossbar bus switch implementation**
- **Allows concurrent, non-blocking accesses from different masters to different slaves**
  - Allowing multiple masters to run bus cycles concurrently increases available system bus bandwidth
- **Up to 8 master ports and 8 slave ports, scalable through parameters and wrapper**
- **32-bit wide and supports byte, word (2 byte), longword (4 byte), and 16 byte burst transfers**
- **Operates at a 1-to-1 clock frequency with the bus masters**
- **Slave arbitration attributes configured on a slave by slave basis**
- **Low-power park mode support**

Cross Bar Switch (XBS) Example



Core reading code from flash

DMA reading from UART
And writing to RAM on FlexBus

DMA fetching graphic buffer
From SDRAM

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DMA Features

16 or 32 channel implementation that performs complex data transfers with minimal CPU intervention

- Number of channels depends on the specific Kinetis device
- Connections to the crossbar switch for bus mastering the data movement

Programmable source and destination addresses and transfer size

- All data movement via dual-address transfers: read from source, write to destination
- Internal data buffer used a temporary storage to support 16-byte burst transfers
- Support for enhanced addressing modes
  - Support for scatter/gather DMA processing
  - Support for complex data structures
- Supports 8-bit, 16-bit, 32-bit, and 16-byte transfer sizes

Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations

- 32-byte TCD stored in local memory for each channel
- An inner data transfer loop defined by a minor byte transfer count
- An outer data transfer loop defined by a major iteration count

Channel activation via one of three methods:

- Explicit software initiation
- Initiation via a channel-to-channel linking mechanism for continuous transfers
- Peripheral-paced hardware requests (one per channel)
- Support for cancelling transfers via hardware or software

Fixed-priority and round-robin channel arbitration

Channel completion reported via optional interrupt requests

- One interrupt per channel, optionally asserted at completion of major iteration count
- Optional error terminations per channel and logically summed together to form
- One error interrupt to the interrupt controller

FSL MPU vs. ARM MPU

Feature	FSL MPU	ARM MPU
Region Descriptors	Up to 16	Up to 8; each with 8 equal sub-regions
Region Sizes	32 byte to 4 GB; allows overlapping protection	32 byte to 4 GB; allows overlapping protection
Access Control Rights	**Up to 8 AHB Master Connections:** • Core Masters: read, write, and execute attributes for supervisor and user accesses • Non-core Masters: read and write attributes	**Core Only:** • Read, write, and execute attributes for supervisor and user accesses
Protected Resources	• TCMU SRAM • TCML SRAM • SRAM via crossbar switch • Flash • FlexBus • DRAM Controller (3 ports) • IPS is protected by AIPS Controller	• TCMU SRAM •SRAM via crossbar switch • FlexBus • DRAM Controller (3 ports) • IPS
Error Reporting Mechanism	• Generates access protection error Multiple error registers (one per slave port) capture the last faulting address, master number, attributes, etc.	• Generates access protection error (MemManage Fault Handler) • Single error registers capture the last faulting address, attributes, etc.

WDOG Features

- **Independent clock source input** (independent from CPU/Bus clock). Choice between two clock sources:
  - 1 KHz Internal Oscillator (external to the WDOG)
  - Bus clock

- **Unlock sequence** for allowing updates to write-once WDOG Control/Configuration bits.

- All **WDOG Control/Configuration bits are writeable once only, within 256 bus clock cycles of being unlocked**.
  - Users need to always update these after unlocking, within 256 bus clock cycles. Failure to update resets the system.

- **Programmable Timeout period,** specified in terms of number of WDOG clock cycles.

- **Ability to test WDOG timer and reset**, with flag indicating watchdog test. This test can be permanently disabled.
  - Quick Test – Small timeout value programmed for quick test.
  - Byte Test – Individual bytes of timer tested one at a time.

WDOG Features

- **Read only Access to WDOG timer**
  - Allows dynamic check that WDOG timer is operational

- **Windowed Refresh Option**
  - Provides robust check that program flow is faster than expected.
  - Programmable window.
  - Refresh outside window leads to reset.

- **Robust refresh mechanism**
  - Write values of 0xA602 and then 0xB480, within 20 bus clock cycles of each other, to WDOG Refresh Register.

- **Count of WDOG resets** as they occur.
  - Configurable **interrupt on timeout** to provide **"debug breadcrumbs".** This is followed by a reset after 256 bus clock cycles.

- **Class B: IEC 60730 compliant** by providing system robustness, diagnostic and self test mechanisms to ensure safe operation of hardware and software in application

EWM Features

- **Independent clock source input** (independent from CPU/Bus clock). Choice between two clock sources:
  - 1 KHz Internal Oscillator (external to the WDOG)

- **Programmable Timeout period,** specified in terms of number of EWM clock cycles.

- **Windowed Refresh Option**
  - Provides robust check that program flow is faster than expected.
  - Programmable window.
  - Refresh outside window leads to EWM_OUT_b pin assertion

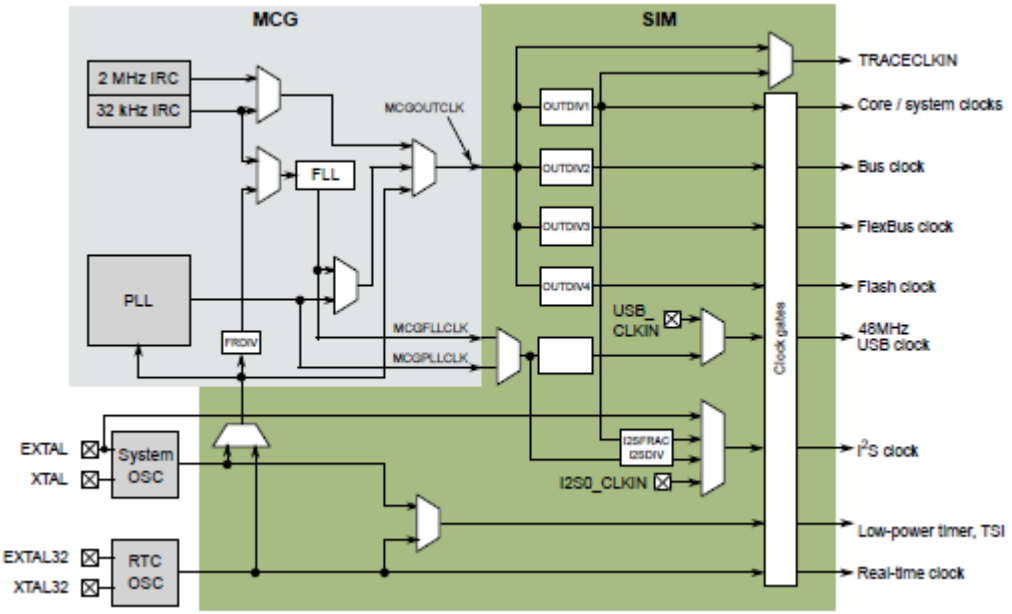
- **Robust refresh mechanism**
  - Write values of 0xB4 and 0x2C to EWM Refresh Register within 15 bus clock cycles of each other, to WDOG Refresh Register.

- **One output pin, EWM_OUT_b**, when asserted is used to reset or place the external circuit into safe mode.

- **One input pin, EWM_IN**, allows an external circuit to control the EWM_OUT_b pin.

High Level Clocking System

- **Two oscillator options**
  - System
    - kHz & MHz range
    - Operates from System power domain
  - RTC
    - kHz range
    - Can be system oscillator
    - Operates from RTC VBAT power domain
- **"On-the-fly" clock dividers with individual clock gating**
  - Core/Platform Clock
  - Peripheral Bus Clock
    - Can operate 1:1 ratio to Core/Platform Clock up to maximum 50 MHz
    - Clock to most peripherals
  - FlexBus Clock
    - Maximum 50 MHz
  - Flash Clock
    - Maximum 25 MHz
  - USB Clock
    - Maximum 48 MHz
    - Fractional clock divider
- **Low power boot option**
  - User non-volatile register bit forces all clock dividers to maximum allowable dividers on system reset or POR for reduced average boot current.



► 1:1 peripheral bus to core/platform clock ratio up to 50 MHz improves peripheral performance while reducing overall power consumption

► Clock gating allows an application unused peripheral clocks to further minimize current consumption

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Oscillator Features

OSC Clock Sources	
External crystal oscillator or resonator	Low Range: 32 – 40 kHz
	Medium Range: 2 - 8 MHz
	High Range: 8 – 32 MHz
External square wave input clock	DC to 50 MHz

- **Multiple crystal oscillator frequencies supported for deriving accurate, low-jitter clocks**
- **Run IEEE 1588 Ethernet and USB simultaneously from 50 MHz clock output from external PHY eliminating need for additional system crystal**

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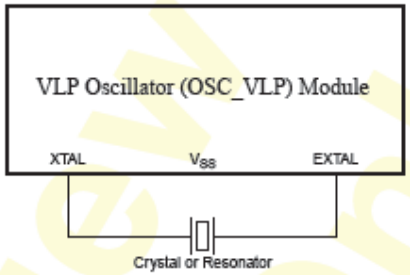
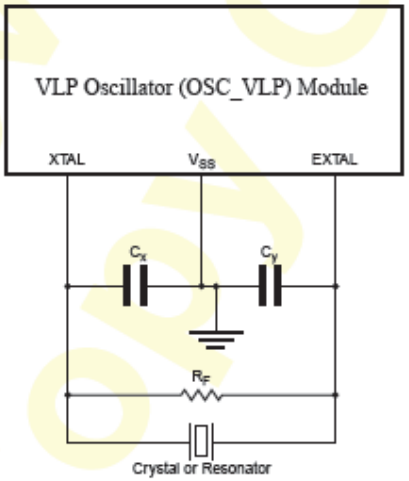
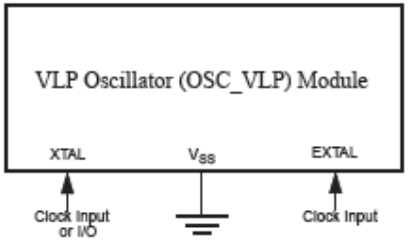
Oscillator Configurations



Configuration for crystal/resonator:
- **Low Frequency, Low Power**





Configuration for external clock

Configuration for crystal/resonator:
- **Low Frequency, High Gain**
- **High Frequency, Low Power**
- **High Frequency, High Gain**

► **Flexible oscillator configuration eliminating external components for cost savings**

► **Options for low power operation and extending battery life operation**

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MCG Flexibility

Internal Reference Clocks
32 kHz oscillator
2 MHz oscillator
1 kHz oscillator (LPO)

Max CPU Frequency Tiers	PLL VCO Ranges
50, 72, and 100 MHz	Up to 100 MHz
120 and 150 MHz	Up to 300 MHz

FLL DCO Ranges		
Frequency Range (DMX32 = 0)		Max Frequency @ 32.768 kHz (DMX32 =1)
Range 0	20 – 25 MHz	24 MHz
Range 1	40 - 50 MHz	48 MHz
Range 2	60 - 75 MHz	72 MHz
Range 3	80 – 100 MHz	96 MHz

► **Increased FLL DCO Ranges and Internal Reference Clock options for fine tuning performance with no external clock components**

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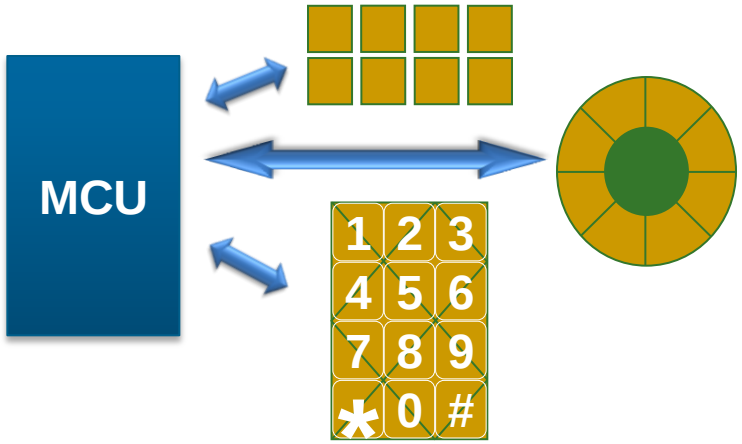
GPIO

- **5V tolerant pins on some devices**
  - Use open drain connections to interface to other 5V devices
- **Pin interrupt and DMA capability**
  - Rising/Falling edges and both edge and level
  - Each 32 pin port can generate an interrupt or DMA request
- **Digital glitch filter**
  - Spurious noise filter
  - Configurable width and clock source
- **Hysteresis and configurable pull up/pull down device on all input pins**
- **Configurable slew rate and drive strength on all output pins**
  - Reduced noise on output pins

Hardware Touch-Sensing Interface (TSI)

- **Capacitive touch sensing detection across all low power modes**
  - Automatic periodic scan with configurable duty cycle
  - Low power mode current adder can be <1uA
- **16 input capacitive touch sensing pins**
  - Each with individual result registers
  - Automatic detection of Electrode Capacitance Change with programmable upper and lower threshold
  - No need for external components
- **TSI interrupts**
  - End of Scan, Out of Range, pad short or conversion overrun



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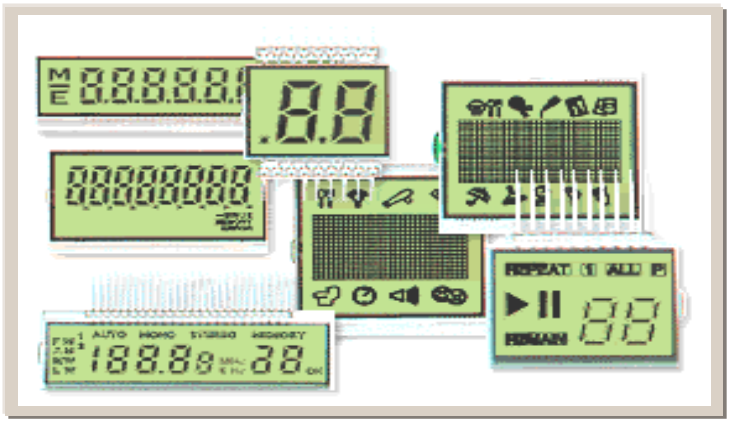
Segment LCD Controller



▶ Segment fault detection capability

- Hardware support for segment LCD display errors

▶ Up to by 8 multiplexing

- Fewer pins required to drive LCD segments

▶ Low power blinking mode

- LCD glass blink capability in low power modes
- Alternate display feature can be activated to display alternate data (i.e. blink temperature and time

▶ Front and back plane re-assignment

- Any LCD pin can be a frontplane or backplane pin or GPIO function

▶ Internal charge pump provides voltage required to power LCD glass

- Internally regulated voltage for constant contrast across MCU VDD
- Trim register for software contrast control
- Drive for 3V or 5V LCD glass

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Graphics LCD (GLCD) Controller

- Same IP as in the i.MX25x family
- Interface to passive and active color panel (TFT)
- Supports up to 8-bit QVGA displays using on-chip memory for frame buffer
- Hardware-generated cursor with blink, color, and size programmability
- Graphic window support for viewfinder function in color display
- 256 transparency levels for alpha blending between graphic window and background plane

FlexTimer (FTM) Features

- Up to 4 FTM modules on Kinetis. FTM0 & FTM3 = 8 channels; FTM1 & FTM2 = 2 channels with quadrature decode
- 16-bit counter with prescaler divide-by 1,2,4,8,16,32,64, or 128
- Each channel can be configured for input capture, output compare, edge-aligned PWM mode, or center-aligned PWM mode
- Each pair of channels can be combined to generate a PWM signal with independent control of both edges of PWM signal
- Each pair can operate as complementary outputs with dead time insertion
- Dual edge capture for pulse and period width measurement
- Quadrature decoder with input filters for relative position counting
- Global Time Base mode shares single time base across multiple FTM instances

SRTC & DryICE Features

Secure Real Time Clock
- On-chip, battery powered real-time clock
- Monotonic counter

Secure Key Storage
- Instantly erased if tamper is detected

Independent power supply (1.71V to 3.6V)

Programmable alarm with interrupt

Hardware compensated clock

Comprehensive Tamper Detection
- Temperature
- Clock
- Supply Voltage
- External tamper inputs

Tamper Sources

- Internal Tamper Detect sources:
  - Seconds Counter overflow
  - Atomic Counter overflow
  - Flash Not Secure
  - Tamper Interrupt Timeout
  - Analog tamper sources
    - Clock monitor
    - High voltage detect
    - High/Low temperature detect
- External Tamper Detect sources:
  - 4 Passive & 2 Active
  - Each external tamper detect has a glitch filter
    - Configurable width from asynchronous to ~250 ms
    - Configurable polarity per pin
    - Pull-up/down enabled so that unconnected pin asserts tamper detect
    - Glitch Filter configured independently for each tamper input

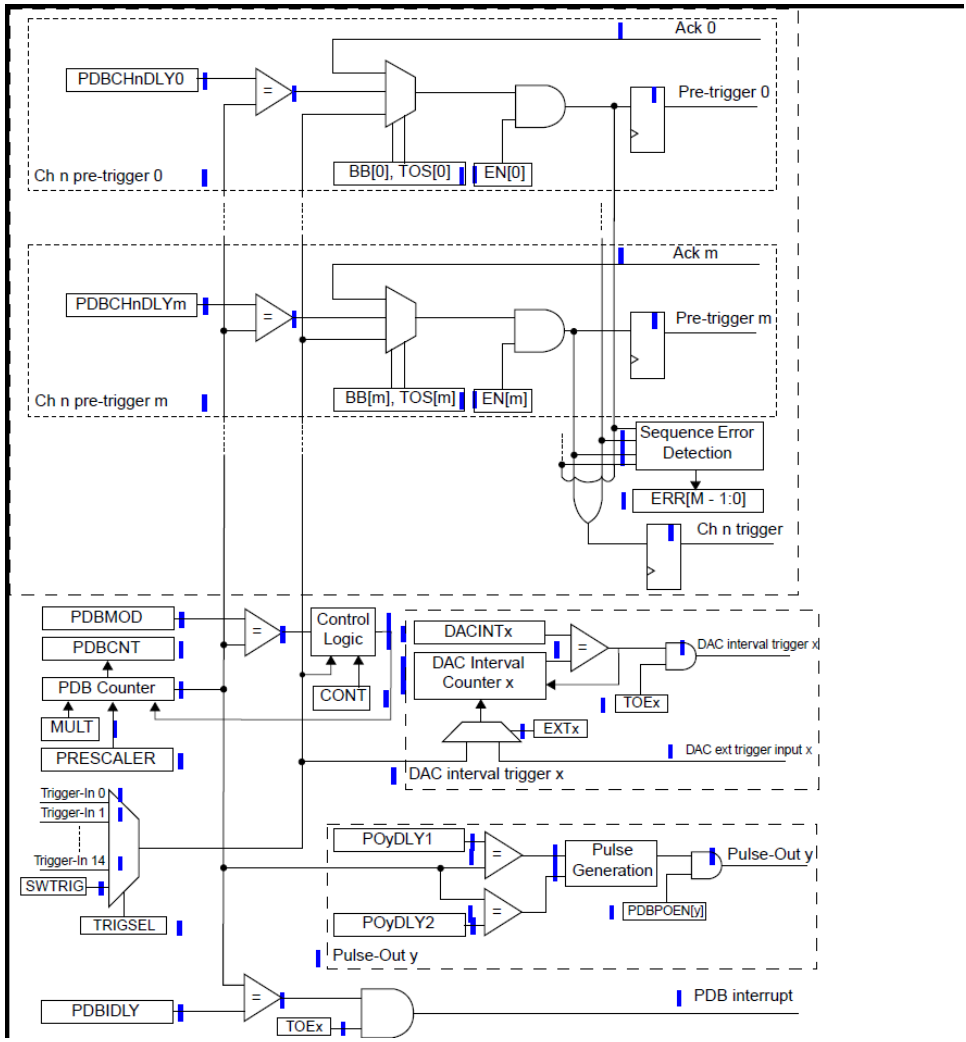
Low Power Timer (LPTMR) Features

- **Selectable clock for prescaler/glitch filter**
  - — 1 kHz internal LPO
  - — 32.768 kHz external crystal
  - — Internal Reference Clock (not usable in low leakage modes)
- **Configurable Glitch Filter or Prescaler with 15-bit counter • 16-bit Time or Pulse Counter with Compare**
- **Interrupt generated on Timer Compare**
- **Hardware trigger generated on Timer Compare (not usable in low leakage modes)**
- **Can be used in conjunction with the HSCMP to count comparator output pulses**

Programmable Delay Block (PDB)

Features

- Provides controllable delays from either internal or external triggers
- Up to 15 trigger input sources and software trigger source
- Up to 8 configurable PDB channels for ADC hardware trigger
- Up to 8 DAC interval triggers
- Supports pulse outputs use as the sample window in CMP



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USB Controllers

Full/Low-speed

- **USB 1.1 and 2.0 compliant host, device and on-the-go (OTG) controller**
  - Supports Full-speed (12 Mbps) and low-speed (1.5 Mbps)
- **16 Bi-directional end points**
- **Paired with on-chip full/low-speed transceiver**
- **Built-in host mode pull down resistors**

High/Full/Low-speed

- **Complies with USB2.0, supports host, device and OTG**
  - Supports High-speed (480 Mbps), Full-speed (12 Mbps) and low-speed host (1.5 Mbps)
  - On-chip transceiver supports full/low-speed modes
  - External transceiver via ULPI interface needed for high-speed modes
  - Allows direct connection of full-speed (FS) or low-speed (LS) devices without an OHCI/UHCI companion controller
- **Defined as any USB class or device for targeted peripheral list, incl. hubs**
- **Suspend/low power mode**
  - Can suspend individual devices or the entire USB subsystem
  - Remote wake-up integrated with processor's low power modes

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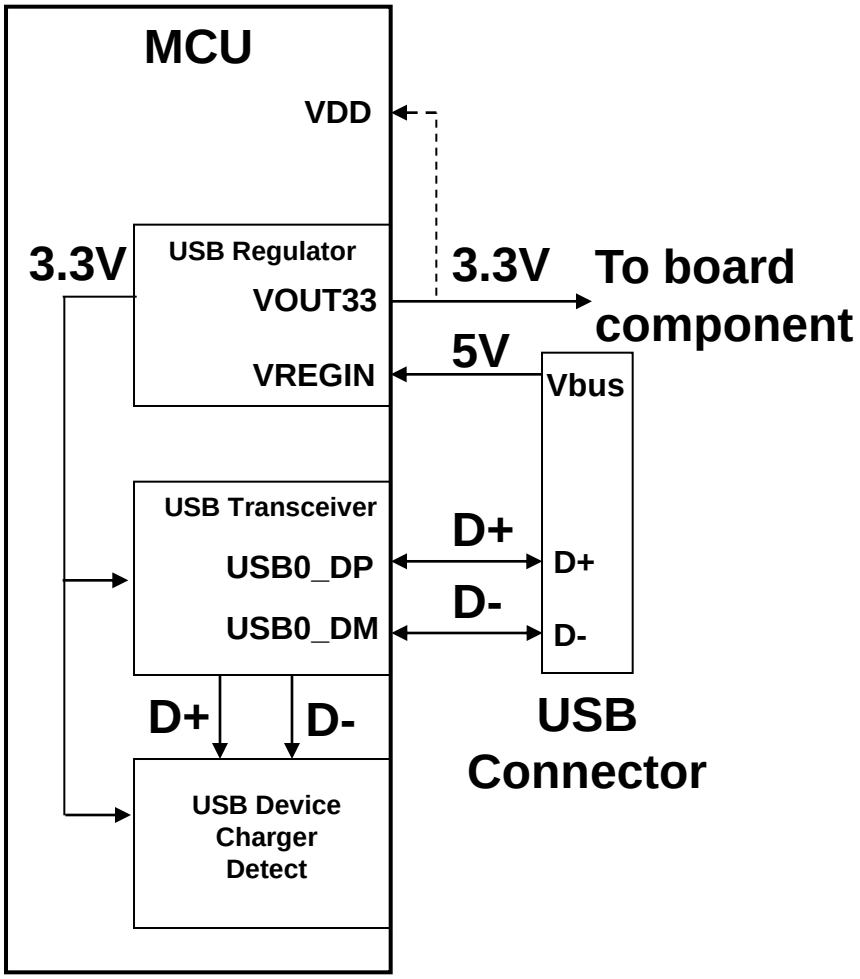
USB Regulator

- 5V regulator input (VREGIN) typically provided by USB Vbus or Rechargeable Battery power
- 3.3V regulated output powers on-chip USB transceiver and device charger detect
- Output pin (VOUT33) from regulator can be used to power external board components and source up to 120mA
- Eliminates cost of external LDO
- 3.3V regulated output can power MCU main power supply



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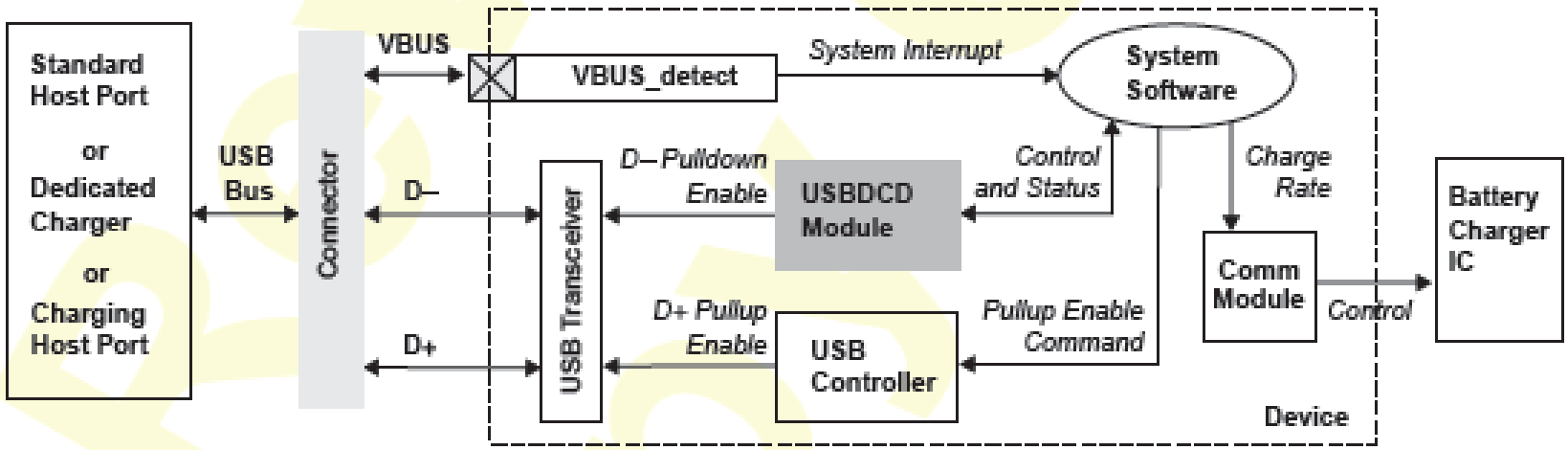
USB Device Charger Detect

- Compliant with the latest industry standard specification: *USB Battery Charging Specification, Revision 1.1*
- Compatible with systems powered from:
  - rechargeable battery
  - non-rechargeable battery
  - external 3.3v LDO regulator powered from USB
  - directly from USB using internal regulator

Charger	Maximum Current Drawn[1]
Standard host port	up to 500 mA
Charging host port	up to 1500 mA
Dedicated charging port	up to 1800 mA



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IEEE 1588 Ethernet Controller

- **Implements the full 802.3 specification**
  - Dynamically configurable to support 10/100 Mbps operation
  - Supports full duplex (w/flow control) and configurable half duplex operation
  - Support for VLAN-tagged frames according to IEEE 802.1Q
- **Supports AMD magic packet detection with interrupt for node remote power management**
- **Seamless interface to commercial Fast Ethernet PHYs**
  - Supports MII and RMII interfaces
  - MDIO master interface for PHY device configuration and management
- **Programmable MAC address: discards frames with mismatching destination address on receive (except broadcast and pause frames)**
- **Hardware time stamping support for IEEE 1588 provides precision clock synchronization for real-time control**

SSI Features

- **Full duplex serial port that allows communication with a variety of serial devices:**
  - Audio codecs that implement the inter-IC sound bus (I2S)
  - Standard codecs
  - Digital signal processors (DSPs)
  - Microprocessors
  - Peripherals
  - AC97 support
- **Independent (asynchronous) or shared (synchronous) transmit and receive sections with separate or shared internal/external clocks and frame syncs, operating in Master or Slave mode**
  - Completely separate clock and frame sync selections for the receive and transmit sections. In the AC97 standard, the clock is taken from an external source and frame sync is generated internally
- **Supports several synchronous operating modes:**
  - Normal mode operation using frame sync
  - Network mode operation allowing multiple devices to share the port with as many as thirty-two time slots
  - Gated clock mode operation requiring no frame sync
  - Programmable data interface modes such as I2S, lsb- and msb-aligned
- **2 sets of Transmit and Receive FIFOs**
  - Each of the four FIFOs is 15x32 bits
  - Can be used in Network mode to provide 2 independent channels for transmission and reception
- **Programmable word length (8, 10, 12, 16, 18, 20, 22 or 24 bits)**
- **Program options for frame sync and clock generation**
- **Programmable I2S modes (master, slave or normal). Oversampling clock (ccm_ssi_clk) available as output from SRCK in I2S master mode**
- **Option to use internal system clock as or an external input clock**

UART Instantiation on Kinetis

SCI Instance	Features	Maximum Baud Rate
UART0	Higher Baud Rates (CPUCLK @ 100 MHz) ISO-7816 8 TX and 8 RX FIFOs	6.25 Mbits/sec
UART1	Higher Baud Rates (CPUCLK @ 100 MHz) 8 TX and 8 RX FIFOs	6.25 Mbits/sec
UART2-UART5	Normal Baud Rates (BUSCLK @ 50 MHz) 1 TX and 1 RX FIFO	3.13 Mbits/sec

SCI baud rate = SCI module clock / (16 * (SBR[12:0] + BRFD)

UART

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 13-bit baud rate selection with /32 fractional divide, based on module clock frequency
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver with programmable input/output polarity

UART (continued)

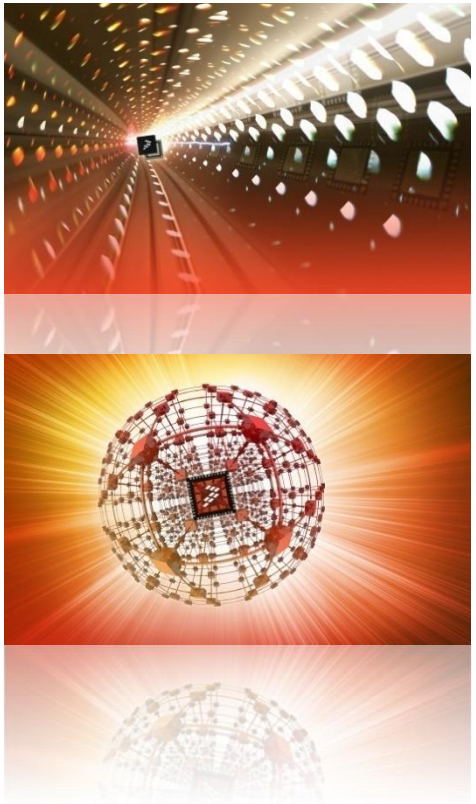
- 13-bit break character option
- 11-bit break character detection option
- Independent FIFO structure for transmit and receive
- Multi-drop support: address match feature in receiver to reduce address mark wakeup ISR overhead
- Ability to select MSB or LSB to be first bit on wire
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Support for ISO-7816 protocol for interfacing with smartcards

SPI Features

- **Serial Peripheral Interface bus:**
  - Full-duplex, three-wire synchronous transfers
  - Master and slave modes
  - Maximum master mode frequency is CPU freq/4 (ex. 100MHz/4 = 25MHz)
  - Maximum slave mode frequency is CPU freq/8 (ex. 100MHz/8 = 12.5MHz)
- **Buffered transmit and receive operation with 4 entry Rx and Tx FIFOs**
- **Programmable transfer attributes on a per-frame basis:**
  - Parameterized number of transfer attribute registers (from two to six depending on device and particular SPI instantiation)
  - Serial clock with programmable polarity and phase
  - Various programmable delays
  - Programmable transfer size of 4 to 16 bits
  - Continuously held chip select capability (for the length of the FIFO)
- **Up to 6 Peripheral Chip Selects, expandable with an external demultiplexer**
  - Exact number of chip selects depend on device and particular SPI instantiation (different SPIs on same device can have different number of chip selects)
- **DMA support for adding entries to TX FIFO and removing entries from RX FIFO:**
- **Modified SPI transfer formats for communication with slower peripheral devices**

Building the Industry's **Most Trusted MCU Solutions**

- Freescale offers leadership in the 32-bit MCU space
  1. 200 scalable devices from 32KB to 1MB of flash and up to 150MHz performance
  2. FlexMemory enables on-chip EEPROM
  3. Incredible mixed-signal integration
  4. Low-power capability
  5. Complete enablement
     - Complimentary MQX RTOS
     - Complimentary CodeWarrior IDE
     - Tower system for rapid prototyping
- **Kinetis by Freescale is the clear choice for your MCU needs**



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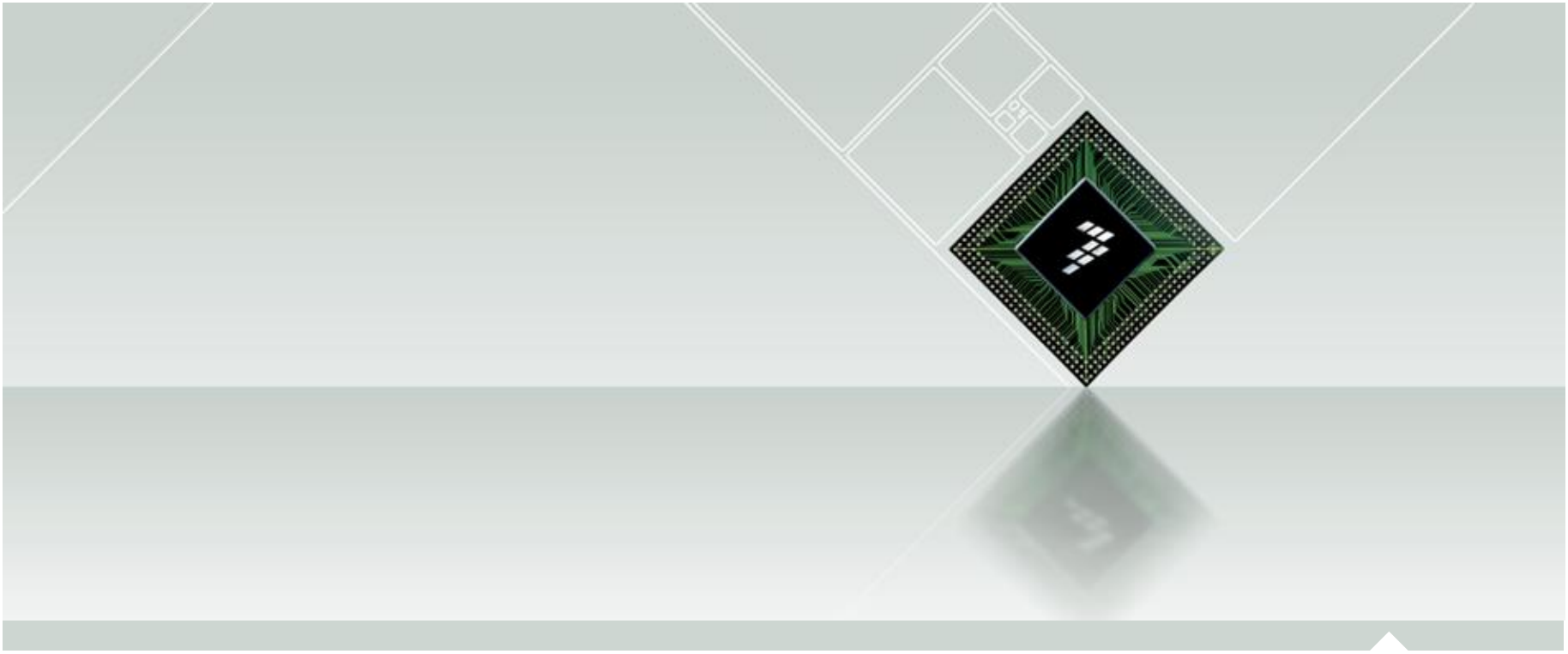

BACK-UP

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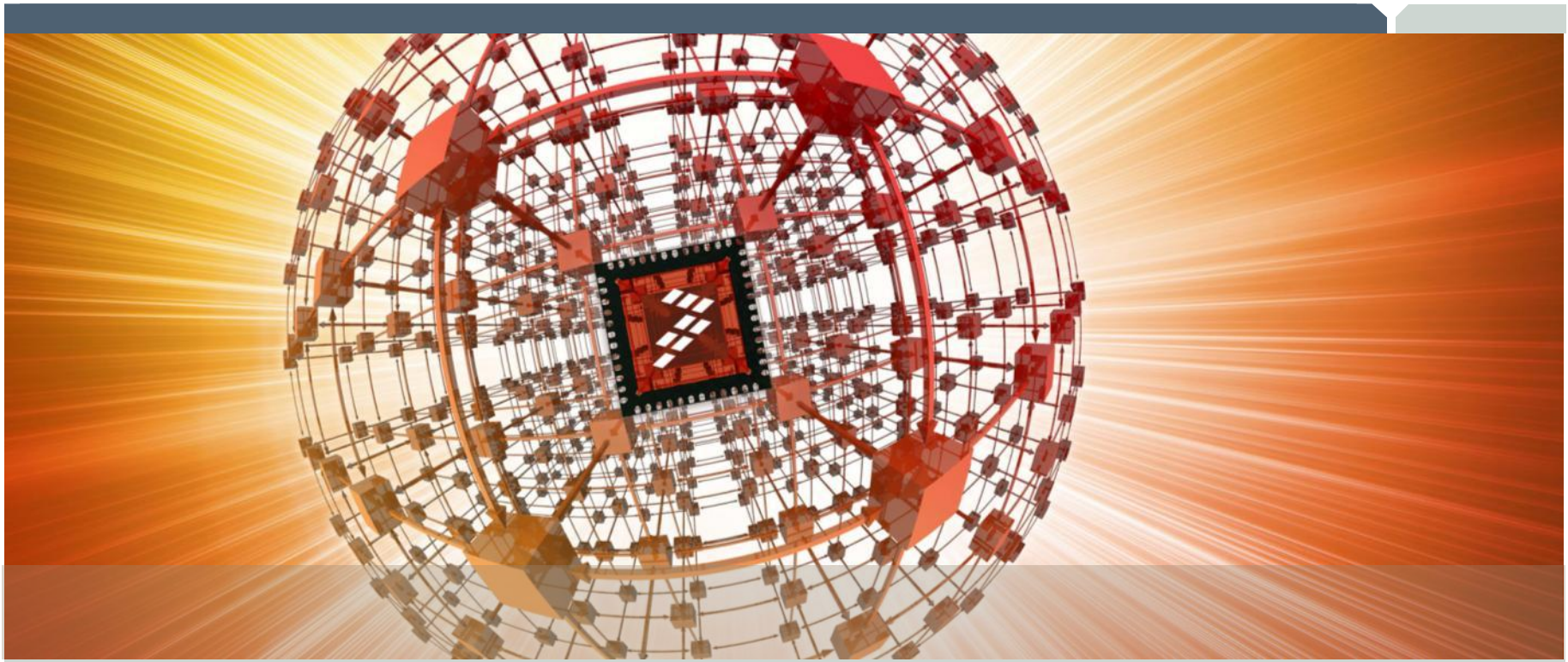

Get to Know your Tower System

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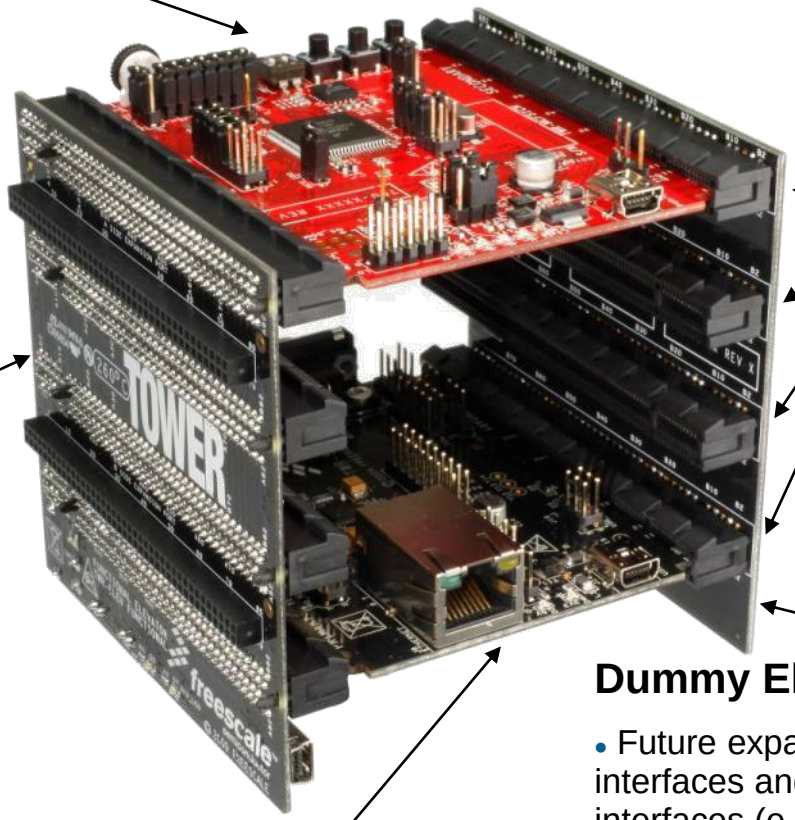
The Tower System

Processor Module:

- Tower controller board
- Works stand-alone or in Tower system
- Features new Open Source BDM (OSBDM) for easy programming and debugging via miniB USB cable



Size: The Tower is approx. 3.5” H x 3.5” W x 3.5” D when fully assembled

Board Connectors:

- Four card-edge connectors
- Uses PCI Express connectors (x16, 90mm/3.5” long, 164 pins)

Functional Elevator:

- Common serial and expansion bus signals
- Two 2x80 connectors on backside for easy signal access and side-mounting board (e.g. LCD module)
- Power regulation circuitry
- Standardized signal assignments (e.g. UART, SPI, Timers, External Bus, I2C, CAN, GPIO, Ethernet, USB, etc.)

Peripheral Module:

Standard peripheral boards compatible with all controller boards (e.g. Serial, Memory, etc.)

Dummy Elevator:

- Future expansion for more serial interfaces and more complex MPU interfaces (e.g. RGB LCD, segment LCD, audio, enhanced Timer, etc.)
- “Dummy” shown with only GND connectivity. Used for structural integrity

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Get to Know the TWR-K60N512 (front)

Figure 1: Front side of TWR-K60N512 Module not including TWRPI.

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Get to Know the TWR-K60N512 (back)

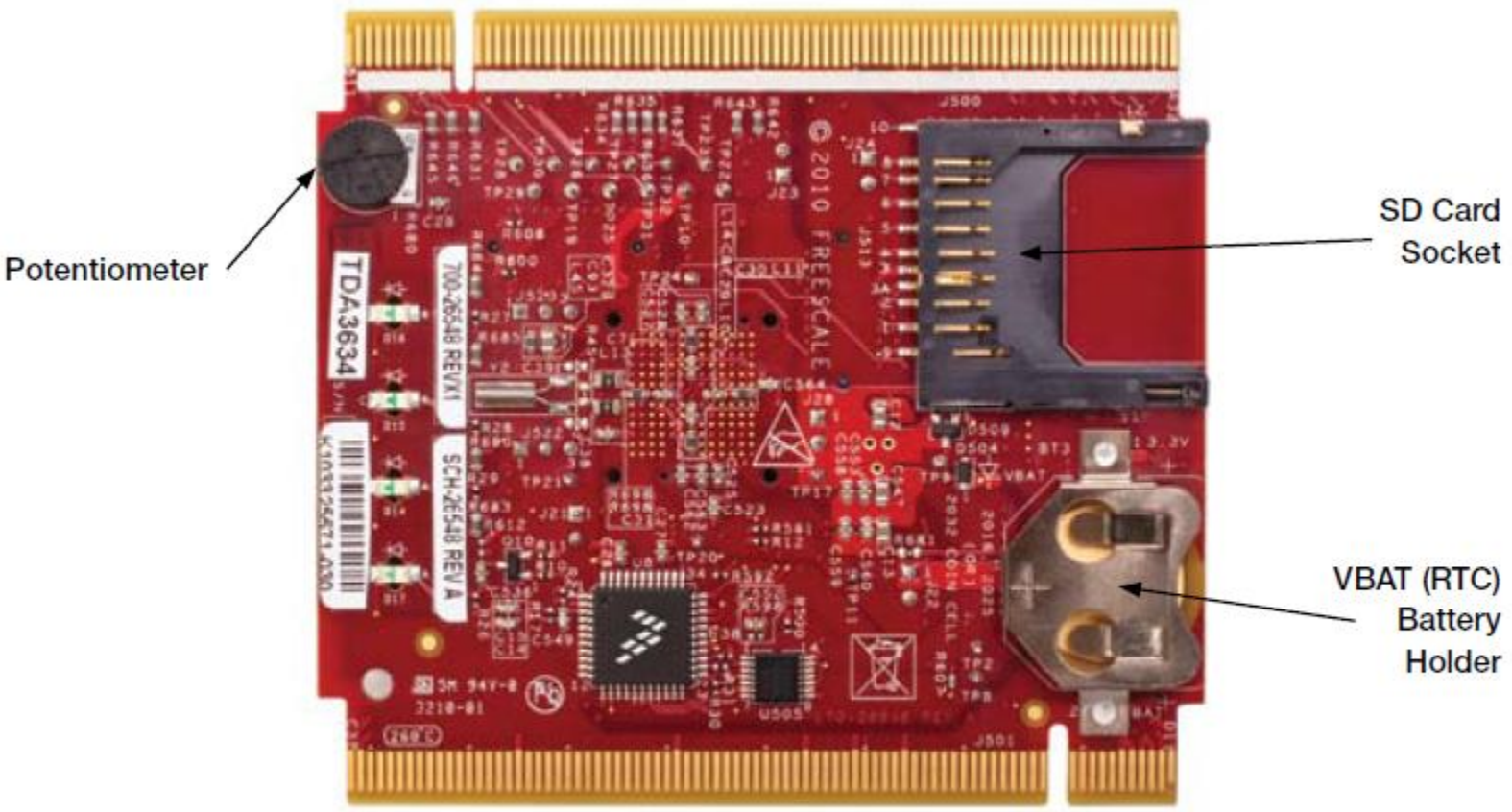

Figure 2: Back side of TWR-K60N512 Module.

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Get to Know the TWR-K40X256 (front)

Figure 1: Front side of TWR-K40X256 Module not including TWRPI.

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Get to Know the TWR-K40X256 (back)

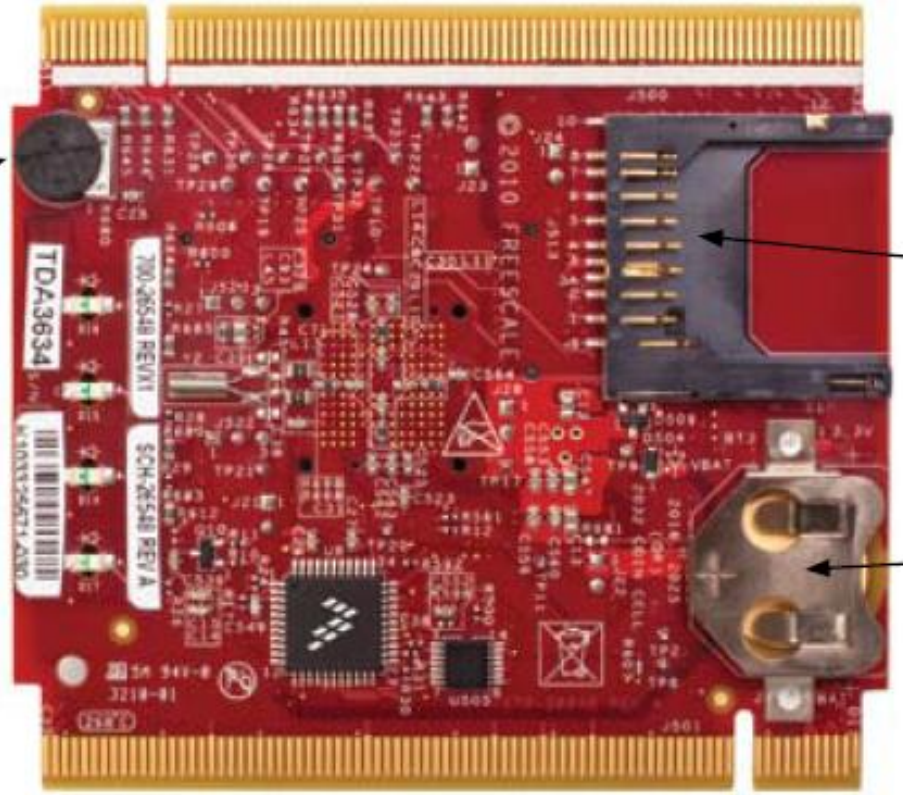

Figure 3: Back side of TWR-K40X256 Module.

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TWR-K40X256 with TWRPI-SLCD

Figure 2: Front side of TWR-K40X256 Module with TWRPI-SLCD attached.

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Available Tower System Modules

www.freescale.com/tower

Processor Modules ($39-$119)

TWR-MCF51CN

TWR-MCF5225X

TWR-S08LL64

TWR-MPC5125

TWR-MCF51MM
TWR-S08MM128
TWR-MCF51JE-KIT

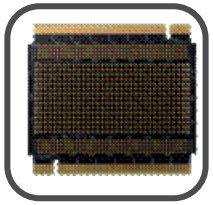
New

TWR-K60N512
TWR-K40X256
TWR-MCF5441X
TWR-MCF51AG
TWR-56F8257

Coming Soon

Peripheral Modules ($15 – $149)

TWR-SER



TWR-PROTO

TWR-ELEV

TWR-MEM

TWR-SENSOR-PAK

TWR-LCD

New

MED-EKG

Coming Soon

New
Wi-Fi 802.11n

TWR-WIFI-RS2101
Sept 20

Wi-Fi 802.11b

TWR-WIFI-G1011MI
Oct 21

Analog Digital Converter

TWR-ADCDAC-LTC
Jan 2011

Dual Ethernet & High-speed USB

TWR-SER2
Sept 27

Audio

TWR-AUDIO
Q4 2010

Industrial Ethernet Module
PISMO Memory Expansion
Home Plug Powerline Comm
Motor Control

Under Development

REDPINE SIGNALS

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Peripheral Module: TWR-SER Serial Module

TWR-SER

Add Serial connectivity to your design

Features:

- RS232 and RS485
- Ethernet
- CAN
- USB

Resale:

TWR-SER = $29

www.freescale.com/tower

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Peripheral Module: TWR-WIFI-RS2101 802.11n Wi-Fi Module

TWR-WIFI-RS2101

Features:

- RS9110-N-11-21 Wi-Fi® module from Redpine Signals
- Compliant to 802.11b/g and single stream 802.11n
- Supports all Wi-Fi client security protocols (WEP, WPA and WPA2)
- Reference design certified for FCC/IC/CE
- RoHS compliant
- Does not require any WLAN driver on the host processor
- Interfaces to MCU via SPI, UART
- Terminates SLIP connections and offers transparent serial modem functionality
- Integrated antenna, frequency reference and low-frequency clock
- Ultra-low-power operation with power save modes
- Ad-hoc and infrastructure modes for maximum deployment flexibility
- Single supply 3.1 to 3.6V operation

Resale:

TWR-WIFI-RS2101= $69

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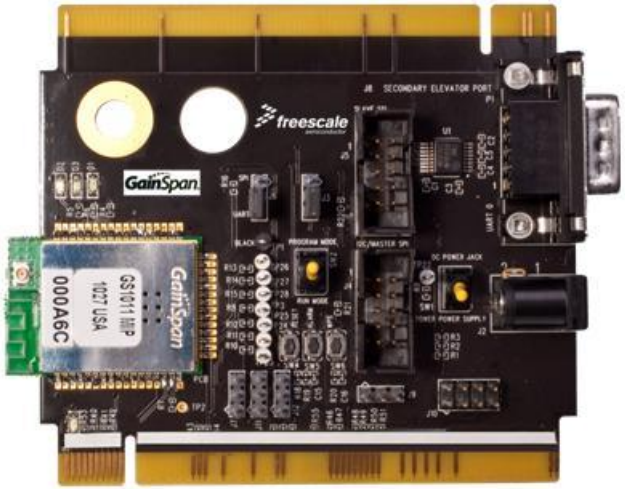
Peripheral Module: TWR-WIFI-G1011MI 802.11b Wi-Fi Module

TWR-WIFI-G1011MI



Resale:

TWR-WIFI-G1011MI= $69

Features:

- Features GS1011MIP Wi-Fi module from GainSpan
- Operates with standard 802.11 b/g/n access points at speeds up to 11 Mbps
  - Infrastructure or Adhoc mode
  - UART and SPI interfaces
  - Up to 3 Mbps in SPI Slave Mode
  - Up to 921.6 kbps on UART
- Full Wi-Fi stack including WPS and optional networking stack and services
- 802.11i Security
  - WEP, WPA, WPA2-PSK, Enterprise
- Certified RF Module: Wi-Fi, FCC, IC, Japan, ETSI, RoHS

Partner:

GainSpan (http://www.gainspan.com/)

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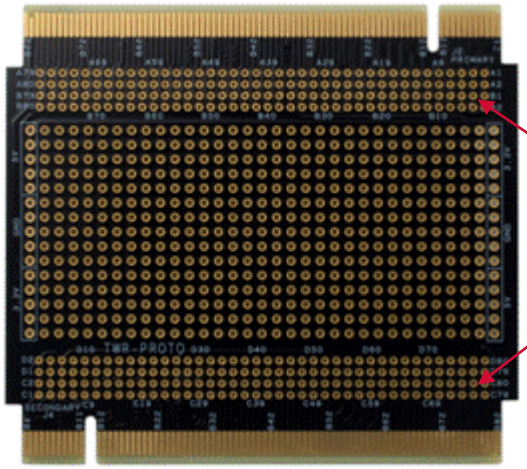
Peripheral Module: TWR-PROTO Prototyping Module

TWR-PROTO



Add custom circuitry easily!

Features:

- Access to all signals
- Generous 8.3 x 3.8cm prototyping area
- 3.3V, 5V and GND

Resale:

TWR-PROTO = $14.99

www.freescale.com/tower

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Peripheral Module: TWR-MEM Memory Module

TWR-MEM

Features:

- CPLD
- Compact flash interface
- Secure digital interface
- MRAM
- Serial flash

Resale:

TWR-MEM = $89

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Peripheral Module: TWR-LCD Graphical LCD Module

TWR-LCD

Features:

- 3.2” TFT QVGA display
- SPI and CPU interface
- Resistive touch screen interface
- 5-position navigation switch
- Piezzo buzzer
- microSD card slot
- Standalone mode

Resale:

TWR-LCD = $99

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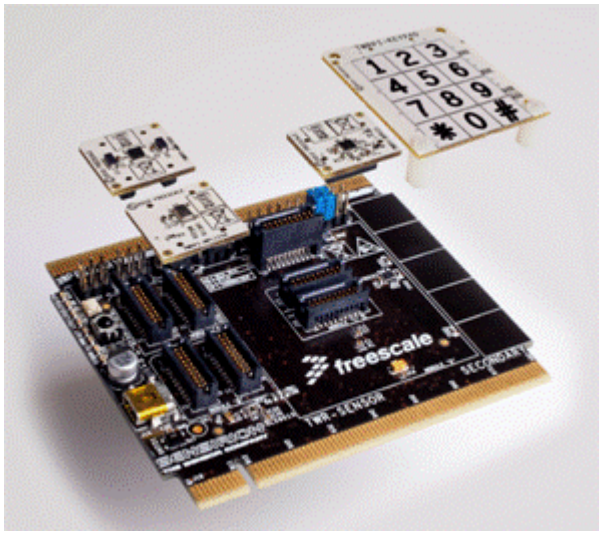
Peripheral Module: TWR-SENSOR-PAK Sensor Module

TWR-SENSOR-PAK



- **Swappable Freescale Sensor Modules**
  - Touch Sense Controller (MPR121)
  - Accelerometer (MMA7660, MMA6900, MMA8450)
  - Pressure Sensor (MPL115A)
- **Swappable Touch Pad Modules**
  - Keypad
  - Rotary
- **On-board Slider / Touch Pad**
  - With dedicated Touch Sense Controller (MPR032)
- **On-board MCU (MC9S08QE96)**
  - Stand-alone operation
  - Slave MCU mode
  - Touch Sense Software
- **On-Board 3rd Party Sensors**
  - Temperature / Humidity
  - Ambient Light / Proximity
  - IR Receiver
- **OSBDM / Serial-to-USB**
  - Onboard MC9S08JM60
  - OSBDM support for QE96
  - Serial-to-USB support

Resale:

TWR-SENSOR-PAK = $139

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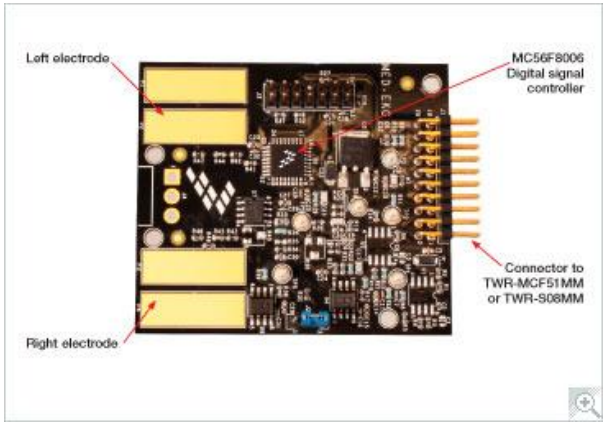
Peripheral Module: MED-EKG Electrocardiograph

MED-EKG



- Freescale Tower System compliant
- Small form factor
- External connector to TWR-S08MM128 and TWR-MCF51MM
- Includes the MC56F8006 DSC used for data filtering
- Electrodes embedded in development board for easy EKG signal detection
- Open connector for any type of EKG electrodes for additional precision

Resale:

TWR-SENSOR-PAK = $35

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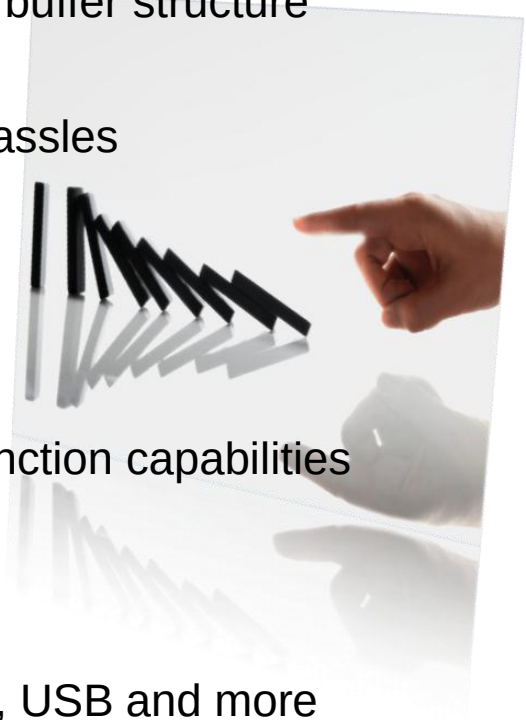
Xtrinsic Touch Sensing Software 2.0 Key Features

- Full API set support
- Support up to 64 electrodes
- No need of extra IC
- Configurable rotary, slider and keypad decoders with optimized buffer structure enabling any arrangement of electrodes.
- Smart auto-calibration mechanisms to prevent environmental hassles
- Noise rejection algorithms, new IIR filtering
- New KBI and IC functions for TSS ATL method
- Ability to enable and disable keys on runtime
- Auto repeat, stuck-up key, gorilla hand and other typical HMI function capabilities
- Ability to co-exist with other application code
- PC GUI application for electrode characterization
- Support multiple communication protocols: I2C, LIN, CAN , SPI, USB and more
- Possibility to have other peripherals working at the same time: LCD, LEDs, buzzer, ADC, other sensors, and more.



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