

STK531U394A-E

Intelligent Power Module (IPM) 600 V, 15 A



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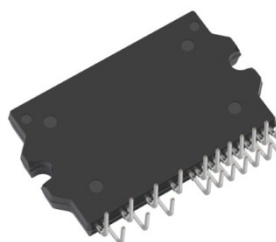
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Overview

This “Inverter IPM” is highly integrated device containing all High Voltage (HV) control from HV-DC to 3-phase outputs in a single SIP module (Single-In line Package). Output stage uses IGBT / FRD technology and implements Under Voltage Protection (UVP) and Over Current Protection (OCP) with a Fault Detection output flag. Internal Boost diodes are provided for high side gate boost drive.

Function

- Single control power supply due to Internal bootstrap circuit for high side pre-driver circuit
- All control input and status output are at low voltage levels directly compatible with microcontrollers
- Built-in cross conduction prevention
- Externally accessible embedded thermistor for substrate temperature measurement
- The level of the over current protection is adjustable with the external resistor, “RSD”



SIP29 44x26.5

Certification

- UL Recognized (File number : E339285)

Specifications

Absolute Maximum Ratings at Tc = 25°C

Parameter	Symbol	Remarks	Ratings	Unit
Supply voltage	V _{CC}	P to N, surge < 500 V *1	450	V
Collector-emitter voltage	V _{CE}	P to U, V, W or U, V, W, to N	600	V
Output current	I _o	P, N, U, V, W terminal current	±15	A
		P, N, U, V, W terminal current at Tc = 100°C	±7	A
Output peak current	I _{op}	P, N, U, V, W terminal current, PW = 1 ms	±30	A
Pre-driver voltage	VD1, 2, 3, 4	VB1 to U, VB2 to V, VB3 to W, V _{DD} to V _{SS} *2	20	V
Input signal voltage	V _{IN}	HIN1, 2, 3, LIN1, 2, 3	−0.3 to V _{DD}	V
FAULT terminal voltage	V _{FAULT}	FAULT terminal	−0.3 to V _{DD}	V
Maximum power dissipation	P _d	IGBT per 1 channel	35	W
Junction temperature	T _j	IGBT, FRD	150	°C
Storage temperature	T _{stg}		−40 to +125	°C
Operating case temperature	T _c	IPM case temperature	−20 to +100	°C
Tightening torque		A screw part *3	0.9	Nm
Isolation voltage	V _{is}	50 Hz sine wave AC 1 minute *4	2000	VRMS

Reference voltage is “V_{SS}” terminal voltage unless otherwise specified.

*1 : Surge voltage developed by the switching operation due to the wiring inductance between P and N terminal.

*2 : VD1 = VB1 to U, VD2 = VB2 to V, VD3 = VB3 to W, VD4 = V_{DD} to V_{SS} terminal voltage.

*3 : Flatness of the heat-sink should be lower than 0.15mm.

*4 : Test conditions : AC 2500 V, 1 second.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

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Electrical Characteristics at Tc = 25°C, VD1, VD2, VD3, VD4 = 15 V

Parameter	Symbol	Conditions		Test circuit	MIN	TYP	MAX	Unit
Power output section								
Collector-emitter cut-off current	I _{CE}	V _{CE} = 600 V		Fig.1	-	-	0.1	mA
Bootstrap diode reverse current	I _R (BD)	V _R (BD) = 600 V			-	-	0.1	mA
Collector to emitter saturation voltage	V _{CE} (SAT)	I _C = 15 A T _J = 25°C	Upper side	Fig.2	-	1.8	2.3	V
			Lower side *1		-	2.2	2.7	
		I _C = 7 A T _J = 100°C	Upper side		-	1.5	-	
			Lower side *1		-	1.7	-	
Diode forward voltage	V _F	I _F = 15 A T _J = 25°C	Upper side	Fig.3	-	1.8	2.1	V
			Lower side *1		-	2.0	3.3	
		I _F = 7 A T _J = 100°C	Upper side		-	1.4	-	
			Lower side *1		-	1.6	-	
Junction to case thermal resistance	θ _{j-c} (T)	IGBT		-	-	-	3.8	°C/W
	θ _{j-c} (D)	FWD			-	-	6.0	
Control (Pre-driver) section								
Pre-driver current consumption	I _D	VD1, 2, 3 = 15 V		Fig.4	-	0.08	0.4	mA
		VD4 = 15 V			-	1.6	4.0	
High level Input voltage	V _{in} H	HIN1, HIN2, HIN3,			2.5	-	-	V
Low level Input voltage	V _{in} L	LIN1, LIN2, LIN3 to V _{SS}			-	-	0.8	V
Input threshold voltage hysteresis *2	V _{inH} (hys)				0.5	0.8	-	V
Logic 1 input leakage current	I _{IN+}	VIN = +3.3 V			-	100	143	μA
Logic 0 input leakage current	I _{IN-}	VIN = 0 V			-	-	2	μA
FAULT terminal sink current	I _{oSD}	FAULT : ON / V _{FAULT} = 0.1 V			-	2	-	mA
FAULT clear time	FLTCLR	Fault output latch time			18	-	80	ms
V _{CC} and V _S undervoltage positive going threshold	V _{CCUV+} V _{SUV+}				10.5	11.1	11.7	V
V _{CC} and V _S undervoltage negative going threshold	V _{CCUV-} V _{SUV-}				10.3	10.9	11.5	V
V _{CC} and V _S undervoltage hysteresis	V _{CCUVH} V _{SUVH-}				0.14	0.2	-	V
Over current protection level	ISD	PW = 100 μs, RSD = 0 Ω		Fig.5	22.0	-	27.8	A
Electric current output signal level	ISO	I _o = 15 A		-	0.36	0.38	0.40	V

Reference voltage is "V_{SS}" terminal voltage unless otherwise specified.

*1 : The lower side's V_{CE(SAT)} and V_F include a loss by the shunt resistance

*2 : Input threshold voltage hysteresis indicates a reference value based on the design value of built-in pre-driver IC

Electrical Characteristics at Tc = 25°C, VD1, VD2, VD3, VD4 = 15 V, V_{CC} = 300 V, L = 3.9 mH

Parameter	Symbol	Conditions	Test circuit	MIN	TYP	MAX	Unit
Switching time	tON	Io = 15 A	Fig.6	0.3	0.5	1.2	μs
	tOFF			-	0.8	1.5	
Turn-on switching loss	Eon	Io = 7 A		-	220	-	μJ
Turn-off switching loss	Eoff			-	180	-	μJ
Total switching loss	Etot			-	400	-	μJ
Turn-on switching loss	Eon	Io = 15 A, Tc = 100°C		-	260	-	μJ
Turn-off switching loss	Eoff			-	220	-	μJ
Total switching loss	Etot			-	480	-	μJ
Diode reverse recovery energy	Erec		IF = 7 A, P = 400 V, Tc = 100°C	-	25	-	μJ
Diode reverse recovery time	trr	-		90	-	ns	
Reverse bias safe operating area	RBSOA	Io = 30 A, VCE = 450 V		Full square			
Short circuit safe operating area	SCSOA	VCE = 400 V, Tc = 100°C		4	-	-	μs

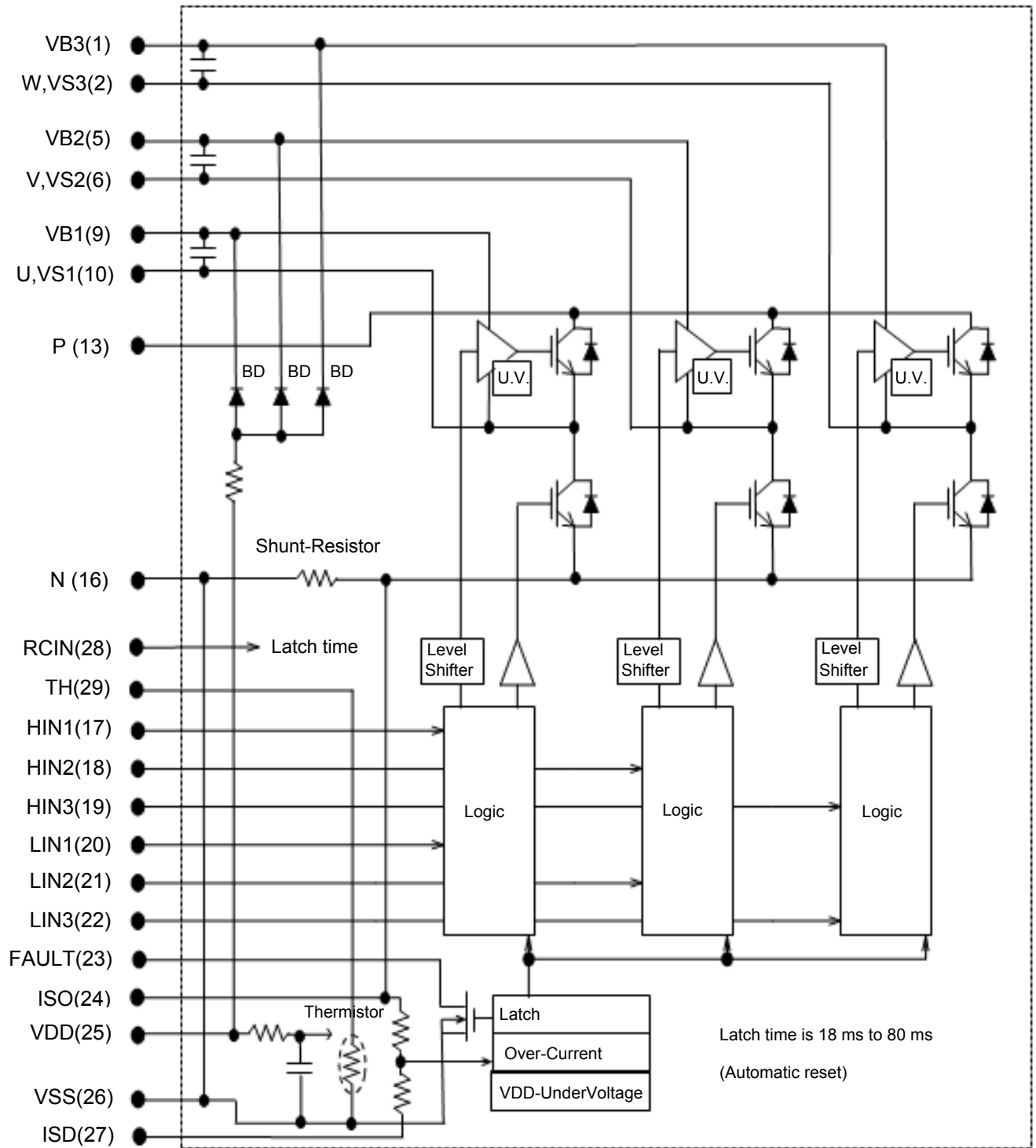
Reference voltage is "V_{SS}" terminal voltage unless otherwise specified.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Notes :

- The pre-drive power supply low voltage protection has approximately 0.2 V of hysteresis and operates as follows.
 Upper side : The gate is turned off and will return to regular operation when recovering to the normal voltage, but the latch will continue till the input signal will turn 'high'.
 Lower side : The gate is turned off and will automatically reset when recovering to normal voltage. It does not depend on input signal voltage.
- The pre-drive low voltage protection is the feature to protect devices when the pre-driver supply voltage falls due to an operating malfunction.

Equivalent Block Diagram



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Module Pin-Out Description

Pin	Name	Description
1	VB3	High Side Floating Supply Voltage 3
2	W, VS3	Output 3 - High Side Floating Supply Offset Voltage
3	–	Without Pin
4	–	Without Pin
5	VB2	High Side Floating Supply voltage 2
6	V, VS2	Output 2 - High Side Floating Supply Offset Voltage
7	–	Without Pin
8	–	Without Pin
9	VB1	High Side Floating Supply voltage 1
10	U, VS1	Output 1 - High Side Floating Supply Offset Voltage
11	–	Without Pin
12	–	Without Pin
13	P	Positive Bus Input Voltage
14	–	Without Pin
15	–	Without Pin
16	N	Negative Bus Input Voltage
17	HIN1	Logic Input High Side Gate Driver - Phase U
18	HIN2	Logic Input High Side Gate Driver - Phase V
19	HIN3	Logic Input High Side Gate Driver - Phase W
20	LIN1	Logic Input Low Side Gate Driver - Phase U
21	LIN2	Logic Input Low Side Gate Driver - Phase V
22	LIN3	Logic Input Low Side Gate Driver - Phase W
23	FAULT	Fault output
24	ISO	Current monitor output
25	VDD	+15 V Main Supply
26	VSS	Negative Main Supply
27	ISD	Over current detection and setting
28	RCIN	Fault clear time setting output
29	TH	Thermistor output

Test Circuit

(The tested phase : U+ shows the upper side of the U phase and U- shows the lower side of the U phase.)

■ $I_{CE} / I_R(BD)$

	U+	V+	W+	U-	V-	W-
M	13	13	13	10	6	2
N	10	6	2	16	16	16

	U(BD)	V(BD)	W(BD)
M	9	5	1
N	26	26	26

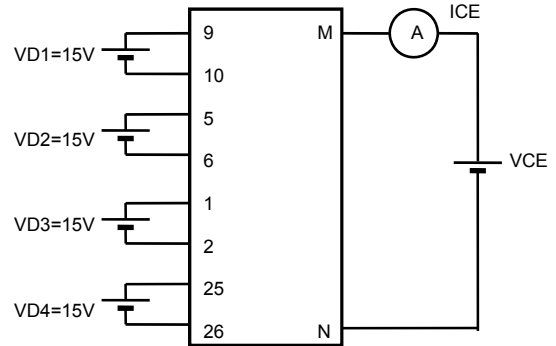


Fig.1

■ $V_{CE(SAT)}$ (Test by pulse)

	U+	V+	W+	U-	V-	W-
M	13	13	13	10	6	2
N	10	6	2	16	16	16
m	17	18	19	20	21	22

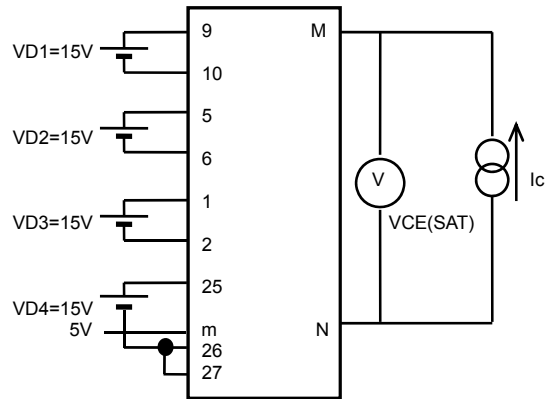


Fig.2

■ V_F (Test by pulse)

	U+	V+	W+	U-	V-	W-
M	13	13	13	10	6	2
N	10	6	2	16	16	16

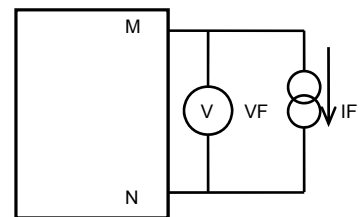


Fig.3

■ I_D

	VD1	VD2	VD3	VD4
M	9	5	1	25
N	10	6	2	26

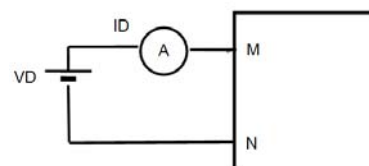


Fig.4

■ ISD

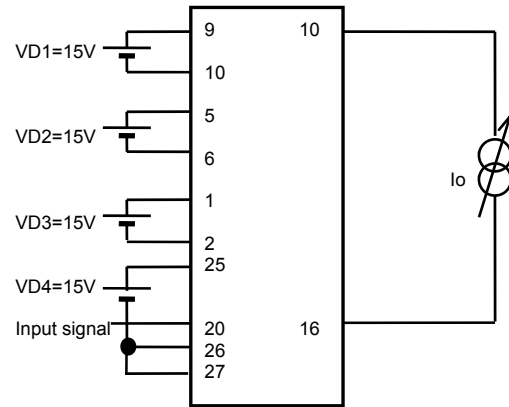
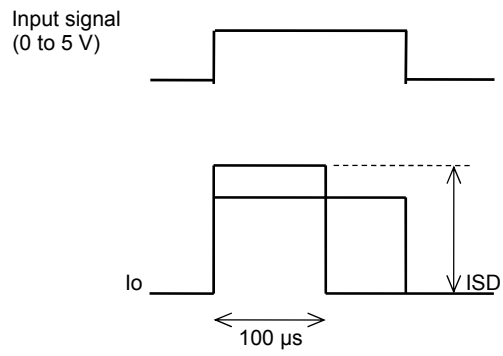


Fig.5

■ Switching time (The circuit is a representative example of the lower side U phase.)

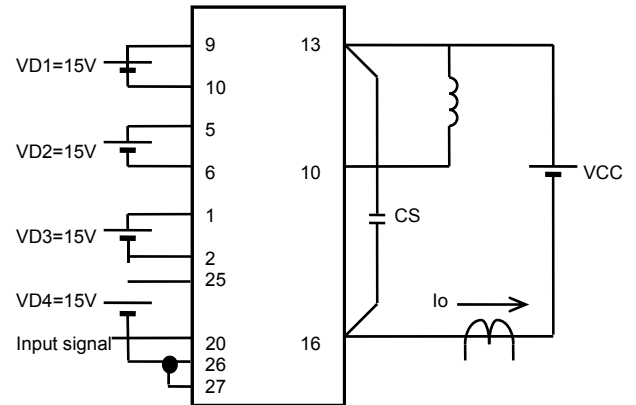
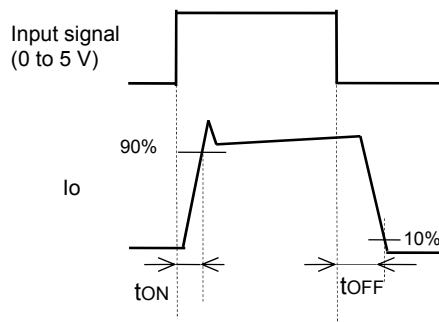


Fig.6

Input / Output Timing Chart

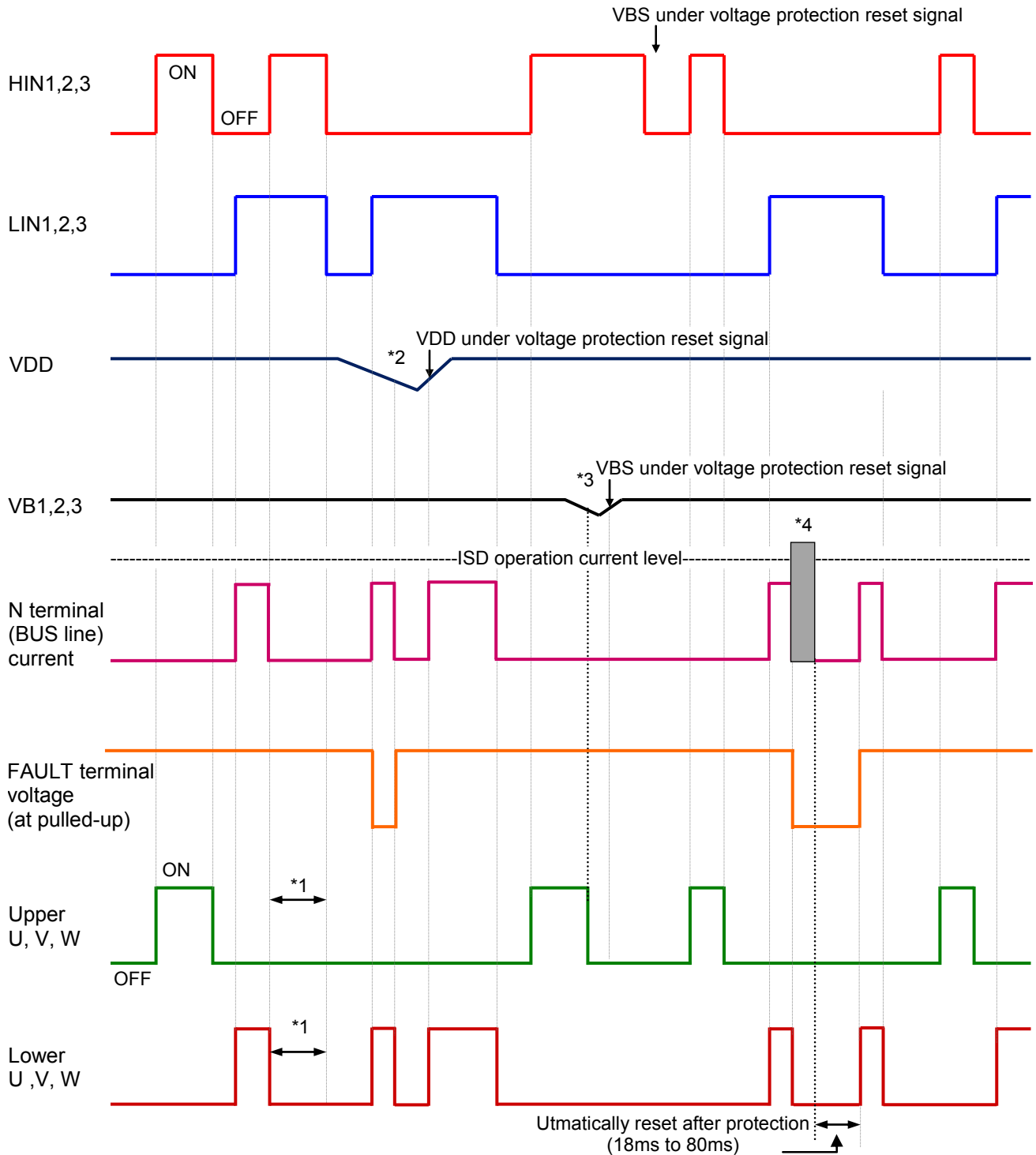
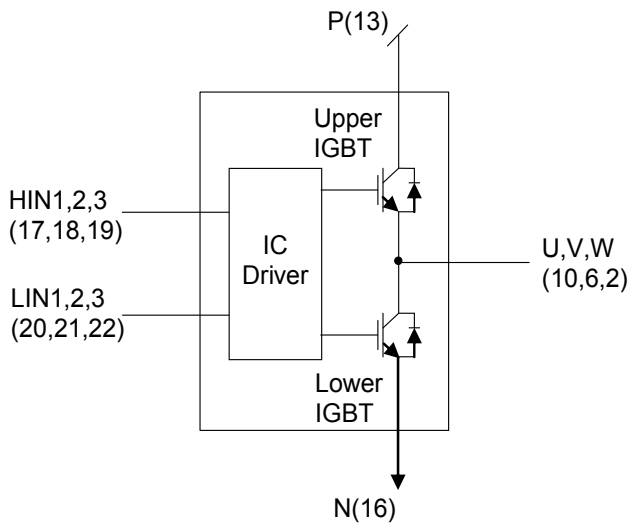


Fig. 7

Notes

- *1 : Diagram shows the prevention of shoot-through via control logic. More dead time to account for switching delay needs to be added externally.
- *2 : When V_{DD} decreases all gate output signals will go low and cut off all of 6 IGBT outputs. When V_{DD} rises the operation will resume immediately.
- *3 : When the upper side gate voltage at VB1, VB2 and VB3 drops only, the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gate voltage rises.
- *4 : In case of over current detection, all IGBT's are turned off and the FAULT output is asserted. Normal operation resumes in 18 to 80 ms after the over current condition is removed.

Logic level table



INPUT			OUTPUT			
HIN	LIN	OCF	Upper IGBT	Lower IGBT	U,V,W	FAULT
H	L	OFF	ON	OFF	P	OFF
L	H	OFF	OFF	ON	N	OFF
L	L	OFF	OFF	OFF	High Impedance	OFF
H	H	OFF	OFF	OFF	High Impedance	OFF
X	X	ON	OFF	OFF	High Impedance	ON

Fig. 8

Sample Application Circuit

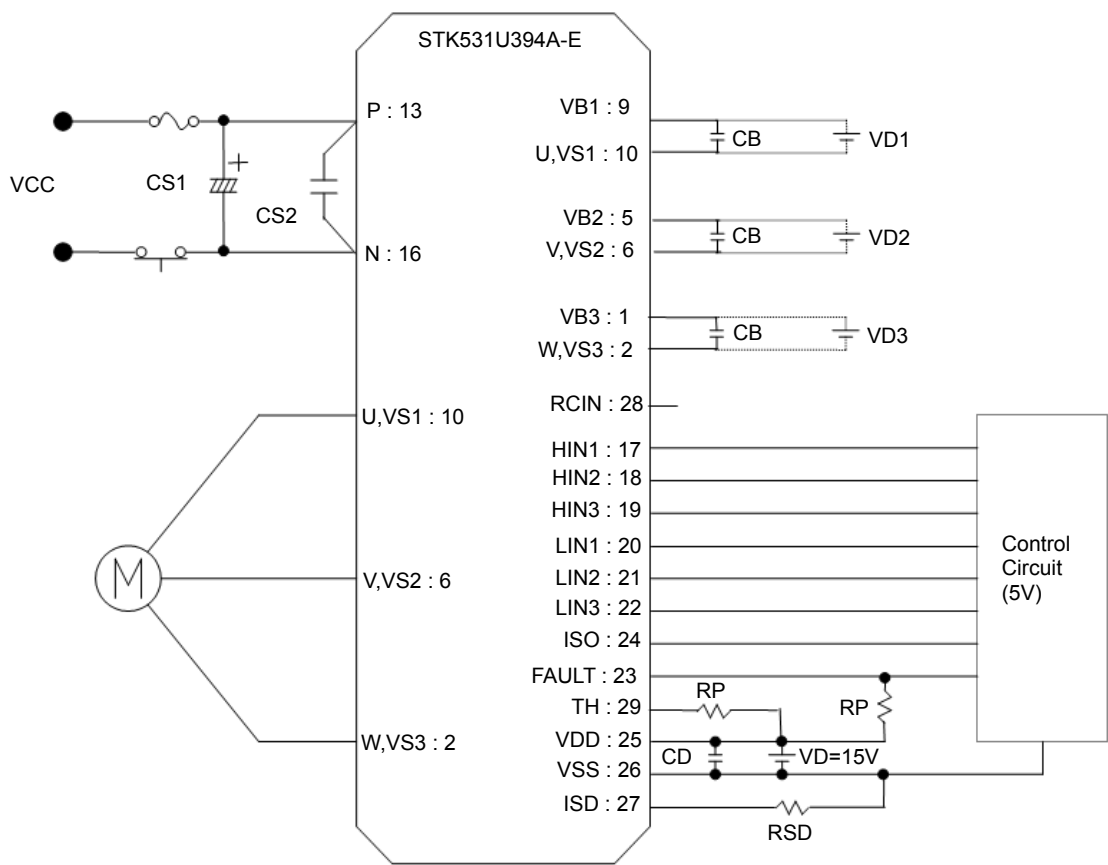


Fig.9

Recommended Operating Condition

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply voltage	V _{CC}	P to N	0	280	450	V
Pre-driver supply voltage	VD1, 2, 3	VB1 to U, VB2 to V, VB3 to W	12.5	15	17.5	V
	VD4	V _{DD} to V _{SS} *1	13.5	15	16.5	
PWM frequency	f _{PWM}		1	-	20	kHz
Dead time	DT	Turn-off to Turn-on	2	-	-	μs
Allowable input pulse width	PWIN	ON and OFF	1	-	-	μs
Tightening torque		'M3' type screw	0.6	-	0.9	Nm

*1 : Pre-drive power supply (VD4 = 15 ±1.5 V) must have the capacity of I_o = 20 mA (DC), 0.5 A (Peak).

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Usage Precaution

1. This IPM includes bootstrap diode and resistors. Therefore, by adding a capacitor "CB", a high side drive voltage is generated; each phase requires an individual bootstrap capacitor. The recommended value of CB is in the range of 1 to 47 μF, however this value needs to be verified prior to production. If selecting the capacitance more than 47 μF (±20%), connect a resistor (about 20 Ω) in series between each 3-phase upper side power supply terminals (VB1, 2, 3) and each bootstrap capacitor. When not using the bootstrap circuit, each upper side pre-drive power supply requires an external independent power supply.
2. It is essential that wiring length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of "CS" is in the range of 0.1 to 10 μF.
3. "ISO" (pin 24) is terminal for current monitor. High current may flow into that course when short-circuiting the "ISO" terminal and "V_{SS}" terminal. Please do not connect them.
4. "FAULT" (pin 23) is open DRAIN output terminal (Active Low). Pull up resistor is recommended more than 6.8 kΩ.
5. Inside the IPM, a thermistor used as the temperature monitor for internal substrate is connected between V_{SS} terminal and TH terminal therefore, an external pull up resistor connected between the TH terminal and an external power supply should be used. The temperature monitor example application is as follows, please refer the Fig.10, and Fig.11 below.
6. Pull down resistor of 33 kΩ is provided internally at the signal input terminals. An external resistor of 2.2 k to 3.3 kΩ should be added to reduce the influence of external wiring noise.
7. The over current protection feature is not intended to protect in exceptional fault condition. An external fuse is recommended for safety.
8. The level of the over current protection might be changed from IPM design value when "ISD" terminal and "V_{SS}" terminal are shorted at external. Be confirm with actual application("N" terminal and "V_{SS}" terminal are shorted at internal).
9. The level of the over current protection is adjustable with the external resistor "RSD" between "ISD" terminal and "V_{SS}" terminal.
10. When input pulse width is less than 1.0 μs, an output may not react to the pulse. (Both ON signal and OFF signal)

This data shows the example of the application circuit, does not guarantee a design as the mass production set.

The characteristic of thermistor

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Resistance	R_{25}	$T_c = 25^{\circ}\text{C}$	99	100	101	$\text{k}\Omega$
	R_{100}	$T_c = 100^{\circ}\text{C}$	5.18	5.38	5.60	$\text{k}\Omega$
B-Constant (25 to 50°C)	B		4208	4250	4293	K
Temperature Range			-40	-	+125	$^{\circ}\text{C}$

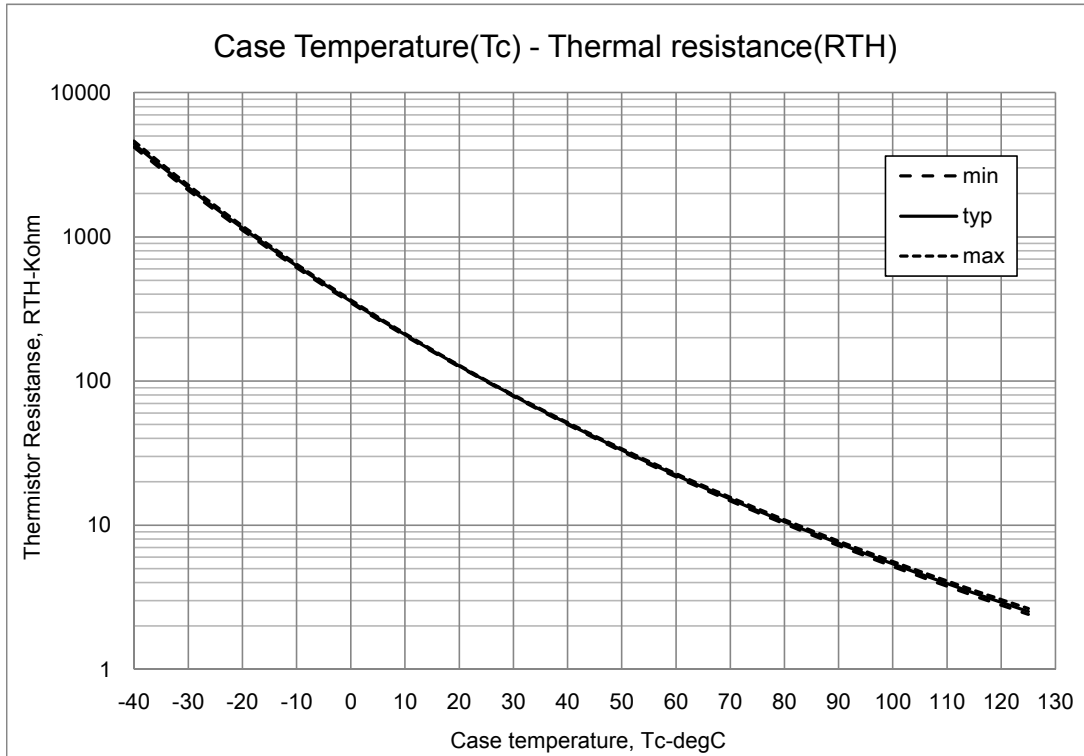


Fig.10 Variation of thermistor resistance with temperature

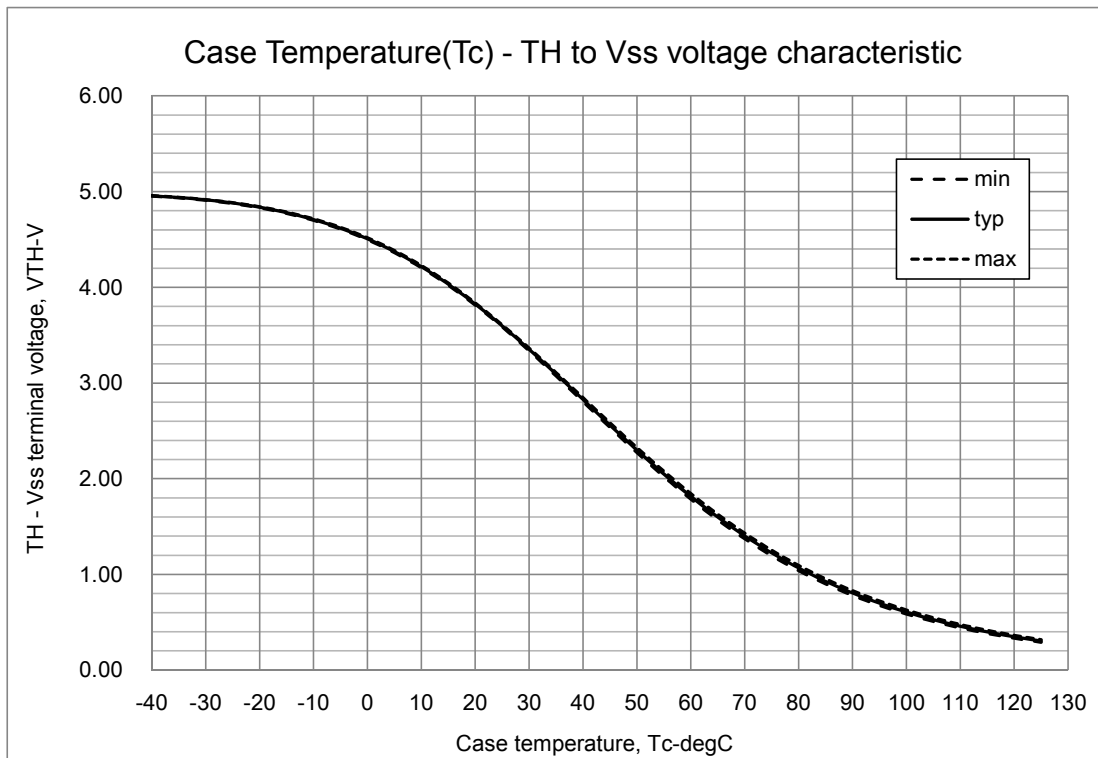


Fig.11 Variation of thermistor terminal voltage with temperature
(39 $\text{k}\Omega$ pull-up resistor, 5 V)

CB capacitor value calculation for bootstrap circuit

Calculate conditions

Parameter	Symbol	Value	Unit
Upper side power supply	VBS	15	V
Total gate charge of output power IGBT at 15 V	QG	132	nC
Upper limit power supply low voltage protection	UVLO	12	V
Upper side power dissipation	IDmax	400	μA
ON time required for CB voltage to fall from 15 V to UVLO	TONmax	-	s

Capacitance calculation formula

Thus, the following formula are true

$$VBS \times CB - QG - IDMAX \times TONMAX = UVLO \times CB$$

therefore,

$$CB = (QG + IDMAX \times TONMAX) / (VBS - UVLO)$$

The relationship between TONMAX and CB becomes as follows. CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47 μF, however, this value needs to be verified prior to production.

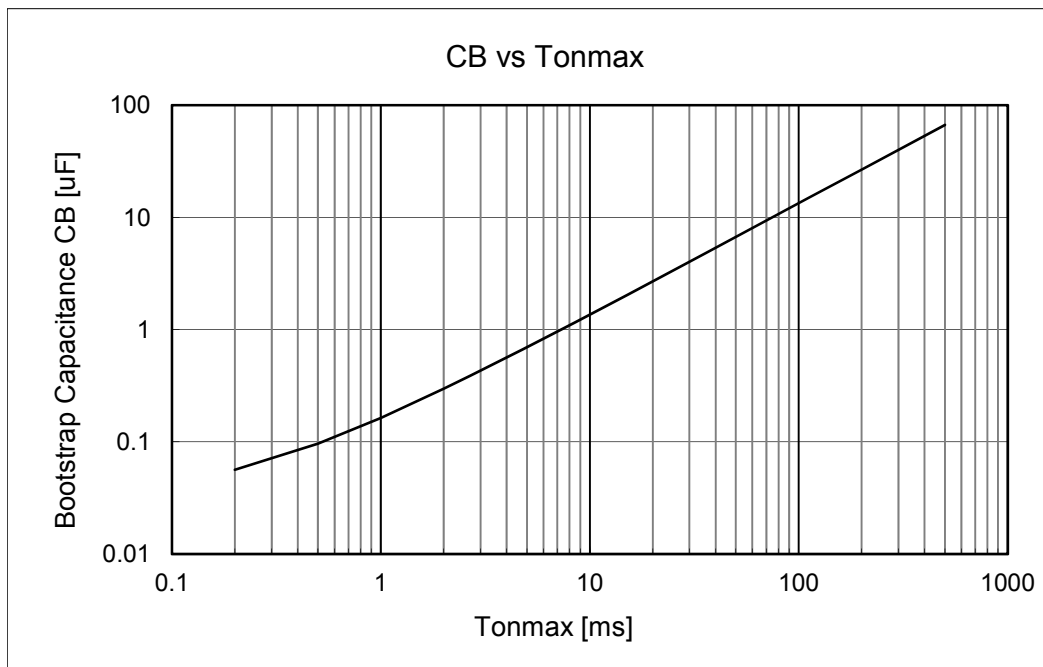


Fig. 12 Tonmax - CB characteristic

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Package Dimensions

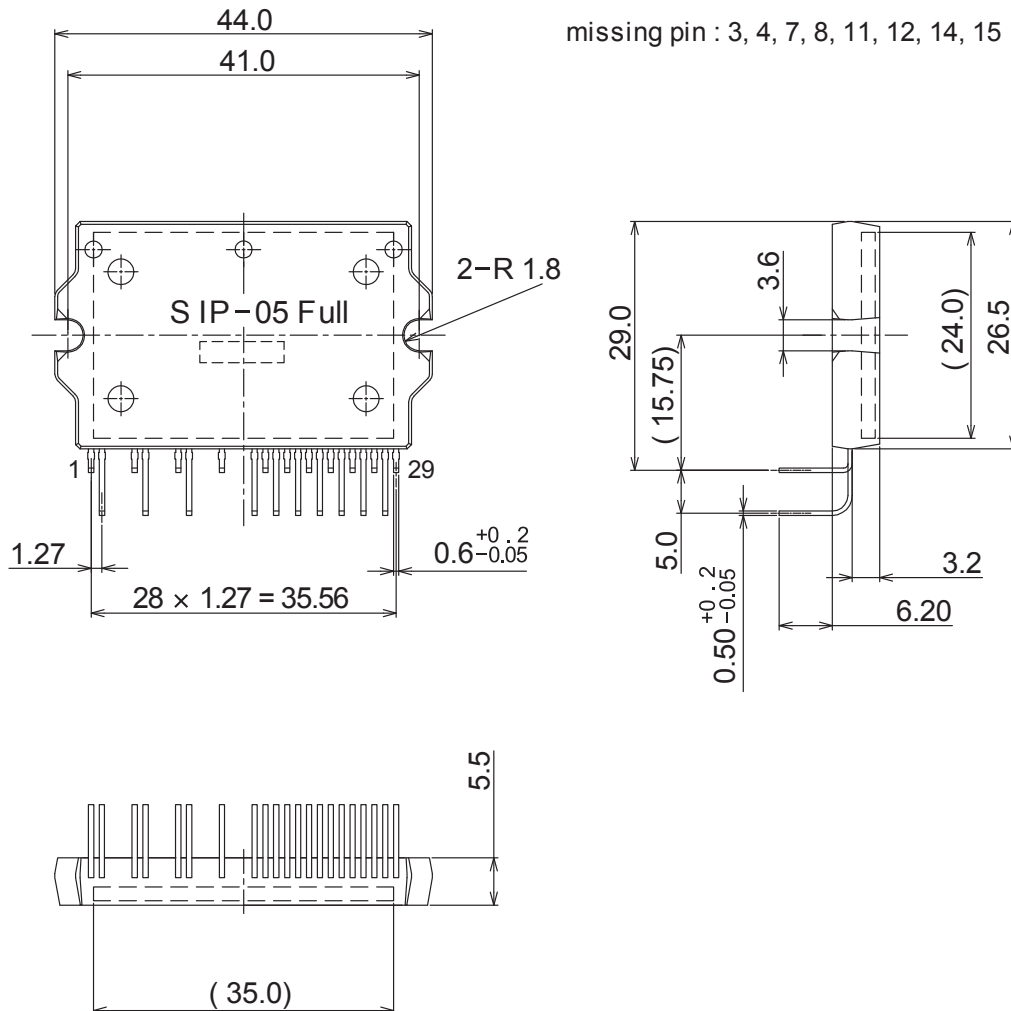
unit : mm

The tolerances of length are ± 0.5 mm unless otherwise specified.

SIP29 44x26.5

CASE 127CH

ISSUE O



STK531U394A-E

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK531U394A-E	SIP29 44x26.5 (Pb-Free)	11 / Tube

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