

N Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
100	0.0082 at $V_{GS} = 10$ V	90 ^d	97

FEATURES

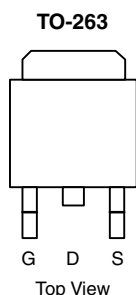
- TrenchFET® Power MOSFETS
- 175 °C Junction Temperature
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



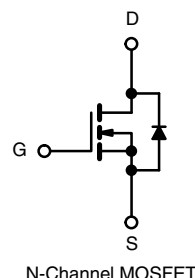
RoHS
COMPLIANT

APPLICATIONS

- Power Supply
 - Secondary Synchronous Rectification
- Industrial
- Primary Switch



Ordering Information: SUM90N10-8m2P-E3 (Lead (Pb)-free)



ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175$ °C)	I_D	$T_C = 25$ °C 90 ^d	A
		$T_C = 70$ °C 90 ^d	
Pulsed Drain Current	I_{DM}	240	
Avalanche Current	I_{AS}	60	
Single Avalanche Energy ^a	E_{AS}	180	mJ
Maximum Power Dissipation ^a	P_D	$T_C = 25$ °C 300 ^b	W
		$T_A = 25$ °C ^c 3.75	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) ^c	R_{thJA}	40	°C/W
Junction-to-Case (Drain)	R_{thJC}	0.5	

Notes:

- Duty cycle ≤ 1 %.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).
- Package limited.

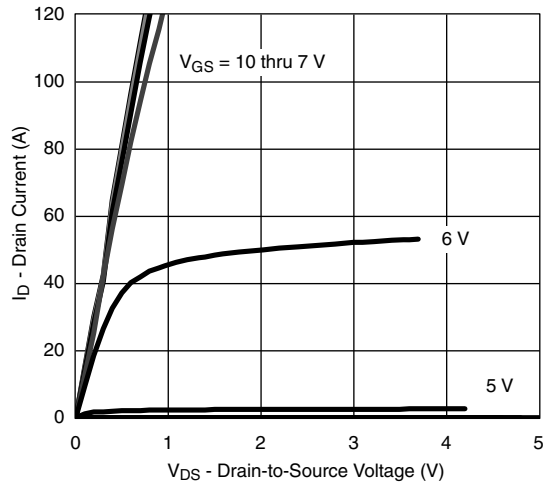
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{DS} = 0 V, I _D = 250 μA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.5		4.5	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 250	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 125 °C			50	
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 150 °C			250	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} = 10 V	70			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.0067	0.0082	Ω
		V _{GS} = 10 V, I _D = 20 A, T _J = 125 °C		0.0127	0.0170	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 20 A		62		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 50 V, f = 1 MHz		6290		pF
Output Capacitance	C _{oss}			535		
Reverse Transfer Capacitance	C _{rss}			182		
Total Gate Charge ^c	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 85 A		97	150	nC
Gate-Source Charge ^c	Q _{gs}			32		
Gate-Drain Charge ^c	Q _{gd}			25		
Gate Resistance	R _g	f = 1 MHz	0.28	1.4	2.8	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 50 V, R _L = 0.588 Ω I _D ≅ 85 A, V _{GEN} = 10 V, R _g = 1 Ω		23	35	ns
Rise Time ^c	t _r			17	26	
Turn-Off Delay Time ^c	t _{d(off)}			34	52	
Fall Time ^c	t _f			9	18	
Source-Drain Diode Ratings and Characteristics (T _C = 25 °C) ^b						
Continuous Current	I _S				85	A
Pulsed Current	I _{SM}				240	
Forward Voltage ^a	V _{SD}	I _F = 30 A, V _{GS} = 0 V		0.85	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 75 A, di/dt = 100 A/μs		61	100	ns
Peak Reverse Recovery Current	I _{RM(REC)}			3	4.5	A
Reverse Recovery Charge	Q _{rr}				91	130

Notes:

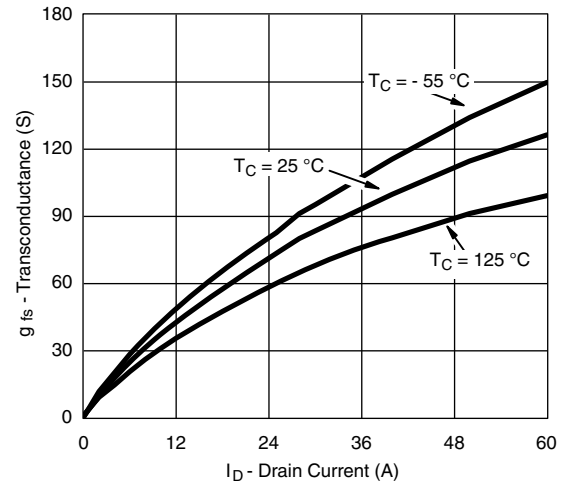
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

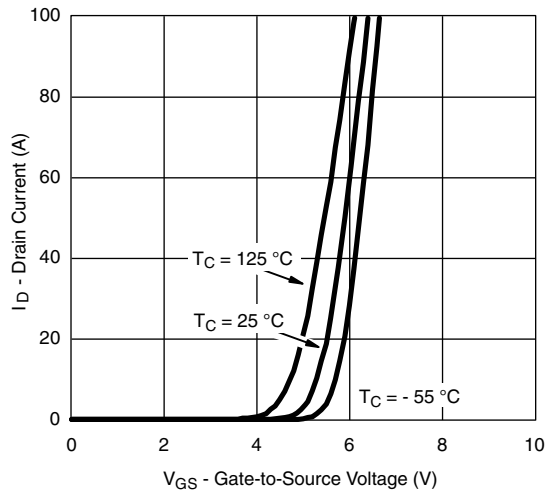
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



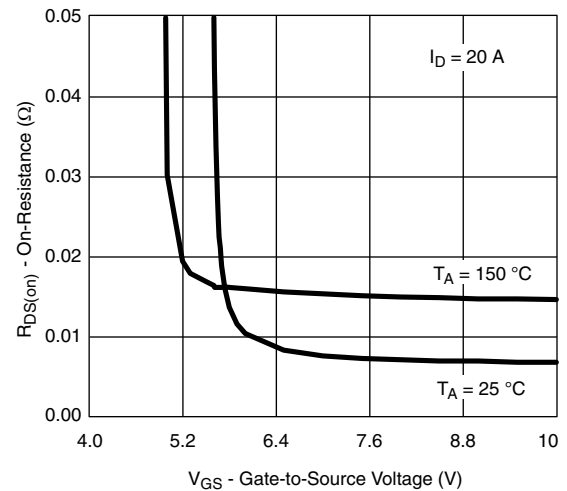
Output Characteristics



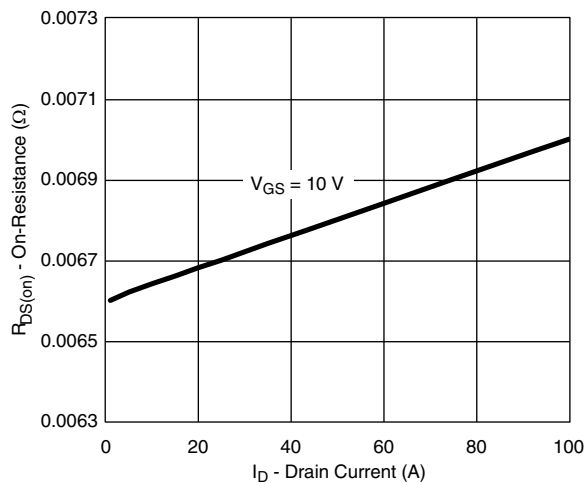
Transconductance



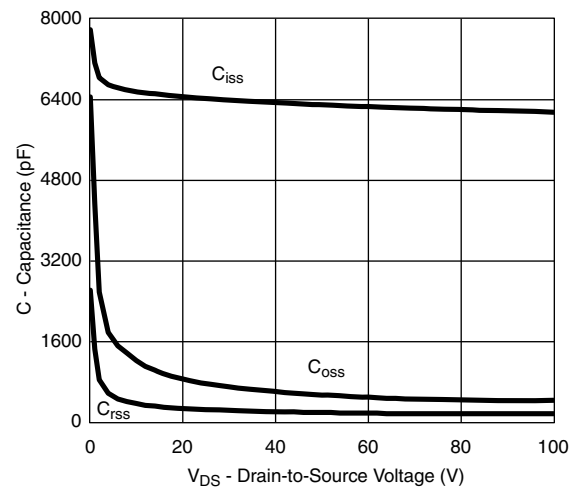
Transfer Characteristics



On-resistance vs. Gate-to-Source Voltage

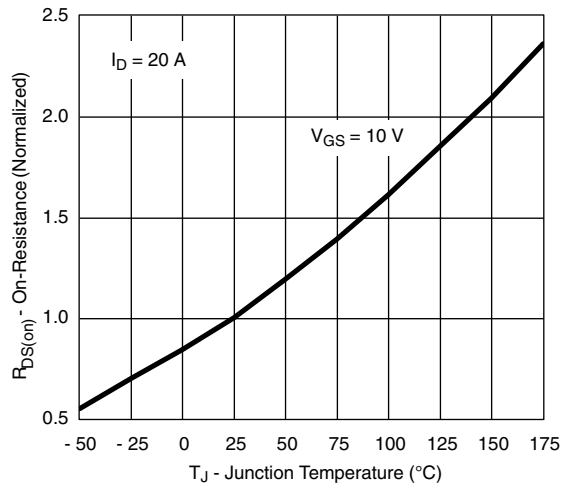


On-Resistance vs. Drain Current

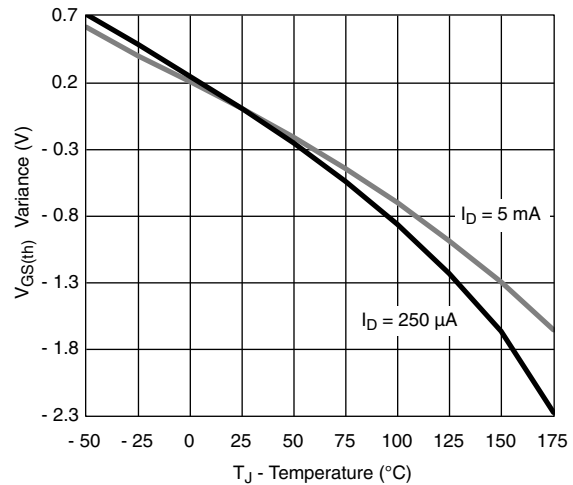


Capacitance

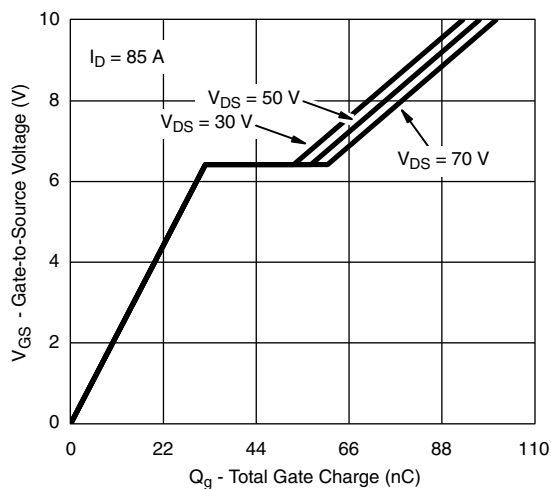
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



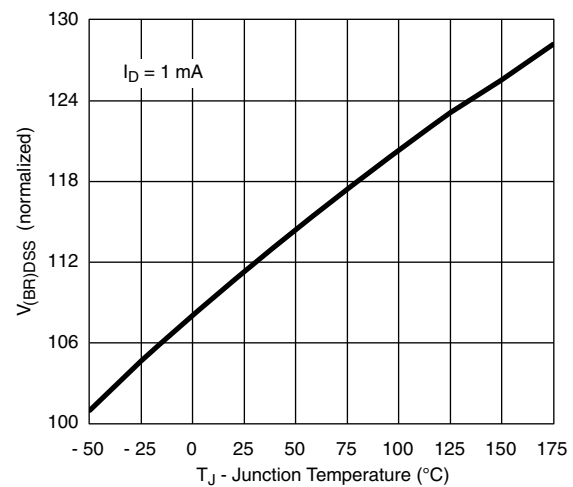
On-Resistance vs. Junction Temperature



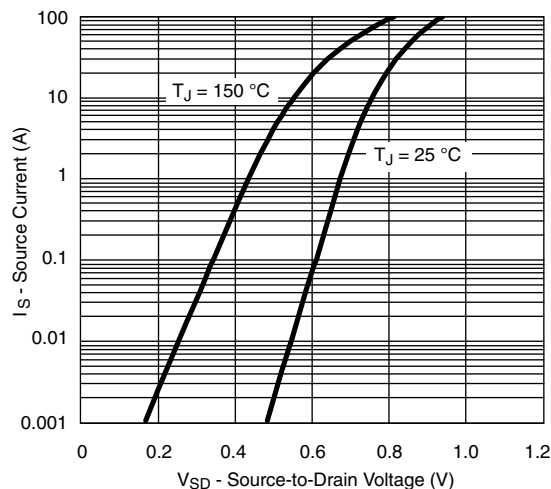
Threshold Voltage



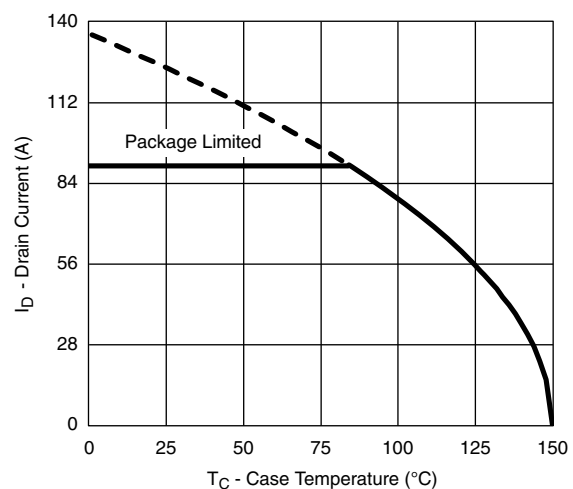
Gate Charge



Drain Source Breakdown vs. Junction Temperature

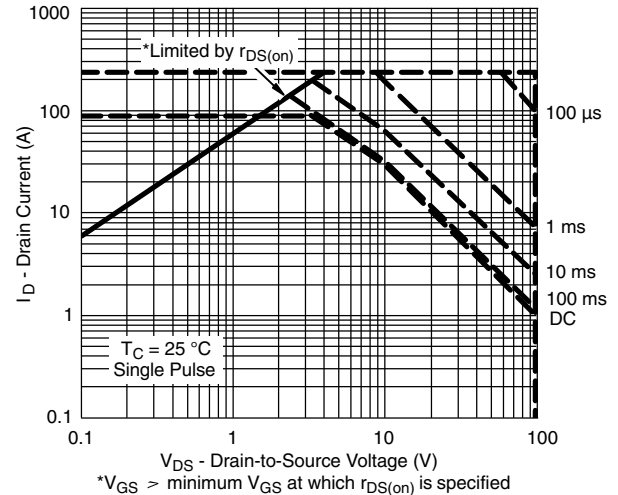
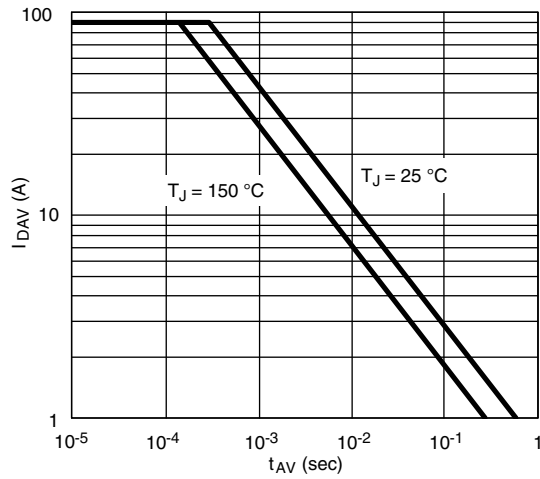


Source-Drain Diode Forward Voltage

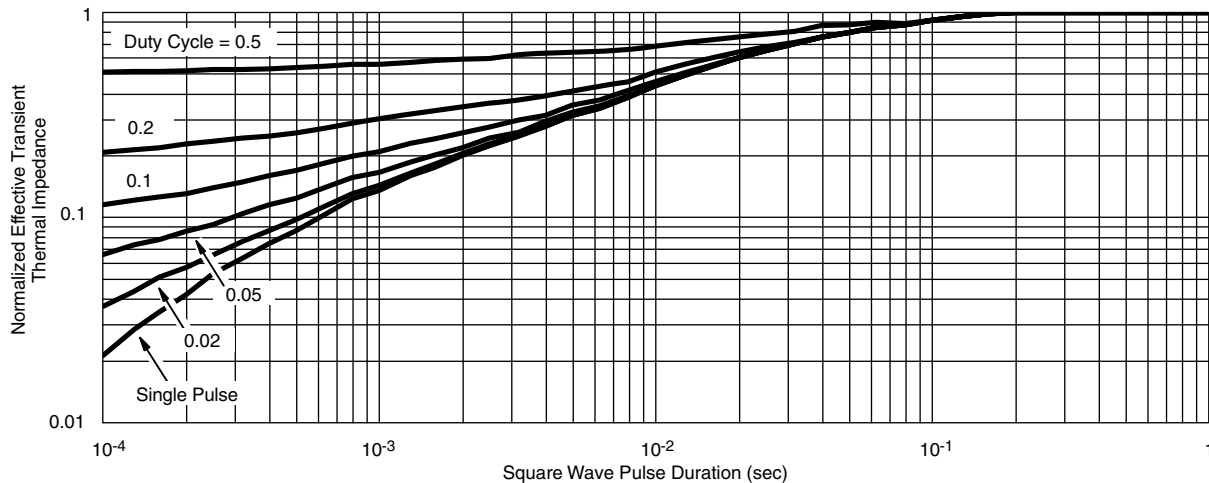


Maximum Drain Current vs. Case Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



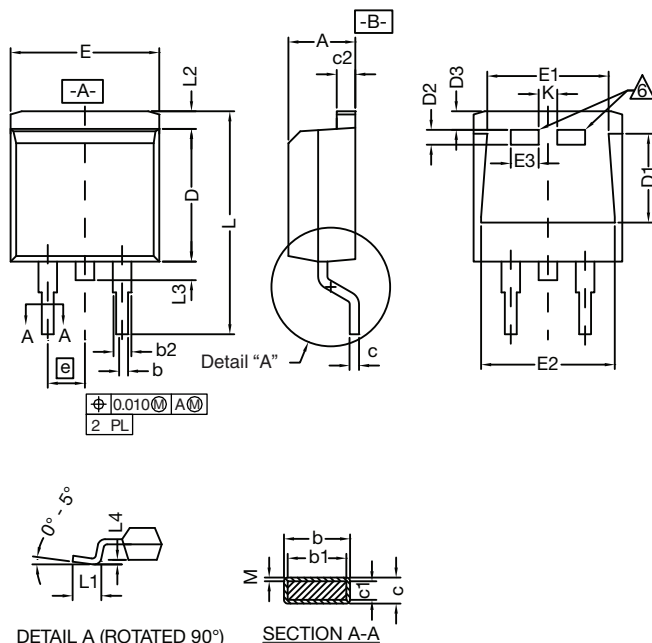
Single Pulse Avalanche Current Capability vs. Time



Normalized Thermal Transient Impedance, Junction-to-Case

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TO-263 (D²PAK): 3-LEAD



DIM.		INCHES		MILLIMETERS	
		MIN.	MAX.	MIN.	MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
E		0.380	0.410	9.652	10.414
E1		0.245	-	6.223	-
E2		0.355	0.375	9.017	9.525
E3		0.072	0.078	1.829	1.981
e		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		-	0.002	-	0.050
ECN: T10-0738-Rev. J, 03-Jan-11					
DWG: 5843					

Notes

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin-to-pin coplanarity max. 4 mils.
4. *: Thin lead is for SUB, SYB.
Thick lead is for SUM, SYM, SQM.
5. Use inches as the primary measurement.
6. This feature is for thick lead.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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