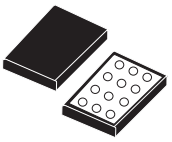
STUSBCD01B

USB charger detection interface

Features

- Capable of detecting dedicated USB chargers and host chargers (current sink and dedicated methods)
- Operates with V_{BAT} supply voltage ranging from 2.2 V to 4.5 V
- Active high open drain hardware detection pin (DETECT)
- GPIO control interface
- 1.6 V - 2.8 V interface voltage range (V_{IO})
- V_{BUS} voltage 6 V clamping circuit
- Low DP-DM input capacitance
- ESD: HBM ± 2 kV, CDM 500 V on every pin
- 12 bumps Flip-Chip package, 1.6 x1.2 mm, pitch 0.4 mm, max thickness 0.60 mm, Halogen free RoHS compliant package



Flip-Chip 12 (1.6 x 1.2 mm)

Applications

- Mobile phones
- PDAs, MP3 players

Description

The STUSBCD01B is a USB charger detection IC which can detect dedicated USB chargers, Host/Hub chargers or standard host ports connected to the USB DP/DM data lines.

The device implements two different detection methods in order to be able to distinguish between a dedicated charger and a Host/Hub charger.

Operation is controlled through three general purpose I/O pins; a hardware open drain detection output is also available.

An internal regulator provides the 1.8 V supply voltage for the internal blocks and state machine while a clamping device prevents V_{BUS} voltage from going over 6 V (typ.).

The STUSBCD01B is available in a 12 bumps Flip-Chip 0.4 mm pitch package.

Table 1. Device summary

Order code	Package	Packaging
STUSBCD01BJR	Flip-Chip 12 (1.6 x 1.2 mm)	3000 parts per reel

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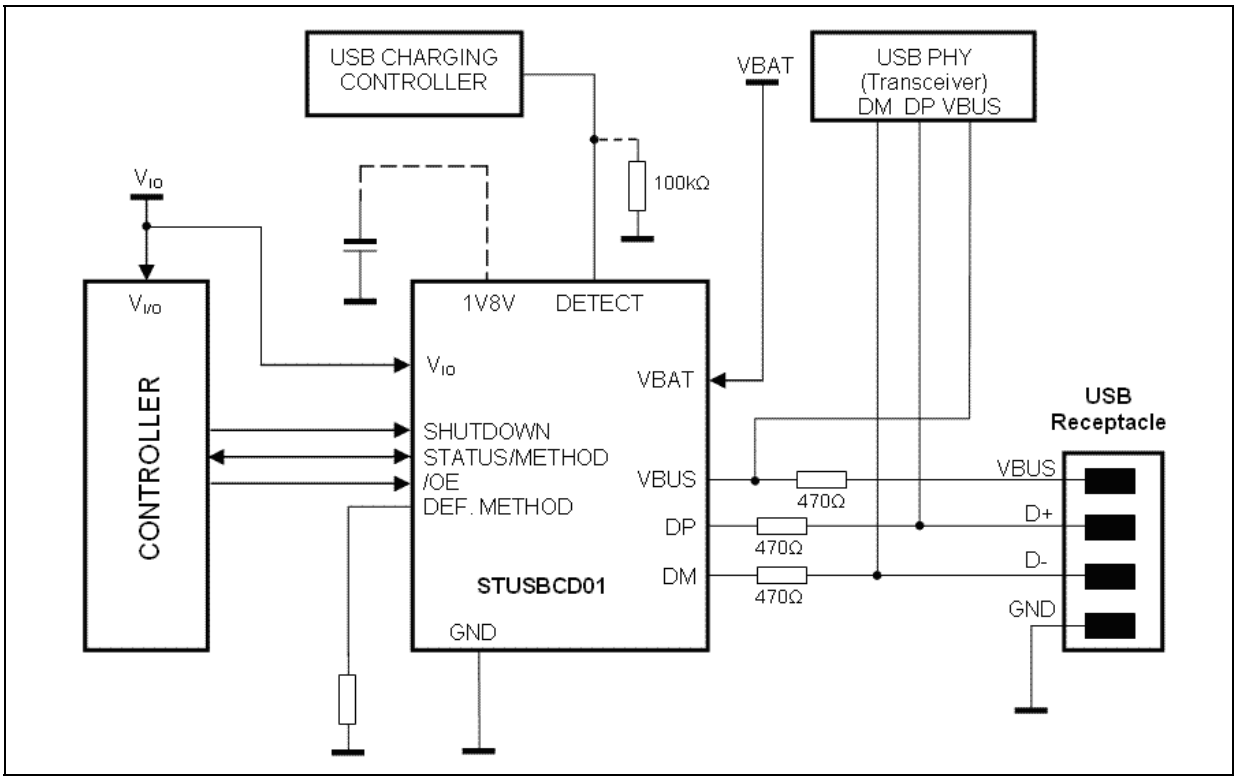
1 Application

Figure 1. Application circuit



2 Pin configuration

Figure 2. Bump configuration (top through view)

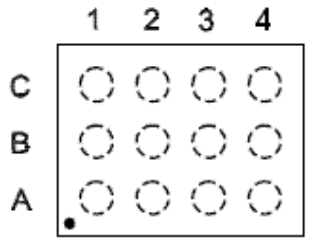


Table 2. Pin description

Bump name	Symbol	Type	Description
C3	VBAT	PWR	Analog supply voltage input (2.2 V - 4.5 V)
C2	GND	PWR	Ground reference
A3	V_{IO}	PWR	Digital interface supply voltage (1.6 V - 2.8 V)
B4	DP	AI/O	Connected to USB D+ Data line
A4	DM	AI/O	Connected to USB D- Data line
B2	DETECT	O	Hardware detection pin (open drain). 300 kΩ internal pull-down resistor. V_{BAT} referred.
A2	SHUTDOWN	I	Standby mode selection pin. Active HIGH. Terminates the detection and resets the device.
A1	/OE	I	Output enable for DETECT output. Active LOW.
B1	STATUS/ METHOD	AI/O	SW detection output: High when Charger detected. Pulled high or low through internal weak pull-up to 1V8V and weak pull-down. Detection method selection input: low for dedicated method, high for current sink method.
B3	DEFAULT METHOD	AI	Hardware selection for detection method. Active only if V_{IO} is not present. Dedicated method is selected if driven low, current sink method if driven high. V_{BAT} referred. Do not leave floating to avoid increased power consumption.
C4	VBUS	AI	V_{BUS} voltage comparator input. Triggers the charger detection. 6V limited voltage when 10 V are applied externally.
C1	1V8V	O	Regulator output voltage. Bypass capacitor not required.

3 Functional description

The STUSBCD01B is designed to provide USB charger detection functionality to USB platforms which do not have this feature integrated in the PHY. The device can work with a supply voltage ranging from 2.2 V to 4.5 V and has an internal regulator which generates the 1.8 V voltage required for the internal blocks and state machine.

The STUSBCD01B can detect a dedicated charger or a Host/Hub charger connected to USB data lines and provides both an open drain pin and a digital I/O pin for the detection output signal. The open drain output can be disabled using the /OE input signal.

Two different detection methods, selectable through the STATUS/METHOD pin, are implemented in order to distinguish between a dedicated charger and a Host/Hub charger. If the interface voltage is not present the detection method is defined by the status of default method pin.

The STUSBCD01B features very low power consumption in Standby mode and low input capacitance on DP/DM pins. An over voltage protection circuit is also implemented on the VBUS pin in order to limit V_{BUS} voltage to 6 V and provide protection to external devices connected to it.

3.1 Detection methods

The STUSBCD01B implements a current source/sink method to detect dedicated chargers (wall chargers) and a current sink method for Host/Hub chargers (based on USB battery charging spec v1.0). If a standard Host/Hub is connected to the device it is recognized thanks to its pull-down resistors on DP/DM lines and therefore DETECT/STATUS outputs will be low.

3.2 Dedicated charger detection method

Selected driving method pin low during the falling edge of shutdown or driving default method pin low if V_{IO} is not present. The dedicated charger detection method uses a current source on DP pin and a current sink on DM pin to detect the resistor (max 200 Ω) which connects DP and DM in dedicated chargers.

3.3 Current sink method

Selected driving method pin high during the falling edge of shutdown or driving default method pin high if V_{IO} is not present. A voltage source of VDAT_SRC is connected to DP and a current of IDAT_SINK is drawn from DM.

If a Host/Hub charger is connected, STUSBCD01B will see a voltage of VDAT_SRC on pin DM. The same happens if a dedicated charger is connected and, therefore, in order to distinguish between the two, if the current sink method detection is successful it is necessary to run the dedicated charger detection method immediately after.

3.4 Detection triggering

USB Charger detection automatically starts when V_{BUS} voltage is over V_{TH_VBUS} threshold and shutdown input is low.

If V_{BUS} drops under V_{TH_VBUS} threshold or shutdown input is pulled high, the charger detection is immediately terminated.

If no charger is detected (DETECT = 0 and /OE = 0), V_{BUS} voltage is kept over V_{TH_VBUS} threshold and V_{IO} is not present then a new detection is started every 1 s.

If a charger is detected, detect and status pins are kept high until V_{BUS} drops under V_{TH_VBUS} threshold or a new detection is started.

Any hardware detection (V_{IO} not present) is terminated as soon as V_{IO} voltage rises above V_{TH_IO} threshold.

3.5 V_{BUS} clamping

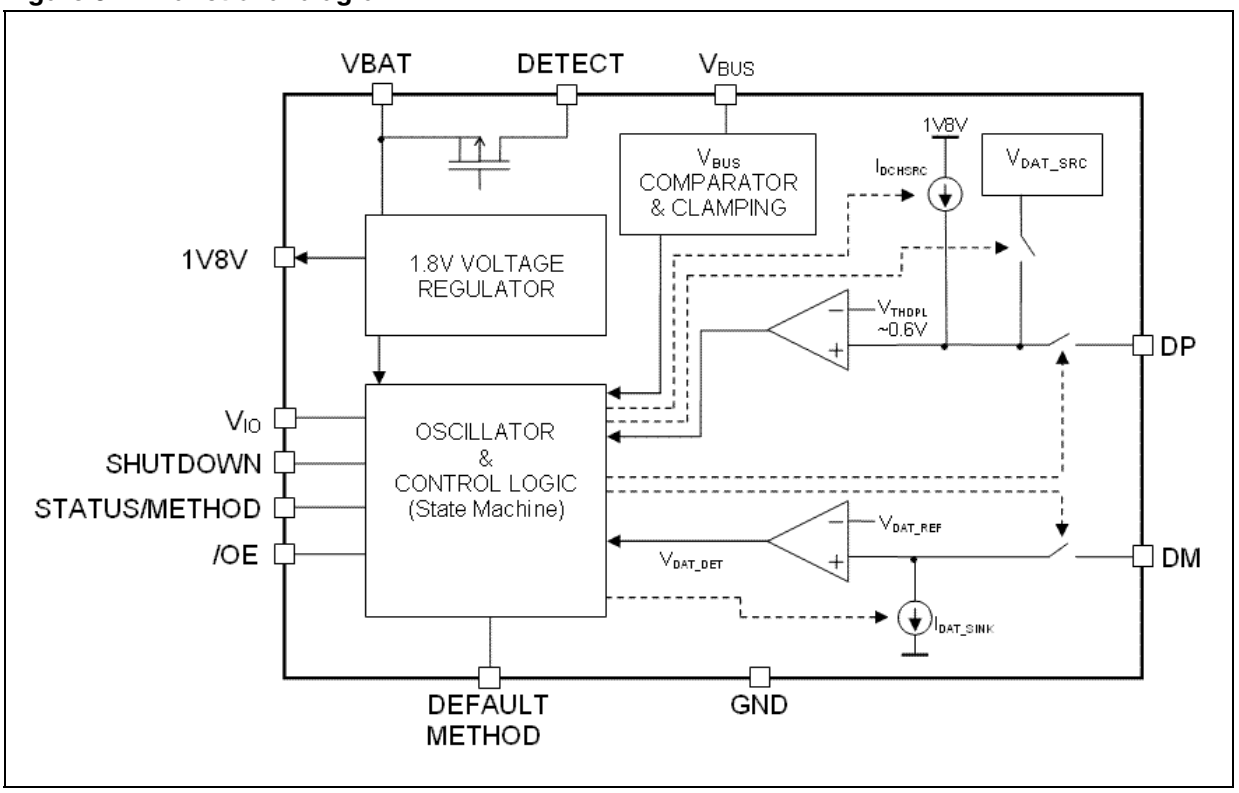
The STUSBCD01B features a built in over voltage protection circuit which prevents V_{BUS} voltage from going over 6 V. The device is able to withstand continuous voltages of up to 10 V applied to V_{BUS} pin through an external resistor; in this case the clamping circuit limits the voltage to 6 V within 1 µs. A 470 Ω resistor in series between V_{BUS} voltage and V_{BUS} pin is required. Any external device needing V_{BUS} over-voltage protection must be connected to STUSBCD01B's V_{BUS} pin.

Minimum input resistance for V_{BUS} pin in normal operating conditions (up to ~ 5.3 V) is 400 kΩ.

3.6 Internal regulator

The STUSBCD01B has an internal regulator which outputs 1.8 V (nominal) to supply internal blocks. The regulator does not require any bypass capacitor for stability.

Figure 3. Functional diagram



4 Functional tables

Table 3. Operating mode

SHUTDOWN	/OE	V_{IO}	VBAT	VBUS	STATUS-DETECT	Operating mode
X	X	X	Not available	X	X	Power down
H	X	Available	Available	Not available	X (1)	Standby (SW control)
-	-	Not available	Available	Not available	L	Standby (NO SW control)
L	X	Available	Available	Available	L	Active, SW detection
-	-	Not available	Available	Available	L	Active, HW detection

1. Low when value is not forced by controller.

Table 4. Output signals

V_{IO}	Shutdown	Detection result	/OE	Status/Method	Detect
Available	L	Charger detected	L	H (pull up active)	Active (driving to V_{BAT})
Available	L	Charger detected	H	H (pull up active)	L (internally pulled down)
Available	L	Charger not detected	X	L (pull down active)	L (internally pulled down)
Available	H	-	X	Input	L (internally pulled down)
Not available	-	Charger detected	-	Undefined	Active (driving to V_{BAT})
Not available	-	Charger not detected	-	Undefined	L (internally pulled down)

Table 5. Pin states during detection

Detection method	DP	DM
Dedicated	Outputs I_{DCH_SRC}	Sinks I_{DAT_SINK}
Current sink	Outputs V_{DAT_SRC}	Sinks I_{DAT_SINK}

Note: See timing diagrams for more details.

5 Maximum ratings

Table 6. Absolute maximum ratings (1)

Symbol	Parameter	Value	Unit
V_{BAT}	Battery supply voltage	6	V
V_{BUS}	USB V_{BUS} voltage	6	V
	USB V_{BUS} voltage with external 470 Ω resistor	12	V
DP, DM, DETECT, DEFAULT METHOD	Detection pins	6	V
V_X	All other pins	-0.5 to 4.6	V
T_{STG}	Storage temperature range	-65 to +150	°C
ESD (2)	Electrostatic discharge voltage (according to HBM JESD22-A114D)	± 2	kV
	Electrostatic discharge voltage (according to CDM JESD22-C101C)	200	V

1. Exceeding the absolute maximum rating may damage the device.
2. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.

Note: Absolute maximum ratings are those values above which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referenced to GND.

Table 7. Recommended operating conditions (1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{BAT}	Analog supply voltage	2.2	4.2	4.5	V
V_{IO}	Interface supply voltage	1.5	1.8	2.8	V
V_{BUS}	V_{BUS} voltage	0		5.25	V

1. The device is not guaranteed to function outside its operating rating.

6 Electrical characteristics

Table 8. DC electrical characteristics (power supply and digital I/O pins) (1)
(V_{BAT} = 4.2 V, T_A = 25°C, specifications over temperature, -40 to 85 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
1V8V	LDO regulated voltage output	$V_{BUS} > V_{TH\_VBUS}$, V_{BAT} = 2.2V to 4.5V	1.76	1.8	1.84	V
I_{BAT}	V_{BAT} supply current	V_{BAT} = 2.2 to 4.5V; Standby mode			20	µA
		V_{BAT} = 2.2 to 4.5V; Detection			1	mA
I_{IO}	V_{IO} supply current	STATUS/METHOD=”open”			5	µA
V_{TH_IO}	V_{IO} detection threshold voltage			1		V
V_{IL}	Low level input voltage (*Note 1*)	V_{IO} = 1.6 to 2.8V			0.15 V_{IO}	V
V_{IH}	High level input voltage (*Note 1*)	V_{IO} = 1.6 to 2.8V	0.85 V_{IO}			V
V_{ILDM}	Low level input voltage (*Note 2*)				0.15 V_{BAT}	V
V_{IHDM}	High level input voltage (*Note 2*)		0.85 V_{BAT}			V
I_{IL}	Low level input leakage (SHUTDOWN, /OE)	V_{IO} = 1.6 to 2.8V, all inputs at GND			±5	µA
I_{IH}	High level input leakage (SHUTDOWN, /OE)	V_{IO} = 1.6 to 2.8V, all inputs at V_{IO}			±5	µA
V_{OL}	Low level output voltage (STATUS)	I_{OL} = +10µA, V_{IO} = 1.8V	0		100	mV
V_{OH}	High level output voltage (STATUS)	I_{OH} = -10µA, V_{IO} = 1.8V	1.7		1.8	V
C_{IN}	Input capacitance (*Note 1*)			4		pF

1. Characterized specification(s), but not production tested.

Note: 1 Specification applies to the following pins: /OE, SHUTDOWN, STATUS/METHOD

2 Specification applies to DEFAULT METHOD pin.

Table 9. DC electrical characteristics (analog pins)
(V_{BAT} = 4.2 V, T_A = 25 °C, specifications over temperature, -40 to 85 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BUS}	V_{BUS} voltage		0		5.25	V
I_{VBUS}	V_{BUS} current	V_{BUS}=0 to 5.25V			10	µA
V_{BUS_CLMP}	V_{BUS} clamping voltage	R_{EXT} = 470Ω	5.3		6	V
V_{TH_VBUS}	V_{BUS} voltage detection threshold		2		4	V
Z_{IN_VBUS}	V_{BUS} input impedance	V_{BUS} max 5.25V	400			kΩ
C_{IN}	DP, DM input capacitance				5	pF
V_{DAT_SRC}	Data source voltage (1)	I_{DP}=I_{DAT_SRC} (2)	0.615	0.65	0.7	V
V_{DAT_REF}	Data detect voltage		0.25		0.34	V
I_{DAT_SINK}	Data sink current	V_{DM}=V_{DAT_SINK} (3)	50		100	µA
I_{DCH_SRC}	Dedicated charger detection DP source current		15		30	µA
V_{THDPL}	DP low threshold			0.6		V
Z_{PD_DET}	DETECT pin pull down impedance	/OE=1	240	300	360	kΩ
V_{OH_DET}	DETECT output driving voltage	I_{OH_DET} = 0.5mA, V_{BAT} = 2.2 to 4.5V	V_{BAT}–0.2		V_{BAT}	V

1. Measured at DP pin. Includes effect of internal switches.
2. I_{DAT_SRC} = 0 to 200 µA according to USB specs.
3. V_{DAT_SINK} = 0.15 V to 3.6 V according to USB specs.

Table 10. AC electrical characteristics (1)
(V_{BAT} = 4.2 V, T_A = 25 °C, specifications over temperature, -40 to 85 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{VBUS_DBNC}	V_{BUS} debounce time		5		8	ms
$T_{DP\_SRC\_ON}$	DP source on time	Current sink method	100		170	ms
$T_{CHGR\_DET\_DBNC}$	Charger detect debounce	Current sink method	20		40	ms
T_{DPSRC_HICRNT}	DP source off to DETECT high time	Current sink method	40		70	ms
T_{D_VDAT}	V_{DAT_SRC} on delay	Current sink method	5		8	ms
$T_{VBUS\_DET\_CS}$	V_{BUS} attach to DETECT high time	Current sink method	150		270	ms
$T_{VBUS\_DET\_DC}$	V_{BUS} attach to DETECT high time	Dedicated charger method	145		248	ms
$T_{IDCH\_SRC\_ON}$	I_{DCH_SRC} on time (2)	Dedicated charger method	140		240	ms
$T_{IDAT\_SINK\_ON}$	I_{DAT_SINK} on time	Dedicated charger method	40		70	ms
$T_{D\_IDAT\_SINK}$	I_{DCH_SRC} on to I_{DAT_SINK} on delay	Dedicated charger method	100		170	ms
T_{PER_DET}	Periodic detection period	Hardware detection, No charger	1		1.6	s
$T_{W\_H/L}$	Minimum pulse width High/Low	All digital inputs	2			µs

1. All AC parameters guaranteed by design but not production tested.
2. $T_{IDCH\_SRC\_ON}$ = $T_{D\_IDAT\_SINK}$ + $T_{IDAT\_SINK\_ON}$

7 Timing diagrams

Figure 4. Current sink method (with charger connected)

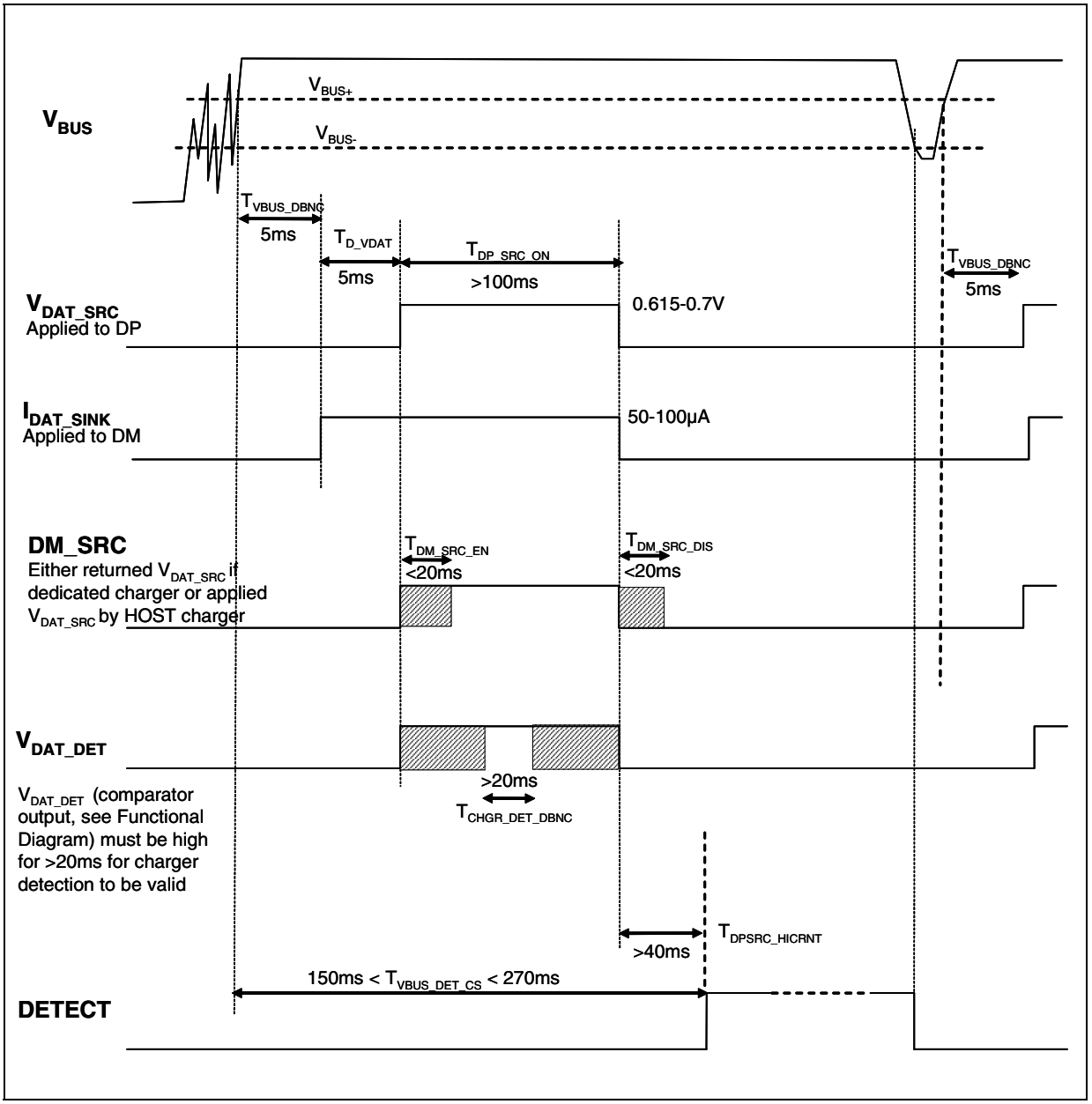
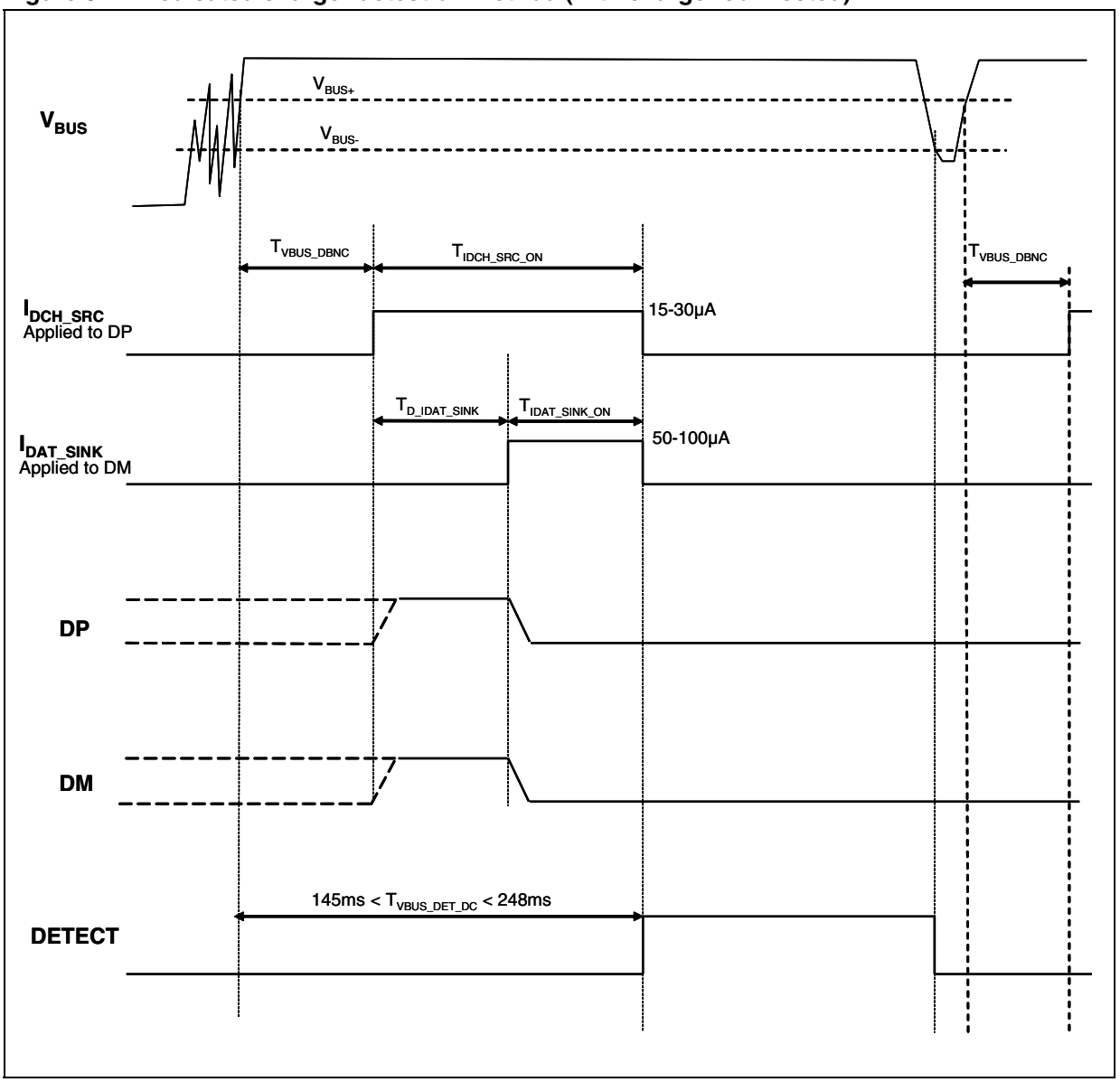


Figure 5. Dedicated charger detection method (with charger connected)

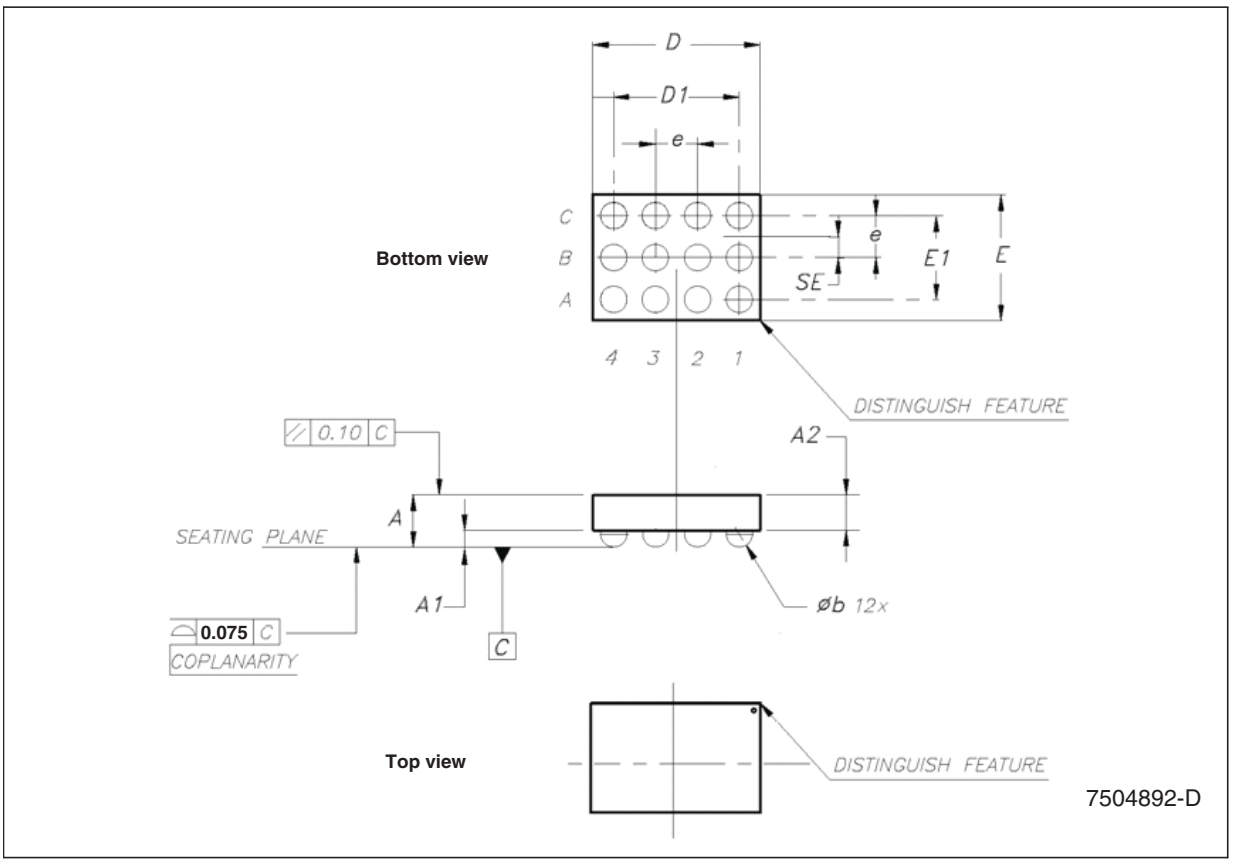


8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

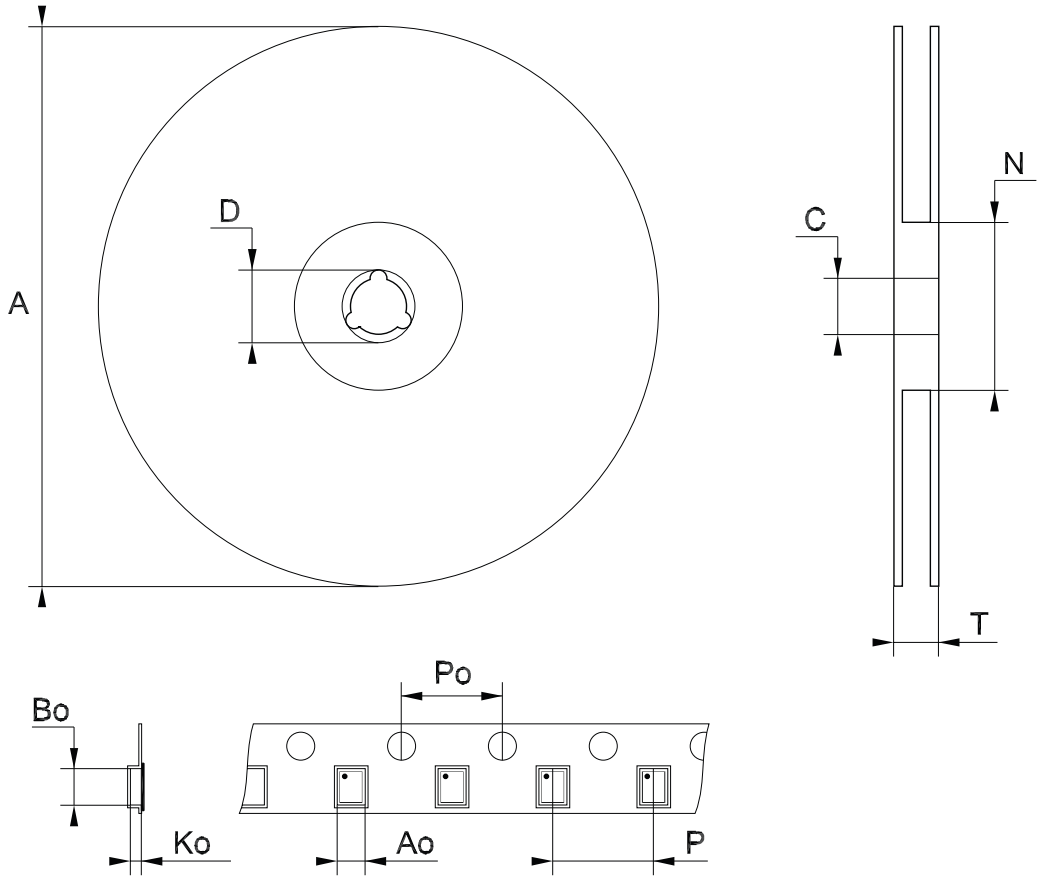
Flip-Chip 12 mechanical data

Dim.	mm.			mils.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.52	0.56	0.60	20.5	22.0	23.6
A1	0.17	0.20	0.23	6.7	7.9	9.1
A2	0.35	0.36	0.37	13.8	14.2	14.6
b	0.23	0.26	0.29	9.1	10.2	11.4
D	1.543	1.593	1.643	60.7	62.7	64.7
D1		1.20			47.2	
E	1.15	1.202	1.25	45.3	47.3	49.2
E1		0.80			31.5	
e		0.40			15.7	
SE		0.20			7.9	



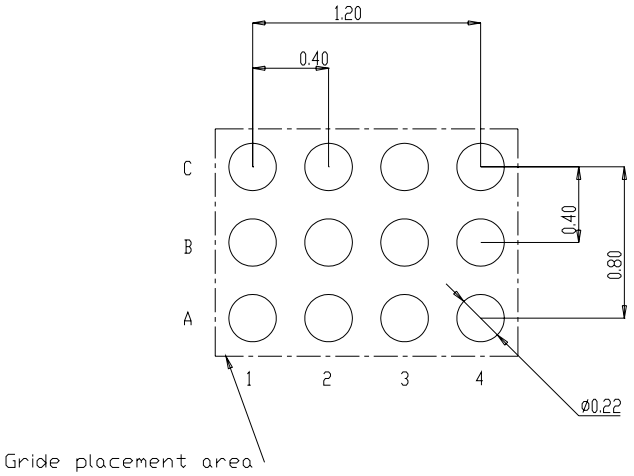
Tape & reel Flip-Chip 12 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			180			7.087
C	12.8		13.2	0.504		0.520
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	1.43	1.48	1.53	0.056	0.058	0.060
Bo	1.71	1.76	1.81	0.067	0.069	0.071
Ko	0.75	0.80	0.85	0.030	0.031	0.033
Po	3.9		4.1	0.154		0.161
P	3.9		4.1	0.154		0.161



Note: Drawing not in scale

Figure 6. Footprint data (mm.)



9 Revision history

Table 11. Document revision history

Date	Revision	Changes
18-Nov-2008	1	Initial release.

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