Quad, 235 MHz, DC-Coupled VGA and Differential Output Amplifier

Data Sheet **AD8264**

FEATURES

- **Low noise**
  - **Voltage noise: 2.3 nV/√Hz**
  - **Current noise: 2 pA/√Hz**
- **Wide bandwidth**
  - **Small signal: 235 MHz (VGAx); 80 MHz (output amplifier)**
  - **Large signal: 80 MHz (1 V p-p)**
- **Gain range**
  - **0 to 24 dB (input to VGA output)**
  - **6 to 30 dB (input to differential output)**
- **Gain scaling: 20 dB/V**
- **DC-coupled**
- **Single-ended input and differential output**
- **Supplies: ±2.5 V to ±5 V**
- **Low power: 140 mW per channel at ±3.3 V**

APPLICATIONS

- **Multichannel data acquisition**
- **Positron emission tomography**
- **Gain trim**
- **Industrial and medical ultrasound**
- **Radar receivers**

GENERAL DESCRIPTION

The AD8264 is a quad, linear-in-dB, general-purpose, variable gain amplifier (VGA) with a preamplifier (preamp), and a flexible differential output buffer. DC coupling, combined with wide bandwidth, makes this amplifier a very good pulse processor. Each channel includes a single-ended input preamp/VGA section to preserve the wide bandwidth and fast slew rate for low distortion pulse applications. A 6 dB differential output buffer with common-mode and offset adjustments enable direct coupling to most modern high speed analog-to-digital converters (ADCs), using the converter reference output for perfect dc matching levels.

The −3 dB bandwidth of the preamp/VGA is dc to 235 MHz, and the bandwidth of the differential driver is 80 MHz. The floating gain control interface provides a precise linear-in-dB scale of 20 dB/V and is easy to interface to a variety of external circuits. The gain of each channel is adjusted independently, and all channels are referenced to a single pin, GNLO. Combined with a multioutput, digital-to-analog converter (DAC), each section of the AD8264 can be used for active calibration or as a trim amplifier.

Operation from a bipolar power supply enables amplification of negative voltage pulses generated by current-sinking pulses into a grounded load, such as is typical of photodiodes or photomultiplier tubes (PMT). Delay-free processing of wideband video signals is also possible.

FUNCTIONAL BLOCK DIAGRAM

ONE CHANNEL SHOWN

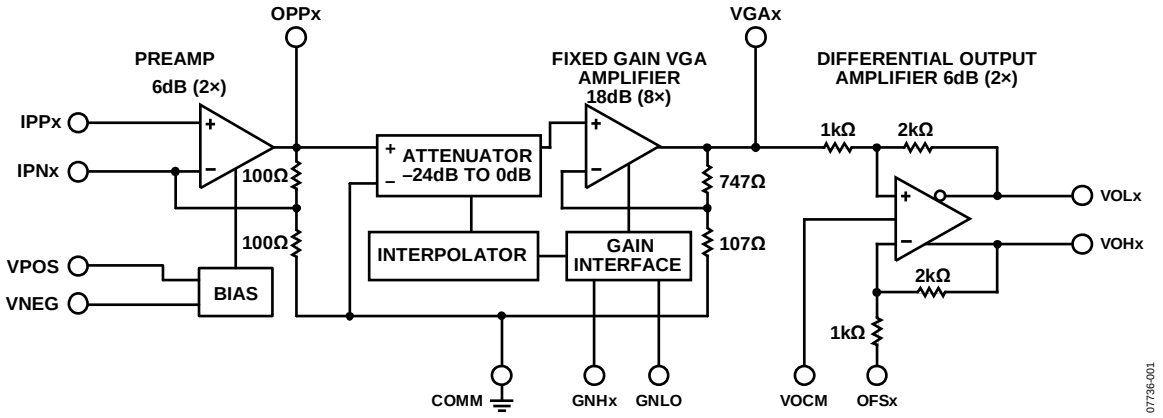

Figure 1.

Rev. C **Document Feedback**

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TABLE OF CONTENTS

REVISION HISTORY

10/2018—Rev. B to Rev. C

Deleted Figure 113 ... 31
Added Figure 113; Renumbered Sequentially ... 31
Updated Outline Dimensions ... 37

1/2016—Rev. A to Rev. B

Changes to Features Section, General Description Section, and Figure 1 ... 1
Changes to Figure 2 ... 7
Changes to VGA Section ... 28
Updated Outline Dimensions ... 37
Changes to Ordering Guide ... 37

1/2011—Rev. 0 to Rev. A

Changes to Figure 1 ... 1
Changes to Connecting and Using the AD8264-EVALZ Section and Figure 117 ... 34
Changes to Figure 118 ... 35

5/2009—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±2.5 V, T_A = 25°C, f = 10 MHz, C_L = 5 pF, R_L = 500 Ω per output (VGAx, VOHx, VOLx), V_{GAIN} = (V_{GNHx} − V_{GNLO}) = 0 V, V_{VOCM} = GND, V_{OFSx} = GND, gain range = 6 dB to 30 dB, unless otherwise specified.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GENERAL PERFORMANCE					
−3 dB Small Signal Bandwidth (VGAx)	V_{OUT} = 10 mV p-p		235		MHz
−3 dB Large Signal Bandwidth (VGAx)	V_{OUT} = 1 V p-p		150		MHz
−3 dB Small Signal Bandwidth (Differential Output)[1]	V_{OUT} = 100 mV p-p		80		MHz
−3 dB Large Signal Bandwidth (Differential Output)[1]	V_{OUT} = 2 V p-p		80		MHz
Slew Rate	VGAx, V_{OUT} = 2 V p-p		380		V/µs
	VGAx, V_{OUT} = 1 V p-p		290		V/µs
	Differential output, V_{OUT} = 2 V p-p		470		V/µs
	Differential output, V_{OUT} = 1 V p-p		220		V/µs
Input Bias Current	Pins IPPx	−8	−5	−3	µA
Input Resistance	Pins IPPx at dc; $\Delta V_{IN}/\Delta I_{BIAS}$		4.2		MΩ
Input Capacitance	Pins IPPx		2		pF
Input Impedance	Pins IPPx at 10 MHz		7.9		kΩ
Input Voltage Noise			2.3		nV/√Hz
Input Current Noise			2		pA/√Hz
Noise Figure (Differential Output)	V_{GAIN} = 0.7 V, R_S = 50 Ω, unterminated		9		dB
Output-Referred Noise (Differential Output)	V_{GAIN} = 0.7 V (Gain = 30 dB)		72		nV/√Hz
	V_{GAIN} = −0.7 V (Gain = 6 dB)		45		nV/√Hz
Output Impedance	VGAx, dc to 10 MHz		3.5		Ω
	Differential output, dc to 10 MHz		<1		Ω
Output Signal Range	Preamp		$\|V_S\|$ − 1.3		V
	VGAx, R_L ≥ 500 Ω		$\|V_S\|$ − 1.3		V
	Differential amplifier, R_L ≥ 500 Ω per side		$\|V_S\|$ − 0.5		V
Output Offset Voltage	Preamp offset	−6	|<1|	+6	mV
	VGAx offset, V_{GAIN} = 0.7 V	−18	|<5|	+18	mV
	Differential output offset, V_{GAIN} = 0.7 V	−38	|<10|	+38	mV
DYNAMIC PERFORMANCE					
Harmonic Distortion	VGAx = 1 V p-p, differential output = 2 V p-p (measured at VGAx)				
HD2	f = 1 MHz		−73		dBc
HD3			−68		dBc
HD2	f = 10 MHz		−71		dBc
HD3			−61		dBc
HD2	f = 35 MHz		−60		dBc
HD3			−53		dBc
	VGAx = 1 V p-p, differential output = 2 V p-p (measured at differential output)				
HD2	f = 1 MHz		−78		dBc
HD3			−66		dBc
HD2	f = 10 MHz		−71		dBc
HD3			−43		dBc
HD2	f = 35 MHz		−56		dBc
HD3			−20		dBc
Input 1 dB Compression Point	V_{GAIN} = −0.7 V, f = 10 MHz		7		dBm[2]
	V_{GAIN} = +0.7 V, f = 10 MHz		−9.6		dBm

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Two-Tone Intermodulation Distortion (IMD3)	VGAx = 1 V p-p, f_1 = 10 MHz, f_2 = 11 MHz		−68		dBc
	VGAx = 1 V p-p, f_1 = 35 MHz, f_2 = 36 MHz		−51		dBc
	V_{OUT} = 2 V p-p, f_1 = 10 MHz, f_2 = 11 MHz		−49		dBc
	V_{OUT} = 2 V p-p, f_1 = 35 MHz, f_2 = 36 MHz		−34		dBc
Output Third-Order Intercept	VGAx = 1 V p-p, f = 10 MHz		32		dBm
			19		dBV_{RMS}
	VGAx = 1 V p-p, f = 35 MHz		23		dBm
			10		dBV_{RMS}
	V_{OUT} = 2 V p-p, f = 10 MHz		30		dBm
			17		dBV_{RMS}
	V_{OUT} = 2 V p-p, f = 35 MHz		21		dBm
			8		dBV_{RMS}
Overload Recovery	V_{GAIN} = 0.7 V, V_{IN} stepped from 0.1 V p-p to 1 V p-p		25		ns
Group Delay Variation	1 MHz < f < 100 MHz, full gain range		±1		ns
ACCURACY					
Absolute Gain Error[3]	−0.7 V < V_{GAIN} < −0.6 V	0	0.2 to 2	3	dB
	−0.6 V < V_{GAIN} < −0.5 V	−1.25	±0.35	+1.25	dB
	−0.5 V < V_{GAIN} < +0.5 V	−1	±0.25	+1	dB
	0.5 V < V_{GAIN} < 0.6 V	−1.25	±0.35	+1.25	dB
	0.6 V < V_{GAIN} < 0.7 V	−3	−0.2 to −2	0	dB
Gain Law Conformance[4]	−0.5 V < V_{GAIN} < +0.5 V, ±2.5 V ≤ V_S ≤ ±5 V		±0.2		dB
	−0.5 V < V_{GAIN} < +0.5 V, −40°C ≤ T_A ≤ +105°C		±0.3		dB
Channel-to-Channel Matching	Single IC, −0.5 V < V_{GAIN} < +0.5 V, −40°C ≤ T_A ≤ +105°C	−0.5	±0.1 to ±0.25	+0.5	dB
	Multiple ICs, −0.5 V < V_{GAIN} < +0.5 V, −40°C ≤ T_A ≤ +105°C		±0.25		dB
GAIN CONTROL INTERFACE					
Gain Scaling Factor	−0.5 V < V_{GAIN} < +0.5 V	19.5	20.0	20.5	dB/V
Over Temperature	−40°C ≤ T_A ≤ +105°C		20 ± 0.5		dB/V
Gain Range			24		dB
Gain Intercept to VGAx		11.5	11.9	12.2	dB
Over Temperature	−40°C ≤ T_A ≤ +105°C		11.9 ± 0.4		dB
Gain Intercept to Differential Output		17.5	17.9	18.2	dB
Over Temperature	−40°C ≤ T_A ≤ +105°C		17.9 ± 0.4		dB
GNHx Input Voltage Range	GNLO = 0 V, no gain foldover	$-V_S$		$+V_S$	V
Input Resistance	$\Delta V_{IN}/\Delta I_{BIAS}$, −0.7 V < V_{GAIN} < +0.7 V		70		MΩ
GNHx Input Bias Current	−0.7 V < V_{GAIN} < 0.7 V	−0.9	−0.4	0	µA
Over Temperature	−0.7 V < V_{GAIN} < 0.7 V, −40°C ≤ T_A ≤ +105°C		−0.4 ± +0.2		µA
GNLO Input Bias Current	−0.7 V < V_{GAIN} < 0.7 V		−1.2		µA
Over Temperature	−0.7 V < V_{GAIN} < 0.7 V, −40°C ≤ T_A ≤ +105°C		−1.2 ± +0.4		µA
Response Time	24 dB gain change		200		ns
OUTPUT BUFFER					
VOCM Input Bias Current		0.3	1.5	2.5	nA
Over Temperature	−40°C ≤ T_A ≤ +105°C		1.5 ± 0.3		nA
VOCM Input Voltage Range	OFSx = 0 V, VGAx = 0 V	−1.4		+1.4	V
Gain (VGAx to Differential Output)		5.75	6	6.25	dB
Over Temperature	−40°C ≤ T_A ≤ +105°C		6 ± 0.5		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Supply Voltage		±2.5		±5	V
Power Consumption					
Quiescent Current					
	V_S = ± 2.5 V	65	79	88	mA
	V_S = ± 2.5 V, −40°C ≤ T_A ≤ +105°C		79 ± 25		mA
	V_S = ± 3.3 V	70	85	95	mA
	V_S = ± 3.3 V, −40°C ≤ T_A ≤ +105°C		85 ± 30		mA
	V_S = ± 5 V	81	99	110	mA
	V_S = ± 5 V, −40°C ≤ T_A ≤ +85°C[5]		99 ± 30		mA
Power Dissipation	V_S = ± 2.5 V		395		mW
	V_S = ±3.3 V		560		mW
	V_S = ±5 V		990		mW
PSRR	From VPOS to differential output, V_{GAIN} = 0.7 V		−15		dB
	From VNEG to differential output, V_{GAIN} = 0.7 V		−15		dB

[1] Differential output = (VOHx − VOLx).
[2] All dBm values are calculated with 50 Ω reference, unless otherwise noted.
[3] Conformance to theoretical gain expression (see Equation 1 in the Theory of Operation section).
[4] Conformance to best-fit dB linear curve.
[5] For supplies greater than ±3.3 V, the operating temperature range is limited to −40°C ≤ T_A ≤ +85°C.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltage	
Supply Voltage (VPOS, VNEG)	±6 V
Input Voltage (INPx)	VPOS, VNEG
Gain Voltage (GNHx, GNLO)	VPOS, VNEG
Power Dissipation	2.5 W
Temperature	
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Package Glass Transition Temperature (T_G)	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. The θ_{JA} values in Table 3 assume a 4-layer JEDEC standard board with zero airflow.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-40-9[1]	31.0	2.3	°C/W

[1] 4-Layer JEDEC board (2S2P).

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the AD8264 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a temperature of 150°C for an extended period can cause changes in silicon devices, potentially resulting in a loss of functionality.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

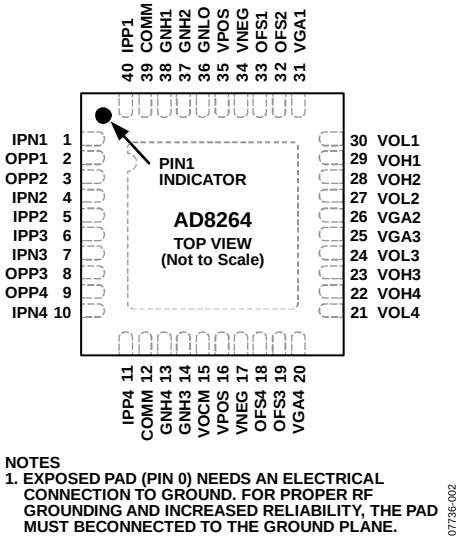


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
0 (EP), 12, 39	COMM	Ground. Exposed pad (EP, Pin 0) needs an electrical connection to ground. For proper RF grounding and increased reliability, the pad must be connected to the ground plane.
1, 4, 7, 10	IPN1, IPN2, IPN3, IPN4	Negative Preamp Inputs for Channel 1 Through Channel 4. Normally, no external connection is needed.
2, 3, 8, 9	OPP1, OPP2, OPP3, OPP4	Preamp Output for Channel 1 Through Channel 4. This pin is internally connected to the attenuator (VGA) input, and normally, no external connection is needed.
5, 6, 11, 40	IPP1, IPP2, IPP3, IPP4	Positive Preamp Input for Channel 1 Through Channel 4. High impedance.
13, 14, 37, 38	GNH1, GNH2, GNH3, GNH4	Positive Gain Control Voltage Input for Channel 1 Through Channel 4. This pin is referenced to GNLO (Pin 36).
15	VOCM	This pin sets the differential output amplifier (VOHx and VOLx) common-mode voltage.
16, 35	VPOS	Positive Supply (Internally Tied Together).
17, 34	VNEG	Negative Supply (Internally Tied Together).
18, 19, 32, 33	OFS1, OFS2, OFS3, OFS4	Voltage sets the differential output offset for Channel 1 through Channel 4. This is the noninverting input to the differential amplifier, and it has the same bandwidth as the inverting input (VGAx).
20, 25, 26, 31	VGA4, VGA3 VGA2, VGA1	VGA Output for Channel 1 Through Channel 4.
21, 24, 27, 30	VOL1, VOL2 VOL3, VOL4	Negative Differential Amplifier Output for Channel 1 Through Channel 4.
22, 23, 28, 29	VOH1, VOH2, VOH3, VOH4	Positive Differential Amplifier Output for Channel 1 Through Channel 4.
36	GNLO	Negative Gain Control Input (Reference for GNHx Pins).

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±2.5 V, T_A = 25°C, f = 10 MHz, C_L = 5 pF, R_L = 500 Ω per output (VGAx, VOHx, VOLx), V_{GAIN} = (V_{GNHx} − V_{GNLO}) = 0 V, V_{VOCM} = GND, V_{OFSx} = GND, gain range = 6 dB to 30 dB, unless otherwise specified.

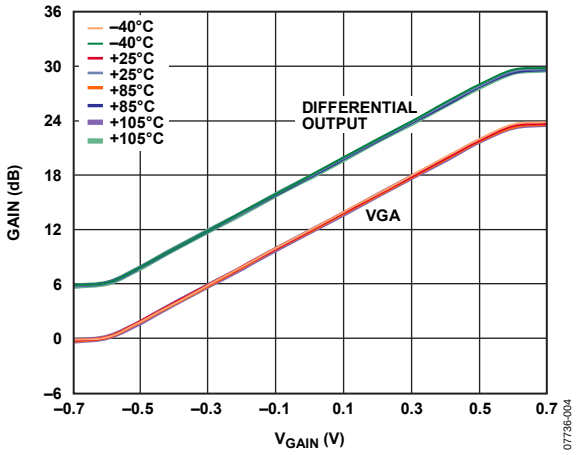


Figure 3. Gain vs. V_{GAIN} vs. Temperature

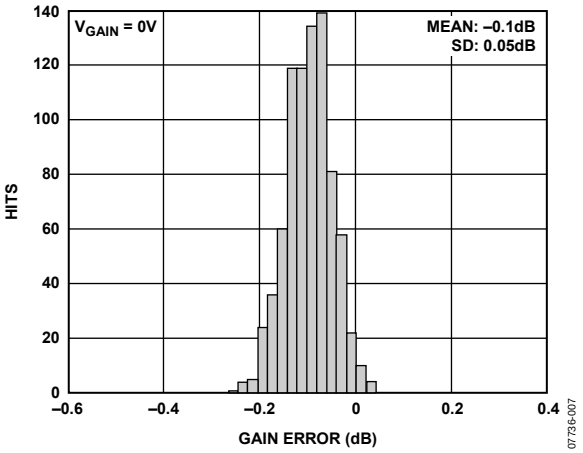


Figure 6. VGA Absolute Gain Error Histogram

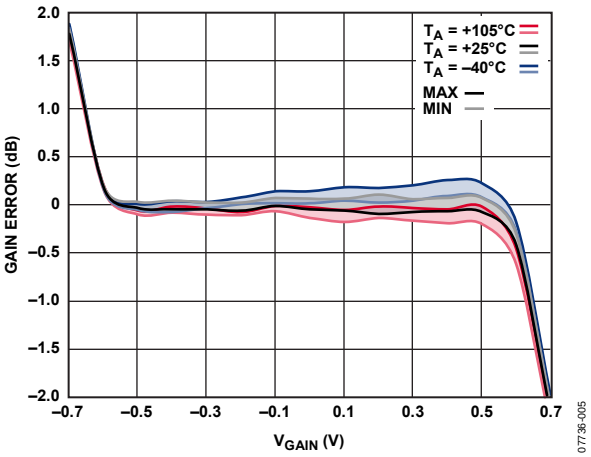


Figure 4. Gain Error vs. V_{GAIN} vs. Temperature

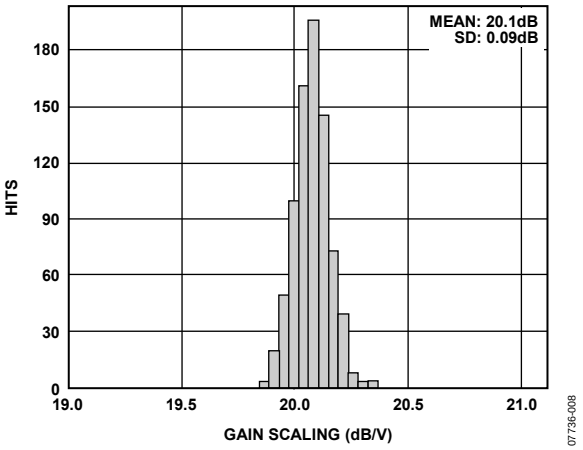


Figure 7. Gain Scale Factor Histogram (–0.4 V < V_{GAIN} < +0.4 V)

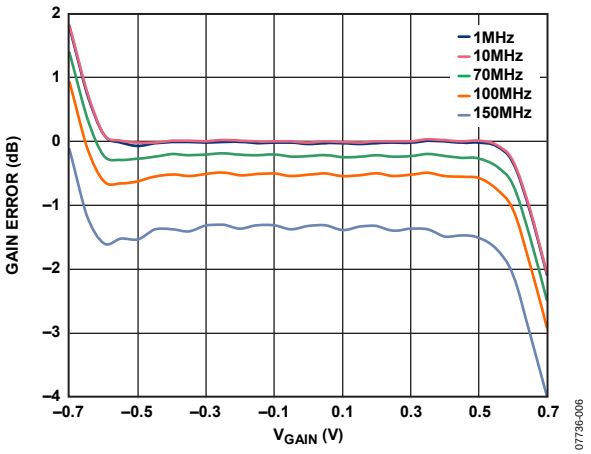


Figure 5. Gain Error vs. V_{GAIN} at Various Frequencies to VGAx

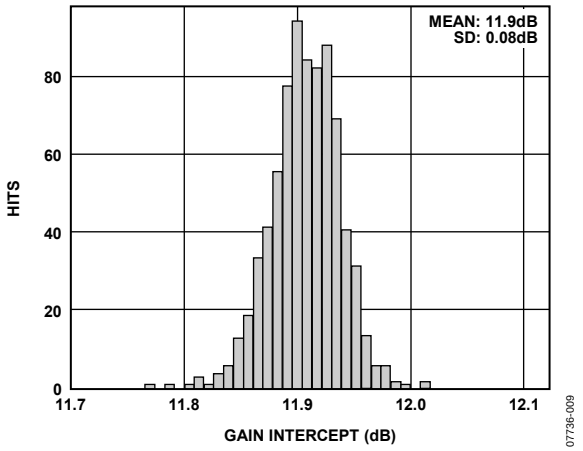


Figure 8. VGA Gain Intercept Histogram

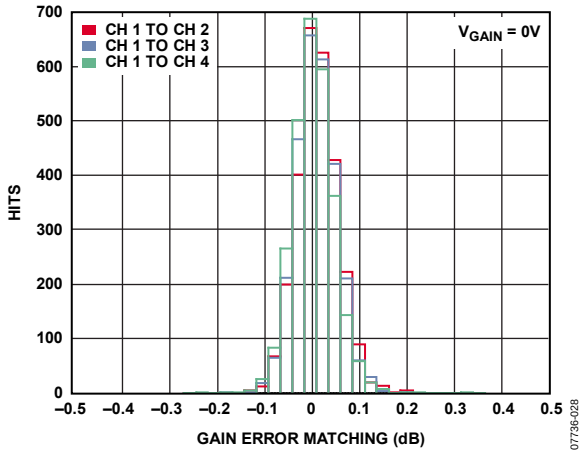


Figure 9. Channel-to-Channel Gain Match Histogram

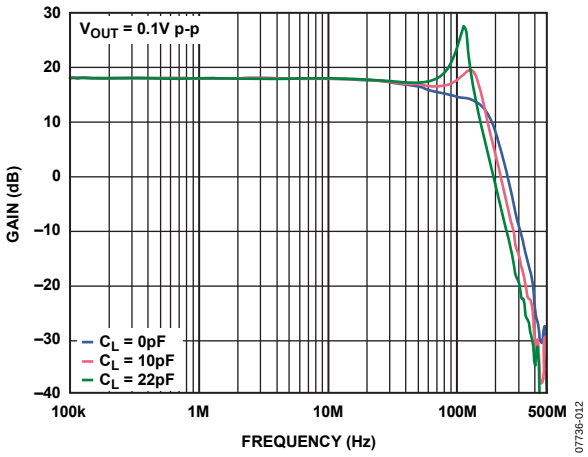


Figure 12. Frequency Response to Differential Output for Various Capacitive Loads

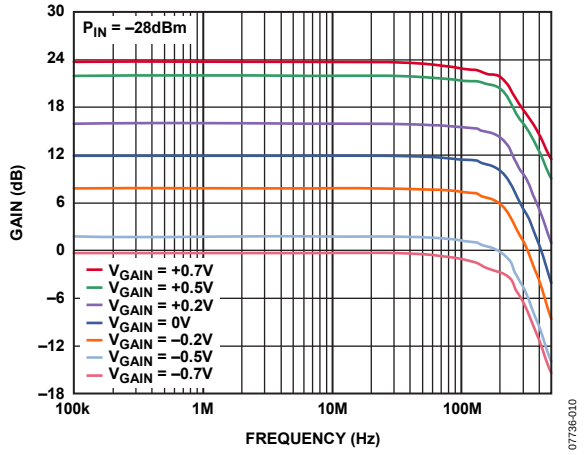


Figure 10. Frequency Response vs. Gain to VGAx for Various Values of V_{GAIN}

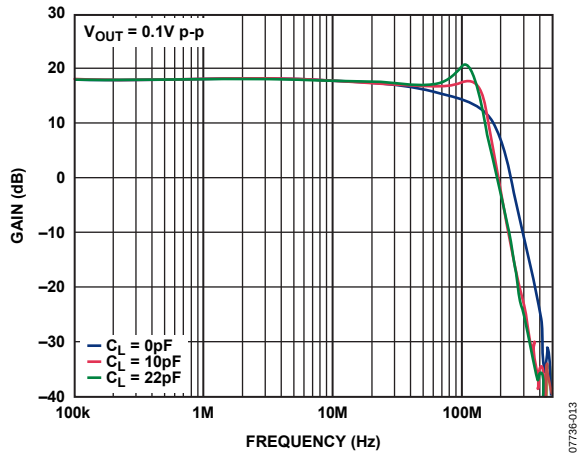


Figure 13. Frequency Response to Differential Output for Various Capacitive Loads with Series R = 10 Ω

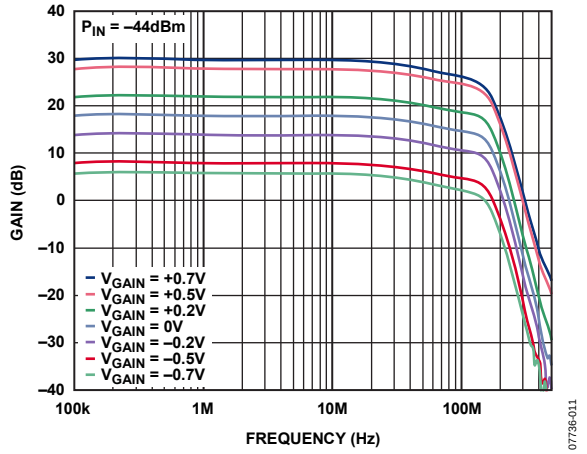


Figure 11. Frequency Response vs. Gain to Differential Output for Various Values of V_{GAIN}

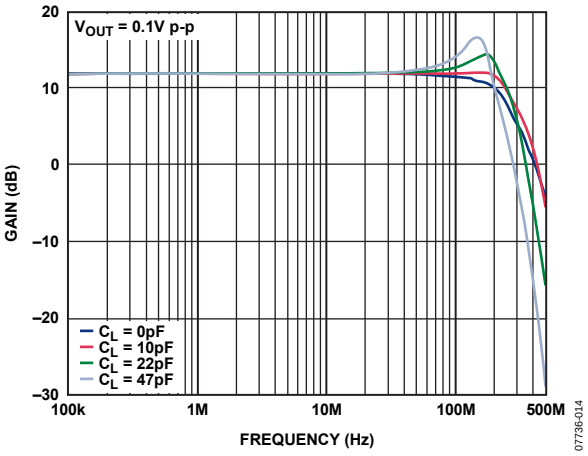


Figure 14. Small Signal Frequency Response to VGAx for Various Capacitive Loads

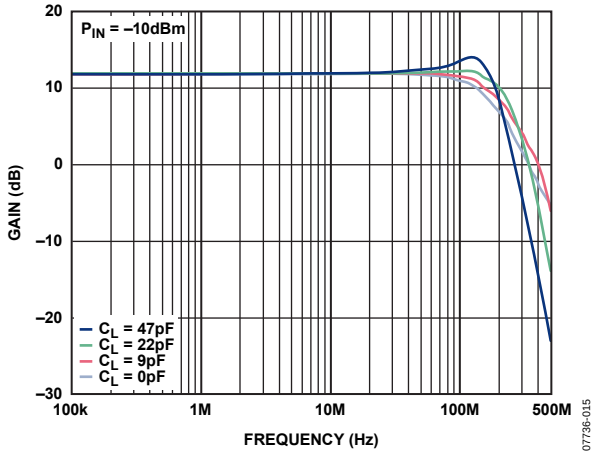


Figure 15. Large Signal Frequency Response to VGAx for Various Capacitive Loads

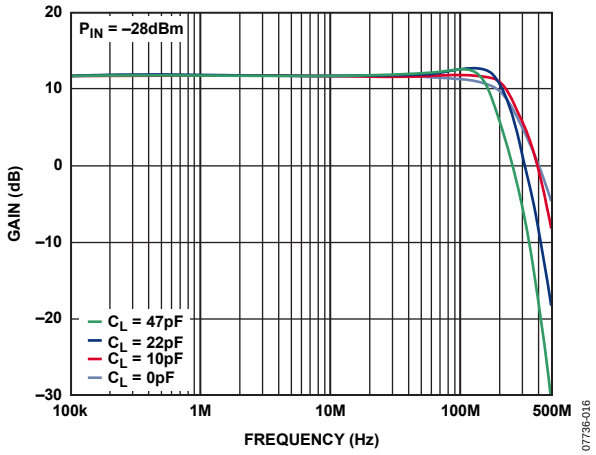


Figure 16. Small Signal Frequency Response to VGAx for Various Capacitive Loads with Series R = 10 Ω

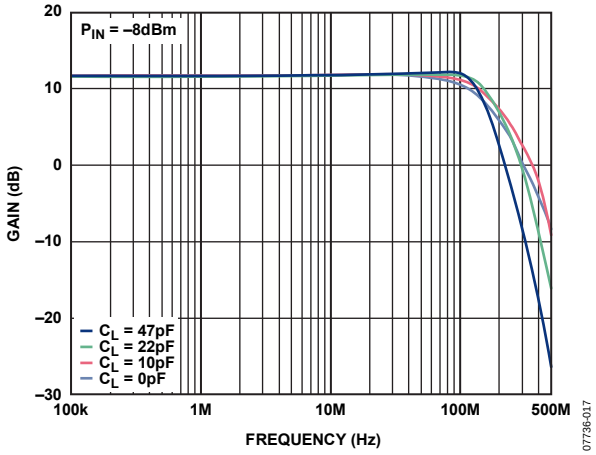


Figure 17. Large Signal Frequency Response to VGAx for Various Capacitive Loads with Series R = 10 Ω

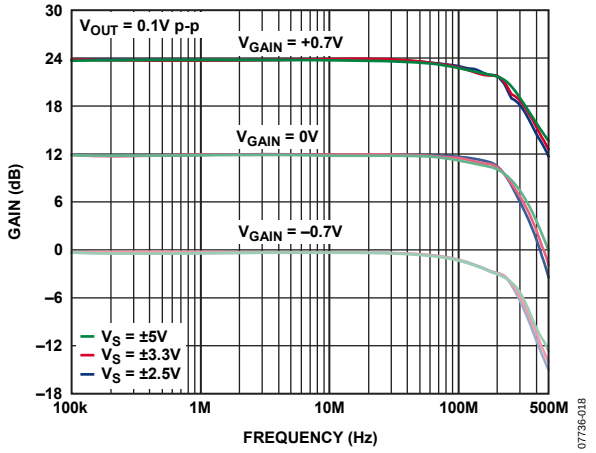


Figure 18. Small Signal Frequency Response vs. Gain to VGAx for Various Supply Voltages

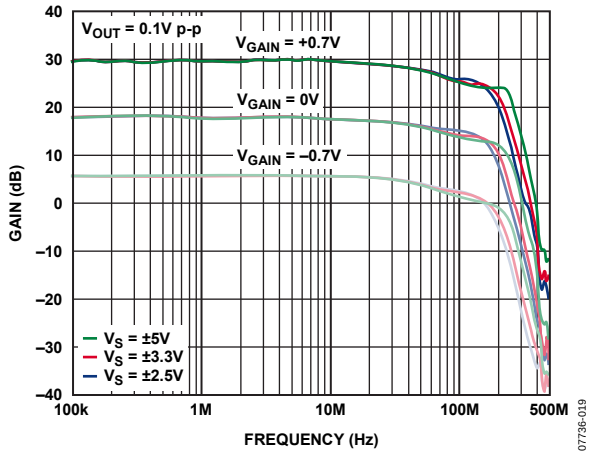


Figure 19. Small Signal Frequency Response vs. Gain to Differential Output for Various Supply Voltages

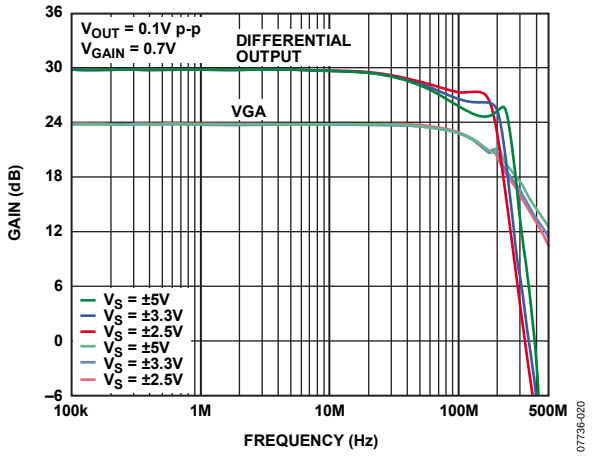


Figure 20. Large Signal Frequency Response to VGAx and Differential Output for Various Supply Voltages

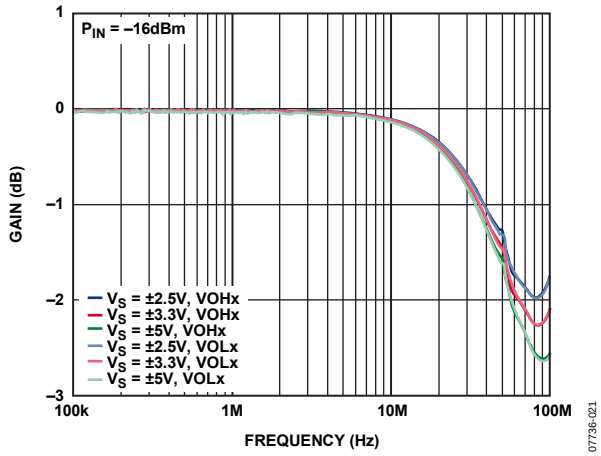


Figure 21. Frequency Response from VOCM to VOHx and VOLx for Various Supplies

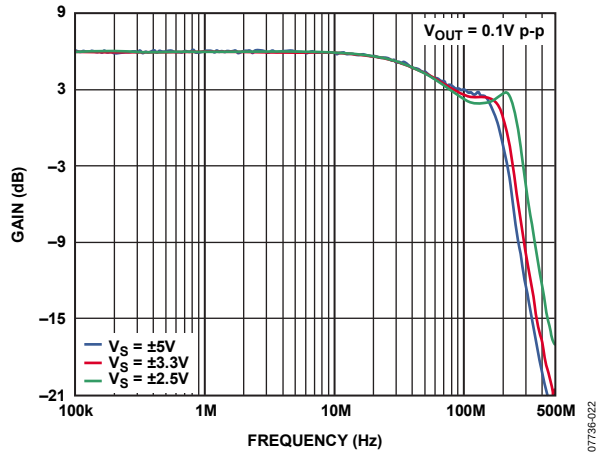


Figure 22. Frequency Response from OFSx to Differential Output for Various Supply Voltages

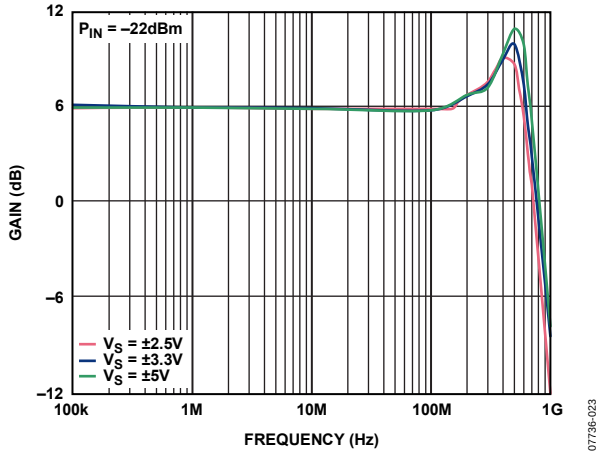


Figure 23. Preamp Frequency Response to OPPx

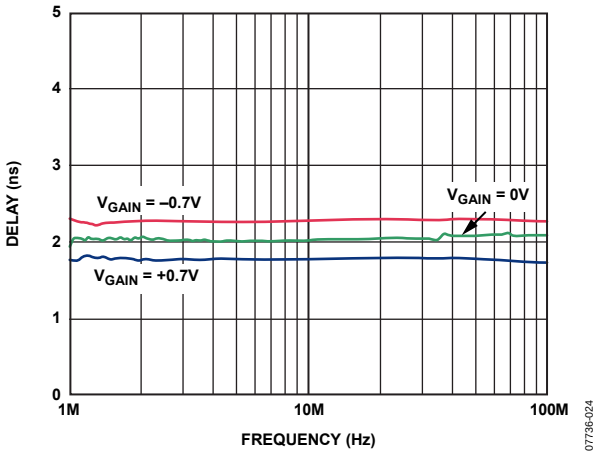


Figure 24. Group Delay vs. Frequency to VGAx

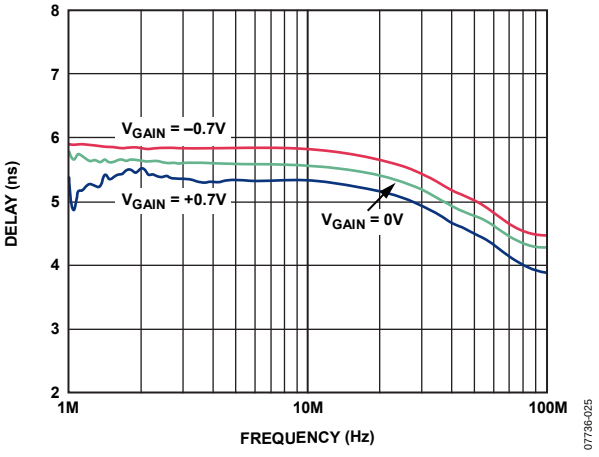


Figure 25. Group Delay vs. Frequency to Differential Output

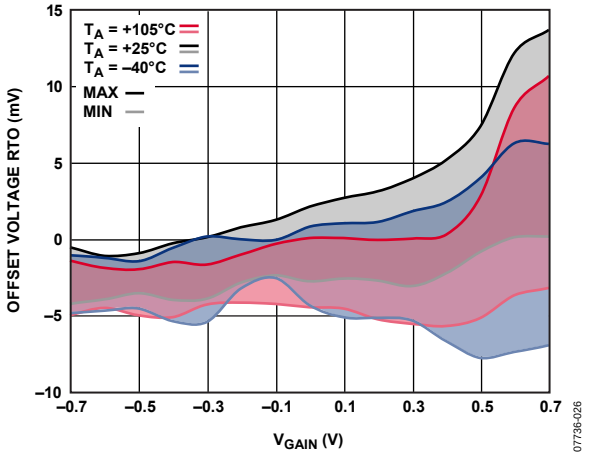


Figure 26. Differential Output Offset Voltage vs. V_{GAIN} vs. Temperature

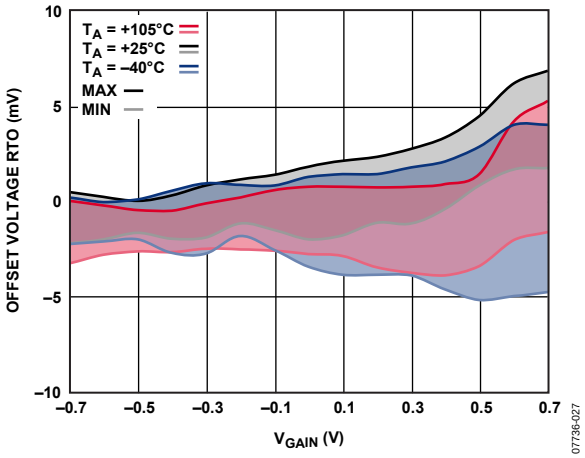


Figure 27. VGAx Output Offset Voltage vs. V_{GAIN} vs. Temperature

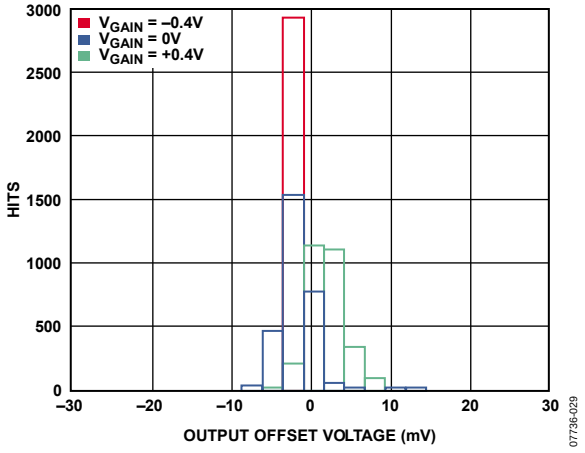


Figure 28. Output Offset Histogram to VGAx

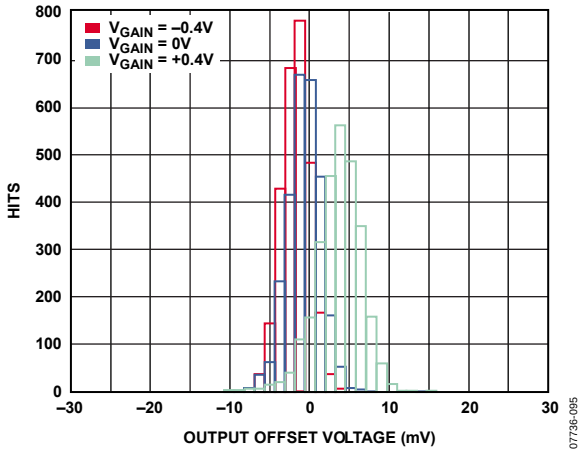


Figure 29. Output Offset Histogram to Differential Output

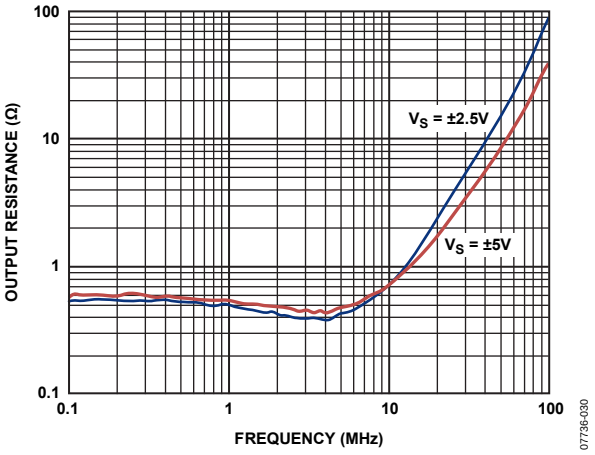


Figure 30. Output Resistance (VOHx, VOLx) vs. Frequency

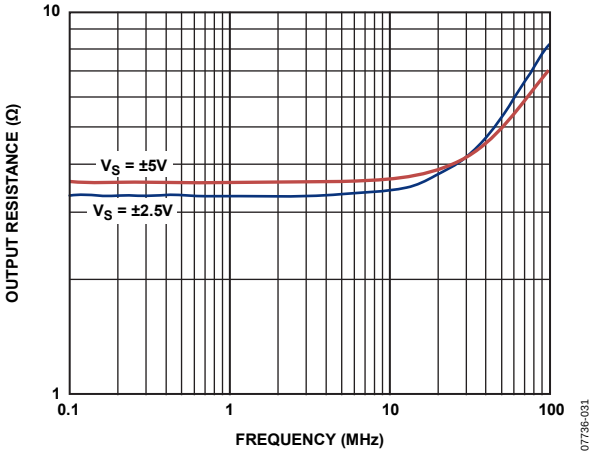


Figure 31. Output Resistance (VGAx) vs. Frequency

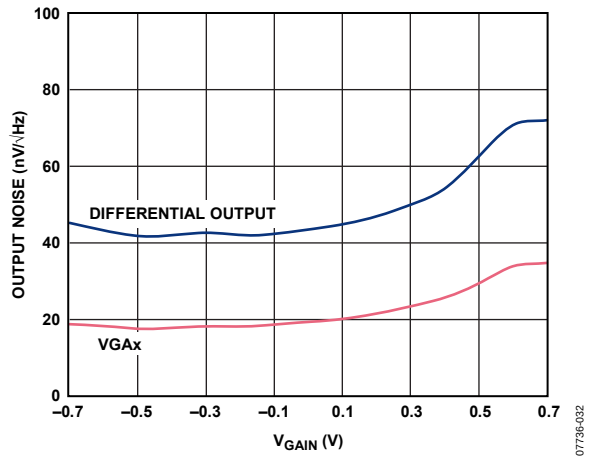


Figure 32. Output Referred Noise to VGAx and Differential Output vs. V_{GAIN}

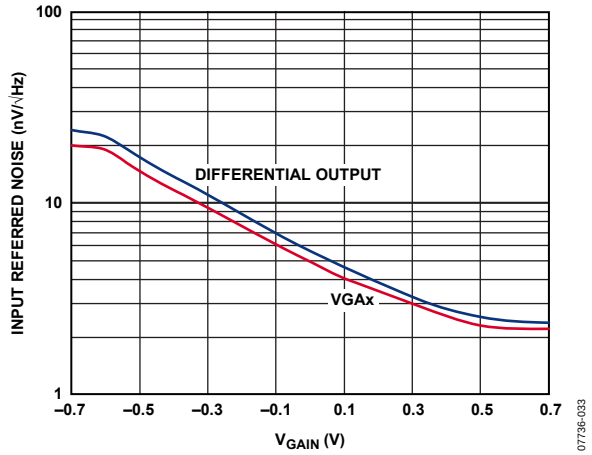


Figure 33. Input Referred Noise from VGAx and Differential Output vs. V_{GAIN}

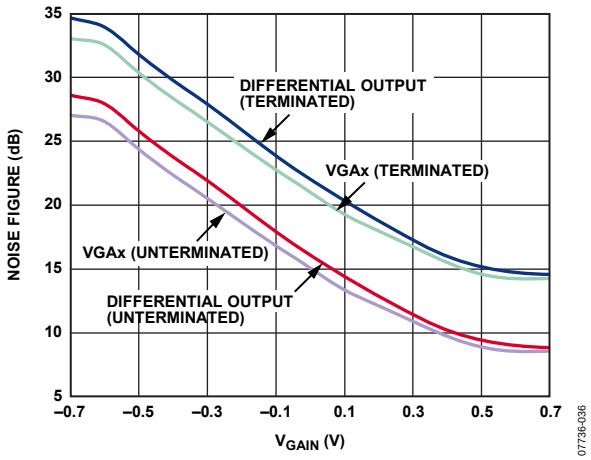


Figure 36. Noise Figure vs. V_{GAIN}

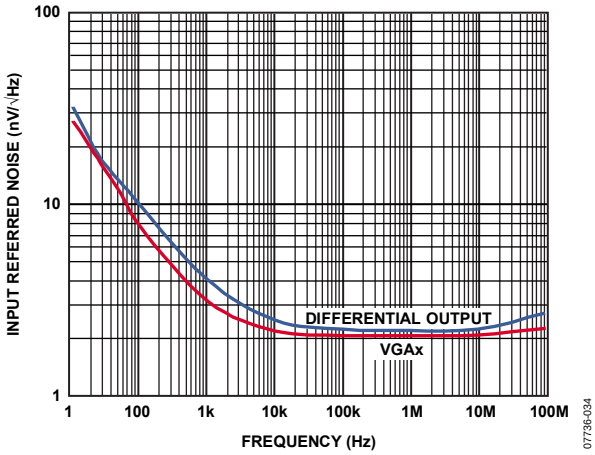


Figure 34. Input Referred Noise vs. Frequency at Maximum Gain

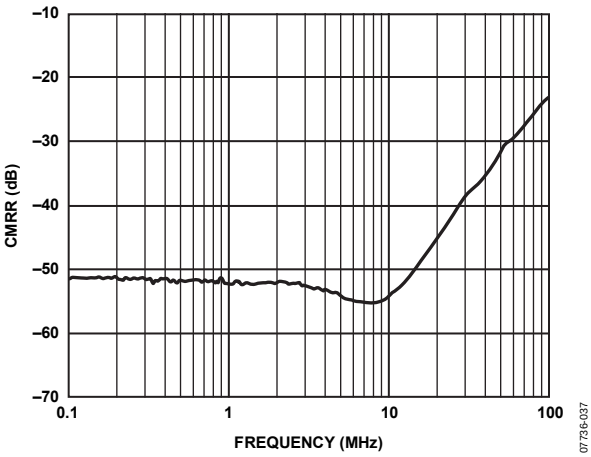


Figure 37. VOCM Common-Mode Rejection Ratio vs. Frequency

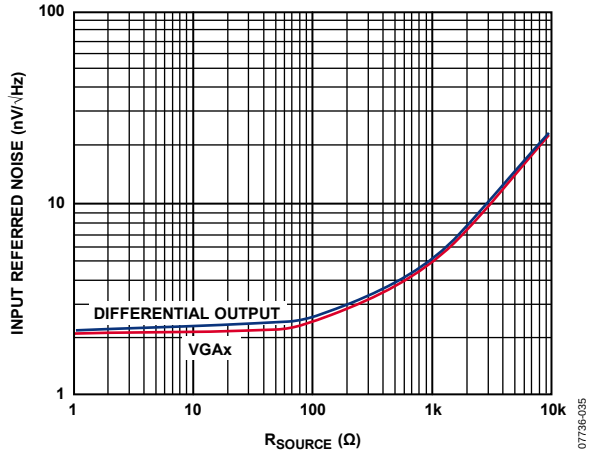


Figure 35. Input Referred Noise vs. R_{SOURCE}

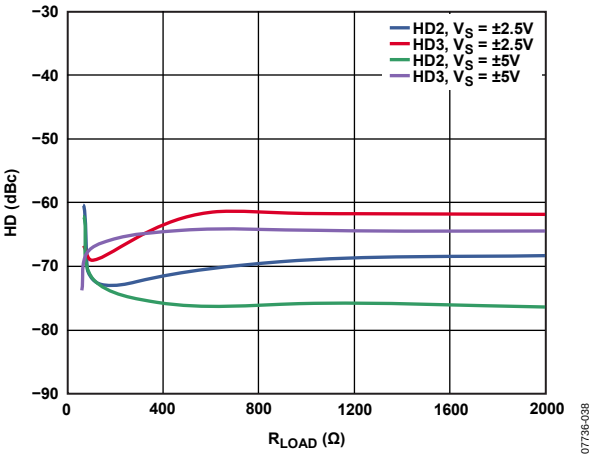


Figure 38. Harmonic Distortion to VGAx vs. R_{LOAD} and Various Supplies

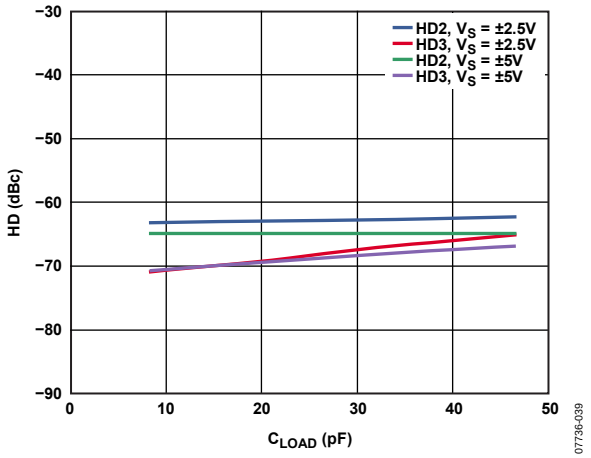


Figure 39. Harmonic Distortion to VGAx vs. C_{LOAD}

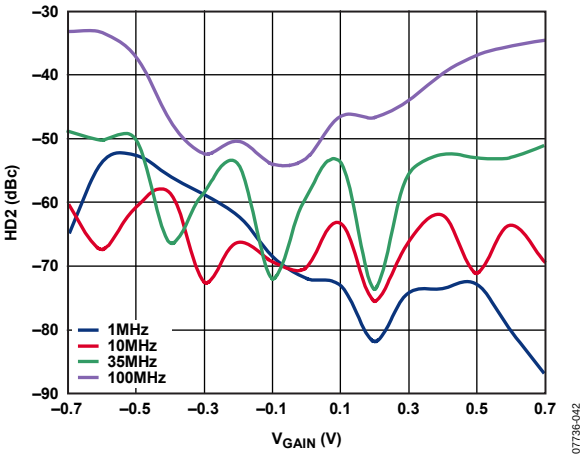


Figure 42. HD2 vs. V_{GAIN} vs. Frequency to VGAx

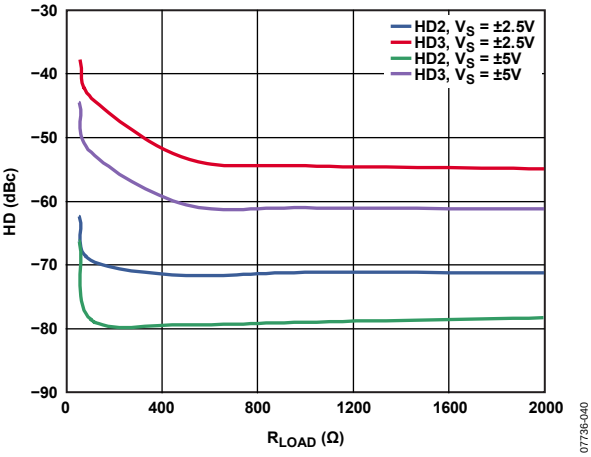


Figure 40. Harmonic Distortion to Differential Output vs. R_{LOAD} and Various Supplies

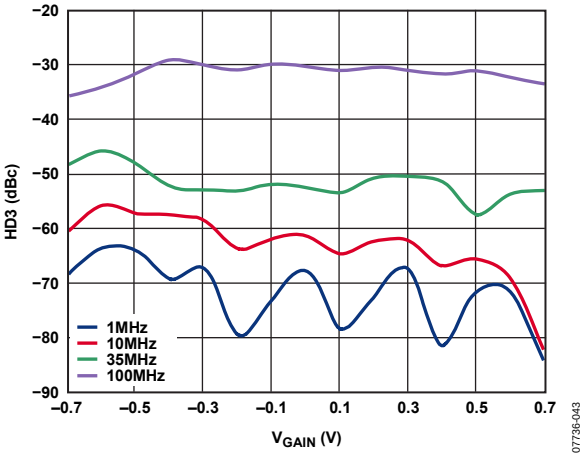


Figure 43. HD3 vs. V_{GAIN} vs. Frequency to VGAx

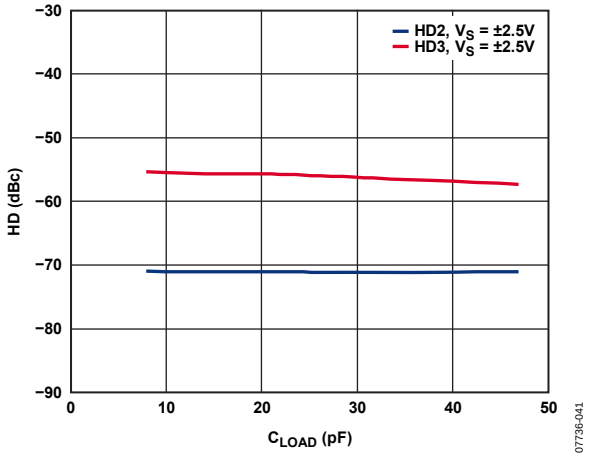


Figure 41. Harmonic Distortion to Differential Output vs. C_{LOAD}

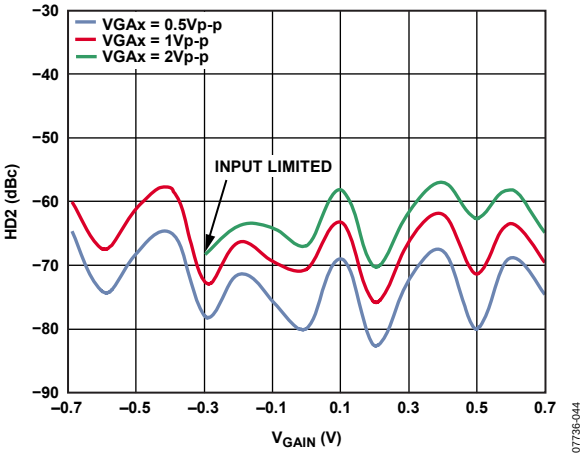


Figure 44. HD2 vs. Amplitude to VGAx

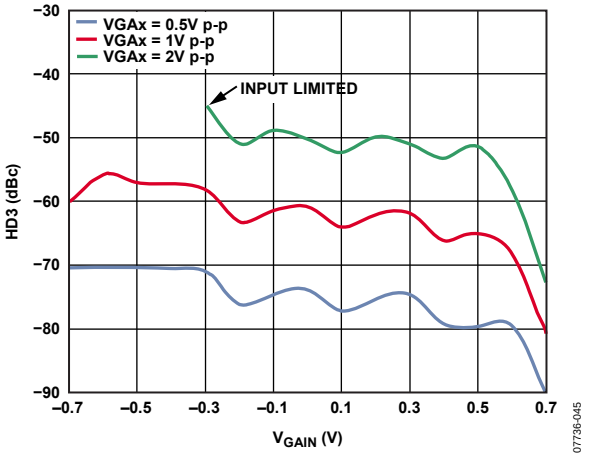


Figure 45. HD3 vs. Amplitude to VGAx

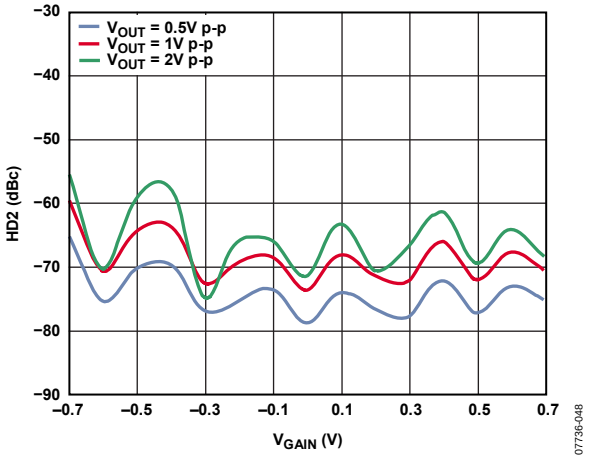


Figure 48. HD2 vs. Amplitude to Differential Output

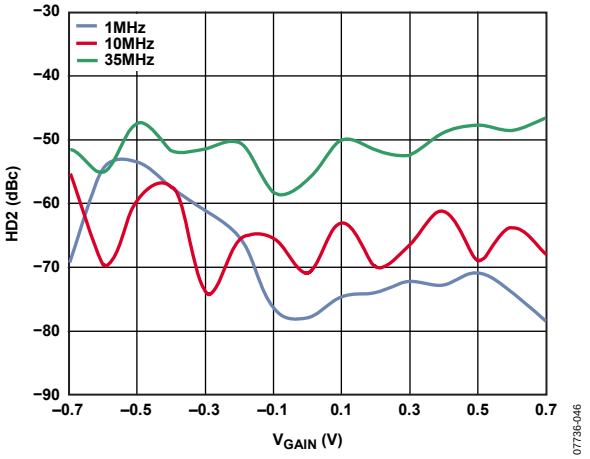


Figure 46. HD2 vs. V_{GAIN} vs. Frequency to Differential Output

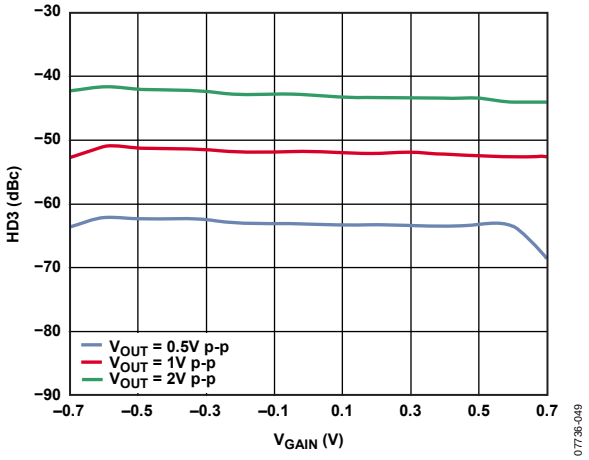


Figure 49. HD3 vs. Amplitude to Differential Output

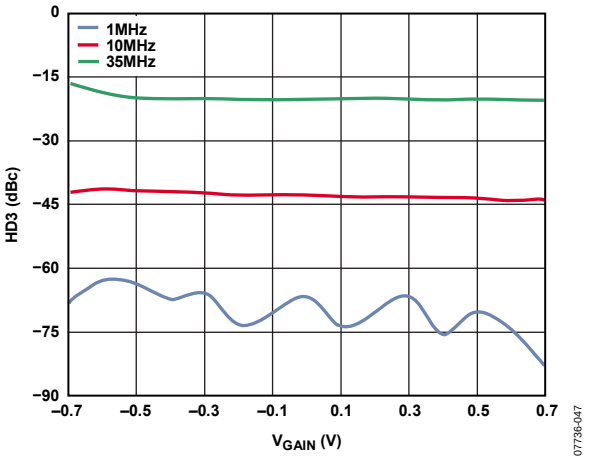


Figure 47. HD3 vs. V_{GAIN} vs. Frequency to Differential Output

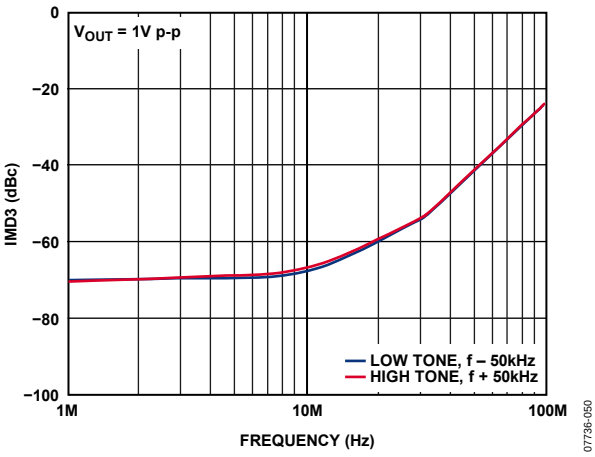


Figure 50. IMD3 vs. Frequency to VGAx

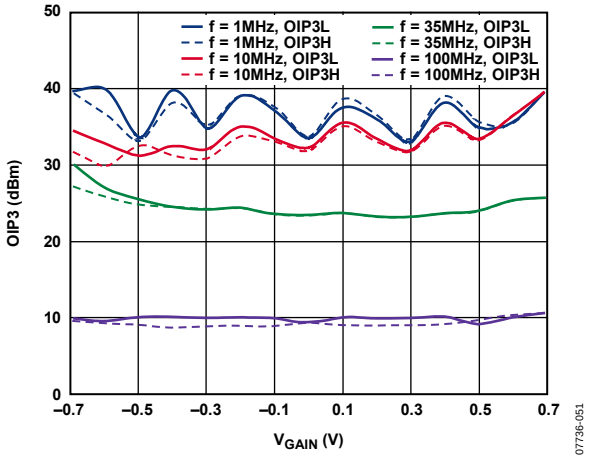


Figure 51. OIP3 vs. V_{GAIN} vs. Frequency to VGAx

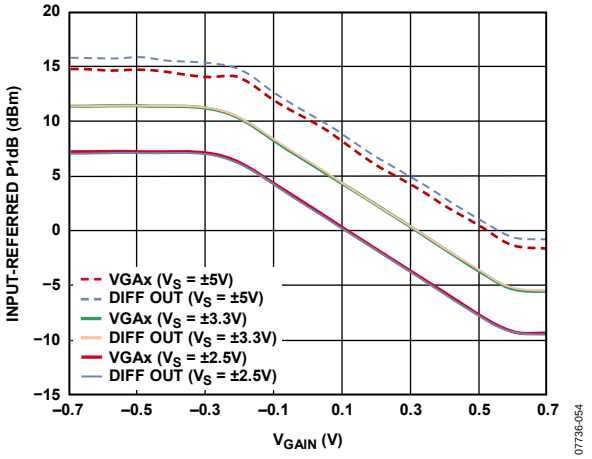


Figure 54. Input P1dB vs. V_{GAIN}

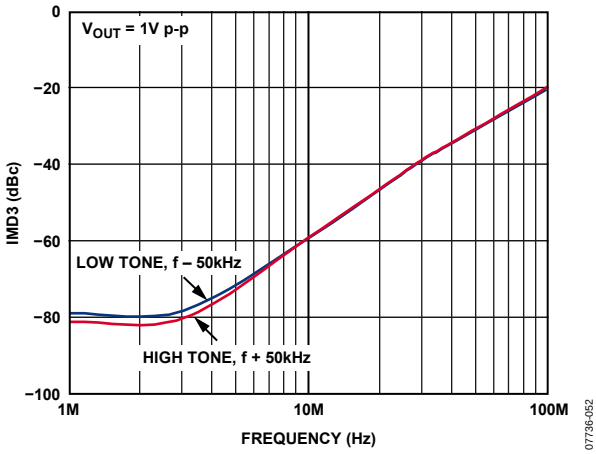


Figure 52. IMD3 vs. Frequency to Differential Output

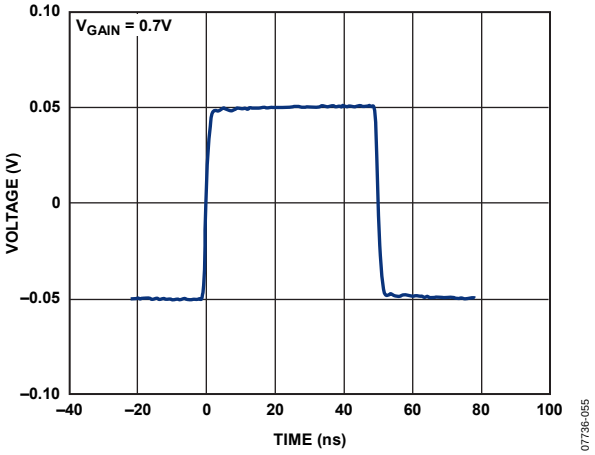


Figure 55. Small Signal Pulse Response to VGAx

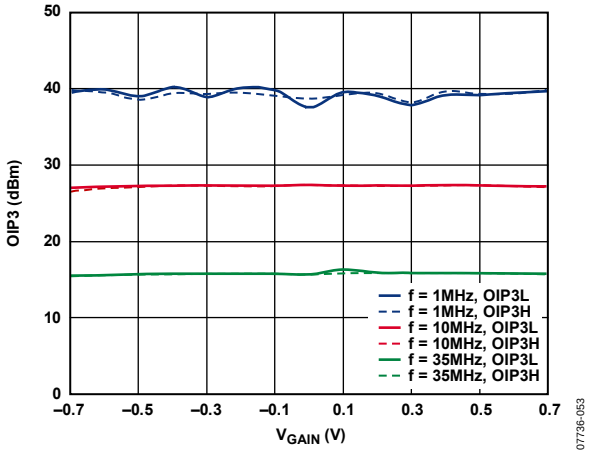


Figure 53. OIP3 vs. Frequency to Differential Output

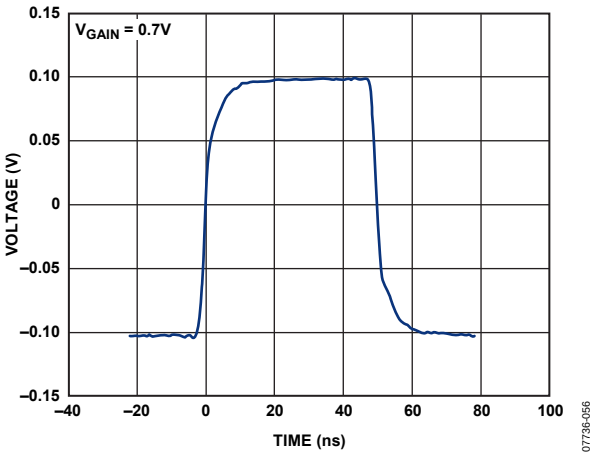


Figure 56. Small Signal Pulse Response to Differential Output

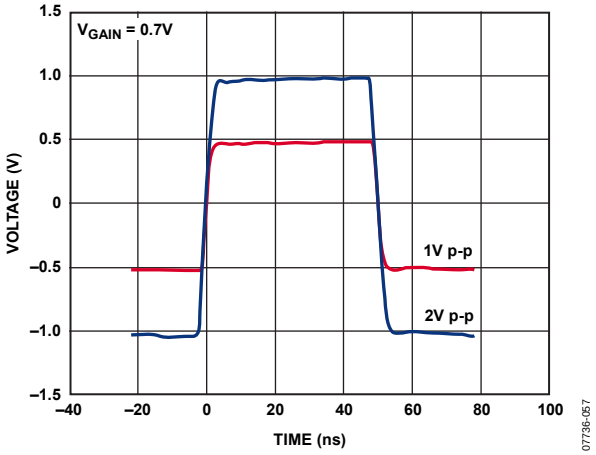


Figure 57. Large Signal Pulse Response to VGAx

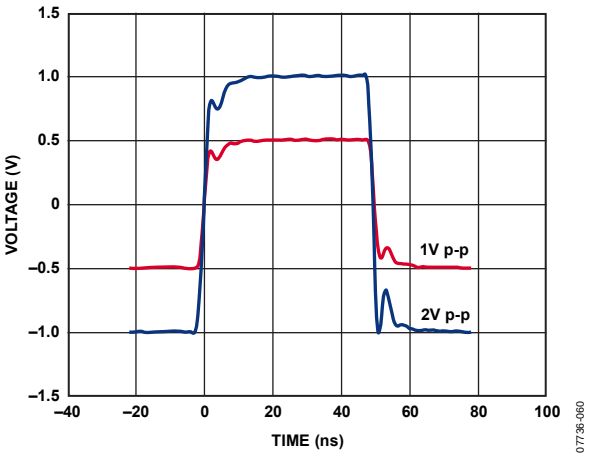


Figure 60. OFSx Large Signal Pulse Response

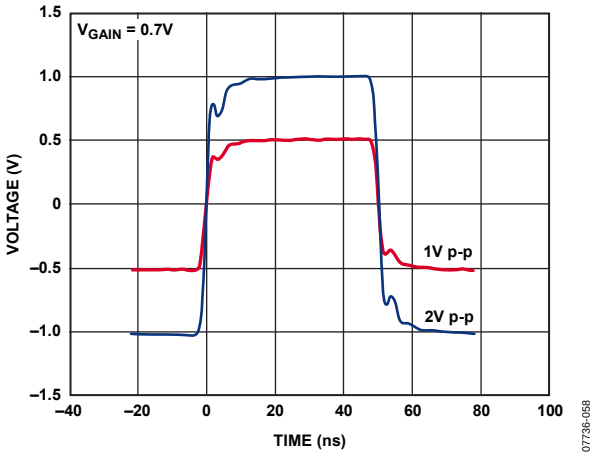


Figure 58. Large Signal Pulse Response to Differential Output

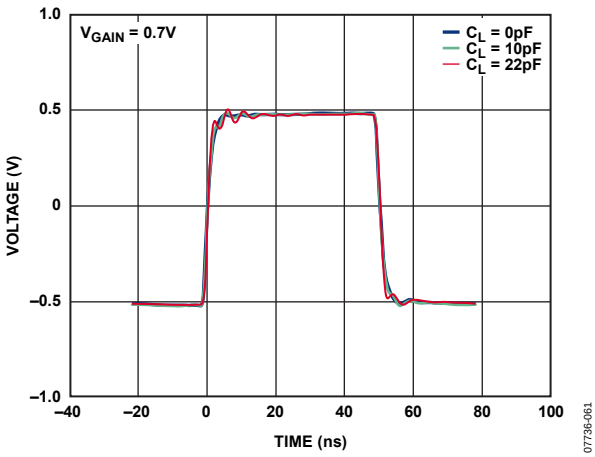


Figure 61. Large Signal Pulse Response to VGAx for Various Capacitive Loads

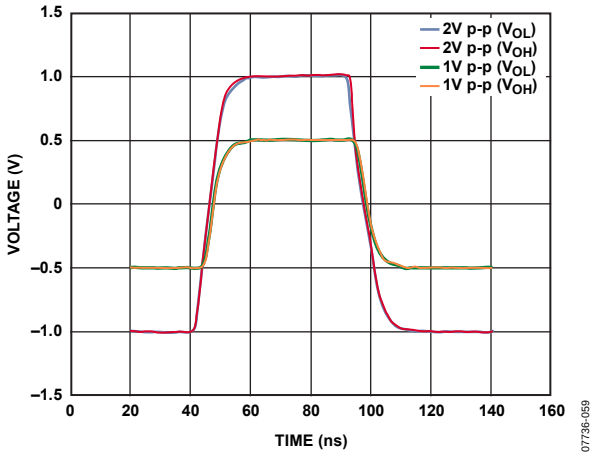


Figure 59. VOCM Large Signal Pulse Response

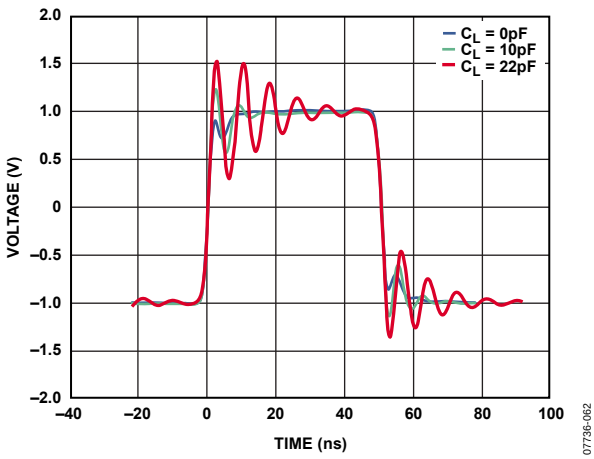


Figure 62. Large Signal Pulse Response to Differential Output for Various Capacitive Loads

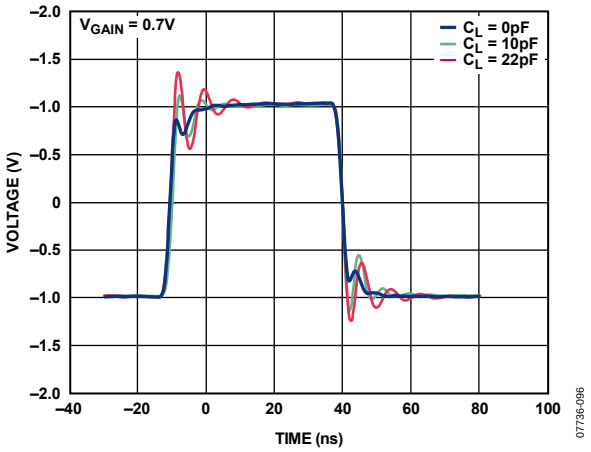


Figure 63. Large Signal Pulse Response to Differential Output for Various Capacitive Loads with Series R = 10 Ω

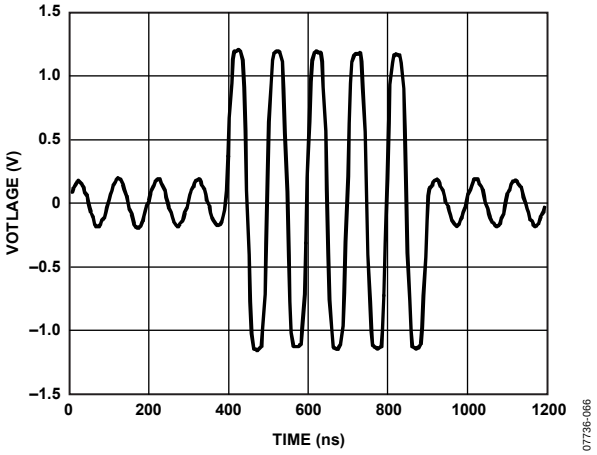


Figure 66. Preamp Overdrive Recovery

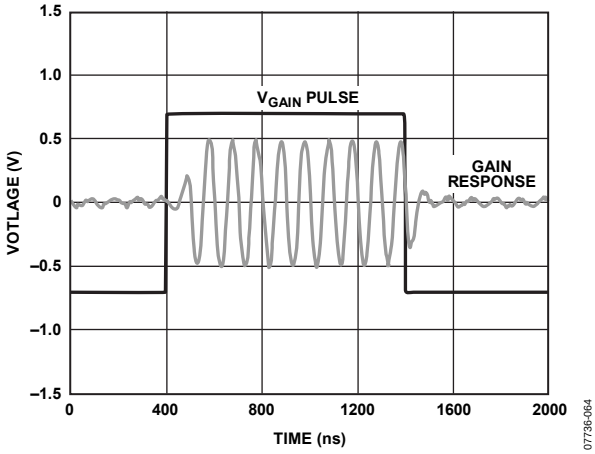


Figure 64. VGAx Response to Change in V_{GAIN}

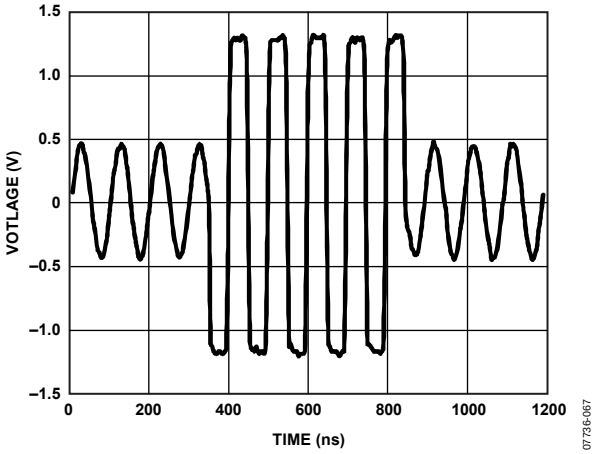


Figure 67. VGA Overdrive Recovery

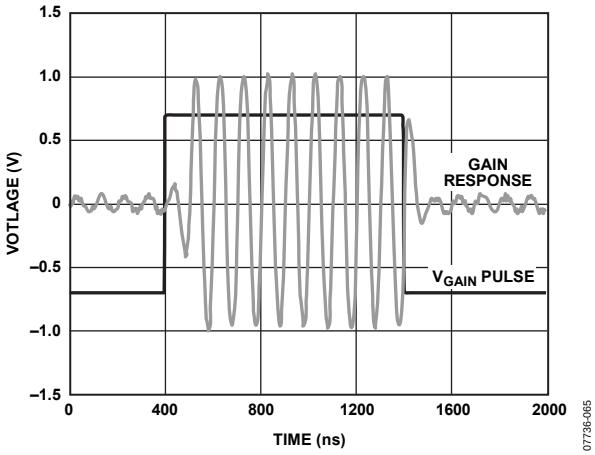


Figure 65. Differential Output Response to Change in V_{GAIN}

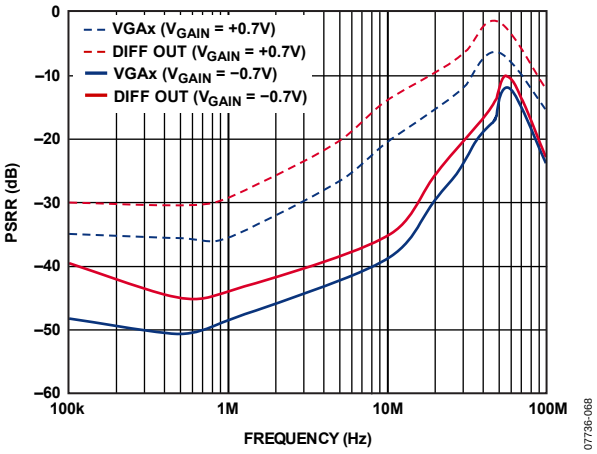


Figure 68. Power Supply Rejection vs. Frequency (VPOS)

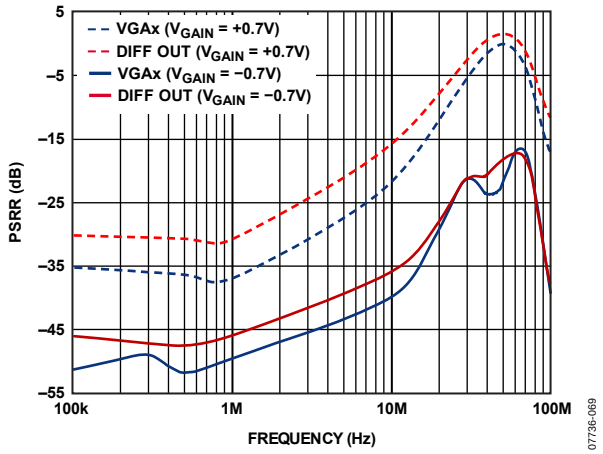


Figure 69. Power Supply Rejection vs. Frequency (VNEG)

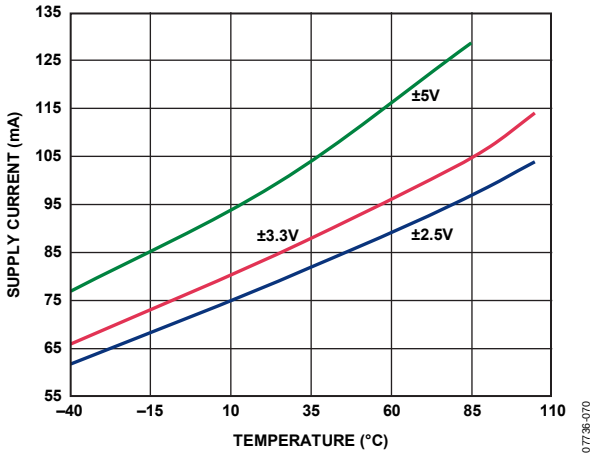


Figure 70. Quiescent Supply Current vs. Temperature

TEST CIRCUITS

V_S = ±2.5 V, T_A = 25°C, f = 10 MHz, C_L = 5 pF, R_L = 500 Ω per output (VGAx, VOHx, VOLx), V_{GAIN} = (V_{GNHx} − V_{GNLO}) = 0 V, V_{VOCM} = GND, V_{OFSx} = GND, gain range = 6 dB to 30 dB, unless otherwise specified.

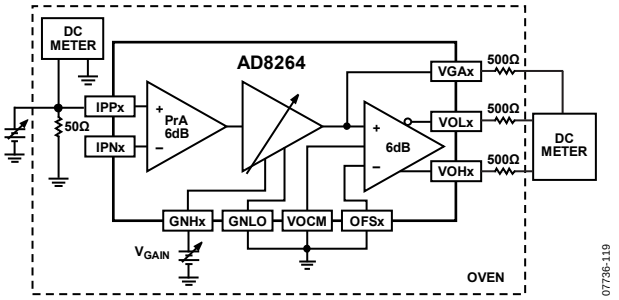


Figure 71. Gain vs. V_{GAIN} vs. Temperature (See Figure 3 and Figure 4)

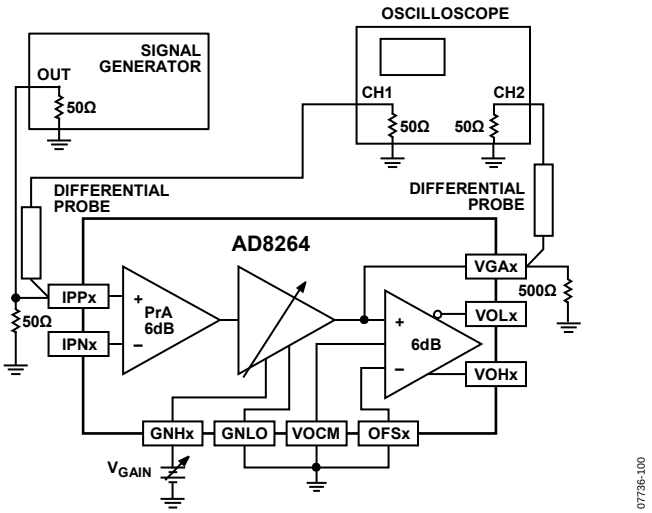


Figure 72. Gain Error vs. V_{GAIN} at Various Frequencies to VGAx (See Figure 5)

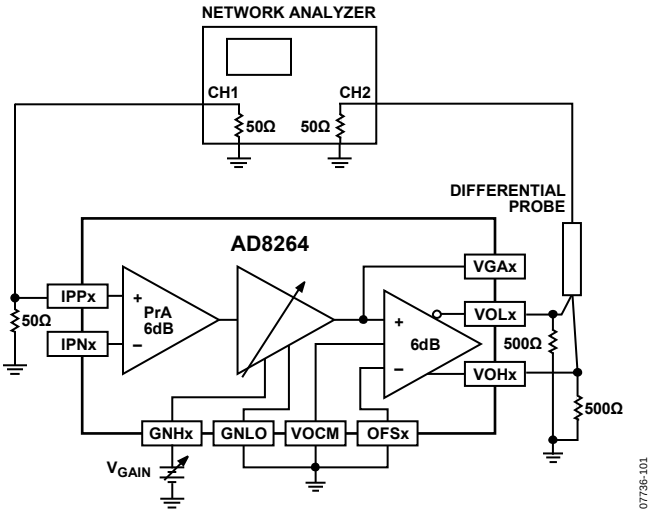


Figure 74. Frequency Response vs. Gain to Differential Output for Various Values of V_{GAIN} (See Figure 11)

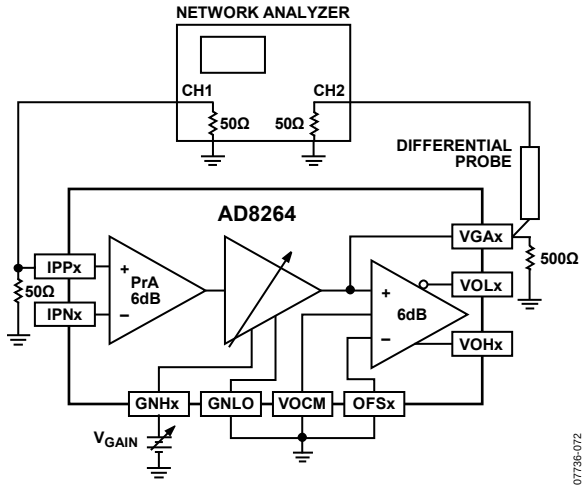


Figure 73. Frequency Response vs. Gain to VGAx for Various Values of V_{GAIN}, V_{GAIN} = GNHx − GNLO (See Figure 10)

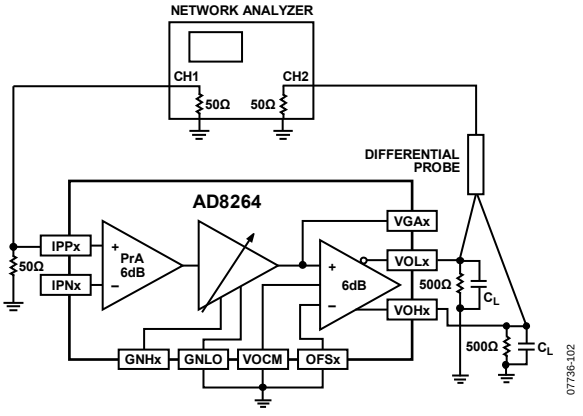


Figure 75. Frequency Response to Differential Output for Various Capacitive Loads (See Figure 12)

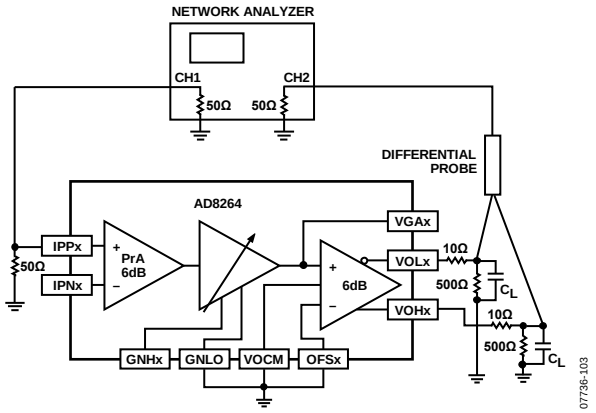


Figure 76. Frequency Response to Differential Output for Various Capacitive Loads with Series R = 10 Ω (See Figure 13)

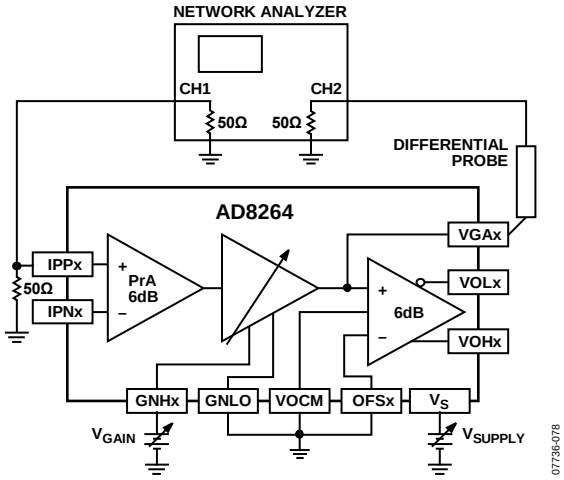


Figure 79. Frequency Response vs. Gain to VGAx for Various Supply Voltages (See Figure 18)

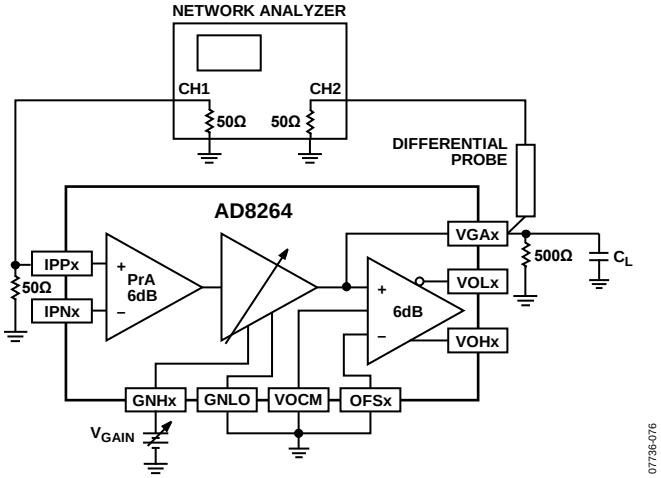


Figure 77. Frequency Response to VGAx for Various Capacitive Loads (See Figure 14)

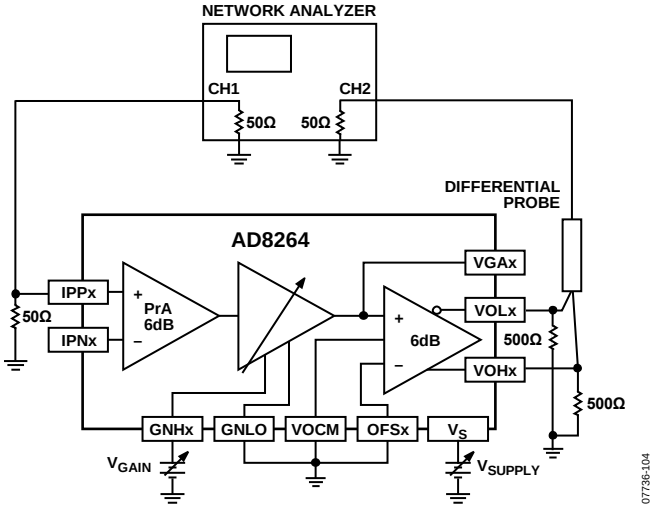


Figure 80. Frequency Response vs. Gain to Differential Output for Various Supply Voltages (See Figure 19)

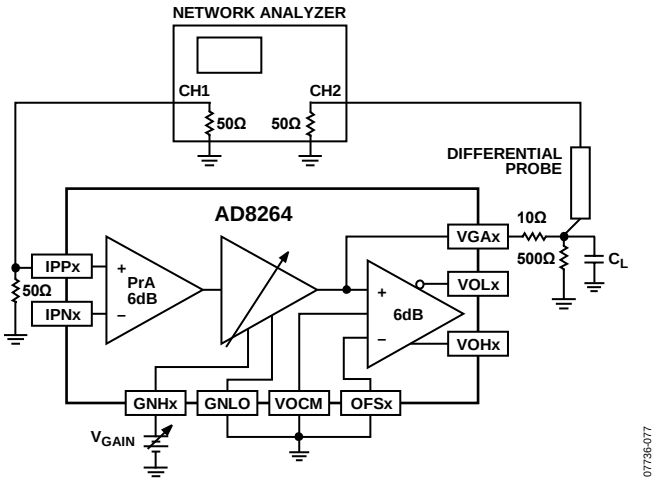


Figure 78. Frequency Response to VGAx for Various Capacitive Loads with Series R =10 Ω (See Figure 16)

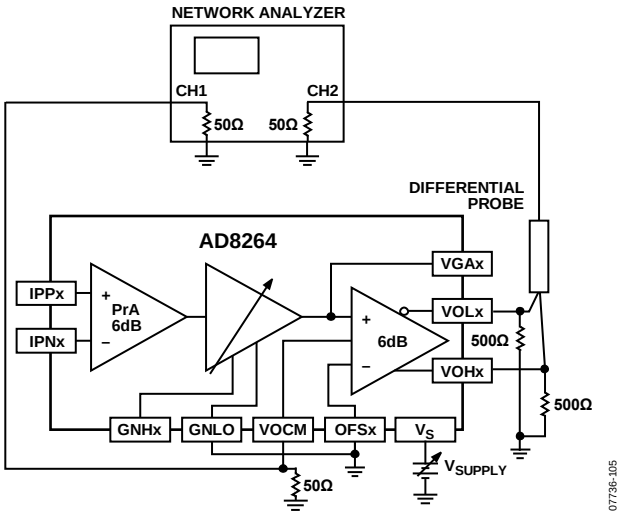


Figure 81. VOCM Frequency Response to Differential Output (See Figure 21)

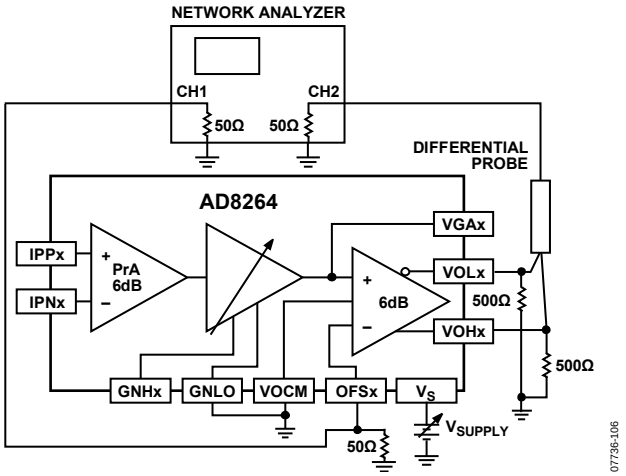


Figure 82. OFSx Frequency Response to Differential Output (See Figure 22)

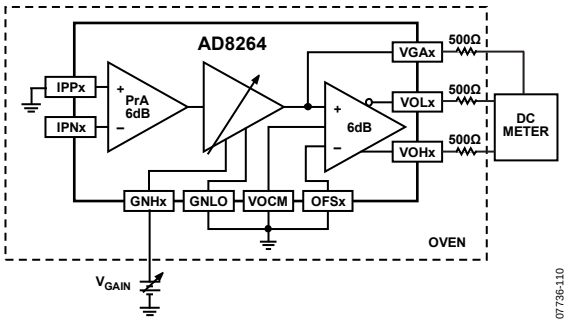


Figure 83. Output Offset Voltage vs. V_{GAIN} vs. Temperature (See Figure 26 and Figure 27)

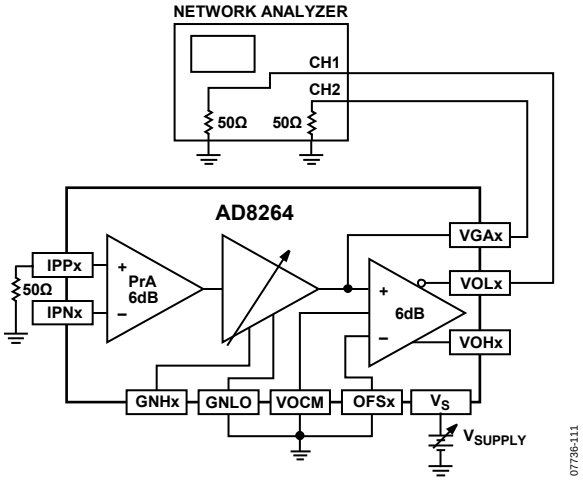


Figure 84. Output Resistance vs. Frequency (See Figure 30 and Figure 31)

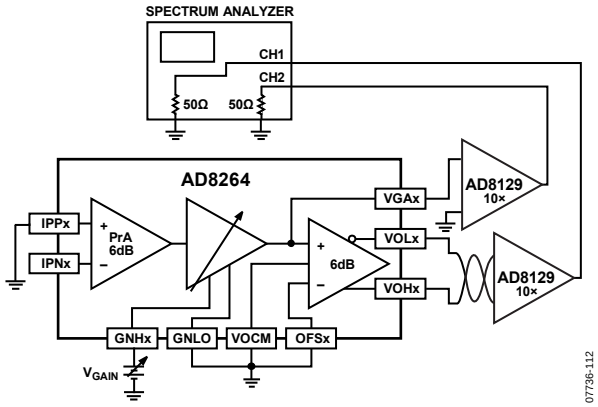


Figure 85. Output Referred Noise vs. V_{GAIN} (See Figure 32)

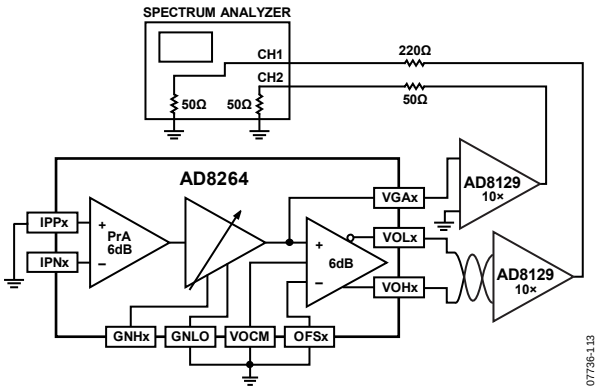


Figure 86. Input Referred Noise vs. Frequency (See Figure 34)

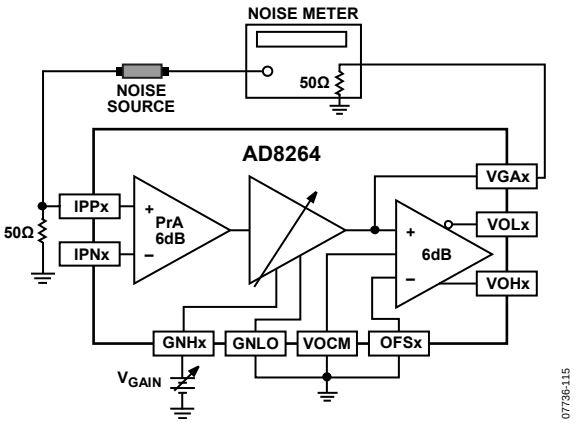


Figure 87. Noise Figure vs. V_{GAIN} (See Figure 36)

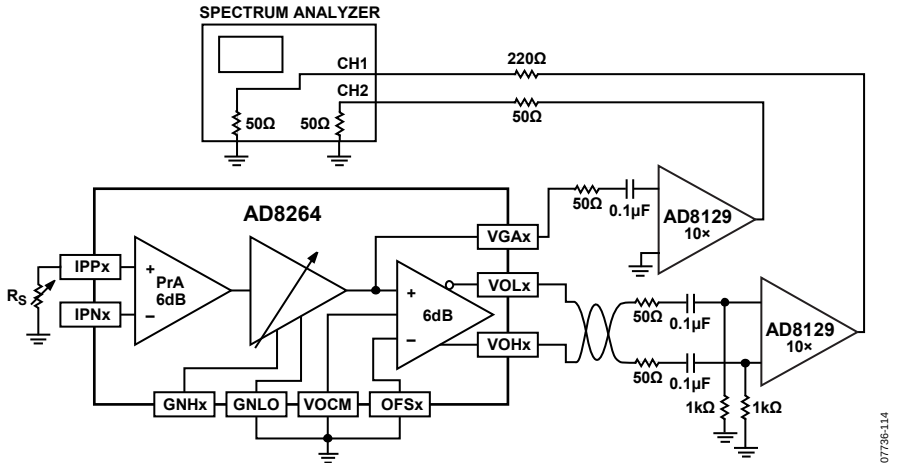


Figure 88. Input Referred Noise vs. R_{SOURCE} (See Figure 35)

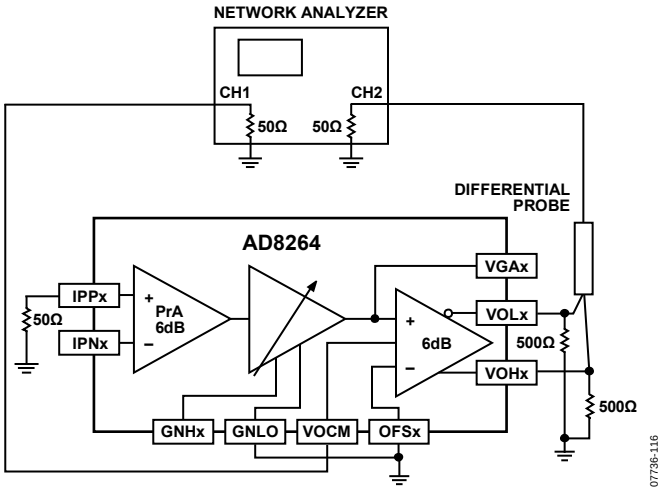


Figure 89. VOCM Common-Mode Rejection vs. Frequency (See Figure 37)

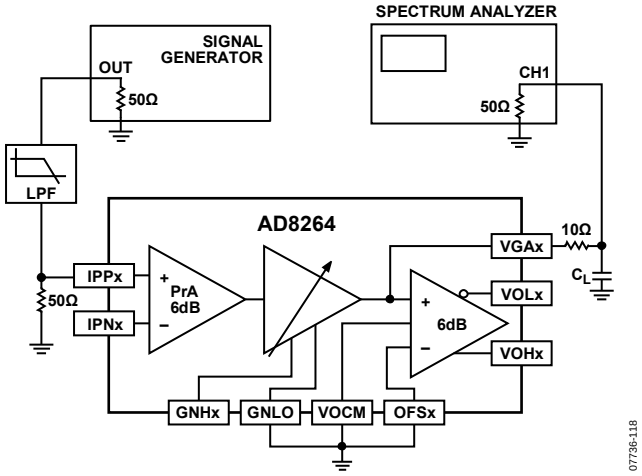


Figure 91. Harmonic Distortion to VGAx vs. C_{LOAD} (Figure 39)

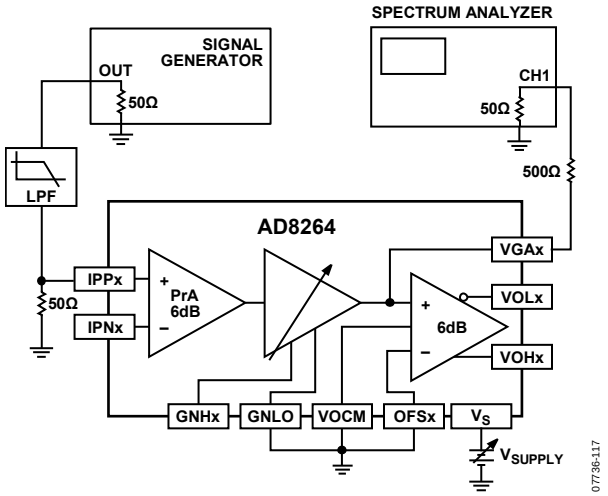


Figure 90. Test Circuit Harmonic Distortion to VGAx vs. R_{LOAD} and Various Supplies (See Figure 38)

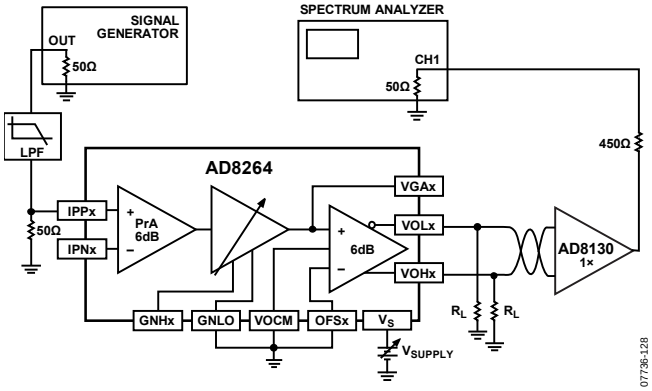


Figure 92. Harmonic Distortion to Differential Output vs. R_{LOAD} and Various Supplies (See Figure 40)

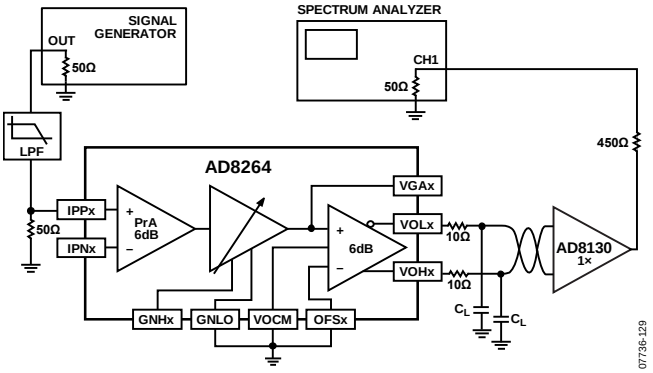


Figure 93. Harmonic Distortion to Differential Output vs. C_{LOAD} (See Figure 41)

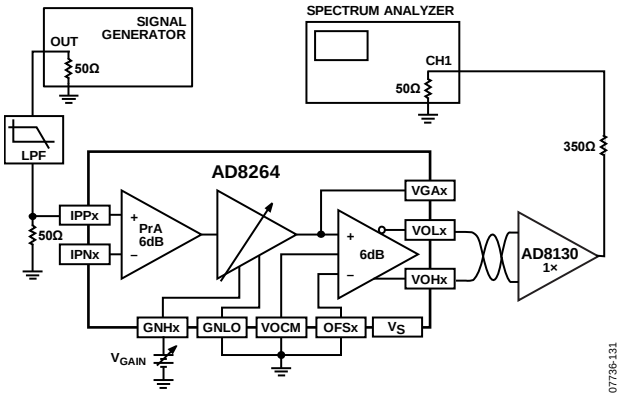


Figure 95. HD2 and HD3 to Differential Output (See Figure 46 through Figure 49)

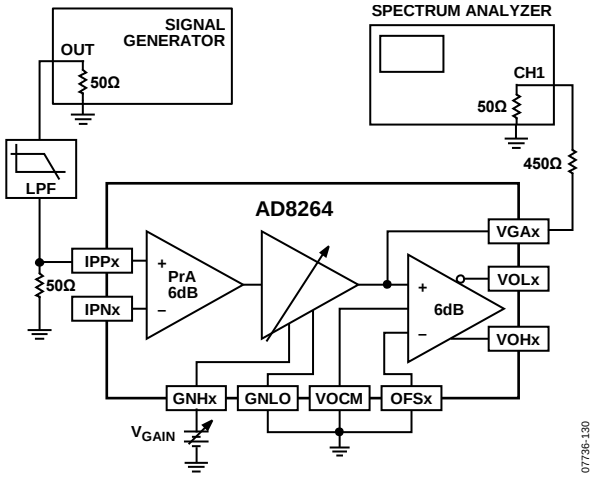


Figure 94. HD2 and HD3 to VGAx (See Figure 42 Through Figure 45)

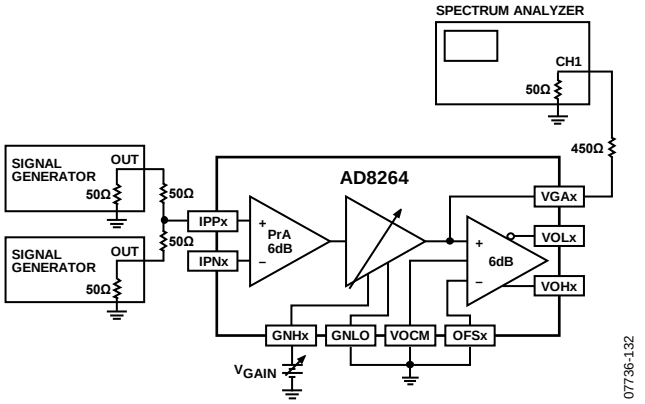


Figure 96. IMD3 and OIP3 to VGAx (See Figure 50 and Figure 51)

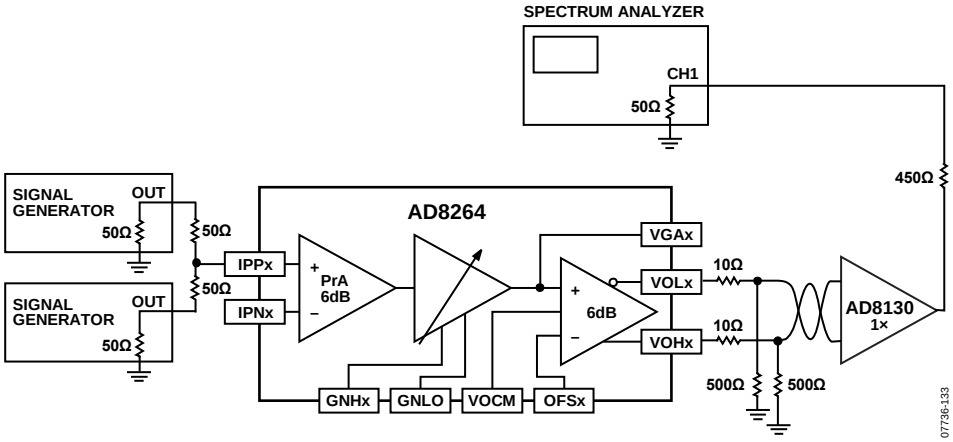


Figure 97. IMD3 and OIP3 to Differential Output (See Figure 52 and Figure 53)

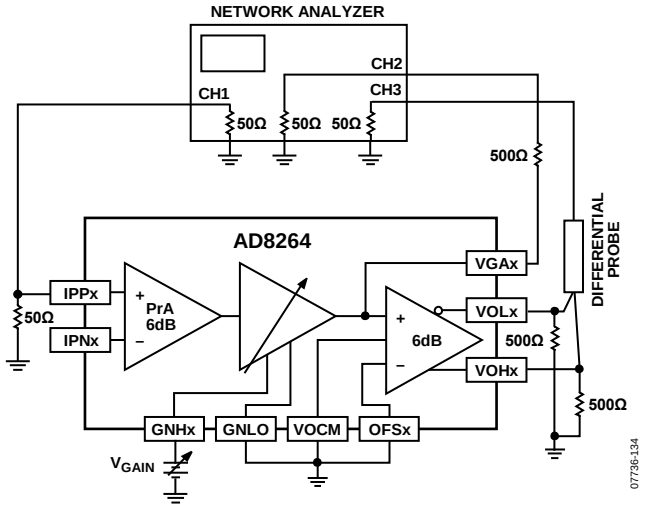


Figure 98. Input P1dB vs. V_{GAIN} (See Figure 54)

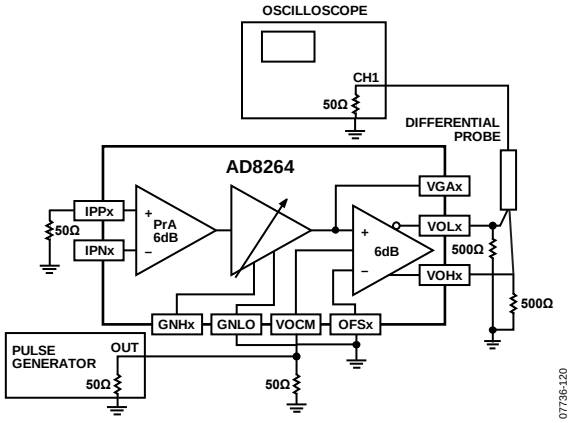


Figure 101. VOCM Pulse Response (See Figure 59)

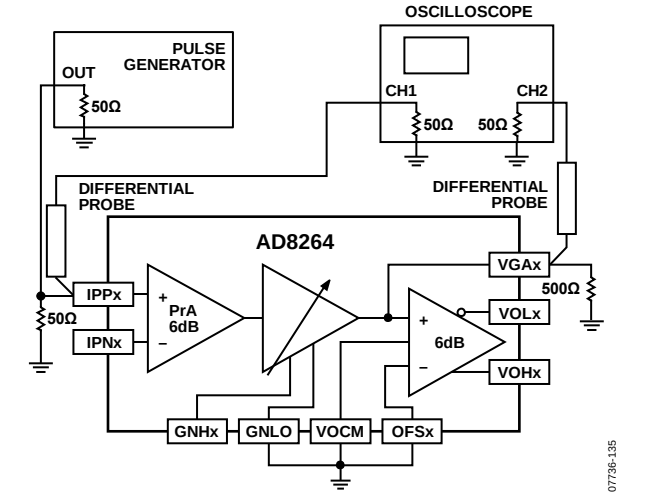


Figure 99. Pulse Response to VGAx, V_{GAIN} = 0.7 V (See Figure 55 and Figure 57)

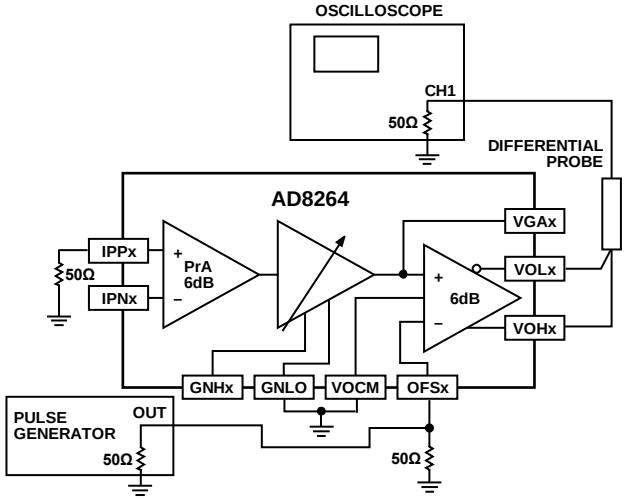


Figure 102. OFSx Pulse Response (See Figure 60)

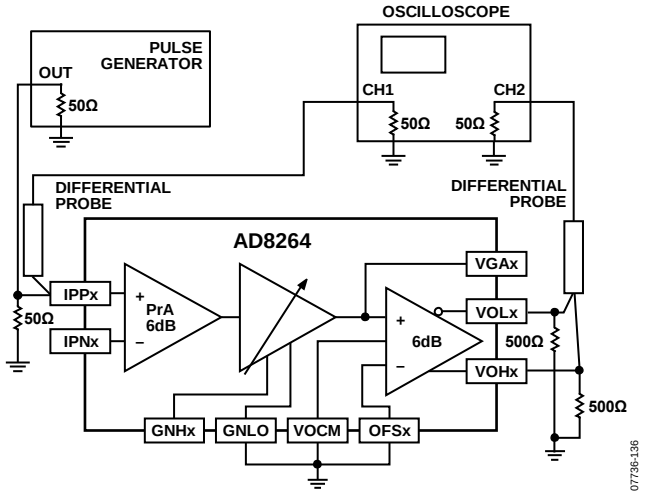


Figure 100. Pulse Response to Differential Outputs, V_{GAIN} = 0.7 V (See Figure 56 and Figure 58)

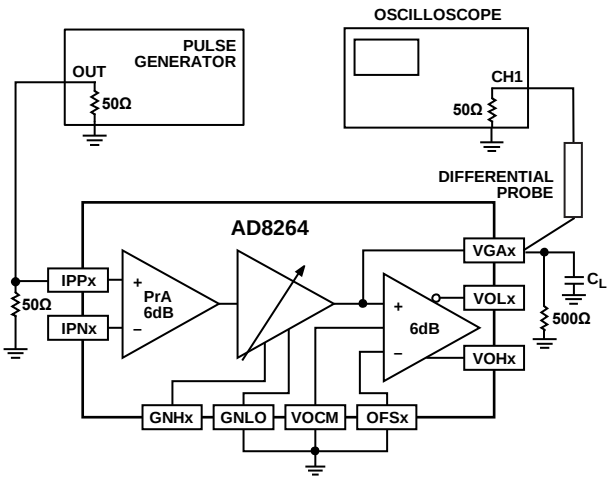


Figure 103. Pulse Response to VGAx for Various Capacitive Loads, V_{GAIN} = 0.7 V (See Figure 61)

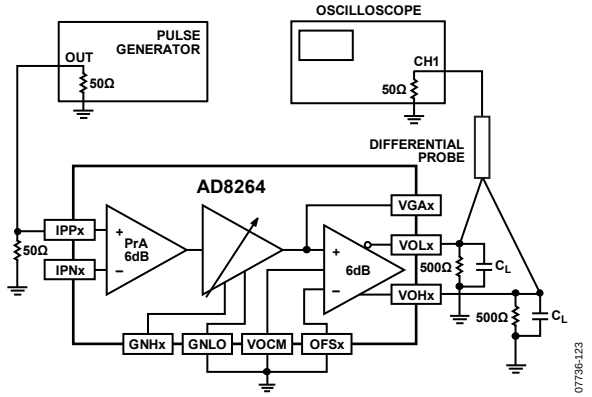


Figure 104. Pulse Response to Differential Output for Various Capacitive Loads, V_{GAIN} = 0.7 V (See Figure 62)

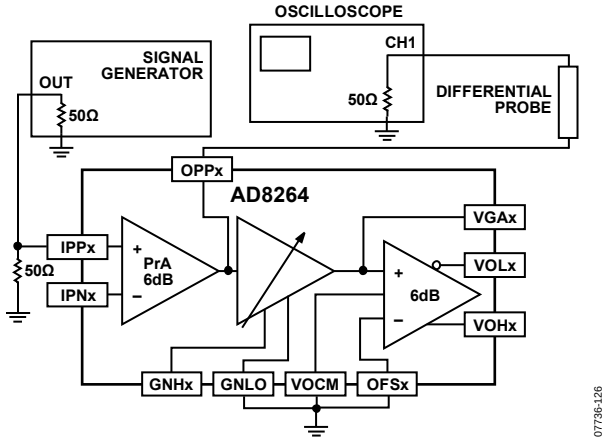


Figure 107. Preamp Overdrive Recovery (See Figure 66)

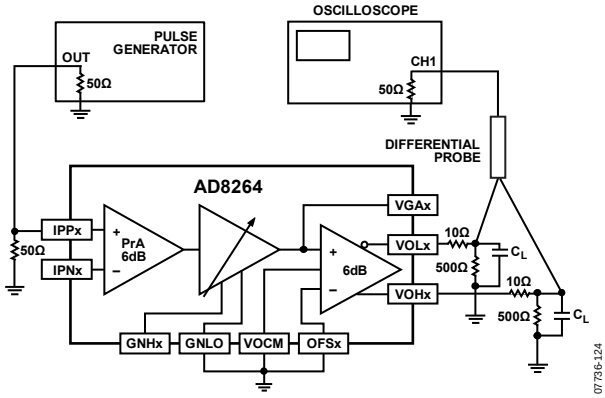


Figure 105. Pulse Response to Differential Output for Various Capacitive Loads with Series R = 10 Ω, V_{GAIN} = 0.7 V (See Figure 63)

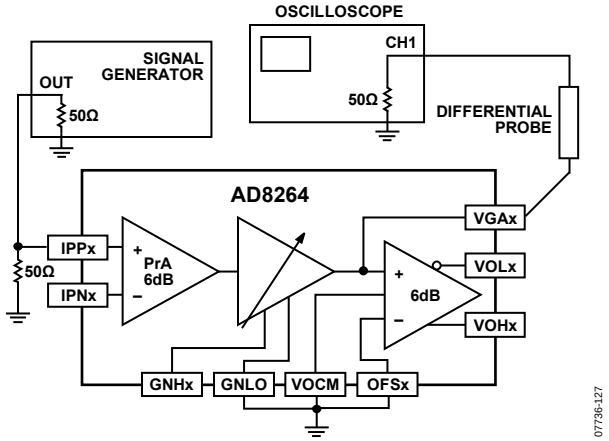


Figure 108. VGA Overdrive Recovery, V_{GAIN} = 0.7 V (See Figure 67)

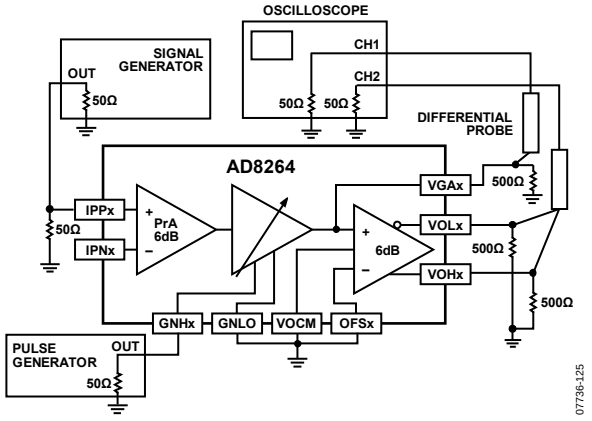


Figure 106. Gain Response to VGAx or Differential Output (See Figure 64 and Figure 65)

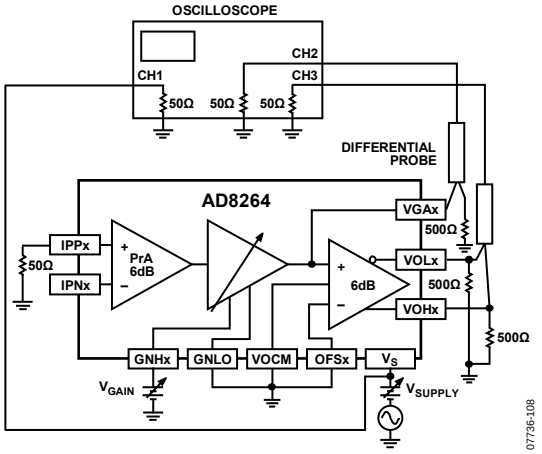


Figure 109. PSRR (See Figure 68 and Figure 69)

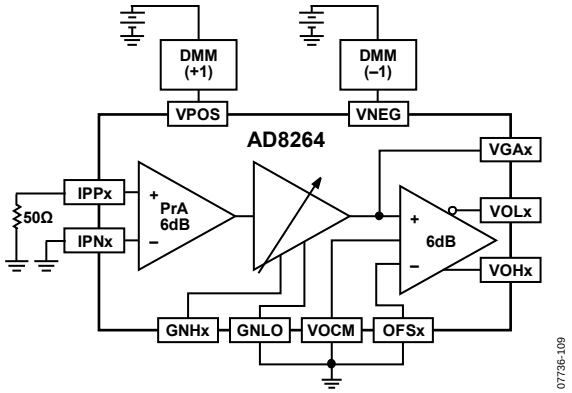


Figure 110. Quiescent Supply Current (See Figure 70)

THEORY OF OPERATION

OVERVIEW

The AD8264 is a dc-coupled quad channel VGA with a fixed gain-of-2 (6 dB) preamplifier and a single-ended-to-differential output amplifier with level shift capability that can be used as an ADC driver. Figure 111 shows a representative block diagram of a single channel; all four channels are identical. The supply can operate from ±2.5 V to ±5 V. The primary application is as a pulse processor for medical positron emission tomography (PET) imaging; however, the device is useful for any dc-coupled application that can benefit from variable gain.

The signal chain consists of three fundamental stages: the preamplifier, the variable gain amplifier, and the differential output buffer amplifier. The preamplifier has an internally fixed gain-of-2 (6 dB). The VGA comprises an attenuator that provides 0 dB to 24 dB of attenuation, followed by a fixed gain 18 dB (8×) amplifier. The single-ended VGA output is connected directly to the noninverting input of the differential output (post) amplifier, which has a differential fixed gain-of-2 (6 dB).

The gain range from the preamp input to the VGA output is 0 dB to 24 dB. The aggregate gain range from preamp input to the differential postamplifier output is 6 dB to 30 dB.

The ideal gain equation for the gain from the single-ended input to the output is

$$V_{GAIN} = V_{GNHx} - V_{GNLO} \quad (1)$$

$$Gain = 20\frac{\text{dB}}{\text{V}} \times V_{GAIN} + ICPT \quad (2)$$

The ideal value for ICPT, or the intercept, is defined at V_{GAIN} = 0 V. The ICPT for the VGA output and differential amplifier outputs equals 12.1 dB and 18.1 dB, respectively. The actual intercept varies with any additional gain or loss along the signal path. The measured values are both approximately 0.2 dB low.

PREAMP

The preamplifier is a current feedback amplifier, designed to drive the internal 100 Ω gain setting resistors and the resistive attenuator, which together result in a nominal load to the preamplifier of about 113 Ω. Normally, the negative preamp input, IPNx, is not connected externally. The positive input IPPx is the high impedance input of the current feedback amp. Note that, at the largest supply voltage of ±5 V, the input signal can become so large that the preamplifier output cannot deliver the required current to drive the 113 Ω load and, therefore, limits at 6 V p-p. This means that the input limits at 3 V p-p.

The short-circuit input referred noise at maximum VGA gain is about 2.3 nV/√Hz, and this accounts for all of the amplifiers and gain setting resistors. When measuring the input referred noise from the VGA output, the number is slightly lower at 2.1 nV/√Hz because the noise of the post-amplifier is not included in the noise calculation.

VGA

The VGA has a voltage feedback architecture and uses analog control to vary the gain. Its low gain range helps to maintain low offset and is intended for gain trim applications. The offset of the preamp and the VGA are trimmed; therefore, the maximum input referred offset is <0.5 mV over temperature (see Figure 26). Keeping the gain of each stage relatively low also allows the bandwidth to stay high.

The gain of the VGA is adjusted using the fully differential control inputs, GNHx and GNLO. The GNLO pin is internally connected to all four channels and must be biased externally. Under typical conditions, the GNLO pin is grounded. The gain high control pins (GNHx) are independent for each channel. The gain slope is nominally 20 dB/V. With GNLO connected to ground, each GNHx input can have a voltage applied from VNEG to VPOS without gain foldover.

To make use of the full gain range of the VGA, the nominal gain control voltage needed at GNHx is ±0.65 V relative to the voltage applied to GNLO. At the lowest supply voltage of ±2.5 V, the GNLO pin must always be grounded. With increasing supply, the common-mode range of the gain control interface increases. This means that GNLO can be anywhere within ±1.2 V at ±3.3 V supplies and ±2.8 V at ±5 V supplies.

Table 5. Gain Control Input Range

Supply Voltage (V)	GNLO Voltage Range (V)	V_{GAIN} Range (V)
±5	±2.8	±0.65
±3.3	±1.2	±0.65
±2.5	0	±0.65

For example, with a 3.3 V supply, the outputs of a quad, single-supply DAC, such as the 10-bit, AD5314, drive the GNHx pins directly. The output current rating of a low voltage ADR4520 LDO reference (2.048 V) is more than adequate to drive the REFHI pin of the AD5314 plus a 2:1, 10 kΩ resistive voltage divider between the V_{OUT} pin and the GND pin. Connect the center tap of the divider (V_{REF}/2) to the GNLO pin of the AD8264.

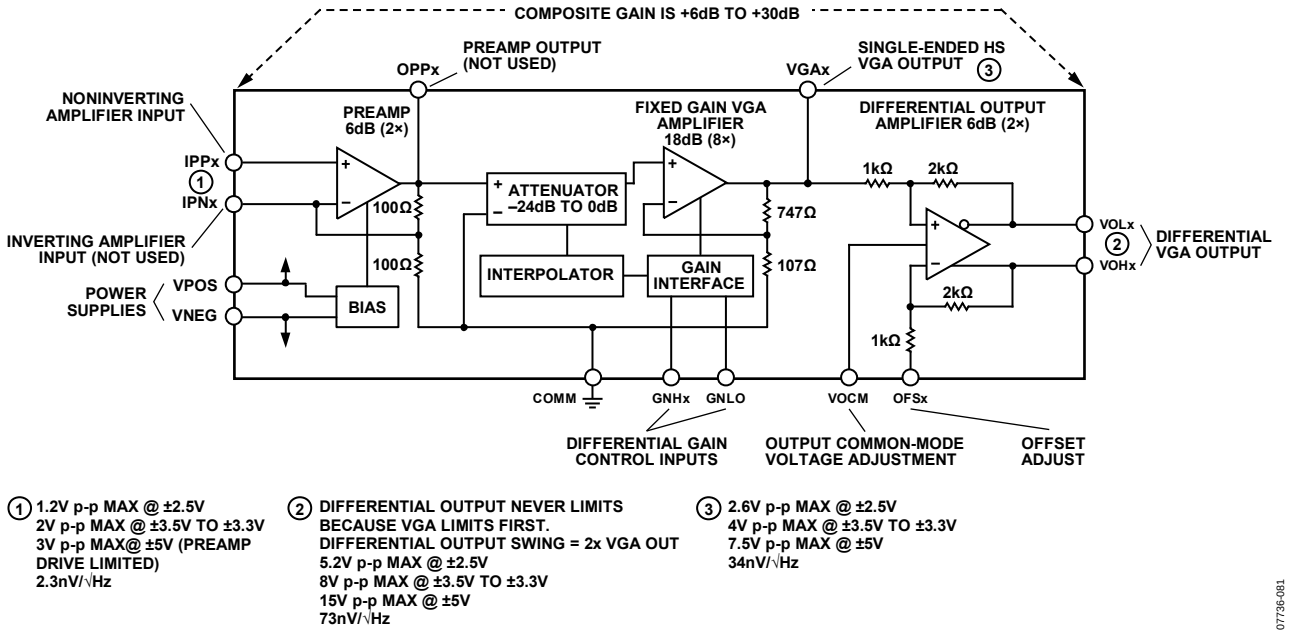


Figure 111. Single-Channel Block Diagram

POST AMPLIFIER

From the preamp input to the VGA output (VGAx), the gain is noninverting. As can be seen in Figure 111, the VGAx pins drive the positive input of the differential amplifier. The gain is inverting from the input of the preamp to the output pin at VOLx, and the gain is noninverting to the output VOHx.

Other than the input from VGAx, each differential amplifier has two additional inputs: VOCM and OFSx. A common VOCM pin is shared among all four postamplifiers, while separate OFSx pins are provided for each channel.

VOCM Pin

The VOCM pin sets the common-mode voltage of the differential output and must be biased by an external voltage. When driving a dc-coupled ADC, the voltage typically comes from the ADC reference, as shown in the Applications Information section.

If dc level shift is not necessary, the VOCM pin is connected to ground.

OFSx Pins

The OFSx pins are the inverting inputs of the differential post amplifiers and can be used to prebias a differential dc offset at the output. This is very useful when the input is a unipolar pulse because the user can set up the gain and the offset in such a way as to optimally map a unipolar pulse into the full-scale input of an ADC, while dc coupling throughout.

If dc offset is not desired, then connect the OFSx pins to ground. However, the OFSx pins can also be used as separate inputs if the user wants this function.

NOISE

At maximum gain, the preamplifier is the primary contributor of noise and results in a differential output referred noise of roughly 73 nV/√Hz. The noise at the VGAx outputs is 34 nV/√Hz, and because of the gain-of-2, the VGA output noise is amplified by 6 dB to 68 nV/√Hz. The differential amplifier, including the gain setting resistors, contributes another 26 nV/√Hz, and the rms sum results in a total noise of 73 nV/√Hz. At the lowest gain, the noise at the VGA output is approximately 19 nV/√Hz, and when multiplied by two, it results in 38 nV/√Hz at the differential output; again, rms summing this with the 26 nV/√Hz of the differential amplifier causes the total output referred noise to be approximately 46 nV/√Hz.

The input referred noise to the preamplifier at maximum gain is 2.3 nV/√Hz and increases with decreasing gain. Note that all noise numbers include the necessary gain setting resistors.

APPLICATIONS INFORMATION

A LOW CHANNEL COUNT APPLICATION CONCEPT USING A DISCRETE REFERENCE

The AD8264 is particularly well suited for use in the analog front end of medical PET imaging systems. Figure 112 shows how to use the AD8264 with the AD5314 (a 4-channel, 10-bit DAC) and the AD9222/AD9228 (an octal or quad, 12-bit ADC, respectively). The DAC sets the gain of the AD8264. Note that the full gain span of 24 dB is achieved with this setup because the gain control input range of the AD8264 is very close to 1.25 V. The GNLO pin must offset by 1.25/2 = 625 mV because the gain control input is bipolar around the voltage applied at GNLO. This is done with two 1 kΩ, 1% resistors. The approximately 1 µA of bias current flowing from the GNLO pin does not contribute a significant error because the basic gain error of the AD8264 is the limiting factor.

The ADR127 1.25 V precision reference with an input of 3.3 V can supply −2 mA to +5 mA from −40°C to +125°C, which is sufficient to drive both the resistive divider and the REFIN pin of the AD5314. The AD5314 is based on the string DAC concept, which means that the REFIN pin looks like a resistor that is nominally 45 kΩ; this results in a current draw of 1.25 V/45 kΩ = 28 µA. Even at the lowest specified resistance of 37 kΩ, this is still only a current of 34 µA. Therefore, the total current draw from the ADR127 is the 625 µA of the resistive divider plus ~30 µA, which equals ~655 µA, well below the 5 mA maximum current.

Figure 112 also includes the DAC output equation, which indicates that the output can vary between 0 V and VREF = 1.25 V.

The output of the AD8264 is ideal to drive an ADC like the 1.8 V quad-channel AD9228. If eight channels are needed, two AD8264s with the octal AD9222 ADC achieve the same thing. The same resistive divider can be used for two AD8264s because the bias current flowing is now ~2 µA, but this still only introduces an error of 1 mV with ideally matched resistors. With 20 dB/V gain scaling, this is a gain error of only 0.02 dB, which is much smaller than the fundamental gain error of the AD8264 (typically ~0.2 dB).

The single-ended-to-differential amplifier of the AD8264 amplifies the VGA output signal by 6 dB and can provide the required dc bias of the AD9222/AD9228, as shown in Figure 112. The ADC is connected with the default internal reference because the SENSE pin is grounded. With this connection, the AD9222/AD9228 VREF pin is an output that provides 1 V; this is then connected to the VOCM input of the AD8264, which sets the output common-mode voltage of the VOHx and VOLx pins to 1 V. This voltage is very close to the recommended optimal value of VDD/2 = 0.9 V. With this configuration, the ADC inputs are set to a full-scale (FS) of 2 V p-p.

Note that it is not recommended for the ADC VREF to drive many loads; therefore, for multiple AD8264s, buffer the VREF.

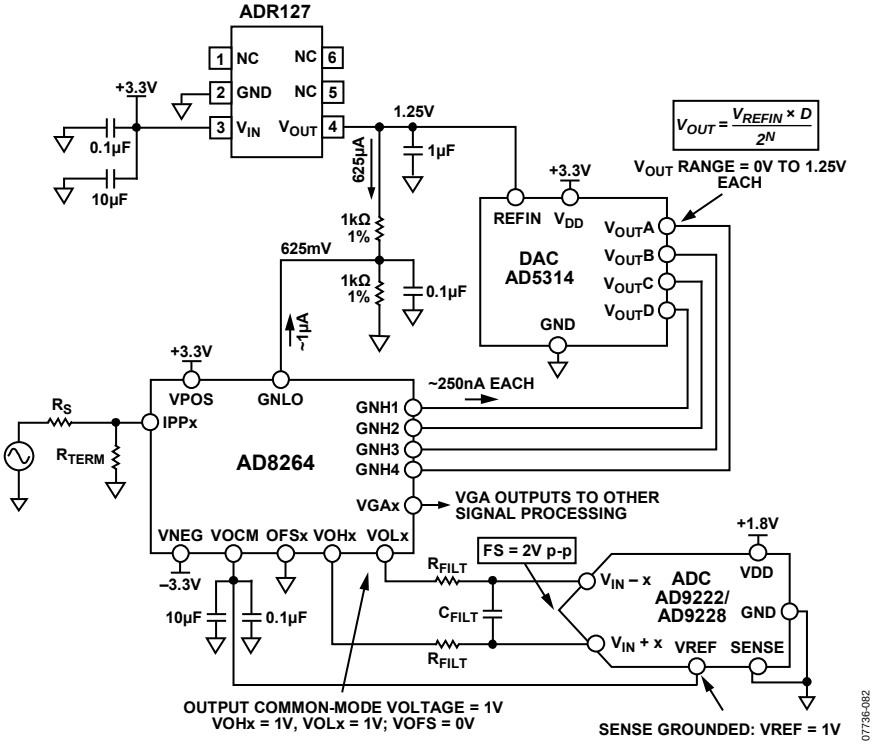


Figure 112. Application Concept of the AD8264 with the AD5314 10-Bit DAC and the AD9222/AD9228 12-Bit ADC

A DC CONNECTED CONCEPT EXAMPLE

The dc connected concept example in Figure 113 is an application with the 40-channel AD5381, 3 V, 12-bit DAC. The main difference between this example and Figure 112 is that, for the same ADR127 1.25 V reference, the full-scale output of the DAC is from 0 V to 2 × VREFIN = 2.5 V. Two options for gain control include the following:

- Use the same circuit as in Figure 112 but use only half the DAC output voltage from 0 V to 1.25 V. This is the simplest solution, requiring the fewest extra components. Note that the overall gain resolution increases by one bit to 11 bits over the 10-bit AD5314.
- Ground GNLO and scale the DAC output so that the GNHx inputs vary from −0.652 V to +0.625 V. Figure 113 shows a possible circuit implementation using a divider between the DAC output and a −1.25 V reference.

GNLO cannot simply be increased to 1.25 V because, for a given supply voltage, GNLO has a limited voltage range to achieve the full gain span (see Table 5).

However, a third possibility is to use another voltage that is between 1.2 V and 625 mV on GNLO, such as 1 V. In this case, the DAC must vary from 0.375 V to 1.625 V to achieve the fully specified gain range.

Note the gain limits when the differential gain control exceeds ±0.625 V, either to 6 dB or to 30 dB. If the differential gain control input voltage is exceeded, no gain foldover occurs.

Figure 113 shows how the AD8264 is connected in a PET application. The PMT generates a negative-going current pulse that results in a voltage pulse at the preamplifier input and a differential output pulse on VOLx and VOHx.

To fully appreciate the advantages of the AD8264, note the common-mode and polarity conversion afforded. The AD9228, as with most modern ADCs, is a low voltage, single-polarity device. Recall that the PMT is a high voltage device that yields a negative pulse. To map the pulse to the input range of the ADC, the pulse must be inverted, shifted, and amplified to the full input range of the ADC. This is done by using the gain control, signal offset, and common-mode features of the AD8264.

The full-scale input of the converter is 0 V to 2 V, with a common-mode of 1 V. Match the VOCM voltage of the AD8264 to the ADC common mode (VREF = 1 V), and the two devices can be connected directly using an appropriate level of the antialiasing filter. The PMT signal is 0 V to −0.1 V. With a gain of 20× (26 dB), the AD8264 output signal range is 2 V p-p. Prebias the signal negative by −0.5 V using the AD8264 OFSx inputs, which sets VOHx = 1.5 V and VOLx = 0.5 V for VOCM = 1 V. The output is perfectly matched to the input of the ADC.

Note that, by connecting VOLx to the positive ADC input and VOHx to the negative ADC input, the negative input pulse is inverted automatically. The VGAx output is still a negative pulse, amplified by 20 dB for this example.

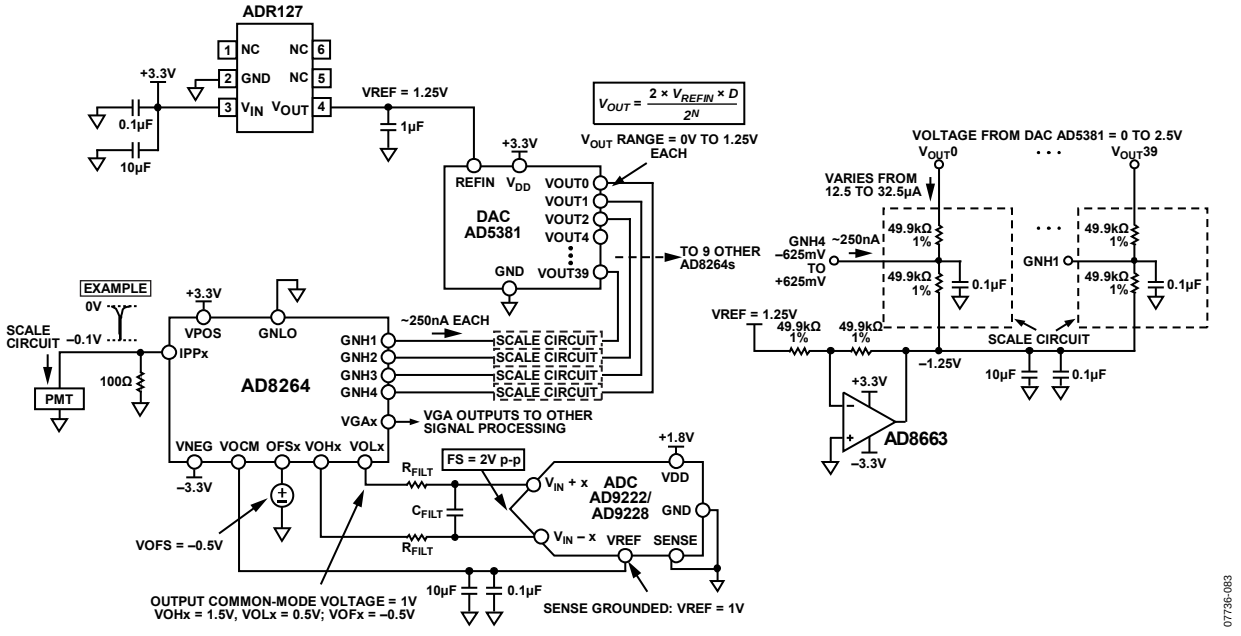


Figure 113. Concept Application of AD8264 with 40-Channel AD5381 12-Bit, 3 V DAC and AD9222/AD9228 12-Bit ADC

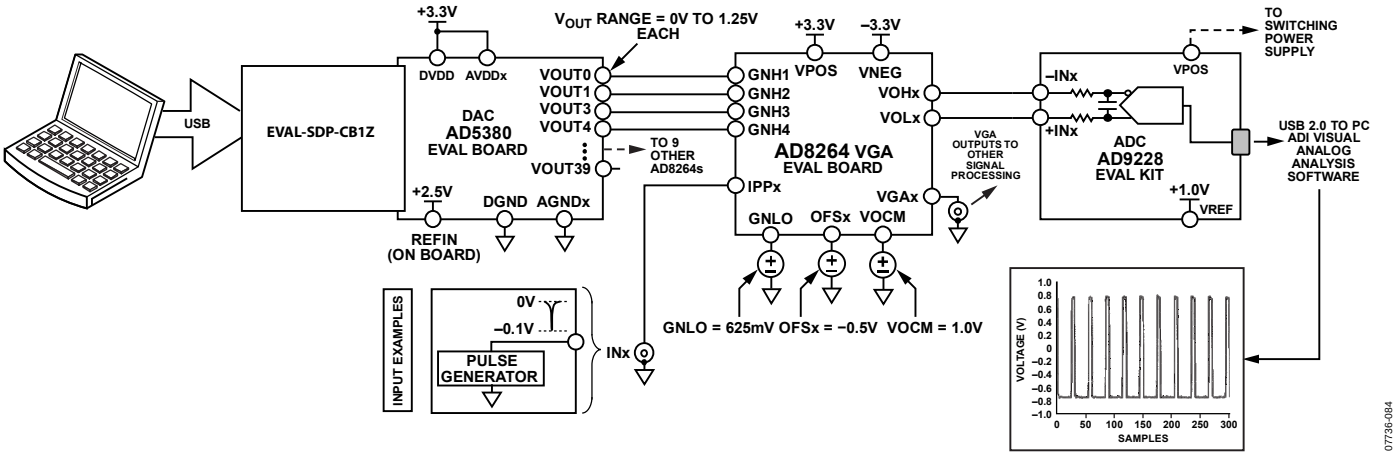


Figure 114. Evaluation Setup for DC-Coupled Analog Front-End Pulse Processing Application Using the AD8264

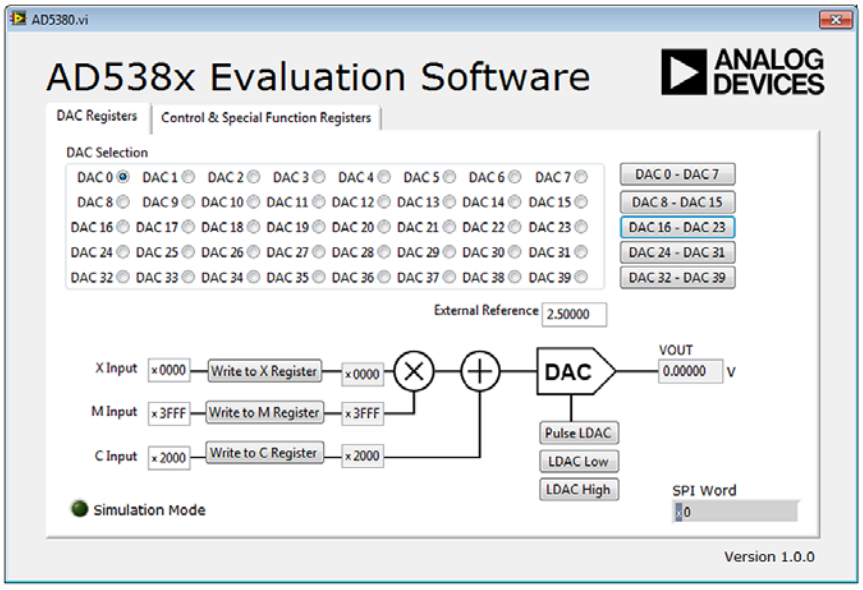


Figure 115. AD5381 Evaluation Software—AD5381 Option Selected.

A convenient method of verifying and customizing the signal chains shown in Figure 112 and Figure 113 is by ordering the corresponding evaluation boards available on www.analog.com. The AD8264-EVALZ is a platform through which the user can quickly become familiar with the features and performance capabilities of the AD8264. See the Evaluation Board section for more information.

When configuring evaluation boards around the AD8264-EVALZ, always be certain to refer to the latest revision of the AD5381 and/or AD9228 data sheets for hardware revisions or updates. The EVAL-AD5380SDPZ (a 40-channel DAC) connects to the EVAL-SDP-CB1Z and includes a software evaluation program to control the DAC. The AD5380 evaluation software allows the user to configure and program DAC parameters such as input codes, offset level, and output range, based on a 2.5 V or 1.25 V reference. For example, as shown in Figure 114, the reference can be set to 1.25 V, with a 0 V to 1.25 V output range to drive the GNHx inputs. For DAC user application information, refer to UG-757.

The ADC evaluation kit includes the AD9228-65EBZ board and the HSC-ADC-FIFO5 board to decode the ADC output. The kit also leverages the capabilities of VisualAnalog®, powerful simulation and data analysis software that enables the user to run FFTs and to perform real-time capture of the output levels.

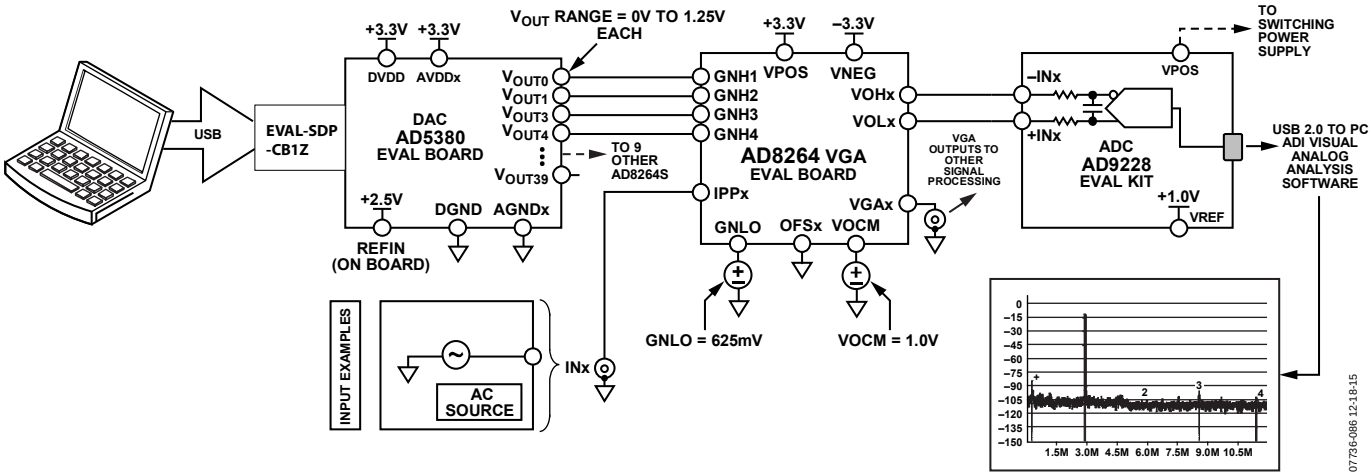


Figure 116. Evaluation Setup for AC Signal Processing Application Using the AD8264

EVALUATION BOARD

Analog Devices, Inc. provides evaluation boards to customers as a support service so that the circuit designer can become familiar with the device in the most efficient way possible. The AD8264 evaluation board provides a fast, easy, and convenient means to assess the performance of the AD8264 before going through the hassle and expense of design and layout of a custom board. The board is shipped fully assembled and tested, and it provides basic functionality as shipped. Standard connectors enable the user to attach standard lab test equipment without having to wait for the rest of the design to be completed. Figure 117 shows a digital image of the top view, and Figure 118 shows the schematic diagram of the AD8264 evaluation board.

The printed circuit board (PCB) artwork for all conductor and silkscreen layers is shown in Figure 119 to Figure 124. A description of a typical test setup can be found in the Applications Information section. The PCB artwork can be used as a guide for circuit layout and placement of devices. This is particularly useful for multiple function circuits with many pins, requiring multiple passive components.

CONNECTING AND USING THE AD8264-EVALZ

The AD8264 operates with bipolar power supplies from ±2.5 V dc to ±5 V dc. Make sure the current capacity is ≥400 mA. Connect a ground reference from the supplies to any of the black test loops, the positive supply to the red test loop (+V), and the negative supply to the blue test loop (−V).

Notice that the board is shipped with jumpers installed on the 2-pin headers marked GN1_2, GN3_4, OFS_12, OFS_34, GNLO, and VOCM. If these jumpers are missing, the offset and common-mode functions float high, substantially increasing the quiescent current of the board.

Apply input signals to any of the preamps at the SMA connectors, IN1 through IN4. These connectors are terminated with 50 Ω to accommodate typical signal generator analyzer voltage source impedances. The gain of the AD8264 preamps is fixed at 6 dB (2×) and can be monitored at the SMA connectors, OP1_2 and OP3_4, if desired. Note that there are output selector switches for each pair of preamps and 453 Ω resistors in series with the preamp outputs.

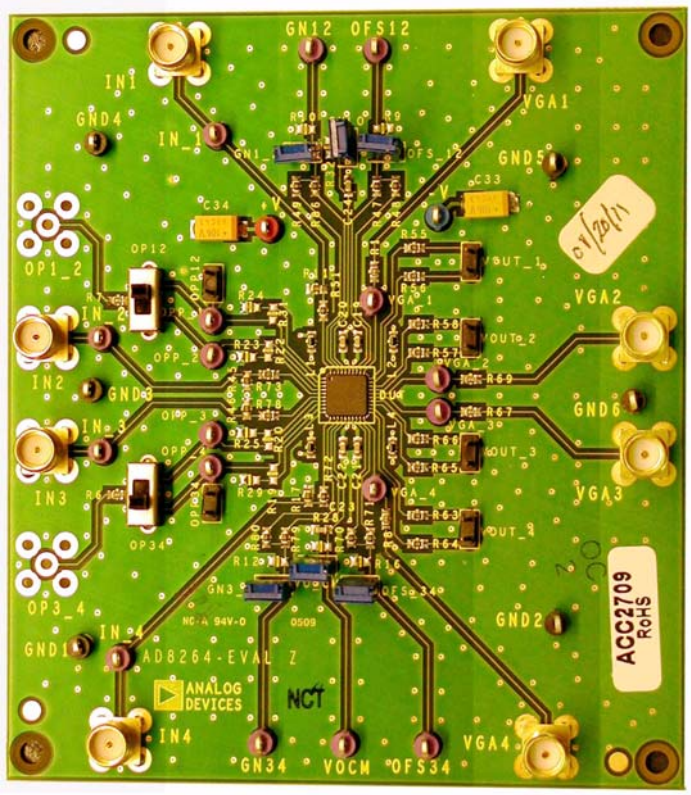


Figure 117. Digital Image of the AD8264-EVALZ (Top View)

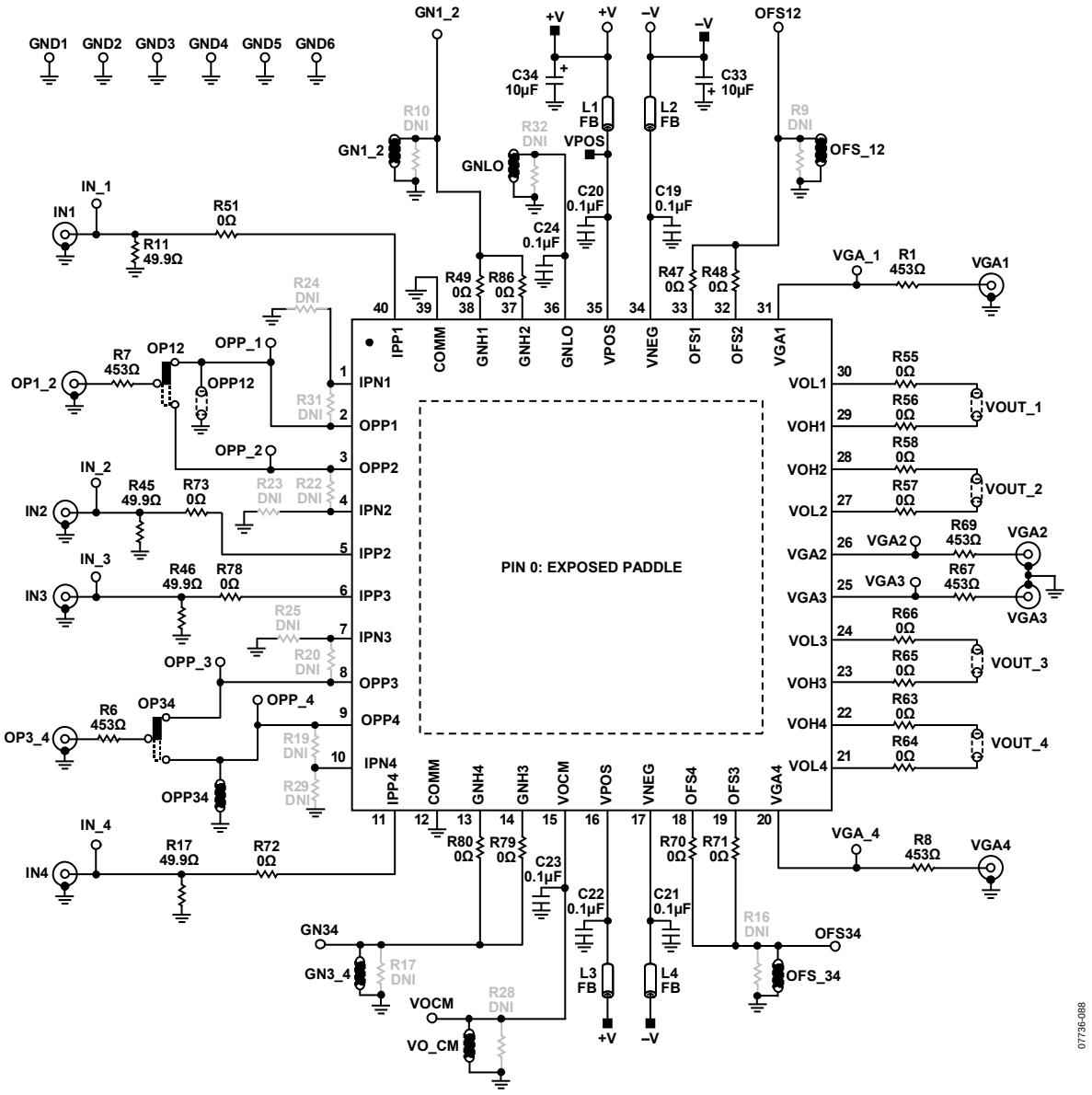


Figure 118. AD8264-EVALZ Schematic

The SMA connectors, VGA1 through VGA4, enable signal monitoring at these nodes, with 453 Ω resistors for protecting the device. These resistors can be shorted at the discretion of the user if wide bandwidth is desired. The differential outputs are provided with 0.1" spacing 2-pin headers, which fit the low capacitance Tektronix differential scope probe P6045 model.

Note that the gain control input of the AD8264 is differential. Each channel has its own gain control pin (GNHx); however, pairs of pins are connected together on the evaluation board and connected to a test loop. The 2-pin headers are provided for jumpers to connect the gain pins to ground, preventing the quiescent gain control voltage at the GNHx pins from floating high. The low sides of the gain controls for each channel are internally connected in the AD8264, and a 2-pin header with jumper is provided to connect this pin (GNLO) to ground as well.

A similar arrangement of 2-pin headers is provided for the output offset voltage. As shipped, the offset pins are connected to ground, preventing the pins from floating high.

For connecting to an ADC, remove the jumpers at the OF1_2 and OF3_4 headers and connect the appropriate offset voltage at the test loops, OF12 and OF34. If the VOCM pin is buffered, it can be connected to the reference of the ADC.

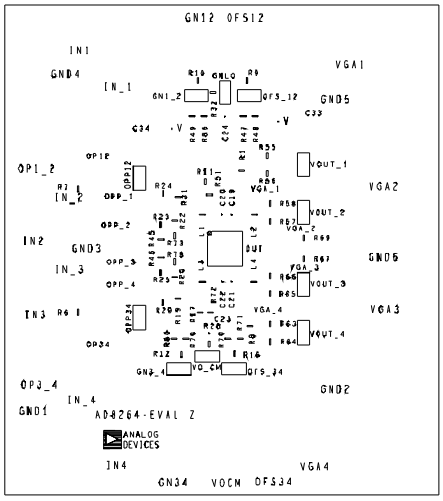


Figure 119. Component Side Assembly

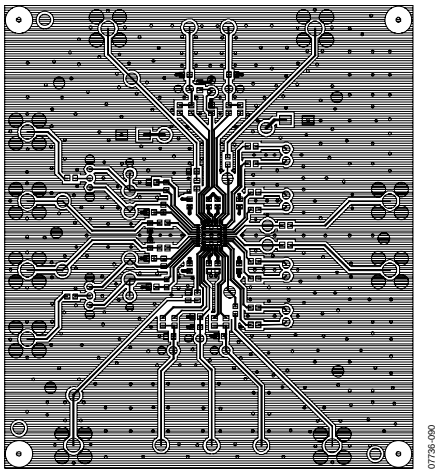


Figure 120. Component Side Copper

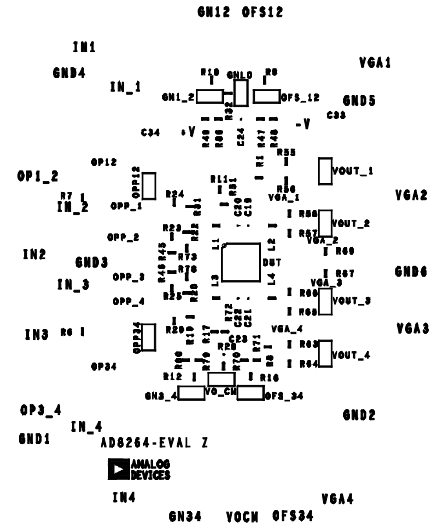


Figure 121. Component Side Silk Screen

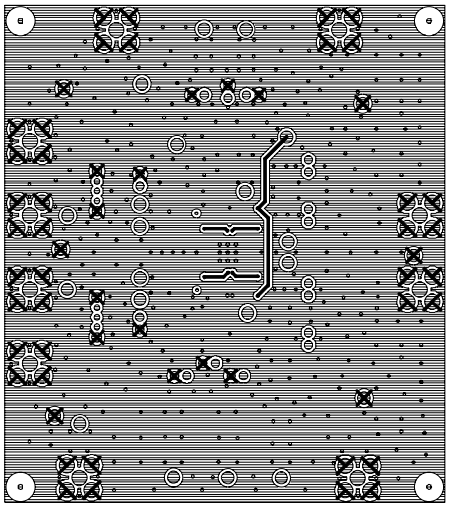


Figure 122. Secondary Side Copper

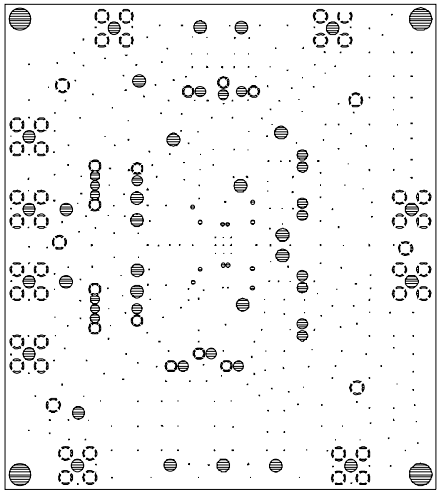


Figure 123. Ground Plane

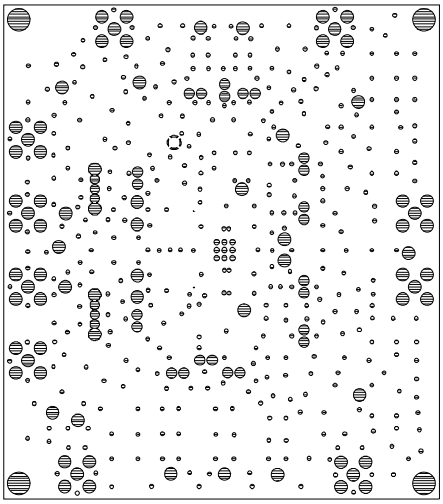
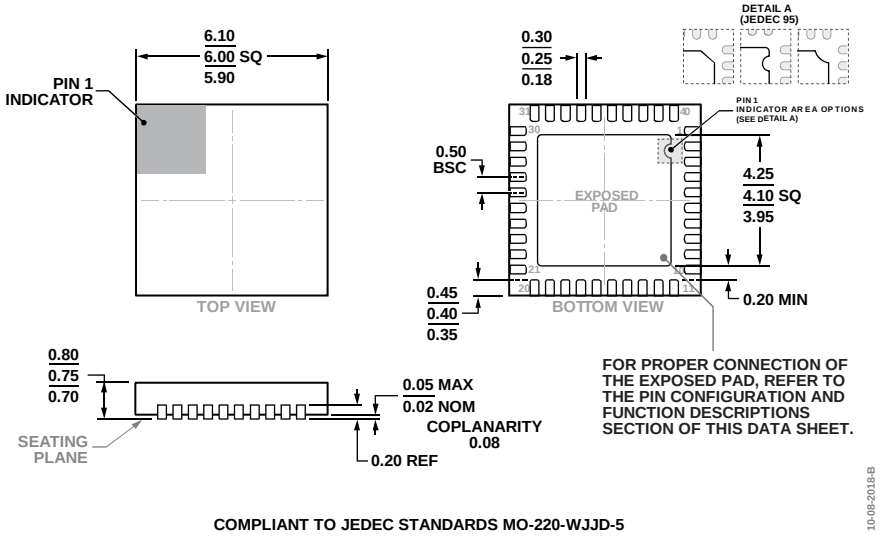


Figure 124. Power Plane

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD-5

Figure 125. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.75 mm Package Height
(CP-40-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Marking Code
AD8264ACPZ	−40°C to +85°C	40-Lead LFCSP	CP-40-9	H1V
AD8264ACPZ-R7	−40°C to +85°C	40-Lead LFCSP, 7″ Tape and Reel	CP-40-9	H1V
AD8264ACPZ-RL	−40°C to +85°C	40-Lead LFCSP, 13″ Tape and Reel	CP-40-9	H1V
AD8264-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.