

1.5V Drive Nch+Pch MOSFET

US6M11

●Structure

Silicon N-channel MOSFET /
 Silicon P-channel MOSFET

●Features

- 1) Nch MOSFET and Pch MOSFET are put in TUMT6 package.
- 2) Low on-resistance.
- 3) Low voltage drive (1.5V drive).
- 4) Built-in G-S Protection Diode.

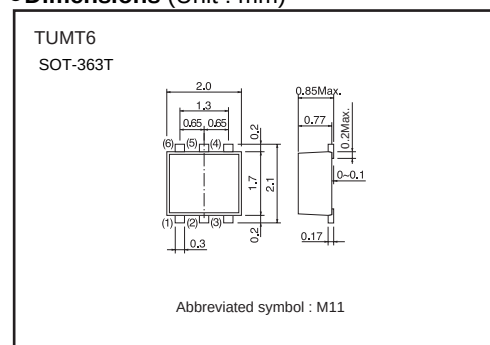
●Applications

Switching

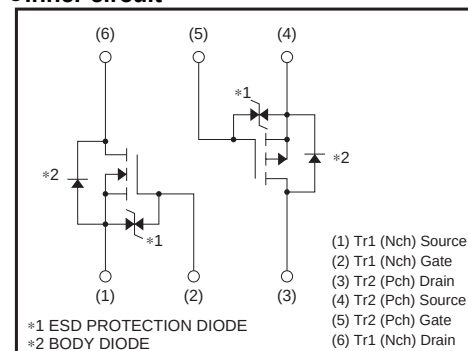
●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
US6M11		○

●Dimensions (Unit : mm)



●Inner circuit



●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit
		Tr1 : Nchannel	Tr2 : Pchannel	
Drain-source voltage	V_{DS}	20	-12	V
Gate-source voltage	V_{GS}	±10	±10	V
Drain current	Continuous	I_D	±1.5	A
	Pulsed	I_{DP}^{*1}	±6	A
Source current (Body diode)	Continuous	I_S	0.5	A
	Pulsed	I_{SP}^{*1}	6	A
Power dissipation	P_D^{*2}	1.0		W / TOTAL
		0.7		W / ELEMENT
Channel temperature	T_{ch}	150		°C
Range of storage temperature	T_{stg}	-55 to +150		°C

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

*2 Mounted on a ceramic board.

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th(ch-a)}^{*}$	125	°C/W / TOTAL
		179	°C/W / ELEMENT

* Mounted on a ceramic board

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●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	± 10	μA	$V_{GS} = \pm 10V, V_{DS} = 0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	20	–	–	V	$I_D = 1mA, V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}	–	–	1	μA	$V_{DS} = 20V, V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	0.3	–	1.0	V	$V_{DS} = 10V, I_D = 1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	–	130	180	m Ω	$I_D = 1.5A, V_{GS} = 4.5V$
		–	170	240	m Ω	$I_D = 1.5A, V_{GS} = 2.5V$
		–	220	310	m Ω	$I_D = 0.8A, V_{GS} = 1.8V$
		–	300	600	m Ω	$I_D = 0.3A, V_{GS} = 1.5V$
Forward transfer admittance	$ Y_{fs} $ *	1.6	–	–	S	$V_{DS} = 10V, I_D = 1.5A$
Input capacitance	C_{iss}	–	110	–	pF	$V_{DS} = 10V$
Output capacitance	C_{oss}	–	18	–	pF	$V_{GS} = 0V$
Reverse transfer capacitance	C_{rss}	–	15	–	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$ *	–	5	–	ns	$V_{DD} \doteq 10V$
Rise time	t_r *	–	5	–	ns	$I_D = 1A$
Turn-off delay time	$t_{d(off)}$ *	–	20	–	ns	$V_{GS} = 4.5V$
Fall time	t_f *	–	3	–	ns	$R_L \doteq 10\Omega$
Total gate charge	Q_g *	–	1.8	–	nC	$V_{DD} \doteq 10V, V_{GS} = 4.5V$
Gate-source charge	Q_{gs} *	–	0.3	–	nC	$I_D = 1.5A$
Gate-drain charge	Q_{gd} *	–	0.3	–	nC	$R_L \doteq 6.7\Omega, R_G = 10\Omega$

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	–	–	1.2	V	$I_S = 1.5A, V_{GS} = 0V$

*Pulsed

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●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	± 10	μA	$V_{GS} = \pm 10V, V_{DS} = 0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	–12	–	–	V	$I_D = -1mA, V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}	–	–	–1	μA	$V_{DS} = -12V, V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	–0.3	–	–1.0	V	$V_{DS} = -6V, I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	–	190	260	m Ω	$I_D = -1.3A, V_{GS} = -4.5V$
		–	280	390	m Ω	$I_D = -0.6A, V_{GS} = -2.5V$
		–	400	600	m Ω	$I_D = -0.6A, V_{GS} = -1.8V$
		–	530	1060	m Ω	$I_D = -0.2A, V_{GS} = -1.5V$
Forward transfer admittance	$ Y_{fs} $ *	1.4	–	–	S	$V_{DS} = -6V, I_D = -1.3A$
Input capacitance	C_{iss}	–	290	–	pF	$V_{DS} = -6V$
Output capacitance	C_{oss}	–	28	–	pF	$V_{GS} = 0V$
Reverse transfer capacitance	C_{rss}	–	21	–	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$ *	–	8	–	ns	$V_{DD} \doteq -6V$
Rise time	t_r *	–	10	–	ns	$I_D = -0.6A$
Turn-off delay time	$t_{d(off)}$ *	–	30	–	ns	$V_{GS} = -4.5V$
Fall time	t_f *	–	9	–	ns	$R_L \doteq 10\Omega$
Total gate charge	Q_g *	–	2.4	–	nC	$V_{DD} \doteq -6V, V_{GS} = -4.5V$
Gate-source charge	Q_{gs} *	–	0.6	–	nC	$I_D = -1.3A$
Gate-drain charge	Q_{gd} *	–	0.4	–	nC	$R_L \doteq 4.6\Omega, R_G = 10\Omega$

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	–	–	–1.2	V	$I_S = -1.3A, V_{GS} = 0V$

*Pulsed

●Electrical characteristic curves

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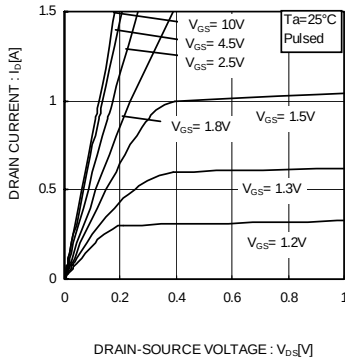


Fig.1 Typical Output Characteristics(I)

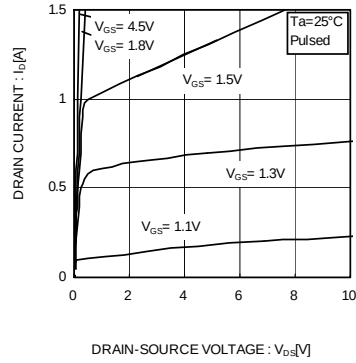


Fig.2 Typical Output Characteristics(II)

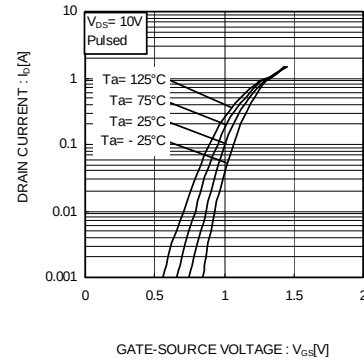


Fig.3 Typical Transfer Characteristics

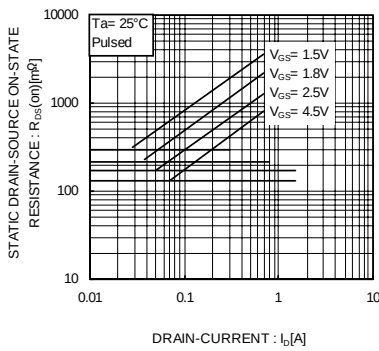


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

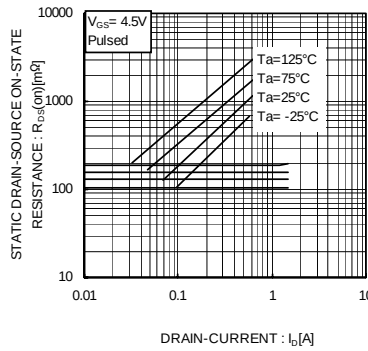


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

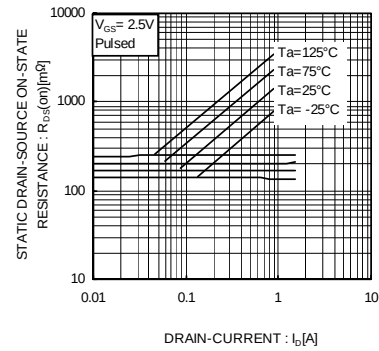


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

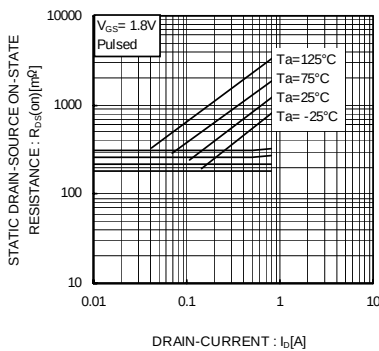


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

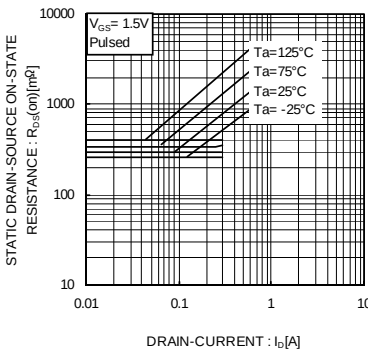


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(V)

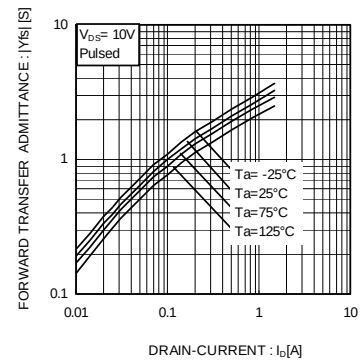


Fig.9 Forward Transfer Admittance vs. Drain Current

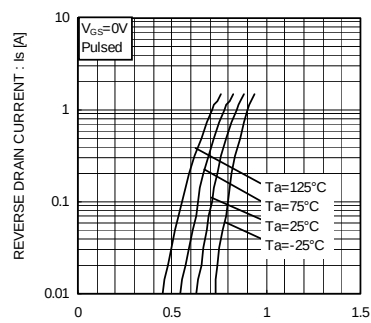


Fig.10 Reverse Drain Current vs. Source-Drain Voltage

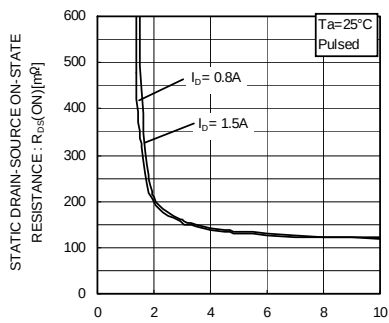


Fig.11 Static Drain-Source On-State Resistance vs. Gate Source Voltage

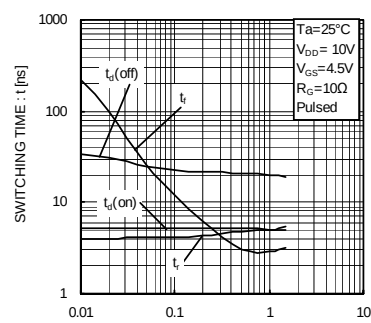


Fig.12 Switching Characteristics

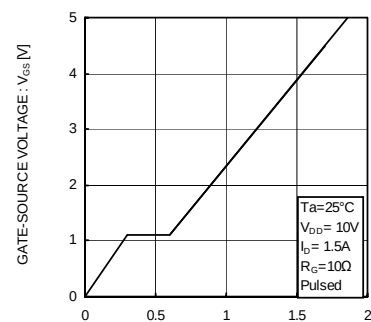


Fig.13 Dynamic Input Characteristics

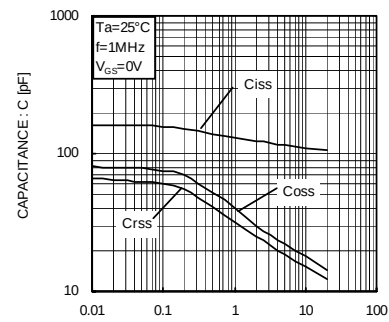


Fig.14 Typical Capacitance vs. Drain-Source Voltage

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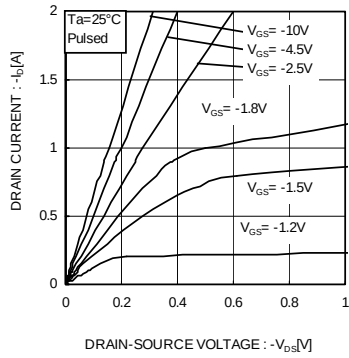


Fig.1 Typical output characteristics(I)

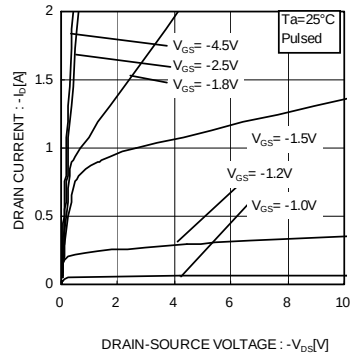


Fig.2 Typical output characteristics(II)

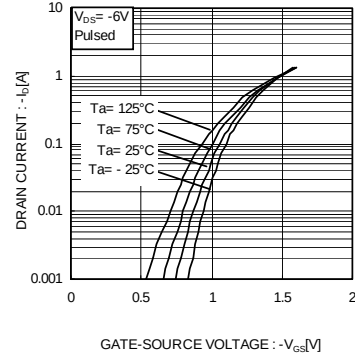


Fig.3 Typical Transfer Characteristics

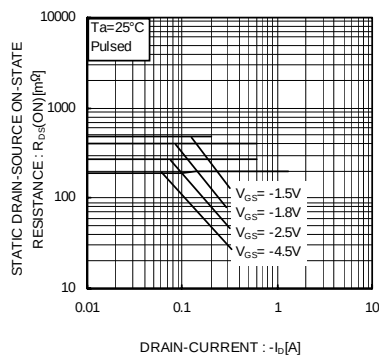


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

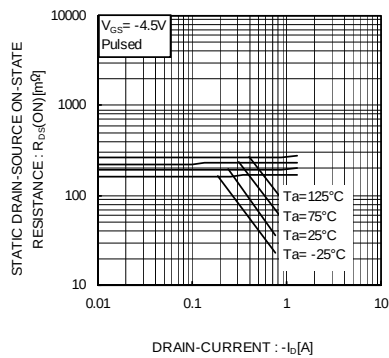


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

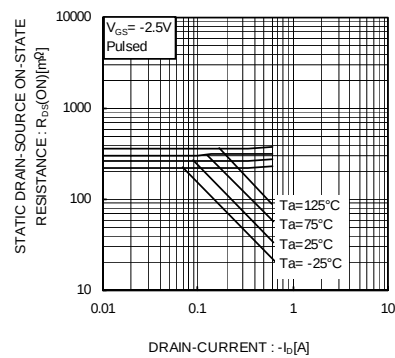


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

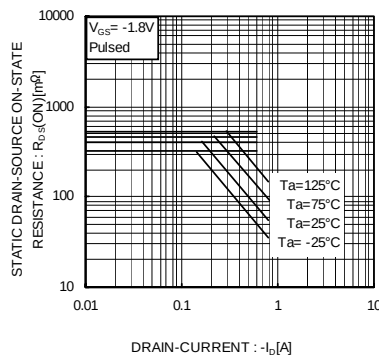


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

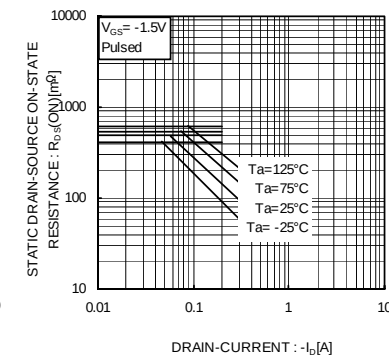


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(IV)

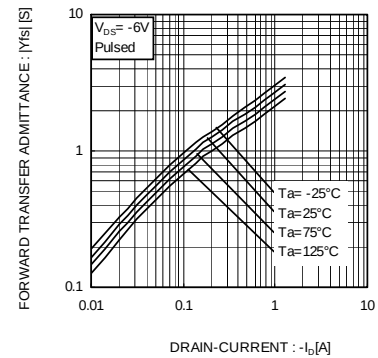
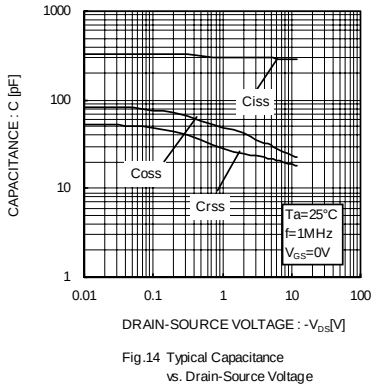
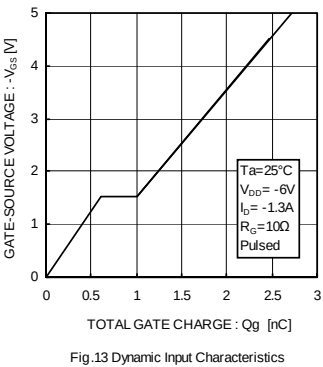
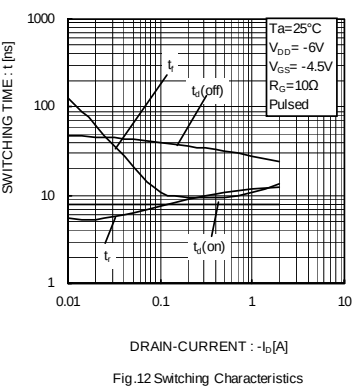
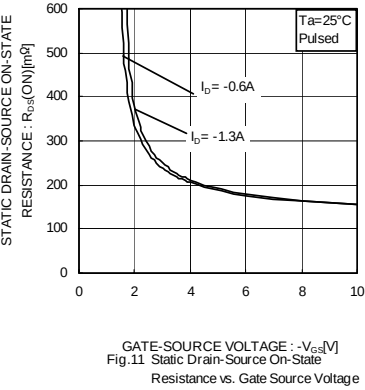
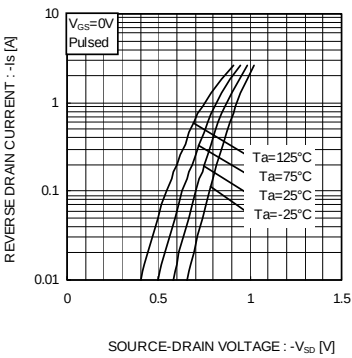


Fig.9 Forward Transfer Admittance vs. Drain Current



●Measurement circuit

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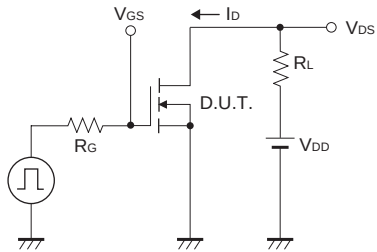


Fig.1-1 Switching Time Measurement Circuit

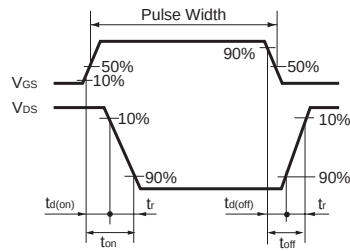


Fig.1-2 Switching Waveforms

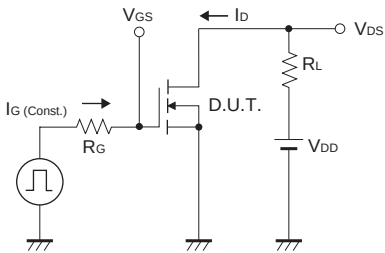


Fig.2-1 Gate Charge Measurement Circuit

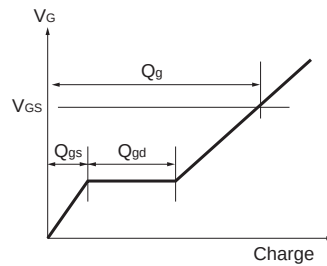


Fig.2-2 Gate Charge Waveform

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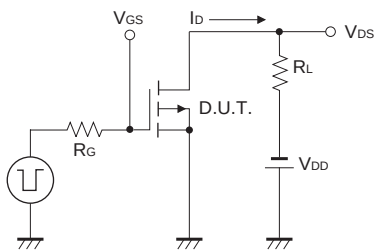


Fig.3-1 Switching Time Measurement Circuit

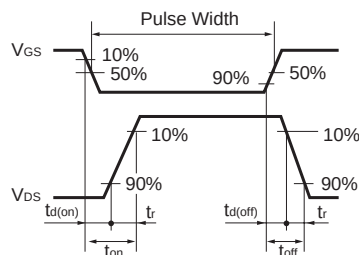


Fig.3-2 Switching Waveforms

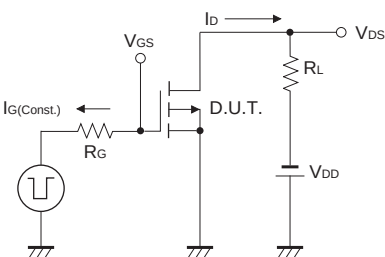


Fig.4-1 Gate Charge Measurement Circuit

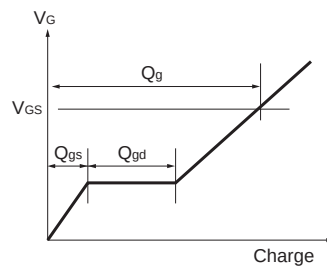


Fig.4-2 Gate Charge Waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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